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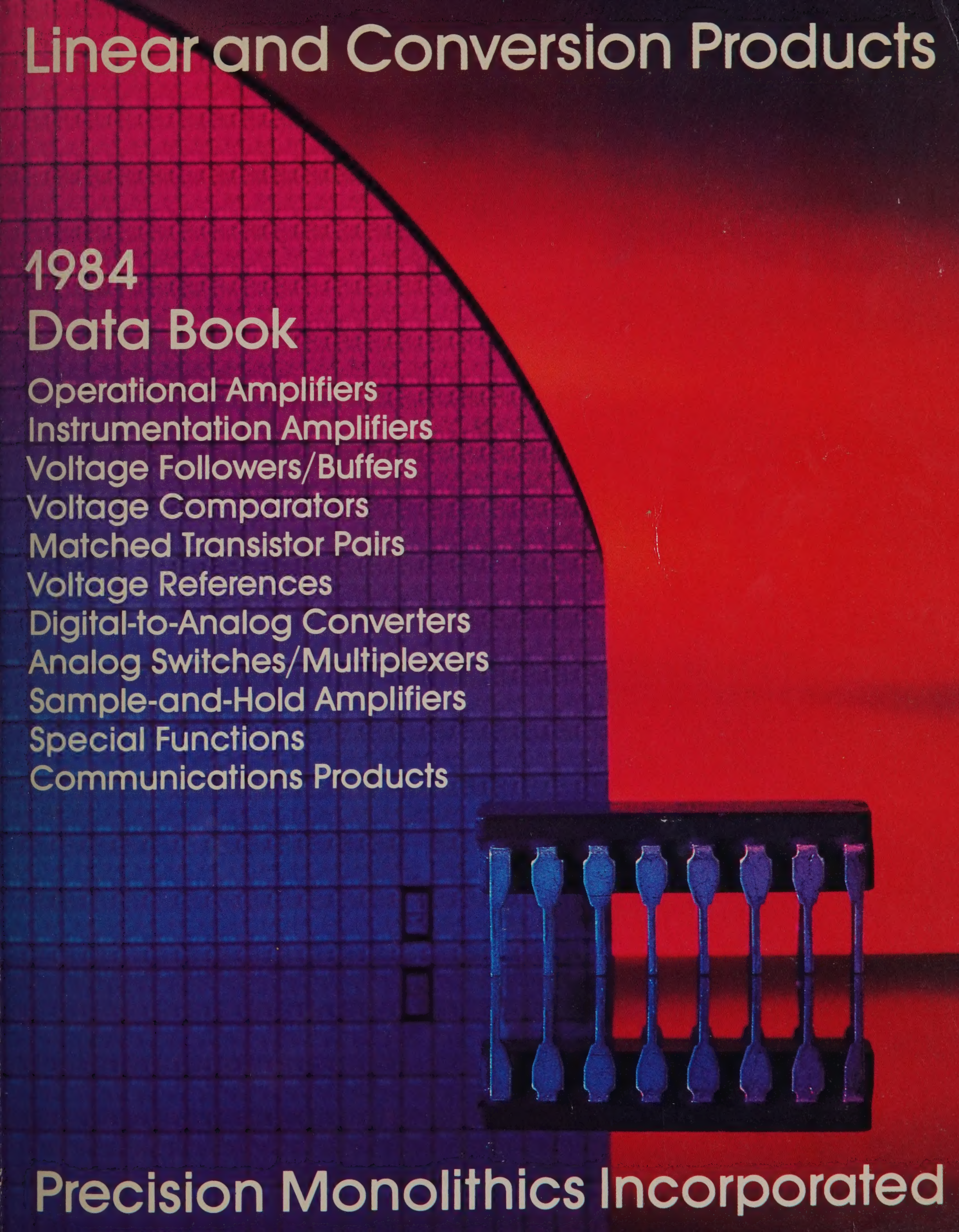

1984
Data Book

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- Instrumentation Amplifiers
- Voltage Followers/Buffers
- Voltage Comparators
- Matched Transistor Pairs
- Voltage References
- Digital-to-Analog Converters
- Analog Switches/Multiplexers
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Precision Monolithics Incorporated

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PMI 1984
DATA BOOK

The PMI Commitment

PMI is committed to building long term customer relationships resulting in mutual growth.

At PMI we dedicate ourselves to leadership in customer service, quality, and technology.

Our goal is flawless performance and professional excellence.

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PMI reserves the right to make changes to the products contained in this data book to improve performance, reliability, or manufacturability. Consequently, contact PMI for the latest available specifications and performance data.

Although every effort has been made to ensure accuracy of the information contained in this data book, PMI assumes no responsibility for inadvertent errors.

PMI assumes no responsibility for the use of any circuits described herein and makes no representation that they are free of patent infringement.

The products in this catalog are manufactured under one or more of the following patents: 4,055,773; 4,056,740; 4,068,254; 4,088,905; 4,092,639; 4,109,215; 4,118,699; 4,131,884; 4,138,671; 4,142,117; 4,168,528; 4,210,830; 4,228,367; 4,260,911; 4,272,656; 4,285,051; 4,333,047; 4,340,851.

Precision Monolithics, Inc. Life Support Policy

As a general policy, Precision Monolithics Inc. does not recommend the use of any of its products in life support applications where the failure or malfunction of the PMI product can be reasonably expected to cause failure of the life support device or to significantly affect its safety or effectiveness. PMI will not knowingly sell its products for use in such applications unless it receives in writing assurances satisfactory to PMI that (a) the risks of injury or damage have been minimized, (b) the customer assumes all such risks, and (c) the liability of PMI is adequately protected under the circumstances.

Examples of devices considered to be life support devices are neonatal oxygen analyzers, nerve stimulators (whether used for anesthesia, pain relief, or other purposes), autotransfusion devices, blood pumps, defibrillators, arrhythmia detectors and alarms, pacemakers, hemodialysis systems, peritoneal dialysis systems, neonatal ventilator incubators, ventilators for both adults and infants, anesthesia ventilators, and infusion pumps as well as other devices designated as "critical" by the FDA. The above are examples only and are not intended to be conclusive or exclusive of any other life support device.

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ORDERING INFORMATION

PACKAGED PRODUCTS PART NUMBERING SYSTEM

Device Type & Model Number

Burn-In Option

Electrical Grade

Package Suffix

MIL-STD-883 Class B Option

All PMI −55° C to +125° C devices are available with Class B MIL-STD-883 screening as standard products. To order an 883B part, simply add the designation /883 to the part number. For example, the DAC-08AQ screened to the 883B requirements would be ordered as a DAC-08AQ/883.

DAC-08 BI E Q /883

Package Type

H = 6 lead TO-78 Can
J = 8 lead TO-99 Can
K = 10 lead TO-100 Can
O = Not used
P = Epoxy DIP
Q = 16 lead Ceramic DIP
R = 20 lead Ceramic DIP
RC = 20 position LCC*

S = Not used
T = 28 lead Ceramic DIP
TC = 28 position LCC*
U = Not used
V = 24 lead Ceramic DIP
X = 18 lead Ceramic DIP
Y = 14 lead Ceramic DIP
Z = 8 lead Ceramic DIP

*Special Order Only

Note: See more complete listing on page 17-2.

Select electrical grade from data sheet.

PMI offers all 0°/70° C and −25°/+85° C devices with burn-in per MIL-STD-883, 160 hours at +125° C or 80 hours at +150° C at PMI's option. Parts with this option are specified with the letters BI added between the model number and the electrical grade. For example, to order DAC-08EQ with burn-in, the part number is DAC-08BIEQ.

Device types are listed on next page. Select model number from product listings.

MIL-M-38510

PMI's factory is certified to produce JAN parts per MIL-M-38510. Consult factory for availability of specific slash sheet part numbers. At this writing, devices with Part 1 or Part 2 approval include PM-155A, PM-156A, PM-157A, PM-108A, PM-2108A and DAC-08. Other types are being qualified.

See Table of Contents for JAN data sheet listings.

ORDERING INFORMATION

DICE PART NUMBERING SYSTEM

Device Type & Model Number

Electrical Grade
N = Top, **G** = Middle, **GR** = Lowest

Temperature-Tested Die Option (125° C)

Visual Criteria
A = MIL-STD-883, Method 2010.2, Test Condition A.
B = MIL-STD-883, Method 2010.2, Test Condition B.

Backing Suffix
C = Plain, **CG** = Gold Backed

DAC-08 N T B C

All PMI chips are available with either plain backing or, for a 50% adder plus a $250 lot charge, 1-micron-thick eutectic-bonded gold backing.

Several PMI devices are available with min/max wafer test limits for dice tested at +125° C. See specific data sheet.

Data sheets give specific available grades for each PMI device.

Device Type
AMP — Instrumentation Amplifier
BUF — Buffer (Voltage Follower)
CMP — Comparator
DAC — Digital-to-Analog Converter
DMX — De-Multiplexer
GAP — General-Purpose Analog Processor
JAN — MIL-M-38510 Slash Sheet
MAT — Matched Transistor
MUX — Multiplexer
OP — Proprietary Operational Amplifier
PKD — Peak Detector
PM — Second-Source, Industry Specifications
REF — Voltage Reference
RPT — PCM Line Repeater
SMP — Sample-and-Hold Amplifier
SW — Analog Switch

Select model number from product listings.

ORDERING INFORMATION

DICE INFORMATION

Triple Passivation

Triple Passivation is a three-step process which provides superior reliability and protection for all PMI integrated circuits. First, a specially treated thermal silicon dioxide layer is grown. This protects the junctions and also attracts any residual ionic impurities to the top surface of the oxide, where they are held fixed. Next, a layer of silicon nitride is applied to prevent the entry of any potential contamination or impurities. The third step is the thick glass overcoat layer which leaves only the bonding pads exposed. This "glassivation" protects the die from damage during assembly and is especially important in minimizing yield loss during shipment and assembly of dice for hybrid circuits.

Quality Assurance

PMI believes that quality and reliability must be built into the product; no amount of testing can replace these inherent properties. For this reason, devices are fabricated and processed to MIL-STD-883 requirements as standard practice with many exclusive processes and controls added to improve quality and reliability. The integrity of aluminum metallization is confirmed by sampling wafer lots using Scanning Electron Microscope (SEM) examinations per Method 2018 specifications.

Mechanical Information

Aluminum metallization with a nominal thickness of 10,000 angstroms is standard for all devices. Die thickness is 6 mils minimum to 16 mils maximum. Minimum bonding pad size is 4.0 mils X 4.0 mils for all devices.

Visual Inspection

All dice are 100% visually inspected to the applicable visual criteria per MIL-STD-883 Method 2010, Condition B.

Electrical Testing

All dice are 100% tested to the 25° C DC wafer test limits shown in this catalog before the wafer is separated into individual dice. Due to variations in assembly methods and normal yield loss, PMI does not guarantee specifications after packaging for standard dice. Sample assembly and testing in standard PMI packages to specified LTPD's and min/max specifications are available at extra cost. Consult factory for dice lot qualification negotiation.

Shipping

Protection during shipment is provided by a wafflepack carrier with anti-static shield and cushioning strip. In addition, the wafflepack is vacuum sealed in a polyethylene bag.

Military/Aerospace Applications

PMI devices are widely used in military and aerospace programs. A partial listing includes:

Equipment

AN/TRC-170
AN/ULR-17
AN/WSC-3
AN/BQQ-5
AN/SPG-51
AN/ALQ-3
AN/ALQ-99
AN/AQS-17
AN/AQS-13E
AN/BQN-17
AN/UYK-20
AN/AQA-7
AN/ARC-150
AN/ALQ-149
AN/SQK-3
AN/ALR-67
AN/ALR-62
AN/ALR-46
AN/ALQ-101
AN/ALQ-131

Military Aircraft

F-4
B-1
Sikorsky UH-60A
A-10
Sikorsky SH-3
YC-15
P-3
S-3A
F-15
B-52
F-18
Alpha Jet
E-3A
F-16
F-5
Tornado

Missile/Spacecraft

Viking
(Mars Orbitor)
Aerosat
Harm Missile
DSCS-3
Sparrow Missile
Trident
TDRSS
TV SAT
Intelsat 5
Voyager
(Jupiter/Saturn)
Stinger Missile
Standard Missile II
Tiros-N
Cruise Missile
Ariane
Roland
Eurosat

Electronic Systems

Omega
Tram
Aims (MK86)
F-16
(Ground Support)
Pave Spike
AWACS
A4KU
MK-48
B-52 Radar Mod
Pathfinder Radar
MK-46
Seaguard
Gepard

Miscellaneous

RFP Model 35 #13
Project 4620
Heads-Up Display
DST 1860
Walleye
PMS
Aerial Surveillance Camera
Cutty Sark
Compass Tie
System 27
ACM
VCS
Naval Submarine Periscope

RELIABILITY INFORMATION

Overview

PMI, in establishing standard procedures for manufacturing, screening, qualification, and conformance, has incorporated the requirements of both MIL-STD-883 and MIL-Q-9858. Devices meeting Class B screening requirements of MIL-STD-883 are available off-the-shelf as standard catalog items.(Refer to the ordering information in this section).

PMI standard "883" parts have been subjected to 100% screening in accordance with Method 5004 of MIL-STD-883, Class B, and have been subjected to Group A Quality Conformance Testing per Method 5005. Complete Quality Conformance Testing (Groups A, B, C, D) in accordance with Method 5005 of MIL-STD-883 is available on special order.

Specials

At PMI, we have a proven track record for handling "customer specials". Many IC manufacturers shy away from processing precision linear ICs to the unique in-house specifications of their customers. PMI recognizes your special needs and welcomes the opportunities provided by the military/aerospace industry. Hi-rel is a cornerstone of PMI's business and we will continue to offer the extra processing that your applications require.

Radiation Resistance

As a leading supplier of precision linear ICs to the military/aerospace industry, PMI is supportive of the system designer's needs for readily available, standard components that are radiation resistant. A number of standard PMI linear integrated circuits have characteristically demonstrated good resistance to radiation. These devices have been subjected to radiation levels necessary to perform effectively in military/aerospace radiation environments, and they are now being used in a number of demanding military and space programs.

Experiments to isolate the processing mechanisms that led to PMI's increased radiation hardness characteristics have pointed heavily toward the use of a silicon nitride passivation layer. While we do not believe that this process is the only radiation hardening advantage of PMI devices, it does add a great deal to survivability.

For more information request PMI's "Radiation Resistance" brochure.

ORDERING INFORMATION

DISCONTINUED DEVICE TYPES ORDERING GUIDE

Between 1978 and 1983 some device types, individual grades, and package options were discontinued. This guide is provided to help the designer to select an appropriate alternative device.

Type	Alternative Device Type	Note(s)
BUF-01	OP-07 connected as a voltage follower.	
BUF-02	OP-16 connected as a voltage follower.	—
DAC-04	DAC-06 nearest grade.	1
DAC-76	DAC-86 nearest grade.	1, 2
DAC-78	DAC-88EX.	1
DAC-87	DAC-89EX.	3
DAC-101	DAC-100 "Q3" nearest grade.	1
DAC-206	DAC-01 nearest grade.	1
OP-03	OP-04 with externally-connected V+ pins.	1
OP-18	LM101 is the most similar device.	—
OP-19	MC1741S is the most similar device.	—
OP-24	OP-27GP, improved replacement.	1
OP-34	OP-37GP, improved replacement.	1
PM-1458	OP-14 nearest grade.	1
PM-1558	OP-14 nearest grade.	1
PM-4136	OP-09 nearest grade.	1
SSS-725	OP-06 or PM-725 nearest grade.	1
SSS-741	OP-02 nearest grade.	1
SSS-747	OP-04 or PM-747 nearest grade.	1
SSS-1458	OP-14 nearest grade.	1
SSS-1558	OP-14 nearest grade.	1

Note 1. Direct, pin-for-pin replacement. No design changes required.

Note 2. DAC-76 −55° C/+125° C types may be ordered as DAC-86 specials.

Note 3. DAC-89EX has idling currents on the outputs requiring matched load resistors. DAC-89EX has higher speed and accuracy and is an improved, direct, pin-for-pin replacement for DAC-87 in most designs.

Package Type	Affected Device Type	Remarks
"K" (TO-100)	PM-747.	Available on Specials.
"N" (Flatpack)	DAC-100N9.	Available on Specials.
"Y" (14-pin DIP)	See list below.	Available on Specials.

"Y" Package Option: Affected Device Types

CMP-01
CMP-02
OP-01
OP-02
OP-06
OP-220
PM-725
PM-741

The "Y" package option was discontinued for some products. They are all available in other package types including "J" (TO-99), "P" (Epoxy DIP), or "Z" (Ceramic 8-pin Mini-DIP). See individual data sheets for available package options for each device.

Discontinued-Electrical-Grade Ordering Guide

The following electrical grades were discontinued but are available with different specifications in the same packages. See individual data sheets.

CMP-01B
CMP-02B
DAC-05B
DAC-05F
DAC-20E
DAC-88C
DAC-89C
DAC-100Q1
DAC-100Q2
MAT-01F
OP-01E
OP-01F
OP-04GR
OP-08B
OP-08F
OP-09C
OP-09G
PM-239
PM-239A
PM-255
PM-256
PM-257
PM-339
PM-355
PM-356
PM-357
PM-2208
PM-2308
REF-01D

5 volt output versions of DAC-02 and DAC-05, "X2" suffix, were discontinued. They may be ordered as DAC-03X2 specials.

60 volt breakdown versions of MAT-01 were discontinued (MAT-01H and MAT-01FH).

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—PRODUCT ASSURANCE

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PRODUCT ASSURANCE

INTRODUCTION

PMI has long been recognized as a High Quality/Reliability supplier of Commercial, Industrial and Military/Aerospace Products. The PMI Product Assurance Department plays a vital role in controlling processes to ensure the manufacture of highly reliable, cost-effective product, and to make certain that all pertinent customer specifications and requirements are met.

ORGANIZATION

Product Assurance Department of PMI is composed of four functional departments: Process Quality Control, Quality Assurance, Reliability, and Program Management.

RESPONSIBILITIES

Process Control — The primary responsibility of the Process Control Department is to establish and maintain effective controls over process integrity by monitoring manufacturing processes and equipment operation; to provide real-time feedback of information concerning the status of these controls; and to initiate statistically valid techniques to further improve quality and reliability levels. These concepts are used extensively throughout all manufacturing processes.

Quality Assurance (Standard and Hi-Rel) — The primary responsibility of the Quality Assurance Department is to assure that the delivered product meets PMI or Customer Product Standards of reliability and quality. Process monitors and gate inspections are designed so that all devices are properly tested and required sample tests are performed prior to shipment. Inspection records and reports concerning monitor and inspection data keep all cognizant personnel fully informed about the status of the quality level of products going through final test operations.

Reliability — The Reliability Department assures a high and consistent reliability of PMI products. The Reliability Department establishes, defines, and maintains evaluation programs to determine process/product reliability. The Reliability Department will issue periodic reports on the results of all evaluation testing. Contact the nearest PMI Sales Office or the Literature Department for the latest issue of the PMI Reliability Bulletin.

The Reliability Department also performs failure analyses as required.

Program Management — The primary responsibility of the Program Management Department is to ensure that the MIL-M-38510 JAN Program and other special customer program requirements are met. This is accomplished by monitoring the in-house procedures used to define each process step of a particular program. If necessary, baselining documentation is written detailing specific procedures and processing flows. A Configuration Control System consisting of maintenance of PMI standard baselining for each device type, as well as notification to customers of major process and product changes, are also responsibilities of this group.

Contact the nearest PMI Sales Office or the Literature Department for a copy of the comprehensive PMI Product Assurance Manual.

QUALITY LEVELS

PMI processes to stringent quality standards. Quality guarantees range from parts-per-million on Standard Product to imposed Quality Levels dictated by customer specification on custom orders.

Current information on Quality Levels is available upon request; contact the nearest PMI Sales Office or the Literature Department.

PROCESSING

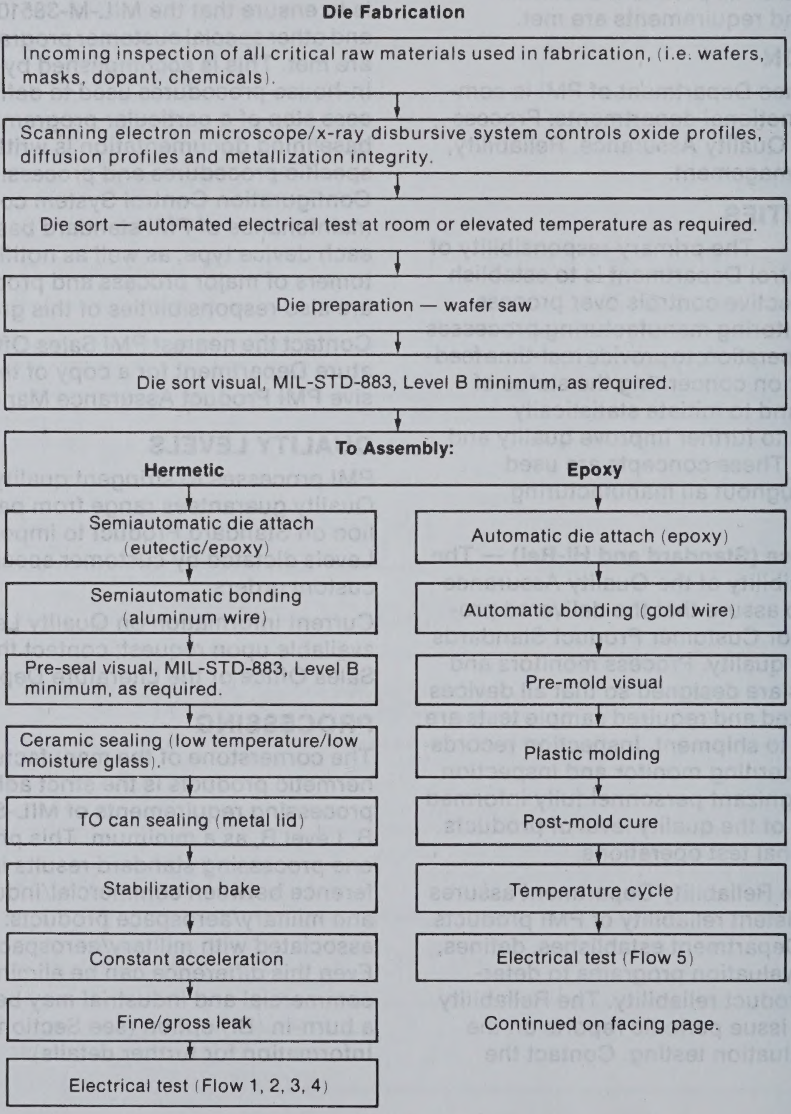
The cornerstone of the manufacturing of PMI hermetic products is the strict adherence to the processing requirements of MIL-STD-883 Rev. B, Level B, as a minimum. This philosophy of one processing standard results in a single difference between commercial/industrial products and military/aerospace products: the burn-in associated with military/aerospace products. Even this difference can be eliminated, as all commercial and industrial may be obtained with a burn-in (BI) option (see Section 2, Ordering Information for further details).

—PRODUCT ASSURANCE

The manufacture of epoxy devices is inherently different from hermetic in the area of assembly. Automation of the assembly line has produced a tightly process-controlled product that requires few interim inspections from wafer fabrication to pre-mold visual. Plastic product may also be obtained with a burn-in (BI) option (see Section 2, Ordering Information for further details).

STANDARD PROCESS FLOWS

(JAN 38510, Class B, 883 Class B; PMI Industrial/Commercial)



Die Fabrication

Incoming inspection of all critical raw materials used in fabrication, (i.e. wafers, masks, dopant, chemicals).

Scanning electron microscope/x-ray disbursive system controls oxide profiles, diffusion profiles and metallization integrity.

Die sort — automated electrical test at room or elevated temperature as required.

Die preparation — wafer saw

Die sort visual, MIL-STD-883, Level B minimum, as required.

To Assembly:

Hermetic

Semiautomatic die attach (eutectic/epoxy)

Semiautomatic bonding (aluminum wire)

Pre-seal visual, MIL-STD-883, Level B minimum, as required.

Ceramic sealing (low temperature/low moisture glass).

TO can sealing (metal lid)

Stabilization bake

Constant acceleration

Fine/gross leak

Electrical test (Flow 1, 2, 3, 4)

Epoxy

Automatic die attach (epoxy)

Automatic bonding (gold wire)

Pre-mold visual

Plastic molding

Post-mold cure

Temperature cycle

Electrical test (Flow 5)

Continued on facing page.

PRODUCT—ASSURANCE

Flow 1 MIL-STD-883 METHOD 5004 CLASS S (See Note 1)	Flow 2 MIL-STD-883 METHOD 5004 CLASS B/ JAN 38510	Flow 3 MIL-STD-883 METHOD 5004 CLASS B (See Note 2)	Flow 4 PMI STANDARD HERMETIC DEVICES	Flow 5 PMI STANDARD PLASTIC DEVICES
100% Non-Destructive Bond Pull				
Preseal Internal Visual Method 2010 Condition A				
Q. A. Sample Inspection				
Stabilization Bake Method 1008 Condition C (24 Hrs)				
Temperature Cycling Method 1010 Condition C				
Constant Acceleration Method 2001 Condition E Y1 Plane				
Seal Method 1014 Condition A_1 & C				
Serialization				
Electrical Test +25° C Read & Record	Electrical Test +25° C	Electrical Test +25° C	Electrical Test +25° C (Optional) (See Note 3)	Electrical Test +25° C (Optional) (See Note 3)
Burn-In Test Method 1015 Cond. B 240 Hrs At +125° C	Burn-In Test Method 1015 Cond. B	Burn-In Test Method 1015 Cond. B	Burn-In Test Multi-Option (See Note 3)	Burn-In Test Multi-Option (See Note 3)
Post Burn-In Electrical Parameters Read & Record At +25° C	Final Electrical Test At +25° C	Final Electrical Test At +25° C	Final Electrical Test At +25° C (See Note 4)	Final Electrical Test At +25° C (See Note 4)
Particle Impact Noise Detection Method 2020				
Seal Method 1014 Condition A_1 & C				
Static Test at +25° C And Min/Max Temperatures	Static Test Min/Max Temperatures	Static Test Min/Max Temperatures		
Dynamic Tests And Switching Tests At +25° C (See Note 5)	Dynamic Tests And Switching Tests At 25° C (See Note 5)	Dynamic Tests And Switching Tests At +25° C (See Note 5)		
Group A Method 5005	Group A Method 5005	Group A Method 5005	Q.A. Sample Test At +25° C	Q.A. Sample Test At +25° C
Radiographic (X-Ray) Method 2012				
External Visual Method 2009	External Visual Method 2009	External Visual Method 2009	External Visual Method 2009	External Visual PMI Standard
Q.A Plant Clearance	Q.A Plant Clearance	Q.A Plant Clearance	Q.A Plant Clearance	Q.A Plant Clearance

NOTES:

1. Class S product is assembled/tested in the U.S. and is tailored to meet specific customer requirements.
2. MIL 883 product is assembled/tested per the requirements of MIL-M-38510, class B, and MIL-STD-883 with the following exceptions: built offshore, non-reflowed matte tin finish, and tested to PMI Electrical Test Programs. LTPD requirements will be to MIL-STD-883 Rev. B:

   Static 25° C = 5 Dynamic 25° C = 5 Switching = 7
   Static Temps = 7 Dynamic Temps = 7
3. Standard product is available with burn-in options. Multiple burn-in conditions are available. PDA requirements will be to MIL-STD-883 Rev. B: PDA = 10% @25° C. At the time of publication of this catalog the input offset voltage (V_{OS}) specification of the following devices is excluded from the above PDA requirements: OP-07A, OP-27A, OP-27E, OP-37A OP-37E.
4. Standard product is tested at 25° C with programs guard banded for all temperatures.
5. As required by detailed specification.

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AMD	PMI
AM1408L6	DAC1408A-6Q
AM1408L7	DAC1408A-7Q
AM1408L8	DAC1408A-8Q
AM1408N6	DAC1408A-6P
AM1408N7	DAC1408A-7P
AM1408N8	DAC1408A-8P
AM1508L8	DAC1508A-8Q
AM1458H	OP14DJ
AM1558H	OP14BJ
AM6012ADC	DAC312ER
AM6012APC	DAC312ER
AM6012DM	DAC312BR
AM6012DC	DAC312FR
AM6012PC	DAC312FR+
AM6070ADC	DAC86EX
AM6070DC	DAC86CX
AM6071ADC	DAC88EX+
AM6072DC	DAC86EX
AM6072DC	DAC88EX+
AM6073DC	DAC89EX+
DAC-08AQ	DAC08AQ
DAC-08CN	DAC08CP
DAC-08CQ	DAC08CQ
DAC-08EN	DAC08EP
DAC-08EQ	DAC08EQ
DAC-08HN	DAC08HP
DAC-08HQ	DAC08HQ
DAC-08Q	DAC08Q
LF155AH	PM155AJ
LF155AH	OP15AJ+
LF155H	PM155J
LF155H	OP15BJ+
LF156AH	PM156AJ
LF156AH	OP16AJ+
LF156H	PM156J
LF156H	OP16BJ+
LF157AH	PM157AJ
LF157AH	OP17AJ+
LF157H	PM157J
LF157H	OP17BJ+
LF255H	PM255J
LF355AH	PM355AJ
LF355AH	OP15EJ+
LF355N	PM355Z+

AMD	PMI
LF356AH	PM356AJ
LF356N	PM356Z+
LF357AH	PM357AJ
LF357N	PM357Z+
LM108AH	PM108AJ
LM108H	PM108J
LM124AD	OP421AY
LM124D	OP421BY
LM139AD	PM139AY
LM148D	OP11AY
LM208AH	PM208AJ
LM208H	PM208J
LM224AD	OP421FY
LM224D	OP421FY
LM239AD	CMP04FY
LM239D	CMP04FY+
LM248D	OP11CY
LM308AH	PM308AJ
LM308AN	PM308AP
LM308H	PM308AJ+
LM308N	PM308P
LM324AD	OP421GY
LM324D	OP421HY
LM339AD	CMP04FY+
LM339AN	CMP04FP+
LM339D	CMP04FY+
LM339N	CMP04FP+
LM348D	OP11FY
LM348N	OP11FP
SSS725BJ	OP06BJ+
SSS725EJ	OP06EJ+
SSS725J	OP06AJ+
SSS741CJ	OP02CJ
SSS741J	OP02J
SSS747CK	OP04CK
SSS747CY	OP04CY
SSS747K	OP04K
SSS747Y	OP04Y
SSS1408A-6Q	DAC1408A-6Q
SSS1408A-7Q	DAC1408A-7Q
SSS1408A-8Q	DAC1408A-8Q
SSS1508A-8Q	DAC1508A-8Q

ADI	PMI
AD108AH	PM108AJ
AD108H	PM108J
AD208AH	PM208AJ
AD208H	PM208J
AD308AH	PM308AJ
AD308AN	PM308AP
AD308H	PM308J
AD308N	PM308P
AD381JH	OP15FJ*
AD381KH	OP15EJ*
AD381SH	OP15BJ*
AD381TH	OP15AJ*
AD517JH	OP07DJ*
AD517KH	OP07CJ*
AD517LH	OP07EJ*
AD517SH	OP07AJ*
AD540JH	OP15GJ
AD540KH	OP15FJ
AD540SH	OP15BJ
AD644CH	OP215EJ
AD644JH	OP215GJ
AD644KH	OP215FJ
AD644SH	OP215AJ
AD741CH	OP02DJ
AD741CN	OP02DP
AD741JH	OP02CJ+
AD741JN	OP02CP+
AD741KH	OP02CJ
AD741KN	OP02CP
AD741LH	OP02EJ*
AD741LN	OP02EP*
AD741H	OP02BJ
AD741SH	OP02J
AD1408-7D	DAC1408A-7Q
AD1408-8D	DAC1408A-8Q
AD1508-8D	DAC1508A-8Q
AD7506JN	MUX16ET*
AD7506KN	MUX16ET*
AD7507JN	MUX28ET*
AD7507KN	MUX28ET*
AD7506JD	MUX16ET*
AD7506KD	MUX16ET*
AD7507JD	MUX28ET*
AD7507KD	MUX28ET*

+Direct replacement with improved specifications

*Identical pinout, some electrical differences, direct replacement in most applications

DIRECT REPLACEMENT GUIDE

ADI	PMI
AD7506SD	MUX16BT*
AD7506TD	MUX16BT*
AD7507SD	MUX28BT*
AD7507TD	MUX28BT*
AD7510DIJD	SW7510FQ*
AD7510DIKD	SW7510FQ*
AD7510DISD	SW7510BQ*
AD7511DIJD	SW7511FQ*
AD7511DIKD	SW7511FQ*
AD7511DISD	SW7511BQ*
AD7511DITD	SW7511BQ*
ADDAC08AD	DAC08AQ
ADDAC08CD	DAC08CQ
ADDAC08D	DAC08Q
ADDAC08ED	DAC08EQ
ADDAC08HD	DAC08HQ
ADDAC100JD	DAC100BCQ7
ADDAC100KD	DAC100ABQ7
ADDAC100LD	DAC100AAQ7
ADDAC100SD	DAC100BCQ5
ADG200AA	SW05BK*
ADG200AP	SW05BY*
ADG200BA	SW05FK*
ADG200BP	SW05FY*
ADG200CJ	SW05GP*
ADG201AP	SW01BQ*
ADG201BP	SW01FQ*
ADG201CJ	SW01FQ*
ADOP07AH	OP07AJ
ADOP07CH	OP07CJ
ADOP07CN	OP07CP
ADOP07DH	OP07DJ
ADOP07DN	OP07CP
ADOP07EH	OP07EJ
ADOP07EN	OP07EP
ADOP07H	OP07J

BURR BROWN	PMI
MPC4D	MUX24FQ*
MPC8D	MUX28FQ*
MPC8S	MUX08FQ*
MPC16S	MUX16FQ*

EXAR	PMI
XR083CN	OP215FY+
XR083CP	OP215GY+
XR083DN	OP215FY+
XR083DP	OP215GY+
XR083M	OP215BY+
XR083N	OP215CY+
XR083P	OP215CY+
XR3403CN	OP11GY*
XR3403CP	OP11GP*
XR3503M	OP11BY*
XR4136CN	OP09FY+
XR4136M	OP09BY+
XR4212CN	OP421HY*
XR4212CP	OP421HY*
XR4212M	OP421CY*
XRC277	RPT82FQ+

FAIRCHILD	PMI
DAC08CDC	DAC08CQ
DAC08CPC	DAC08CP
DAC08DM	DAC08Q
DAC08DMQB	DAC08Q/883
DAC08EDC	DAC08EQ
DAC08EPC	DAC08EP
DAC1408ADC	DAC1408A-8Q
DAC1408APC	DAC1408A-8P
DAC1408BDC	DAC1408A-7Q
DAC1408BPC	DAC1408A-7P
DAC1408CDC	DAC1408A-6Q
DAC1408CPC	DAC1408A-6Q
DAC1508DM	DAC1508A-8Q
μA108AH	PM108AJ
μA108H	PM108J
μA124DM	OP421BY
μA139ADM	PM139AY
μA139DM	PM139Y
μA148DM	OP11AY
μA208AH	PM208AJ
μA208H	PM208J
μA224DC	OP421FY
μA248DC	OP11BY
μA308AH	PM308AJ
μA308H	PM308J
μA324DC	OP421HY
μA339ADC	PM339AY
μA348DC	OP11FY
μA348PC	OP11FP
μA714EHC	OP07EJ
μA714HC	OP07CJ
μA714HM	OP07AJ+
μA714LHC	OP07DJ+
μA725HC	PM725CJ
μA725HM	PM725J
μA725TC	PM725CP
μA741AHM	OP02AJ+
μA741EHC	OP02EJ+
μA741HC	OP02CJ
μA741HM	OP02J
μA741RC	OP02DP
μA741TC	OP02CP
μA747ADM	OP04AK+
μA747AHM	OP04AY+
μA747CM	OP04Y
μA747DC	OP04CY
μA747EDC	OP04EY+
μA747EHC	OP04EK+
μA747HC	OP04CK
μA747HM	OP04BK
μA747IDC	OP04CY
μA747IDM	OP04AY+
μA747IHC	OP04K
μA747IHM	OP04K
μA747PC	OP04DY+
μA772ARC	OP215EZ
μA772ARM	OP215BZ
μA772BRC	OP215FZ
μA772BRM	OP215CZ
μA772RC	OP215GZ
μA776C	OP22HZ
μA776HC	OP22HJ
μA776HM	OP22BJ
μA1458CHC	OP14CJ+
μA1458CRC	PM1458Z
μA1458CTC	OP14DP
μA1458HC	OP14EJ+
μA1458TC	OP14CP
μA3303PC	OP11FP
μA3403DC	OP11GY

+Direct replacement with improved specifications

*Identical pinout, some electrical differences, direct replacement in most applications

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FAIRCHILD	PMI
µA3403PC	OP11FP
µA4136DC	OP09FY
µA4136DM	OP09BY
µA4136PC	OP09GP
µAF155AHM	PM155AJ
µAF155AHM	OP15AJ+
µAF155HM	PM155J
µAF155HM	OP15BJ+
µAF156AHM	PM156AJ
µAF156HM	PM156J
µAF156HM	OP16BJ+
µAF157AHM	PM157AJ
µAF157AHM	OP17AJ+
µAF157HM	PM157J
µAF157HM	OP17BJ+
µAF355AHC	PM355AJ
µAF355AHC	OP15EJ+
µAF355HC	OP15FJ+
µAF356AHC	OP16EJ+
µAF356AHM	PM356AJ
µAF356HM	OP16FJ+
µAF357AHM	PM357AJ
µAF357AHM	OP17EJ+
µAF357HM	OP17FJ+

HARRIS	PMI
HA2-2650-2	OP215BJ*
HA2-2655-5	OP215FJ*
HA4-4602-2	OP11AY*
HA4-4605-5	OP11EY*
HA-5082AH-5	OP215EJ
HA-5082AJ-5	OP215EZ
HA-5082BH-5	OP215FJ
HA-5082BJ-5	OP215FZ
HA-5082H-2	OP215J
HA-5082H-5	OP215HJ
HA-5082J-2	OP215BZ
HA2-5130-2	OP07AJ*
HA2-5130-5	OP07EJ*
HA7-5130-2	OP07AZ*
HA7-5130-5	OP07EZ*
HA2-5135-2	OP07J*
HA2-5135-5	OP07EJ*
HA7-5135-2	OP07Z*
HA7-5135-5	OP07EZ*

HARRIS	PMI
HA-5142H-2	OP221AJ
HA-5142H-5	OP221EJ
HA-5142J-2	OP221AZ
HA-5142J-5	OP221EZ
HI-200D-2	SW05BY*
HI-200D-4	SW05FY*
HI-200H-5	SW05GP*
HI-200T-2	SW05BK*
HI-200T-4	SW05FK*
HI-201E-2	SW201BQ*
HI-201E-4	SW201FQ*
HI-201J-5	SW201GP*
HI1-506A-2	MUX16BT*
HI1-506A-5	MUX16ET*
HI1-506-2	MUX16BT*
HI1-506-5	MUX16FT*
HI1-507-2	MUX28BT*
HI1-507-5	MUX28ET*
HI1-507A-2	MUX28AT*
HI1-507A-5	MUX28ET*
HI-516N-2	MUX28BT*
HI-516N-5	MUX28FT*
HI1-1840-2	MUX16BT*
HI1-1840-5	MUX16ET*
HI3-506A-5	MUX16ET*
HI3-506-5	MUX16FT*
HI3-507A-5	MUX28ET*
HI3-507-5	MUX28FT*
HI3-508A-5	MUX08EP*
HI3-509A-5	MUX24EP*
HI4-508A-2	MUX08BQ*
HI4-508A-5	MUX08EQ*
HI4-509A-2	MUX24BQ*
HI4-509A-5	MUX24FQ*
HI-516N-2	MUX28BT*
HI-516N-5	MUX28FT*
LF155AH	PM155AJ
LF155AJ	PM155AZ
LF155H	PM155J
LF156AH	PM156AJ
LF156AJ	PM156AZ
LF156H	PM156J
LF156J	PM156Z
LF157AH	PM157AJ
LF157AJ	PM157AZ
LF157H	PM157J
LF157J	PM157Z

HARRIS	PMI
LF353AH	OP215EJ
LF353BH	OP215FJ
LF353H	OP215GJ
LF355AH	PM355AJ
LF355AJ	PM355AZ
LF355BJ	OP15FZ
LF355BH	OP15FJ
LF355H	OP15GJ
LF355J	OP15GZ
LF356AH	PM356AJ
LF356AJ	PM356AZ
LF356H	OP16FJ
LF356J	OP16FZ
LF357AH	PM357AJ
LF357AJ	PM357AZ
LF357H	OP17FJ
LF357J	OP17FZ
LM108AH	PM108AJ
LM108AJ-8	PM108AZ
LM108H	PM108J
LM108J-8	PM108Z
LM148AJ	OP11AY*
LM148J	OP11BY*
LM308AH	PM308AJ
LM308AJ-8	PM308AZ
LM308H	PM308J
LM308J-8	PM308Z
LM348AJ	OP11EY*
LM348AN	OP11EP*
LM348J	OP11FY*
LM348N	OP11FP*
LM1458AH	OP14EJ+
LM1458AJ-8	OP14EZ+
LM1458AN	OP14EP+
LM1458N	OP14GP+
LM1558AH	OP14AJ+
LM1558AJ	OP14AZ+
LM2908J	OP421HY
LM2908N	OP421HY
LM4250CH	OP22HJ
LM4250CJ	OP22HZ
LM4250CN	OP22HZ
LM4250H	OP22BJ
LM4250J	OP22BZ
OP07AJ	OP07AJ
OP07J	OP07J

+Direct replacement with improved specifications
*Identical pinout, some electrical differences, direct replacement in most applications

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MCE	PMI
MCE6012ADC	DAC312ER
MCE6012DC	DAC312FR
MCE6012DM	DAC312BR

MPS	PMI
MP200DIAAD	SW05BY*
MP200DIAAH	SW05BK*
MP200DIAPH	SW05BK*
MP200DIBAD	SW05FY*
MP200DIBAH	SW05FK*
MP200DIBPD	SW05FY*
MP200DIBPH	SW05FK*
MP200DIBPN	SW05GP*
MP200DICJN	SW05GP*
MP201DIAPD	SW201BQ*
MP201DIBPD	SW201FQ*
MP201DICJN	SW201GP*
MP4136CY	OP09FY+
MP4136Y	OP09BY+
MP5509EP	OP09EY
MP5560ACQ7	DAC100ACQ7
MP7506JD	MUX16ET*
MP7506JN	MUX16FT*
MP7506KD	MUX16ET*
MP7506KN	MUX16FT*
MP7506SD	MUX16BT*
MP7506TD	MUX16BT*
MP7507JD	MUX28ET*
MP7507JN	MUX28FT*
MP7507KD	MUX28ET*
MP7507KN	MUX28FT*
MP7507SD	MUX28BT*
MP7507TD	MUX28BT*
MP7508DIJD	MUX08EQ*
MP7508DIJN	MUX08EP*
MP7508DIKD	MUX08EQ*
MP7508DISD	MUX08AQ*
MP7509DIJD	MUX24EQ*
MP7509DIJN	MUX24EP*
MP7509DIKD	MUX24EQ*
MP7509DIKN	MUX24EP*
MP7509DISD	MUX24AQ*
MP7510DIJD	SW7510FQ*
MP7510DISD	SW7510BQ*
MP7510DITD	SW7510BQ*

MOTOROLA	PMI
LF155AH	PM155AJ
LF155AJ	PM155AZ
LF155H	PM155J
LF155J	PM155Z
LF156AH	PM156AJ
LF156AJ	PM156AZ
LF156H	PM156J
LF156J	PM156Z
LF157AH	PM157AJ
LF157AJ	PM157AZ
LF157H	PM157J
LF157J	PM157Z
LF355AH	PM355AJ
LF355AJ	PM355AZ
LF355AN	PM355AZ+
LF355BH	PM355AJ+
LF355BJ	PM355AZ+
LF355BN	PM355AZ+
LF356AH	PM356AJ
LF356AJ	PM356AZ
LF356AN	PM356AZ+
LF356BH	PM356AJ+
LF356BJ	PM356AZ+
LF356BN	PM356AZ+
LF357AH	PM357AJ
LF357AJ	PM357AZ
LF357AN	PM357AZ+
LF357BH	PM357AJ+
LF357BJ	PM357AZ+
LF357BN	PM357AZ+
LM108AD	PM108AZ
LM108AH	PM108AJ
LM108D	PM108Z
LM108H	PM108J
LM208AD	PM208AZ
LM208AH	PM208AJ
LM208AN	PM208AZ+
LM208D	PM208Z
LM208H	PM208J
LM208N	PM208Z+
LM308AD	PM308AZ
LM308AH	PM308AJ
LM308AN	PM308AP
LM308D	PM308Z
LM308H	PM308J
LM308N	PM308P

MOTOROLA	PMI
LM139AJ	PM139AY
LM339AJ	PM339AY
LM339AN	CMP04FP
LM339N	CMP04FP+
MC1400AU5	REF02EZ
MC1400AU10	REF01EZ
MC1400U5	REF02HZ
MC1400U10	REF01HZ
MC1404AU5	REF02CZ
MC1404AU10	REF01CZ
MC1404U5	REF02DZ
MC1404U10	REF01DZ
MC1500U5	REF02AZ
MC1500U10	REF01AZ
MC1504U5	REF02BZ
MC1504U10	REF01BZ
MC1408L6	DAC1408A-6Q
MC1408L7	DAC1408A-7Q
MC1408L8	DAC1408A-8Q
MC1458CG	OP14CJ+
MC1458CP1	OP14CP+
MC1458CU	OP14CZ+
MC1458G	OP14CJ+
MC1458NP1	OP14EP+
MC1458NU	OP14EZ+
MC1458P1	OP14DP
MC1458U	OP14DZ
MC1508L8	DAC1508A-8Q
MC1558NG	OP14AJ+
MC1558NU	OP14AZ+
MC1558G	OP14J
MC1558U	OP14Z
MC1741CG	OP01CJ+
MC1741CP1	OP01CP+
MC1741CU	OP01CZ+
MC1741G	OP01J+
MC1741NCG	OP01HJ+
MC1741NCP1	OP01HZ+
MC1741NCU	OP01FZ+
MC1741NG	OP01J+
MC1741NU	OP01Z+
MC1741U	OP01Z+
MC1747CG	OP14EJ+
MC1747CL	OP04EY+
MC1747CP2	OP04EY+
MC1747G	OP14AJ+
MC1747L	OP04AY+

+Direct replacement with improved specifications

*Identical pinout, some electrical differences, direct replacement in most applications

DIRECT REPLACEMENT GUIDE

MOTOROLA	PMI
MC1776CG	OP22HJ+
MC1776CP1	OP22HZ+
MC1776CU	OP22HZ+
MC1776G	OP22AJ+
MC1776U	OP22AZ+
MC3403L	OP11FY
MC3403P	OP11FP
MC4558ACP1	OP215EZ+
MC4558CG	OP215FJ+
MC4558CP1	OP215GZ+
MC4558CU	OP215FZ+
MC4558G	OP215BJ+
MC4558U	OP215BZ+
MC4741CL	OP420FY
MC4741CP	OP420HY
MC4741L	OP11AY+
MC34001AG	OP15EJ+
MC34001AP	OP15EZ+
MC34001AU	OP15EZ+
MC34001BG	OP15FJ+
MC34001BP	OP15FZ+
MC34001BU	OP15FZ+
MC34001G	OP15GJ+
MC34001P	OP15GZ+
MC34001U	OP15GZ+
MC34002AG	OP215EJ+
MC34002AP	OP215EZ+
MC34002AU	OP215EZ+
MC34002BG	OP215FJ+
MC34002BP	OP215FZ+
MC34002BU	OP215FZ+
MC34002G	OP215GJ+
MC34002P	OP215GZ+
MC34002U	OP215GZ+
MC35001AG	OP15AJ+
MC35001AU	OP15AZ+
MC35001BG	OP15GJ+
MC35001BU	OP15BZ+
MC35002AG	OP215AJ+
MC35002AU	OP215AZ+
MC35002BG	OP215BJ+
MC35002BU	OP215BZ+

NATIONAL	PMI
DAC0800LCJ	DAC08EQ
DAC0800LCN	DAC08EP
DAC0801LCJ	DAC08CQ
DAC0801LCN	DAC08CP
DAC0802LCJ	DAC08HQ
DAC0802LCN	DAC08HP
DAC0806LCJ	DAC1408A-6Q
DAC0806LCN	DAC1408A-6P
DAC0807LCJ	DAC1408A-7Q
DAC0807LCN	DAC1408A-7P
DAC0808LCJ	DAC1408A-8Q
DAC0808LCN	DAC1408A-8P
DAC0808LD	DAC1508A-8Q
LF155AH	PM155AJ
LF155AH	OP15AJ+
LF155H	PM155J
LF155H	OP15BJ+
LF156AH	PM156AJ
LF156AH	OP16AJ+
LF156H	PM156J
LF156H	OP16BJ+
LF157AH	PM157AJ
LF157AH	OP17AJ+
LF157H	PM157J
LF157H	OP17BJ+
LF351H	OP15FJ
LF351N	OP15FZ+
LF353H	OP215FJ
LF353N	OP215FZ+
LF355AH	PM355AJ
LF355AH	OP15EJ+
LF356AH	PM356AJ
LF357AH	PM357AJ
LF357N	PM357Z+
LF411ACH	OP15EJ
LF411ACN	OP15EZ
LF411AMH	OP15AJ
LF411CH	OP15FJ
LF411CN	OP15GZ
LF412ACH	OP215EJ
LF412ACN	OP215EZ
LF412AMH	OP215AJ
LF412CH	OP215FJ
LF412CN	OP215GZ+
LF412MH	OP215BJ

NATIONAL	PMI
LF441ACH	OP21EJ
LF441ACN	OP21EP
LF441AMH	OP21AJ
LF441CH	OP21FJ
LF441CN	OP21FP
LF442ACH	OP221EJ*
LF442ACN	OP221FZ*
LF442AMH	OP221AJ*
LF442CH	OP221GJ*
LF442CN	OP221GZ*
LM124AJ	OP421BY
LM124J	OP421CY
LM224AJ	OP421FY
LM224J	OP421GY
LM324AN	OP421HY+
LM324J	OP421HY
LM148J	OP11BY
LM158AH	OP221AJ
LM158H	OP221BJ
LM248J	OP11CY
LM258AH	OP221EJ
LM258H	OP221FJ
LM348J	OP11GY
LM348N	OP11GP
LM358AH	OP221GJ
LM358H	OP221GJ
LM358N	OP221GZ+
LM2902J	OP421HY
LM2902N	OP421HY
LM2904N	OP221GZ+
LM4250H	OP22AJ
LM4250CH	OP22FJ
LM4250CN	OP22HZ
LM4250CJ	OP22FZ
LM4250J	OP22BJ
LF11201D	SW201BQ
LF11202D	SW202BQ
LF11333D	SW06BQ
LF11508D	MUX08AQ+
LF11509D	MUX24AQ+
LF12201D	SW201FQ
LF12201N	SW201FQ
LF12202D	SW202FQ
LF12202N	SW202FQ
LF12333D	SW06FQ
LF12333N	SW06FQ

+Direct replacement with improved specifications
*Identical pinout, some electrical differences, direct replacement in most applications

DIRECT REPLACEMENT GUIDE

NATIONAL	PMI
LF13201D	SW201FQ+
LF13201N	SW201GP
LF13202D	SW202FQ
LF13202N	SW202GP
LF13508D	MUX08EQ+
LF13508N	MUX08EP+
LF13509D	MUX24EQ+
LF13509N	MUX24EP+
LF13333D	SW06FQ+
LF13333N	SW06GP
LM108AH	PM108AJ
LM108H	PM108J
LM139AD	PM139AY
LM148J	OP11AY*
LM158AH	OP220AJ+
LM158H	OP220BJ+
LM194H	MAT01AH*
LM208AH	PM208AJ
LM208H	PM208J
LM239AD	CMP04FY
LM248J	OP11BY*
LM258AH	OP220EJ+
LM258H	OP220FJ+
LM308AH	PM308AJ
LM308AN	PM308AP
LM308H	PM308J
LM308N	PM308P
LM339AD	PM339AY
LM339AN	CMP04FP+
LM339D	PM339AY
LM348J	OP11FY*
LM348N	OP11FP*
LM358AH	OP220GJ+
LM358AN	OP220HZ+
LM358H	OP220HJ+
LM358N	OP220HZ+
LM394H	MAT01AH*
LM394CH	MAT01GH*
LM725AH	OP06AJ+
LM725CH	OP06EJ+
LM725CN	OP06GZ+
LM725H	OP06BJ+
LM741AH	OP02AJ+
LM741CH	OP02EJ+
LM741CJ	OP02EZ+

NATIONAL	PMI
LM741CN	OP02CP+
LM741EN	OP02EP+
LM741H	OP02J
LM747AH	OP04K
LM747AJ	OP04AY+
LM747CH	OP04CK
LM747CJ	OP04CY
LM747CN	OP04DY+
LM747EH	OP04EK+
LM747EJ	OP04EY+
LM747EN	OP04CY+
LM747H	OP04BK
LM747J	OP04Y
LM1458H	OP14CJ+
LM1458J	OP14CZ+
LM1458N	OP14CP
LM2901J	CMP04BY*
LM2904N	OP220HZ*
LM3302N	CMP04FP*

NEC	PMI
µPC151C	OP02CZ
µPC151D	OP02BZ+
µPC154D	OP05CZ
µPC156D	PM208Z
µPC251C	OP14EP+
µPC251D	OP14EZ+
µPC254D	OP05CZ
µPC258C	OP215FZ+
µPC258D	OP215EZ+
µPC259C	OP215FZ+
µPC339C	CMP04FP+
µPC354D	OP07CZ
µPC358C	OP220HZ+
µPC454D	OP10CY
µPC458C	OP11FP*
µPC610D	DAC02CCX
µPC624C	DAC08EP
µPC624D	DAC08EQ
µPC648D	DAC312FR
µPC741C	OP02CP
µPC801C	OP15FZ+
µPC803C	OP215GZ+
µPC803D	OP215EZ+

NEC	PMI
µPC1251C	OP220GZ+
µPC1251D	OP220FZ+
µPC4082C	OP215FZ+
µPC4281C	OP15GZ+
µPC4558C	OP215GZ+
µPC4560C	OP215GZ+
µPC4741C	OP11GP*

RCA	PMI
CA108AT	PM108AJ
CA108T	PM108J
CA158AT	OP220AJ+
CA158T	OP220BJ+
CA208AT	PM208AJ
CA208T	PM208J
CA258AT	OP220EJ+
CA258T	OP220FJ+
CA308AT	PM308AJ
CA308E	PM308P
CA308T	PM308J
CA358AG	OP220HJ+
CA358AT	OP220GJ+
CA358G	OP220HJ+
CA358T	OP220HJ+
CA741CE	OP02CZ+
CA741CG	OP02CZ+
CA741CS	OP02CJ
CA741CT	OP02CJ
CA741S	OP02AJ+
CA741T	OP02AJ+
CA747CE	OP04CY+
CA747CG	OP04CY+
CA747CT	OP04CK
CA747T	OP04K
CA1458E	OP14CP
CA1458G	OP14EP+
CA1458S	PM14EJ
CA1458T	OP14CJ
CA1558S	OP14J
CA1558T	OP14J
CA2904G	OP220HJ+

+Direct replacement with improved specifications
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DIRECT REPLACEMENT GUIDE

RAYTHEON	PMI
DAC08ADM	DAC08AQ
DAC08CDC	DAC08CQ
DAC08DM	DAC08Q
DAC08EDC	DAC08EQ
DAC08HDC	DAC08HQ
DAC10BDM	DAC10BX
DAC10CDM	DAC10CX
DAC10FDC	DAC10FX
DAC10GDC	DAC10GX
DAC6012ADC	DAC312BR+
DAC6012ADM	DAC312FR+
DAC6012DC	DAC312FR
DAC6012DM	DAC312BR
LM108AH	PM108AJ
LM108H	PM108J
LM139D	PM139Y
LM208AH	PM208AJ
LM208H	PM208J
LM308AH	PM308AJ
LM308H	PM308J
LM339N	CMP04FP+
RC725T	PM725CJ
RC741DP	OP02CP+
RC741T	OP02DJ
RC747DB	OP04DY+
RC747T	OP04CK
RC1458NB	OP14CP
RC3302DB	CMP04FP*
RC4136DB	OP09FP
RC4136DC	OP09BY+
RC4558NB	OP215GZ+
RC4558T	OP215CJ+
RM725T	PM725J
RM741T	PM741J
RM747DC	OP04Y
RM4136DC	OP09BY+
RM4558T	OP215BJ+
RM4805ADE	CMP05AZ
RM4805DE	CMP05BZ

SIGNETICS	PMI
AM6012F	DAC312FR
DAC08AF	DAC08AQ
DAC08CF	DAC08CQ
DAC08CN	DAC08CP
DAC08EF	DAC08EQ
DAC08F	DAC08Q
DAC08HC	DAC08HP
DAC08HF	DAC08HQ
LF355H	OP15FJ
LF355N	OP15GZ+
LF356H	OP15FJ
LF356N	OP15GZ+
LM124F	OP421BY
LM139F	PM139Y
LM139N	CMP04BY+
LM158FE	OP221AZ
LM158H	OP221AJ
LM224F	OP421FY
LM224N	OP421GY
LM239N	CMP04FY+
LM258FE	OP221FZ
LM258H	OP221FJ
LM258N	OP221FZ
LM324F	OP421HY
LM324N	OP421HY
LM339N	CMP04FP+
LM358H	OP221GJ
LM2901F	CPM04FY+
LM2901N	CMP04FP+
MC1408-7F	DAC1408A-7Q
MC1408-8F	DAC1408A-8Q
MC1458N	OP14CP
MC1508-8F	DAC1508A-8Q
MC3302N	CMP04FP
MC3303F	OP420HY
MC3303N	OP420HY
MC3403F	OP420FY
MC3403N	OP420HY
MC3503F	OP420BY
NE532FE	OP220HZ+
NE532H	OP220HJ+
NE532N	OP220HZ+
NE535FE	OP15GZ
NE535H	OP15GJ
NE4558FE	OP215GZ
NE4558N	OP215GZ
NE5007F	DAC08CQ
NE5008F	DAC08EQ
NE5009F	DAC08HQ
NE5514F	OP421HY
NE5514N	OP421HY
NE5535H	OP215GJ
NE5535N	OP215GZ
SA532N	OP220GZ+
SA741CN	OP02BZ+
SA747CN	OP04BY+
SA1458N	OP14BZ+
SA4558FE	OP215BZ
SA4558N	OP215CZ+
SE532FE	OP220BZ+
SE532H	OP220BJ+
SE535FE	OP15Z
SE535H	OP15GJ
SE5008F	DAC08Q
SE5009F	DAC08AQ
SE5514F	OP421CY
SE5535H	OP215BJ
SE5535N	OP215BZ+
μA741CFE	OP02CZ
μA741CN	OP02DZ+
μA741N	OP02BZ+
μA747CN	OP04DY+
μA747F	OP04Y

SILICONIX	PMI
DG200AA	SW05BK*
DG200AP	SW05BY*
DG200BA	SW05FK*
DG200BP	SW05FY*
DG200CJ	SW05GP*
DG201AAK	SW01BQ*
DG201ABK	SW01FQ*
DG201AP	SW201BQ*
DG201BP	SW201FQ*
DG201CJ	SW201GP*
DG202AK	SW202BQ*
DG202BK	SW202FQ*
DG202CK	SW202FQ*
DG202CJ	SW202GP*
DG506AR	MUX16AT*
DG506BR	MUX16ET*
DG506CJ	MUX16FT*
DG507AR	MUX28AT*
DG507BR	MUX28ET*

+Direct replacement with improved specifications

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DIRECT REPLACEMENT GUIDE

SILICONIX	PMI
DG507CJ	MUX28FT*
DG508AP	MUX08AQ*
DG508BP	MUX08EQ*
DG508CJ	MUX08FP*
DG509AP	MUX24AQ*
DG509BP	MUX24EQ*
DG509CJ	MUX24FP*

TELEDYNE	PMI
TSC9495CE	REF02HJ
TSC9495CJ	REF02HP
TSC9495EE	REF02EJ
TSC9496CE	REF01HJ
TSC9496CJ	REF01HP
TSC9496EE	REF01EJ

TI	PMI
LM139AJ	PM139AY
LM139J	PM139Y
LM158JG	OP220AZ+
LM239N	CMP04FY+
LM258JG	OP220EZ+
LM258P	OP220GZ+
LM339AJ	PM339AY
LM339AN	CMP04FP+
LM358JG	OP220HZ+
LM358P	OP220HZ+
LM2901J	CMP04BY+
LM2904N	OP220HZ+
LM3302N	CMP04FP+
MC1458P	OP14CP
MC3403J	OP11FY*
MC3403N	OP11FP*
MC3503J	OP11BY*
RC4136J	OP09FY+
RC4136N	OP09FP+
RC4558JG	OP215CZ+
RC4558P	OP215GZ+
RM4136J	OP09BY+
RM4558JG	OP215BZ+
TL022CJG	OP220HZ+
TL022CP	OP220HZ+
TL022MJG	OP220BZ+

TI	PMI
TL081ACJG	OP16EZ+
TL081ACP	OP16FZ+
TL081BCJG	OP16FZ+
TL081BCP	OP16GZ+
TL081CJG	OP16GZ+
TL081MJG	OP16BZ+
TL088CJG	OP16EZ+
TL088MJG	OP16AZ+
TL322IP	OP220GZ+
μA741CJG	PM741CZ
μA741CP	OP02CP
μA741IP	OP02BZ+
μA747CJ	OP04CY
μA747CN	OP04DY
μA747MJ	OP04Y

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FUNCTIONAL REPLACEMENT GUIDE

AMD	PMI	PMI DIFFERENCES
AM685	CMP05	Higher accuracy, lower speed
AM686	CMP05	Higher accuracy, lower speed
AM6080	DAC888	Faster settling, simplified microprocessor interfacing
LF198	SMP11	Higher speed, accuracy
LF398	SMP11	Higher speed, accuracy
LM110	BUF03	Lower input bias, higher slew rate, bandwidth
LM112	OP12	Internal compensation, no nulling capabilities
SSS747	OP03	Higher gain, improved input specifications

ADI	PMI	PMI DIFFERENCES
AD108D	PM108Z	Packaged in hermetic DIP
AD503	OP15	Wider bandwidth
AD504	OP05	No compensation required externally
AD507	OP17	Internally compensated
AD508	OP02	Lower cost
AD509	OP16	No compensation required externally
AD510	OP05	Lower input-bias-current, higher long-term stability
AD517	OP07	Higher accuracy, greater stability
AD518	OP01	Inverting gains only
AD524	AMP01	Lower noise, superior output drive capabilities
AD542	OP15	Higher slew-rate, bandwidth, higher supply current
AD544	OP15	Higher speed, gain, bandwidth
AD545	OP15	Faster, lower noise, higher input bias current
AD547	OP15	Wider bandwidth
AD558	DAC888	Faster, multiplying
AD559	DAC08	Multiplying
AD561	DAC100	M.C.R. reference
AD580	REF01/02	Higher stability, lower noise, lower cost
AD581	REF01/02	Better temperature stability, lower cost
AD582	SMP10/11	Faster acquisition time, higher accuracy
AD583	SMP10/11	Lower droop rate, pin-for-pin $A_V = 1$
AD590	REF02	Monolithic, voltage output
AD2700	REF01	Monolithic, lower power consumption
AD7110	DAC88	Higher resolution
AD7501	MUX08	BIFET, overvoltage protected
AD7502/03	MUX08	BIFET, overvoltage protected
AD7520/30/33	DAC10	Bipolar, higher compliance
AD7524	DAC888	Bipolar, higher speed

The PMI components listed in this guide are functionally equivalent. The devices differ in pinout or specifications.

FUNCTIONAL REPLACEMENT GUIDE

BURR BROWN	PMI	PMI DIFFERENCES
BB3500	OP15	V_{OS} 0.5mV, TCV_{OS} 5μV/C
BB3501	OP15	Null to V+, $f_t = 4$MHz
BB3505	OP16	Highest speed applications
BB3506	OP15/16/17	Medium speed applications
BB3510	OP07	Pin compatible, 25μV V_{OS}
BB3521	OP15	Null to V+, 10V/μs slew rate
BB3542	OP15	Null to V+, 10V/μs slew rate
BB3550	OP15	Null to V+, 10V/μs slew rate
INA101	AMP01	Superior D.C. performance, greater linearity

EXAR	PMI	PMI DIFFERENCES
XR4136CP	OP09FP	Higher accuracy, gain, lower speed
XR4741CN	OP11FY	Higher accuracy, gain, lower speed
XR4741CP	OP11FP	Higher accuracy, gain, lower speed
XR4741M	OP11BY	Higher accuracy, gain, lower speed

FAIRCHILD	PMI	PMI DIFFERENCES
μA108D	PM108Z	Packaged in hermetic MINI-DIP
μA198-398	SMP11	Higher speed, accuracy
μA734	CMP01	Higher accuracy, higher speed
F4051	MUX08	Lower leakage, higher R_{ON}, BIFET, O.V. protected
F4052	MUX24	Lower leakage, higher R_{ON}, BIFET, O.V. protected

HARRIS	PMI	PMI DIFFERENCES
HA909	OP37	Higher accuracy, lower noise, faster
HA911	OP37	Higher accuracy, lower noise, faster
HA1600/02/05	REF01	Higher I_{OUT}, lower power consumption
HA1608	REF01	Higher accuracy, lower noise
HA1610/15	REF01	Higher input range, lower noise, lower cost
HA2420/25	SMP10/11	Superior D.C. specs, lower noise, lower cost, pin-for-pin $A_V = 1$
HA2500/02/05	OP17	Higher accuracy, gain, slew rate
HA2507	OP17	Higher accuracy, gain, slew rate
HA2510/12/15	OP15/16/17	Superior D.C. specs, lower speed, lower cost
HA2600/02/05	OP16	Superior D.C. specs, higher speed
HA2604U	OP215Z	Packaged in hermetic DIP
HA2654U	OP215Z	Packaged in hermetic DIP
HA2720	OP22	Pin-for-pin, superior D.C. specs, higher gain, lower speed
HA2725	OP22	Pin-for-pin, superior D.C. specs, higher gain, lower speed
HA4741	OP11	Pin-for-pin, higher gain, lower speed
HA4900	CMP04	Higher accuracy, lower power consumption, lower speed

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FUNCTIONAL REPLACEMENT GUIDE

HARRIS	PMI	PMI DIFFERENCES
HA4920	CMP04	Higher accuracy, lower power consumption, lower speed
HA4950	CMP05	Superior D.C. specs, lower speed
HA5082	OP215	Pin-for-pin, higher speed, higher supply current
HA5100	OP16	Higher gain, slew rate
HA5105	OP16	Higher gain, slew rate
HA5110	OP17	Higher gain, slew rate
HA5115	OP17	Higher gain, slew rate
HA5130	OP07	Higher stability, lower speed
HA5135	OP07	Higher stability, lower speed
HA5320	SMP11	Equivalent specifications, $A_V = 1$
HI201	SW201	BIFET, overvoltage protected
HI516	MUX16/28	BIFET, overvoltage protected
HI518	MUX08/24	BIFET, overvoltage protected
HI1080/85	DAC208	Faster settling, packaged in 16-pin DIP
HI1800A	SW06	BIFET, overvoltage protected
HI1818A	MUX08	BIFET, overvoltage protected
HI1828A	MUX24	BIFET, overvoltage protected
HI5042	SW06	BIFET, overvoltage protected
HI5043	SW06	BIFET, overvoltage protected
HI5045	SW7510	BIFET, overvoltage protected
HI5046	SW06	BIFET, overvoltage protected
HI5047	SW7510	BIFET, overvoltage protected
HI5049	SW01	BIFET, overvoltage protected
HI5050	SW06	BIFET, overvoltage protected
HI5051	SW06	BIFET, overvoltage protected
HI5610	DAC10	Higher compliance, lower cost
HI5618A	DAC08	Higher compliance, lower power, lower speed
HI5618B	DAC08	Higher compliance, lower power, lower speed
LM5141	OP21	Lower slew rate, higher supply current

MPS	PMI	PMI DIFFERENCES
MP561	DAC100	M.C.R. reference
MP7501	MUX08	BIFET, overvoltage protected
MP7502/03	MUX08	BIFET, overvoltage protected
MP7520	DAC10	Bipolar, higher compliance
MP7523	DAC10	Bipolar, higher compliance
MP7524	DAC888	Bipolar, higher speed
MP7530	DAC10	Bipolar, higher compliance

The PMI components listed in this guide are functionally equivalent. The devices differ in pinout or specifications.

FUNCTIONAL REPLACEMENT GUIDE

MOTOROLA	PMI	PMI DIFFERENCES
LM158	OP207	Higher accuracy, gain
MC1403	REF02	Higher stability, higher output drive
MC1406	DAC01	Complete, voltage output
MC1430/31	OP01	Higher accuracy, faster, lower power
MC1435	OP207	Higher accuracy, gain, internally compensated
MC1437	OP207	Superior D.C. specs, internally compensated
MC1439	OP17	Faster, internally compensated
MC1456	OP27	Faster, lower noise
MC1500AU5	REF05AJ	Packaged in TO-99
MC1500AU10	REF10AJ	Packaged in TO-99
MC1504AU5	REF05BJ	Packaged in TO-99
MC1504AU10	REF10BJ	Packaged in TO-99
MC3510	DAC100	Higher stability, on-board reference
MC6890	DAC888	Lower cost

NATIONAL	PMI	PMI DIFFERENCES
AD7520/30	DAC10	Bipolar, higher compliance
DAC0830/31	DAC888	Bipolar, higher speed
DAC1000	DAC888	8-Bits, lower cost
DAC1020/21	DAC10	Bipolar, higher compliance
LF198-398	SMP11	Higher speed, accuracy
LF11331	SW04	Overvoltage protected, constant R_{ON}
LH0002	BUF03	Monolithic, higher accuracy, higher speed
LH0023	SMP11	Monolithic, higher accuracy, faster acquisition time
LH0033	BUF03	Monolithic, lower cost, reduced slew rate
LH0044	OP27	Monolithic, lower noise, higher speed
LH0053	SMP11	Monolithic, higher accuracy, faster acquisition
LM11	OP21	Higher accuracy, gain, lower power
LM102-302	BUF03	Higher accuracy, bandwidth, slew rate
LM110	BUF03	Lower input bias, higher slew rate, bandwidth
LM112	OP12	Internally compensated
LM118-318	OP01	Internally compensated, inverting only
LM135-335	REF02	Higher accuracy, lower noise
LM136-336	REF05	Higher accuracy, stability, lower noise
LM163	AMP01	Lower noise, faster settling, higher output drive
LM199-399	REF01/02	Lower power
LM4250	OP22	Pin-for-pin, superior D.C. specs, gain, lower speed

The PMI components listed in this guide are functionally equivalent. The devices differ in pinout or specifications.

FUNCTIONAL REPLACEMENT GUIDE

NEC	PMI	PMI DIFFERENCES
μPC253	OP22	Superior D.C. specs, internally compensated
μPC4250	OP22	Superior D.C. specs, gain, lower speed

RCA	PMI	PMI DIFFERENCES
CA4250	OP22	Superior performance, different programming

RAYTHEON	PMI	PMI DIFFERENCES
RM1556	OP215	BIFET, superior A.C. & D.C. performance
RM5532	OP227	Superior D.C. specs, lower noise, reduced B.W., output drive

SIGNETICS	PMI	PMI DIFFERENCES
LF198-398	SMP11	Higher speed, accuracy, superior specifications
MC1456	OP27	Faster, lower noise
NE530	OP17	BIFET, faster, A_{VCL} greater than 5
NE531	OP01	Higher accuracy, inverting gains only
NE5018/19	DAC888	Higher speed, M.C.R. reference, current output
NE5118/19	DAC888	Higher speed, M.C.R. reference
NE5532	OP227	Superior D.C. specs, higher gain, lower speed
NE5534	OP37	Superior D.C. specs, higher gain, lower noise
NE5535	OP215	BIFET, wider bandwidth
NE5537	SMP11	Higher accuracy, faster acquisition

SILICONIX	PMI	PMI DIFFERENCES
DG243	SW06	BIFET, overvoltage protected
DG5042	SW06	BIFET, overvoltage protected
DG5043	SW06	BIFET, overvoltage protected
DG5045	SW7510	BIFET, overvoltage protected

TI	PMI	PMI DIFFERENCES
NE5532	OP227	Superior D.C. specs, higher gain, lower speed
NE5534	OP37	Superior D.C. specs, higher gain, lower noise
TL044	OP421	Higher speed, lower noise, higher supply current
TL070-71	OP15	Pin-for-pin, higher speed, lower noise, higher supply current
TL072	OP215	Pin-for-pin, higher speed, lower noise, higher supply current
TL080	OP16	Superior D.C. specs, higher speed
TL082	OP215	Pin-for-pin, higher speed, higher supply current
TL510	CMP05	Superior D.C. specs, slower response time
TL191	SW06	BIFET, overvoltage protected

The PMI components listed in this guide are functionally equivalent. The devices differ in pinout or specifications.

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OPERATIONAL AMPLIFIERS

INTRODUCTION

Precision Monolithics pioneered in the development of low-offset, high-gain operational amplifiers for use in precision applications. A proprietary linear bipolar process with nitride passivation was developed to achieve low noise, enhanced long-term reliability, and improved resistance to radiation effects. PMI operational amplifier processing capability includes JFET and super-beta devices as well as standard NPN and PNP devices. A zener-zap trimming technique was designed to reduce input offset voltage at the wafer testing stage. Offset trimming is performed in discrete steps by applying high-current pulses through automatically-selected zener diodes. High-current pulsing shorts the zener which is parallel-connected to a trim resistor. Zener-zap trimming provides a very reliable and stable reduction of input offset voltage. PMI has developed many innovative operational-amplifier circuit designs based on their low-noise, low-drift processing in combination with zener-zap offset trimming.

The table below summarizes the PMI families of operational amplifiers. All feature low input offset voltage, low drift, and high open-loop gain.

Operational Amplifiers

General Purpose, Bipolar Input	
OP-02	Singles
OP-04, OP-14	Duals
OP-09, OP-11	Quads
OP-01	High Speed, Inverting
General Purpose, BIFET Input	
PM-155, PM-156, PM-157	Standard BIFETs
38510 Versions	MIL-Grade, 38510
Precision, High-Speed BIFET Input	
OP-15, OP-16, OP-17, OP-215 (Dual)	Improved BIFETs
High Accuracy	
OP-05, OP-06, OP-07	Low V_{OS}, High Gain
OP-27, OP-37	Low V_{OS}, Low Noise
OP-227, OP-207	Duals
OP-08, OP-12	Low I_B, Low Power
Low Power, Low Input-Bias-Current	
PM-108/208/308, PM-2108 (Dual)	Low I_B, LM-108 Type
Micropower	
OP-20/21	Singles, Low I_{SY}
OP-22/32	Programmable
OP-220, OP-221	Duals
OP-420, OP-421	Quads

DEFINITIONS

Average Bias Current Drift (TCI_B) — The ratio of change in input bias current to a change in temperature.

Average Offset Current Drift (TCI_{OS}) — The ratio of change in input offset current to a change in temperature.

Average Offset Voltage Drift (TCV_{OS}) — The ratio of change in input offset voltage to a change in temperature.

Average Offset Voltage Drift With External Trimming (TCV_{OSN}) — The ratio of the change in input offset voltage to a change in temperature with the input offset voltage trimmed to zero at room temperature.

Common-Mode Input Resistance (R_{InCM}) — The ratio of input voltage range to the change in input bias current over this range.

Common-Mode Rejection Ratio (CMRR) — The ratio of the common-mode voltage range (CMVR) to the peak-to-peak change in equivalent input offset voltage (CME) over this range. CMRR is specified for a specific CMVR.

$CMRR = 20 \log_{10} (CMVR/CME)$

OPERATIONAL AMPLIFIERS

Gain-Bandwidth Product (GBW) — The frequency at which the open-loop gain equals unity.

Input Bias Current (I_B) — The average of the currents into the two input terminals when the output is at zero volts with no load. I_B is measured at $V_{CM} = 0$.

Input Noise Current ($i_{np\text{-}p}$) — The peak-to-peak noise current within a specified frequency band.

Input Noise Current Density (i_n) — The rms noise current in a 1Hz band centered on a specified frequency.

Input Noise Voltage ($e_{np\text{-}p}$) — The peak-to-peak noise voltage within a specified frequency band.

Input Noise Voltage Density (e_n) — The rms noise voltage in a 1Hz band centered on a specified frequency.

Input Offset Current (I_{OS}) — The difference between the currents into the two input terminals when the output is at zero volts with no load.

Input Offset Voltage (V_{OS}) — The voltage which must be applied between the input terminals to obtain zero output voltage with no load.

Input Resistance-Differential Mode (R_{IN}) — The ratio of small-signal change in input voltage to a change in input current at either input terminal with the other grounded.

Input Voltage Range (IVR) — The range of input voltage for which the device will operate as a linear amplifier.

Large-Signal Voltage Gain (A_{VO}) — The ratio of change in output voltage (over a specified range) to a change in input voltage.

Open-Loop Output Resistance (R_O) — The small-signal driving-point resistance of the output terminal with respect to ground at a specified quiescent DC output voltage and current.

Output Voltage Swing (V_O) — The peak output voltage that can be obtained without clipping into a specified load resistance.

Power Dissipation (P_d) — The total power dissipated in the amplifier with the output at zero volts with no load.

Power Supply Rejection Ratio (PSRR) — The inverse ratio of change in input offset voltage to a change in power supply voltage. PSRR can be specified in dB or μV/V.

Slew Rate (SR) — The ratio of a change in output voltage to the minimum time required to effect this change under large-signal drive conditions. Slew rate may be specified separately for positive and negative-going changes.

Supply Current (I_{SY}) — The current required from the power supply to operate the amplifier with no load and the output at zero volts.

Unity-Gain Closed-Loop Bandwidth (BW) —The frequency at which the magnitude of the small-signal voltage gain of the amplifier, operated closed-loop as a unity-gain follower, is 3dB below unity.

MATCHING PARAMETER DEFINITIONS

Input Offset Voltage Match (ΔV_{OS}) — The difference between the offset voltages of side A and side B (V_{OSA} - V_{OSB}). If $V_{OSA} = V_{OSB}$, the net differential offset voltage at the output of the amplifier pair equals zero.

Input Offset Voltage Tracking ($TC\Delta V_{OS}$) — The ratio of change in ΔV_{OS} to a change in temperature.

Average Noninverting Bias Current (I_B+) — The average of the side A and side B noninverting input bias currents:

$$\frac{I_{BA}+ + I_{BB}+}{2}$$

Noninverting Input Offset Current ($I_{OS}+$) — The difference between the noninverting input bias currents of side A and side B; ($I_{BA}+ - I_{BB}+$).

Inverting Input Offset Current ($I_{OS}-$) — The difference between the inverting input bias currents of side A and side B; ($I_{BA}- - I_{BB}-$).

Average Drift Of Noninverting Bias Current (TCI_{B+}) — The ratio of change in noninverting bias current to a change in temperature.

Average Drift of Noninverting Offset Current ($TCI_{OS}+$) — The ratio of change in noninverting offset current to a change in temperature.

Common-Mode Rejection-Ratio Match (ΔCMRR) — The difference between the common-mode rejection ratios (expressed in volt/volt of side A and side B. ΔCMRR in dB = $20 \log_{10}$ (ΔCMRR in volt/volt).

Power Supply Rejection-Ratio Match (ΔPSRR) — The difference between the power supply rejection ratios (expressed in volt/volt) of side A and side B. ΔPSRR in dB = $20 \log_{10}$ (ΔPSRR in volt/volt).

Channel Separation — The ratio of change in offset voltage of one channel to a change in output voltage in the second channel.

SELECTION PRINCIPLES

Selecting an operational amplifier can be a frustrating experience. The choice of circuit configuration, and of associated component values, interrelates to the choice of op amp for a given application. Op amps are specified as open-loop devices, but in a circuit application they generally have feedback applied. The designer must predict the closed-loop circuit performance as determined by his choice of op amp and choice of circuit configuration (and component tolerances). Detailed literature is available on circuit configurations to accomplish particular analog circuit functions using op amps. This Selection Guide gives recommended guidelines and a design strategy for selecting op amps to best meet your needs.

The first design steps are to:

1. Completely define the design objectives.

Input Signal — Determine the signal level, frequency content, and impedance of the input.

Accuracy Required — For linear amplification, this consists of limits for offset, gain error, and nonlinearity. Establish your bandwidth and slew rate needs. Distortion is often critical for audio use and fast settling may be essential in a data-conversion application.

Output Load — Op amps are sometimes called upon to drive long cables, storage capacitors, transformers, or other semiconductors. High-speed circuits generally require low-impedance feedback elements and the load is usually low impedance; therefore, relatively high output current drive is needed for high-speed circuits.

Environmental Conditions — Temperature range and power supply characteristics are very important factors. Power supply drain is often critical in battery-powered equipment, process control systems, and satellites. In addition, op-amp package type is generally dictated by environmental and cost factors. Another factor to consider is the *electrical environment.* Minimize accuracy degradation from unavoidable ground noise and power supply fluctuations by choosing an op amp with high CMRR and PSRR.

2. Use the published op-amp specifications and characterization graphs.

PMI provides comprehensive specification tables with well-defined test conditions for operation at 25° C and over specific temperature ranges. The "Typical Performance Curves" show the characteristic response of an op amp to variations in frequency, temperature, supply voltage, or load impedance. Since op amps often perform much better than indicated by their min/max specification limits, the designer may be tempted to ask for special selection to tighter limits. Although sometimes necessary, special selection tends to be costly. A better strategy is to select a standard op amp that meets the application need on a worst-case basis. Careful initial selection of a high-performance standard op amp will provide predictable circuit performance on a continuing basis.

OPERATIONAL AMPLIFIERS

Selection Process
Operational amplifiers can be divided into four basic functional categories:

Category	Primary Characteristics
General Purpose	"741" types.
High Accuracy	Low input offsets ($V_{OS} < 1mV$), high DC gain, high CMRR, and low noise. Leading part types are OP-05, OP-07, and OP-27.
High Speed	Optimized for high slew rate, high gain-bandwidth, and fast settling time.
Low Power, Wide Supply Range	Low supply drain ($I_{SY} < 1mA$), wide input and output voltage range. Includes micropower ($I_{SY} < 100\mu A$) units for battery operation.

There can be overlap between some categories, while others are mutually exclusive. For example, the PMI OP-22 covers both "High Accuracy" and "Low Power". However, "High Speed" and "Low Power" tend to be mutually exclusive; it is difficult to simultaneously optimize both speed and power.

Economics is another important dimension of the selection process. The "General Purpose" category is generally lowest in cost, but a "High Accuracy" op amp with low input-offset-voltage may be more cost effective if it eliminates the need for external trimming components. The PMI high-accuracy OP-07 is often used in place of general-purpose 741-types because of its low input-offset-voltage and high gain.

AC Considerations
Consideration of AC requirements for an application is a good starting point in the op amp selection process. If high frequency ($GBW > 10MHz$, $SR > 10V/\mu s$) is the primary concern, then the choice quickly narrows down to the "High Speed" category.

Two factors will generally dictate the op amp choice:

1. The loop gain (excess of open-loop gain over closed-loop gain) must be sufficient at the highest frequency of interest. For example, if 1.0% accuracy at 10kHz is required when operating at closed-loop gain of 10, then the op amp must have an open-loop gain of at least 1000 at 10kHz (10/1000 = 1%). When operating at high closed-loop gains, decompensated op amps generally offer the advantage of better gain bandwidth product without a price/performance penalty.

2. Slew rate must be high enough to follow the fastest signal input without causing distortion or other anomalies. Slew-rate symmetry, linearity, and overload recovery should be considered. The detrimental effects of slew-rate limiting can be subtle; it is best to avoid trouble by choosing an op amp with at least a 20% safety margin in minimum slew-rate.

High speed implies a need for high output current. Applications such as audio amplifiers, active filters, DAC-output amplifiers, and fast integrators often require high output currents for driving feedback capacitors or low-impedance networks. Driving such capacitive loads as long cables or storage capacitors at high frequency requires high output currents.

DC Considerations
If the frequency requirements are relatively modest ($SR < 10V/\mu s$) and the circuit requires closed-loop gain above unity, choose a "High Accuracy" op amp. These op amps feature:

Low Input Offsets	
Low Input Offset Voltage	$V_{OS} \leq 1mV$, $TCV_{OS} \leq 2\mu V/°C$
Low Input Bias Current	
— Bipolar Input Stage	$I_B \leq 100nA$ ($I_B \leq 10nA$ is desirable)
— BIFET Input Stage	$I_B \leq 200pA$

High Open-Loop DC Gain	$A_{VOL} \geq 200{,}000$
High Common-Mode Rejection	$CMRR \geq 100dB$
Low Input Noise at 100Hz	$e_n \leq 15nV/\sqrt{Hz}$

A leading op amp in the High-Accuracy category is the PMI OP-07 with these key specifications:

$V_{OS} \leq 75\mu V$
$I_B \leq \pm 3nA$, $I_{OS} \leq 2.8nA$
$A_{VOL} \geq 200{,}000$
$CMRR \geq 110dB$
$e_n \leq 13nV/\sqrt{Hz}$ at 100Hz

The OP-07 performs very well even at high closed-loop gains. For example, consider a noninverting configuration with a closed-loop gain of 100. Assume a signal source with a range of ±0.1V and source impedance of 10kΩ. If the feedback resistances are chosen to be relatively low, then the maximum offset caused by input bias current will be 4.4nA ($I_B + I_{OS}/2 = 4.4nA$) multiplied by the 10kΩ source resistance, or 44μV. Total input offset, even without external offset nulling, will be less than 119μV (approximately 0.12% of full-scale). The effect of CMRR is negligible in this example; the ±0.1V input divided by 110dB of common-mode rejection is only 0.3μV referred-to-input. Gain error factor is $1/(1 + A_{VCL}/A_{VOL})$, which is a gain error of approximately A_{VCL}/A_{VOL}. The DC gain error at A_{VCL} of 100 will be less than 100/200,000, a 0.05%-of-full-scale gain error. The worst-case sum of offset and gain errors for this example is only 0.17% of full-scale, and is achieved without any external trimming of offset or gain.

Selection of a specific op-amp type within the High-Accuracy category is generally determined by impedance levels of the input signal and feedback elements. High impedances ($R_S > 10k\Omega$) imply a need for an op amp with low input bias currents. This need for low bias current can be met through use of FET-input op amps, or by using bipolar-input op amps specifically designed for low input-bias-current.

The OP-05, OP-07, and OP-27 have input current-cancellation circuitry that significantly reduces input bias current, while the OP-08 relies on superbeta input transistors to minimize input bias current. FET-input op amps have well under 1nA input bias current at 25° C, but the current rises with increasing temperature to values above the bipolar-input types. The OP-08, an improved LM108, has a superbeta input stage and is very good for high-temperature, high-impedance operation ($I_B \leq 3nA$ at 125° C). The OP-22, a programmable micropower op amp, has a PNP- input stage with very low input bias current. Input bias current is also very stable over temperature due to the PNP inputs.

Low noise, always desirable, is sometimes the primary consideration. In many high-gain active-filter or audio-amplifier applications, low noise can be more important than DC offset. These are the three basic rules for obtaining low noise:

1. Design with low impedances — Using low impedances minimizes the effect of current noise flowing through the source impedance, reduces resistor thermal noise, and reduces stray pick-up of RF noise.

2. Restrict the system bandwidth — Noise outside the frequency range of interest can usually be attentuated by filtering. Block high-frequency power-supply noise from the signal path by use of decoupling capacitors at the op-amp supply inputs.

3. Select a low-noise op amp — Some op amps, such as the bipolar-input OP-27, are designed for minimum noise. The input stage current is set to a relatively high value which reduces input noise ($5.5nV/\sqrt{Hz}$ max at 10Hz). Output swing is increased to ±10V into 600Ω to allow the use of low-impedance, low-noise feedback elements.

Power Supply Considerations

The op-amp power-supply requirements are the next factors to consider. If the circuit is to be operated from a battery, such as in portable instruments, missiles, or spacecraft, then narrow the selection to the "Low-Power, Wide Supply

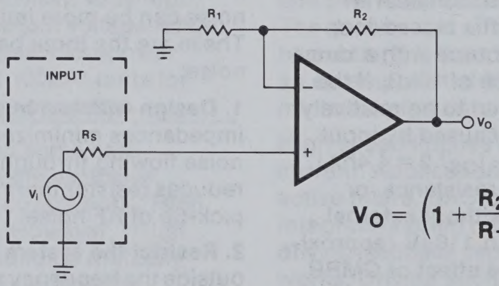
Range" category. Low-power op amps are designed for minimum quiescent supply current. Speed is traded off for lower power consumption and output drive is generally reduced. The input and output stages are designed for linear operation over a wide voltage range which is very helpful for single-power-supply operation.

The PMI line of low-power, wide-supply-range op amps all feature high open-loop gain, low input offsets, and high CMRR. They can provide high accuracy even at high closed-loop gain.

The low-power family includes *programmable* micropower op amps that offer the designer another dimension in circuit design. The quiescent supply current is set by an external resistor which allows the circuit designer to trade off quiescent supply current against speed. Since the quiescent current directly controls slew rate and gain-bandwidth product, these programmable op amps are easily frequency-compensated in such circuits as active filters, oscillators, or multi-stage instrumentation amplifiers.

DC ERROR CALCULATIONS FOR STANDARD CONFIGURATIONS

NONINVERTING CONFIGURATION



$$V_O = \left(1 + \frac{R_2}{R_1}\right) V_i$$

$$\text{Output Offset} = \left(1 + \frac{R_2}{R_1}\right) \left[V_{OS} + \left(\frac{R_1 R_2}{R_1 + R_2} - R_S\right) I_B + \left(\frac{R_1 R_2}{R_1 + R_2} + R_S\right) \frac{I_{OS}}{2} \right]$$

Special Cases:

$$\text{Max Output Offset} = \left(1 + \frac{R_2}{R_1}\right) \left(V_{OS} + R_S I_{OS}\right) \text{ if } R_S = \frac{R_1 R_2}{R_1 + R_2}$$

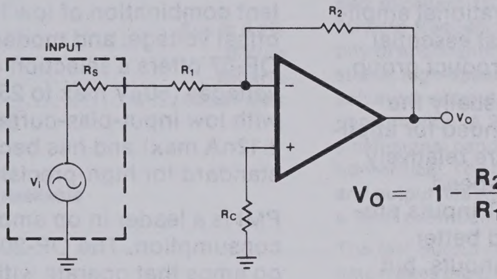
$$\sim \left(1 + \frac{R_2}{R_1}\right) \left[V_{OS} + \left| \frac{R_1 R_2}{R_1 + R_2} - R_S \right| I_B \right] \text{ if } I_{OS} \ll I_B$$

$$\sim \left(1 + \frac{R_2}{R_1}\right) \left[V_{OS} + R_S \left(I_B + \frac{I_{OS}}{2}\right) \right] \text{ if } R_S \gg \frac{R_1 R_2}{R_1 + R_2}$$

Note: I_B is the average of the input bias currents and I_{OS} is the difference.

$$\text{Gain Error} \sim \left(1 + \frac{R_2}{R_1}\right) \frac{1}{A_{VO}} + \frac{1}{CMRR}, \text{ where } A_{VO} = \text{Open-Loop Gain and } A_{VO} \gg \left(1 + \frac{R_2}{R_1}\right)$$

INVERTING CONFIGURATION



$$V_O = 1 - \frac{R_2}{R_1}\, V_i\,,\quad R_S \sim 0$$

$$\text{Output Offset} = \left(1 + \frac{R_2}{R_1}\right)\left[V_{OS} + \left(\frac{R_1 R_2}{R_1 + R_2} - R_C\right) I_B + \left(\frac{R_1 R_2}{R_1 + R_2} + R_C\right)\frac{I_{OS}}{2}\right] \text{ if } R_S \sim 0$$

Special Cases:

$$\text{Max Output Offset} = \left(1 + \frac{R_2}{R_1}\right)\left(V_{OS} + R_C\, I_{OS}\right) \text{ if } R_C = \frac{R_1 R_2}{R_1 + R_2}$$

$$\sim \left(1 + \frac{R_2}{R_1}\right)\left[V_{OS} + \left|\frac{R_1 R_2}{R_1 + R_2} - R_C\right| I_B\right] \text{ if } I_{OS} \ll I_B$$

$$\sim \left(1 + \frac{R_2}{R_1}\right)\left[V_{OS} + \frac{R_1 R_2}{R_1 + R_2}\left(I_B + \frac{I_{OS}}{2}\right)\right] \text{ if } R_C = 0$$

Note: I_B is the average of the input bias currents and I_{OS} is the difference.

$$\text{Gain Error} \sim \left(1 + \frac{R_2}{R_1}\right)\frac{1}{A_{VO}} + \frac{R_S}{R_1}\;\frac{R_2}{R_1}$$

, where A_{VO} = Open-Loop Gain and $R_S \ll R_1$

OPERATIONAL AMPLIFIERS

OPERATIONAL AMPLIFIER SELECTION GUIDE

The Operational Amplifier Selection Guide chart highlights PMI's line of operational amplifiers. The matrix indicates the most essential parametric differences for each product group.

"General Purpose" op amps are usually the least expensive and are recommended for applications where impedance levels are relatively low, closed-loop gain is low, and speed requirements are moderate. BIFET inputs provide lower input-bias-currents and better bandwidth than standard bipolar inputs, but input voltage offsets and noise are generally better for the bipolar input amplifiers.

The "High Accuracy" category presents the best amplifiers for high-gain applications. A combination of low input-offset-voltage, high open-loop gain, and high CMRR provide excellent DC accuracy even at high closed-loop gain. The OP-27/37 are best for minimum input voltage noise. The OP-08/12 provide an excellent combination of low input-bias-current, low offset voltage, and moderate power drain. The OP-07 offers a selection of the lowest offset voltages (60μV max to 250μV max) combined with low input-bias-current (±2nA max to ±12nA max) and has become an industry standard for high-precision applications.

PMI is a leader in op amps featuring low power consumption. The OP-20/21/22 are micropower op amps that operate with only a few microamps of supply drain. PSRR and CMRR are high, and the input-voltage-range is wide. Such features work together to make these amplifiers ideal for battery-powered applications or for operation from a single supply voltage. The OP-22 can be programmed to operate over any supply current from 1μA to 400μA and is excellent for battery-powered designs.

	General Purpose						Precision High Speed BIFET Input			High Accuracy				Low Power Low Input Bias Current		Micropower						
	Bipolar				BIFET																	
Monolithic Technology	OP-01	OP-02	OP-04, OP-14	OP-09, OP-11	PM-155	PM-156, PM-157	OP-15	OP-16, OP-17	OP-215	OP-05, OP-06, OP-07	OP-08, OP-12	OP-27, OP-37	OP-207, OP-227	PM-108	PM-2108	OP-20	OP-21	OP-22, OP-32	OP-220	OP-221	OP-420	OP-421
Bipolar Input	●	●	●	●						●	●	●	●	●	●	●	●	●	●	●	●	●
BIFET					●	●	●	●	●													
Packages																						
Single	●	●			●	●	●	●		●	●	●		●		●	●	●				
Dual			●						●				●		●				●	●		
Quad				●																	●	●
Low Offset, $V_{OS} \leq 1mV$	●			●			●	●	●	●	●	●	●			●	●	●	●	●		
Low Bias Current																						
$I_B < 100pA$					●	●																
$I_B < 2nA$							●	●	●		●			●	●							
High Gain, $A_{VOL} \geq 200,000$										●		●	●			●	●	●	●	●	●	
High Slew Rate, $SR \geq 10V/\mu s$	●					●		●				●										
Low Power																						
$I_{SY} \leq 1mA$/Amplifier											●			●	●		●			●		●
$I_{SY} \leq 100\mu A$/Amplifier																●		●	●		●	

INVERTING HIGH-SPEED OPERATIONAL AMPLIFIER

OP-01

FEATURES

- **Fast Settling Time** .... **1μs to 0.1%**
- **High Slew Rate** **18V/μs**
- **Power Bandwidth** **250kHz**
- **Low Power Consumption** .... **90mW Max**
- **Excellent DC Specifications**
- **Internally Compensated**
- **Ideal DAC Output Amplifier**
- **MIL-STD-883 Processing Available**
- **Fits Standard 741 Sockets**
- **Low Cost**

GENERAL DESCRIPTION

The OP-01 series of monolithic inverting high-speed operational amplifiers combines high slew rate, fast settling time and excellent DC input characteristics. An internal feed-forward frequency compensation network provides simplicity of application — no external capacitors are required for stable, high-speed performance. The fast output response is achieved without sacrifice of input bias current or power consumption. A 250kHz power bandwidth is attained with a small-signal bandwidth of only 2.5MHz, thus board layout is non-critical. The OP-01 is completely protected at both input and output, fits standard 741 sockets, and is offset nulled with a 10kΩ potentiometer.

The fast output response combined with excellent settling time makes the OP-01 ideal for use as a D/A converter output amplifier.

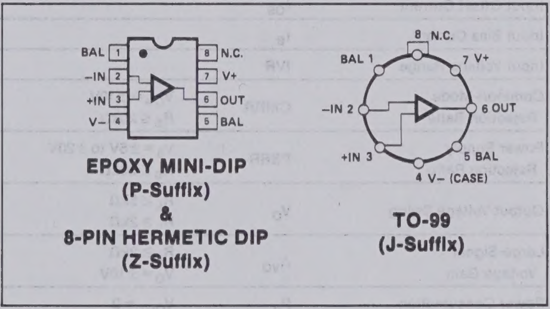
ORDERING INFORMATION†

$T_A = 25°C$ V_{OS} MAX (mV)	PACKAGE HERMETIC TO-99 8-PIN	HERMETIC DIP 8-PIN	PLASTIC DIP 8-PIN	OPERATING TEMPERATURE RANGE
0.7	OP01J*	OP01Z*		MIL
0.7	OP01HJ	OP01HZ	OP01HP	COM
5.0	OP01GJ*	OP01GZ*	—	MIL
5.0	OP01CJ	OP01CZ	OP01CP	COM

*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

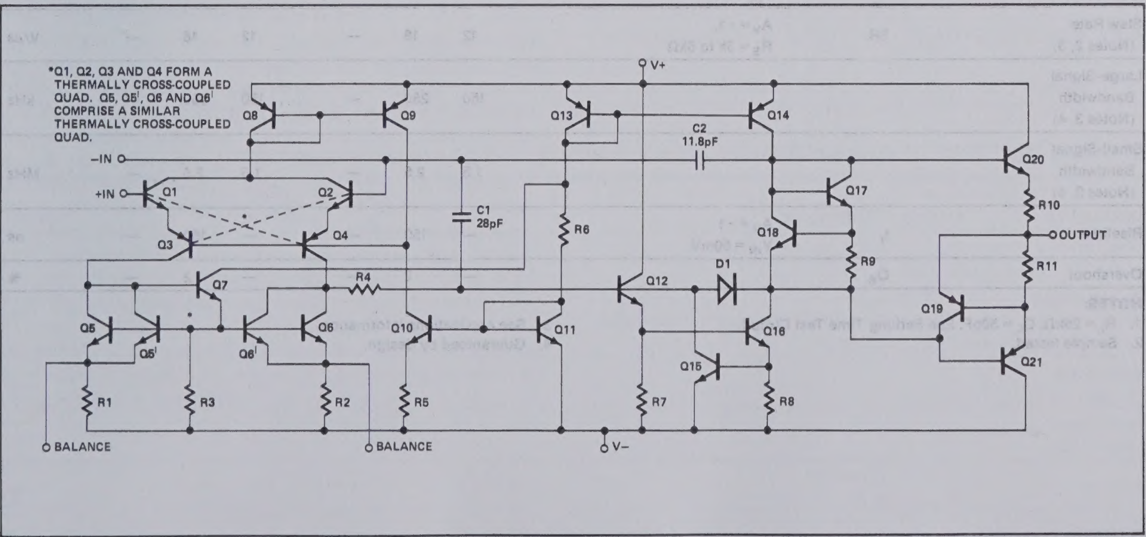
PIN CONNECTIONS


BAL 1
–IN 2
+IN 3
V– 4
5 BAL
6 OUT
7 V+
8 N.C.
8 N.C.
BAL 1
7 V+
–IN 2
6 OUT
+IN 3
5 BAL
4 V– (CASE)

EPOXY MINI-DIP (P-Suffix) & 8-PIN HERMETIC DIP (Z-Suffix)

TO-99 (J-Suffix)

SIMPLIFIED SCHEMATIC


*Q1, Q2, Q3 AND Q4 FORM A THERMALLY CROSS-COUPLED QUAD. Q5, Q5', Q6 AND Q6' COMPRISE A SIMILAR THERMALLY CROSS-COUPLED QUAD.
V+
–IN
+IN
Q1
Q2
Q3
Q4
Q5
Q5'
Q6'
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q19
Q20
Q21
C1 28pF
C2 11.8pF
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
D1
OUTPUT
BALANCE
BALANCE
V–

ABSOLUTE MAXIMUM RATINGS (Note 2)

Total Supply Voltage, OP-01, OP-01H, OP-01N, OP-01NT,
OP-01G, OP-01GT .... ±22V
OP-01G, OP-01C, OP-01GR .... ±20V
Power Dissipation (Note 1) 500mW
Differential Input Voltage .... ±30V
Input Voltage (Note 3) .... ±15V
Short-Circuit Duration .... Indefinite
Operating Temperature Range
OP-01, OP-01G .... −55° C to +125° C
OP-01H, OP-01C .... 0° C to +70° C
DICE Junction Temperature (T_j) .... −65° C to +150° C
Storage Temperature Range
J and Z Packages .... −65° C to +150° C
P Package .... −65° C to +125° C
Lead Temperature (Soldering, 60 sec) .... 300° C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80° C	7.1mW/° C
8-Pin Hermetic DIP (Z)	75° C	6.7mW/° C
8-Pin Plastic DIP (P)	35° C	5.6mW/° C

2. Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.
3. For supply voltages less than ±15V, the maximum input voltage is the supply voltage.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25° C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-01 OP-01H			OP-01G OP-01C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	—	0.3	0.7	—	2.0	5.0	mV
Input Offset Current	I_{OS}		—	0.5	2.0	—	2.0	20	nA
Input Bias Current	I_B		—	18	30	—	25	100	nA
Input Voltage Range	IVR		±12	±13	—	±12	±13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20k\Omega$	85	110	—	80	100	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$ $R_S \leq 20k\Omega$	—	10	60	—	100	150	μV/V
Output Voltage Swing	V_O	$R_L \geq 5k\Omega$ $R_L \geq 2k\Omega$	±12.5 ±12.0	±13.5 ±13.0	— —	±12.5 ±12.0	±13.5 ±13.0	— —	V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	50	100	—	25	75	—	V/mV
Power Consumption	P_d	$V_{OUT} = 0$	—	50	90	—	50	90	mW
Settling Time to 0.1% (Summing Node Error)	t_S	$A_V = -1$ (Notes 1, 2) $V_{IN} = 5V$	—	0.7	1.0	—	0.7	1.0	μs
Slew Rate (Notes 2, 3)	SR	$A_V = -1$, $R_S = 3k$ to $5k\Omega$	12	18	—	12	18	—	V/μs
Large-Signal Bandwidth (Notes 3, 4)			150	250	—	150	250	—	kHz
Small-Signal Bandwidth (Notes 3, 4)			1.5	2.5	—	1.5	2.5	—	MHz
Risetime	t_r	$A_V = -1$ $V_{IN} = 50mV$	—	150	—	—	150	—	ns
Overshoot	O_S		—	2	—	—	2	—	%

NOTES:

1. $R_L = 25k\Omega$; $C_L = 50pF$. See Settling Time Test Circuit.
2. Sample tested.
3. See applications information.
4. Guaranteed by design.

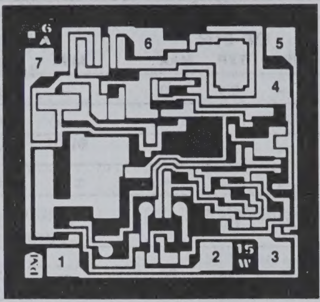
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \le T_A \le +125°C$ for OP-01, OP-01G and $0°C \le T_A \le +70°C$ for OP-01H, OP-01C, unless otherwise noted.

			OP-01 OP-01H			OP-01G OP-01C			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}	$R_S \le 20k\Omega$	—	0.4	1.0	—	3.0	6.0	mV
Input Offset Current	I_{OS}		—	1	4	—	4	40	nA
Input Bias Current	I_B		—	30	50	—	50	200	nA
Input Voltage Range	IVR		±10	±13	—	±10	±13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \le 20k\Omega$	85	110	—	80	100	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$ $R_S \le 20k\Omega$	—	10	60	—	100	150	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$ $V_O = \pm 10V$	30	60	—	15	50	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 5k\Omega$ $R_L \ge 2k\Omega$	±12.5 ±12.0	±13.5 ±13.0	— —	±12.5 ±12.0	±13.5 ±13.0	— —	V
Offset Voltage Drift (Note 1)	TCV_{OS}	$R_S \le 5k\Omega$	—	2	8	—	5	20	μV/°C

NOTE:

1. Sample tested.

DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)



DIE SIZE 0.046 × 0.042 inch, 1932 sq. mils
(1.17 × 1.07 mm, 1.25 sq. mm)

1. NULL
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V−
5. NULL
6. OUTPUT
7. V+

For additional DICE information refer to Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$ for OP-01N, OP-01G and OP-01GR devices; $T_A = 125°C$ for OP-01NT and OP-01GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-01NT LIMIT	OP-01N LIMIT	OP-01GT LIMIT	OP-01G LIMIT	OP-01GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	1.0	0.7	3.0	2.0	5.0	mV MAX
Input Offset Current	I_{OS}		4	2	10	5	20	nA MAX
Input Bias Current	I_B		50	30	100	50	100	nA MAX
Input Voltage Range	IVR		±10	±12	±10	±12	±12	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20k\Omega$	85	85	80	80	80	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$ $R_S \leq 20k\Omega$	60	60	100	100	150	μV/V MAX
Output Voltage Swing	V_{OM}	$R_L \geq 5k\Omega$ $R_L \geq 2k\Omega$	±12.5 ±12.0	±12.5 ±12.0	±12.5 ±12.0	±12.5 ±12.0	±12.5 ±12.0	V MIN
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	30	50	25	50	25	V/mV MIN
Power Consumption	P_d	$V_{OUT} = 0$	—	90	—	90	90	mW MAX

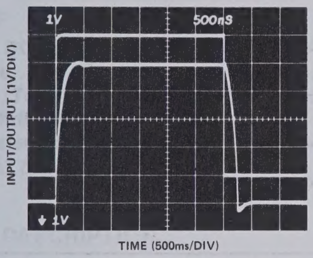
NOTE: For 25° C characteristics of NT & GT devices, see N & G characteristics respectively.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

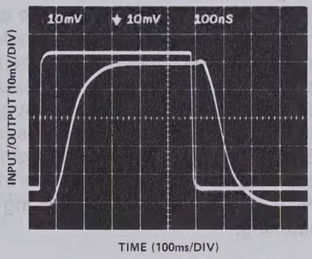
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	ALL GRADES TYPICAL	UNITS
Slew Rate	SR	$A_{VCL} = -1$, $R_S = 3k\Omega$ to $5k\Omega$	18	V/μs
Settling Time to 0.1% (Summing Node Error)	t_S	$V_{IN} = 5V$ $A_V = -1$ $R_L = 2k\Omega$ (See Settling Time Test Circuit) $C_L = 50pF$	1.0	μs
Large-Signal Bandwidth			250	kHz
Small-Signal Bandwidth			2.5	MHz
Risetime	t_r	$V_{IN} = 50mV$ $A_V = -1$	150	ns

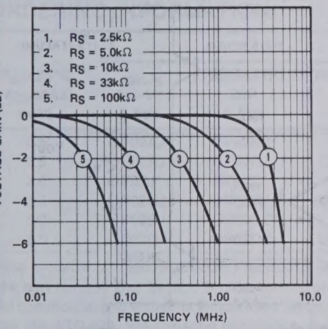
TYPICAL PERFORMANCE CHARACTERISTICS

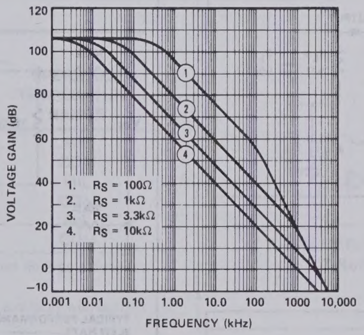

LARGE-SIGNAL PULSE RESPONSE

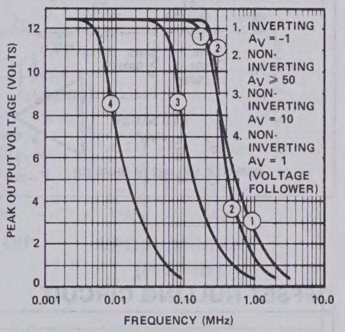
$V_S = \pm15V, A_V = -1, R_L = 2k\Omega, C_L = 50pF$


SMALL-SIGNAL PULSE RESPONSE

$V_S = \pm15V, A_V = -1, R_L = 2k\Omega, C_L = 50pF$


UNITY-GAIN BANDWIDTH vs SOURCE RESISTANCE

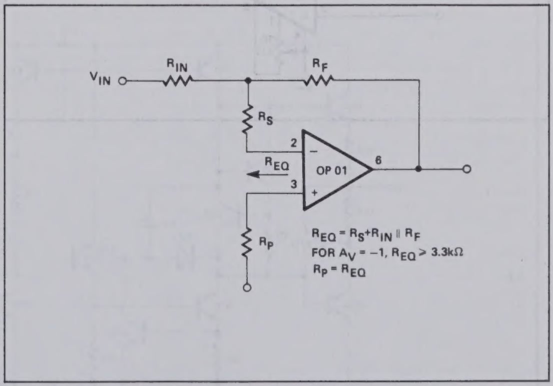

OPEN-LOOP GAIN vs FREQUENCY


LARGE-SIGNAL OUTPUT SWING vs FREQUENCY

APPLICATIONS INFORMATION

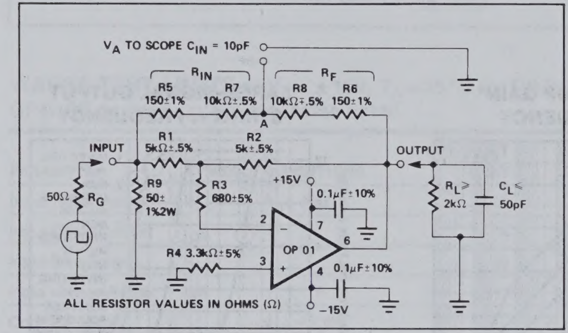
The OP-01 incorporates an internal feed-forward compensation network to provide fast slewing and settling times in all inverting and moderate-to-high-gain noninverting applications. Unity-gain bandwidth is a function of the total equivalent source resistance seen by the inverting terminal. Proper choice of this resistance will allow the user to maxmize bandwidth while assuring proper stability. The equivalent-inverting-terminal-resistance is defined as $R_{IN} \| R_F$, and it must be greater than 3.3kΩ to assure stability in all closed-loop gain configurations including unity gain. Should $R_{IN} \| R_F \leq 3.3k\Omega$, a resistor ($R_S$) may be placed between the nverting input and the sum node to provide the required esistance. (See Fast Inverting Amplifier Diagram.) Lower alues of total equivalent resistance may be used to improve andwidth in higher closed-loop gain configurations, as ndicated by the Open-Loop Gain vs. Frequency plot.

FAST INVERTING AMPLIFIER

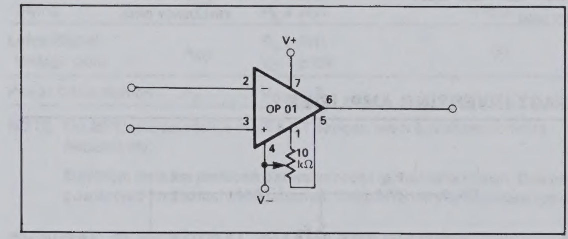


SETTLING-TIME TEST CIRCUIT

Settling time may be measured using the circuit shown below. This circuit incorporates the "false sum node" technique to produce accurate, repeatable results. For a 5V input step, 0.1% settling will be achieved when the false sum node settles to within ±2.5mV of its final value. The oscilloscope used for observation of the false sum node should have wide bandwidth, fast overload recovery time, and be used with a low capacity probe (≤ 10pF, including strays). A Tektronix 7504 scope with a 7A11 probe or equivalent is suggested. The pulse generator should have a 50Ω output impedance and be capable of a 5V rise time in ≤ 20ns with ringing less than 2.5mV after 0.5μs. Measurements to 0.1% require R_{IN} to equal R_F within 0.01%; R_5 and R_6 are used as trimming resistors to achieve this matching.

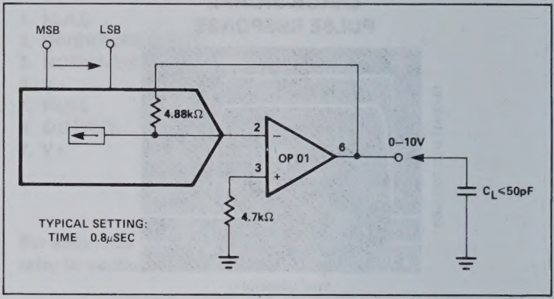

V_A TO SCOPE C_IN = 10pF
R_IN
R_F
R5 150±1%
R7 10kΩ±.5%
R8 10kΩ±.5%
R6 150±1%
A
INPUT
R1 5kΩ±.5%
R2 5k±.5%
OUTPUT
50Ω
R_G
R9 50± 1%2W
R3 680±5%
+15V
0.1μF±10%
R_L ≥ 2kΩ
C_L ≤ 50pF
2
7
6
3
4
OP 01
R4 3.3kΩ±5%
0.1μF±10%
−15V
ALL RESISTOR VALUES IN OHMS (Ω)

OFFSET NULLING CIRCUIT

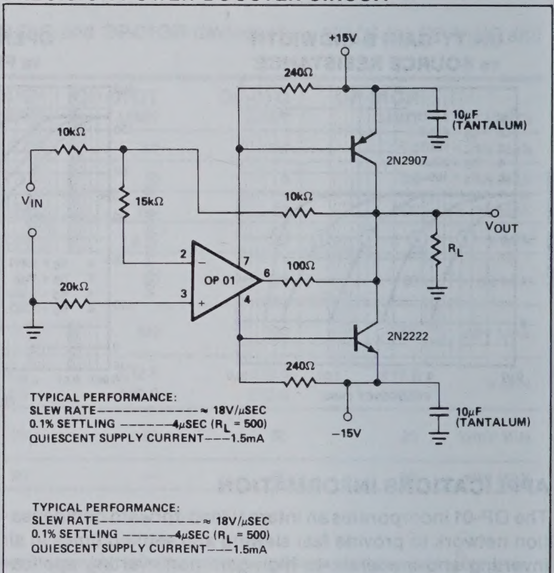

V+
2
7
6
3
5
OP 01
1
4
10 kΩ
V−

TYPICAL APPLICATIONS

FAST VOLTAGE-OUTPUT D/A CONVERTER


MSB
LSB
4.88kΩ
2
3
6
OP 01
0–10V
C_L<50pF
4.7kΩ
TYPICAL SETTING:
TIME 0.8μSEC

PRECISION POWER-BOOSTER CIRCUIT


+15V
240Ω
10μF (TANTALUM)
10kΩ
2N2907
V_IN
15kΩ
10kΩ
V_OUT
R_L
2
7
6
3
4
OP 01
100Ω
20kΩ
2N2222
240Ω
−15V
10μF (TANTALUM)

TYPICAL PERFORMANCE:
SLEW RATE————————≈ 18V/μSEC
0.1% SETTLING ————4μSEC (R_L = 500)
QUIESCENT SUPPLY CURRENT——1.5mA

TYPICAL PERFORMANCE:
SLEW RATE————————≈ 18V/μSEC
0.1% SETTLING ————4μSEC (R_L = 500)
QUIESCENT SUPPLY CURRENT——1.5mA

GENERAL-PURPOSE OPERATIONAL AMPLIFIER

OP-02

FEATURES

- **Excellent DC Specifications**
- **Low Noise .... 0.65$\mu V_{p\text{-}p}$**
- **Low Drift (TCV_{OS}) .... 8μV/° C Max**
- **Silicon-Nitride Passivation**
- **125° C Tested Dice Available**
- **"Premium" 741 Replacement**

GENERAL DESCRIPTION

This high-performance general-purpose operational amplifier provides significant improvements over industry-standard and "premium" 741 types while maintaining pin-for-pin compatibility, ease of application, and low cost. Key specifications, such as V_{OS}, I_{OS}, I_B, CMRR, PSRR, and A_{VO} are guaranteed over the full operating temperature range. Precision Monolithics' exclusive Silicon-Nitride "Triple Passivation" process reduces "popcorn noise." A thermally-symmetrical input-stage design provides low input offset voltage drift and insensitivity to output load conditions.

The OP-02 is a direct replacement for the 741. It is ideal for upgrading existing designs where accuracy improvements are required and for eliminating special low-drift or low-noise selected types.

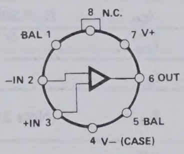
ORDERING INFORMATION†

T_A = 25° C V_{OS} MAX (mV)	PACKAGE TO-99 8-PIN	 HERMETIC DIP 8-PIN	 PLASTIC DIP 8-PIN	OPERATING TEMPERATURE RANGE
0.5	OP02AJ*	OP02AZ*		MIL
0.5	OP02EJ	OP02EZ	OP02EP	COM
2.0	OP02J*	OP02Z*		MIL
2.0	OP02CJ	OP02CZ	OP02CP	COM
5.0	OP02BJ*	OP02BZ*		MIL
5.0	OP02DJ	OP02DZ	OP02DP	COM

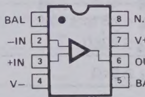
*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

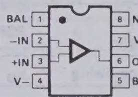
PIN CONNECTIONS


8 N.C.
BAL 1
7 V+
–IN 2
6 OUT
+IN 3
5 BAL
4 V– (CASE)

TO-99 (J-Suffix)

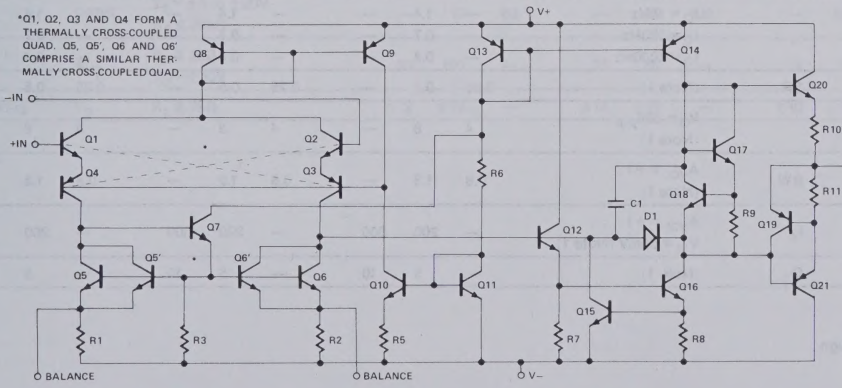

BAL 1
–IN 2
+IN 3
V– 4
8 N.C.
7 V+
6 OUT
5 BAL

8-PIN HERMETIC DIP (Z-Suffix)


BAL 1
–IN 2
+IN 3
V– 4
8 N.C.
7 V+
6 OUT
5 BAL

EPOXY MINI-DIP (P-Suffix)

SIMPLIFIED SCHEMATIC


V+
Q8
Q9
Q13
Q14
Q20
–IN
+IN
Q1
Q2
Q4
Q3
R6
R10
Q17
OUT
Q18
R11
C1
D1
R9
Q19
Q7
Q12
Q5
Q5'
Q6'
Q6
Q10
Q11
Q16
Q21
Q15
R1
R3
R2
R5
R7
R8
BALANCE
BALANCE
V–

*Q1, Q2, Q3 AND Q4 FORM A THERMALLY CROSS-COUPLED QUAD. Q5, Q5', Q6 AND Q6' COMPRISE A SIMILAR THERMALLY CROSS-COUPLED QUAD.

ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage	±22V
Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage	Supply Voltage
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	
OP-02A, OP-02, OP-02B	−55°C to +125°C
OP-02E, OP-02C, OP-02D	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C
DICE Junction Temperature (T_j)	−65°C to +150°C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
8-Pin Plastic DIP (P)	36°C	5.6mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C

2. Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

			OP-02A OP-02E			OP-02 OP-02C			OP-02B OP-02D			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \le 20k\Omega$	—	0.3	0.5	—	1	2	—	3	5	mV
Input Offset Current	I_{OS}		—	0.5	2	—	1	5	—	5	25	nA
Input Bias Current	I_B		—	18	30	—	20	50	—	30	100	nA
Input Resistance-Differential-Mode	R_{IN}	(Note 2)	3.8	7.5	—	2.3	7	—	1	5	—	MΩ
Input Voltage Range	IVR		±10	±13	—	±10	±13	—	±10	±13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \le 20k\Omega$	85	100	—	80	95	—	70	85	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5$ to $\pm 20V$ $R_S \le 20k\Omega$	—	10	60	—	30	100	—	100	150	μV/V
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±12	±13	—	±12	±13	—	±12	±13	—	V
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$ $V_O = \pm 10V$	100	250	—	50	200	—	25	150	—	V/mV
Power Consumption	P_d	$V_O = 0V$	—	40	70	—	50	90	—	50	90	mW
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	—	0.65	—	—	0.65	—	—	0.65	—	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10Hz$	—	25	—	—	25	—	—	25	—	$nV/\sqrt{Hz}$
		$f_O = 100Hz$	—	22	—	—	22	—	—	22	—	
		$f_O = 1000Hz$	—	21	—	—	21	—	—	21	—	
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	—	12.8	—	—	12.8	—	—	12.8	—	pA_{p-p}
Input Noise Current Density	i_n	$f_O = 10Hz$	—	1.4	—	—	1.4	—	—	1.4	—	$pA/\sqrt{Hz}$
		$f_O = 100Hz$	—	0.7	—	—	0.7	—	—	0.7	—	
		$f_O = 1000Hz$	—	0.4	—	—	0.4	—	—	0.4	—	
Slew Rate	SR	(Note 1)	0.25	0.5	—	0.25	0.5	—	0.25	0.5	—	V/μs
Large-Signal Bandwidth		$V_O = 20V_{p-p}$ (Note 1)	4	8	—	4	8	—	4	8	—	kHz
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$ (Note 1)	0.8	1.3	—	0.8	1.3	—	0.8	1.3	—	MHz
Risetime	t_r	$A_{VCL} = +1$ $V_{IN} = 50mV$ (Note 1)	—	200	300	—	200	300	—	200	300	ns
Overshoot	O_S	(Note 1)	—	5	10	—	5	10	—	5	10	%

NOTE:

1. Sample tested.
2. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \le T_A \le +125°C$, unless otherwise noted.

			OP-02A			OP-02			OP-02B			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \le 20k\Omega$	—	0.5	1	—	1.4	3	—	3	6	mV
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	$R_S = 50\Omega$	—	2	8	—	4	10	—	8	20	µV/°C
Input Offset Current	I_{OS}		—	1	5	—	2	10	—	5	50	nA
Average Input Offset Current Drift (Note 1)	TCI_{OS}		—	7.5	75	—	15	150	—	30	300	pA/°C
Input Bias Current	I_B		—	30	60	—	40	100	—	50	200	nA
Input Voltage Range	IVR		±10	±13	—	±10	±13	—	±10	±13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \le 20k\Omega$	80	95	—	80	95	—	70	85	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5$ to $\pm 20V$ $R_S \le 20k\Omega$	—	10	60	—	30	100	—	100	150	µV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$ $V_O = \pm 10V$	50	100	—	25	60	—	25	60	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±12	±13	—	±12	±13	—	±10	±13	—	V

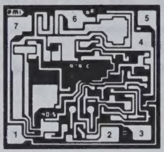
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $0°C \le T_A \le +70°C$, unless otherwise noted.

			OP-02E			OP-02C			OP-02D			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \le 20k\Omega$	—	0.4	1	—	1.2	3	—	3	6	mV
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	$R_S = 50\Omega$	—	2	8	—	4	10	—	8	20	µV/°C
Input Offset Current	I_{OS}		—	0.7	4	—	1.4	10	—	5	50	nA
Average Input Offset Current Drift (Note 1)	TCI_{OS}		—	7.5	120	—	15	250	—	70	500	pA/°C
Input Bias Current	I_B		—	22	50	—	25	100	—	50	200	nA
Input Voltage Range	IVR		±10	±13	—	±10	±13	—	±10	±13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \le 20k\Omega$	80	100	—	80	90	—	70	85	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5$ to $\pm 20V$ $R_S \le 20k\Omega$	—	10	60	—	30	100	—	100	150	µV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$ $V_O = \pm 10V$	50	100	—	25	60	—	15	25	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±12	±13	—	±12	±13	—	±10	±13	—	V

NOTE:

1. Sample tested.

DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)



DIE SIZE 0.046 × 0.042 inch, 1932 sq. mils
(1.17 × 1.07 mm, 1.25 sq. mm)

1. NULL
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V−
5. NULL
6. OUTPUT
7. V+

For additional DICE information refer to Section 2.

WAFER TEST LIMITS at $V_S = \pm15V$, $T_A = 25°C$ for OP-02N, OP-02G and OP-02GR devices; $T_A = 125°C$ for OP-02NT and OP-02GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-02NT LIMIT	OP-02N LIMIT	OP-02GT LIMIT	OP-02G LIMIT	OP-02GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	1	0.5	3	2	5	mV MAX
Input Offset Current	I_{OS}		5	3	6	5	25	nA MAX
Input Bias Current	I_B		50	30	60	50	200	nA MAX
Input Voltage Range	IVR		±13	±13	±13	±13	±13	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm10V$ $R_S \leq 20k\Omega$	80	85	80	80	70	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm5V$ to $\pm20V$ $R_S \leq 20k\Omega$	60	60	100	100	150	μV/V MAX
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	±12	±12	±12	±12	V MIN
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm10V$	50	100	25	50	25	V/mV MIN
Power Consumption	P_d	$V_O = 0V$	—	90	—	90	90	mW MAX

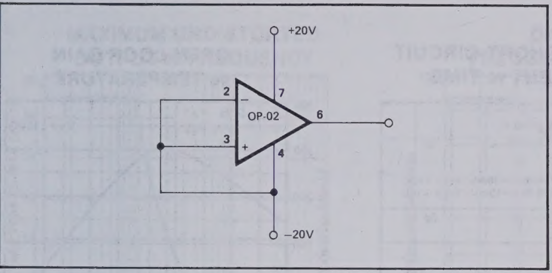
NOTE: For 25° C characteristics of NT and GT devices, see N and G characteristics, respectively.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

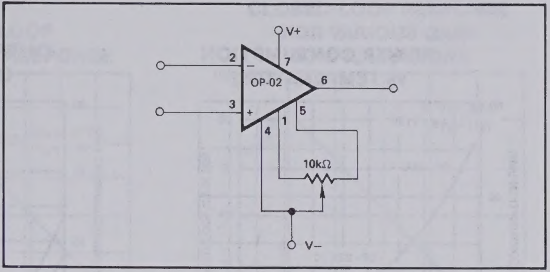
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-02NT OP-02N TYPICAL	OP-02GT OP-02G TYPICAL	OP-02GR TYPICAL	UNITS
Input Resistance Differential-Mode	R_{IN}		7.5	7	5	MΩ
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	0.65	0.65	0.65	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10Hz$ $f_O = 100Hz$ $f_O = 1000Hz$	25 22 21	25 22 21	25 22 21	$nV/\sqrt{Hz}$
Input Noise Current	I_{np-p}	0.1Hz to 10Hz	12.8	12.8	12.8	pA_{p-p}
Input Noise Current Density	i_n	$f_O = 10Hz$ $f_O = 100Hz$ $f_O = 1000Hz$	1.4 0.7 0.4	1.4 0.7 0.4	1.4 0.7 0.4	$pA/\sqrt{Hz}$
Slew Rate	SR		0.5	0.5	0.5	V/μs
Large-Signal Bandwidth		$V_O = 20V_{p-p}$	8	8	8	kHz
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$	1.3	1.3	1.3	MHz
Risetime		$A_V = +1$ $V_{IN} = 50mV$	200	200	200	ns
Overshoot			15	15	15	%
Average Input Offset Voltage Drift	TCV_{OS}	$R_S = 500\Omega$ (Note 1)	2	4	8	μV/°C
Average Input Offset Current Drift	TCI_{OS}		7.5	15	30	pA/°C

BURN-IN CIRCUIT

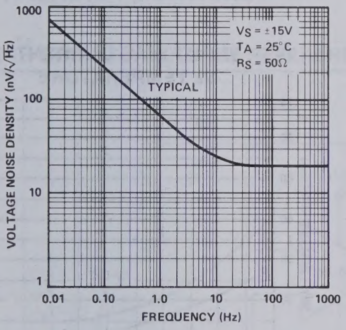


OFFSET NULLING CIRCUIT

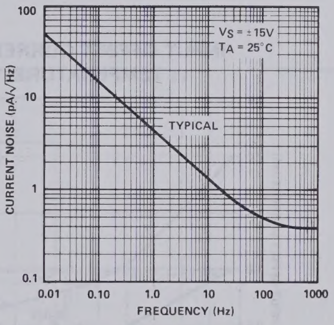


TYPICAL PERFORMANCE CHARACTERISTICS

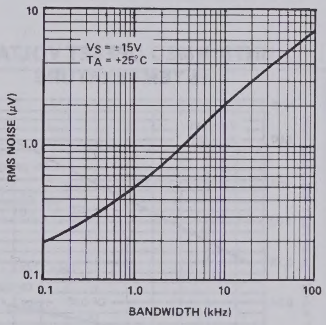
INPUT SPOT NOISE VOLTAGE vs FREQUENCY



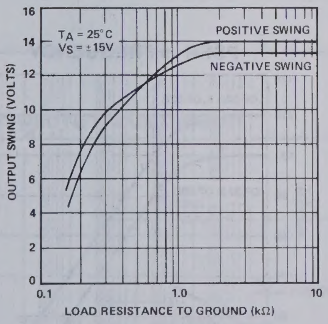
INPUT SPOT NOISE CURRENT vs FREQUENCY



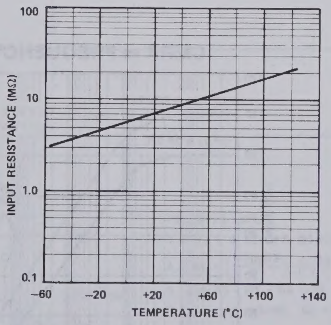
INPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



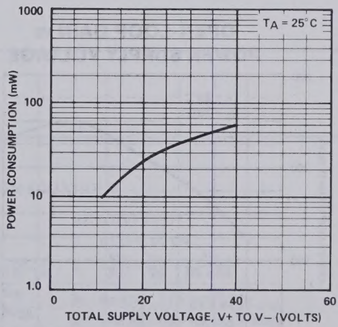
OUTPUT VOLTAGE vs LOAD RESISTANCE



DIFFERENTIAL INPUT RESISTANCE vs TEMPERATURE

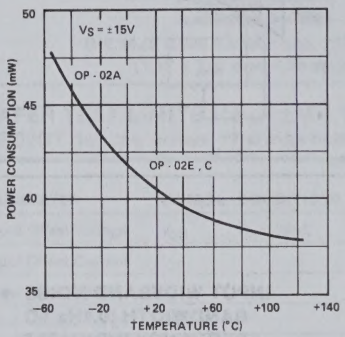


POWER CONSUMPTION vs POWER SUPPLY

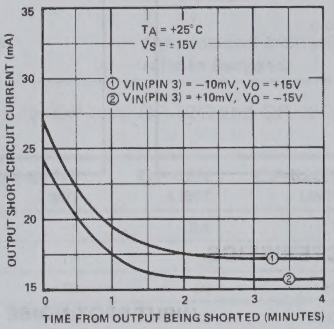


TYPICAL PERFORMANCE CHARACTERISTICS

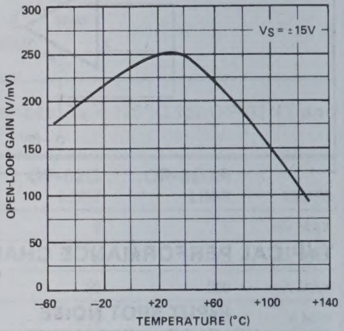
POWER CONSUMPTION vs TEMPERATURE



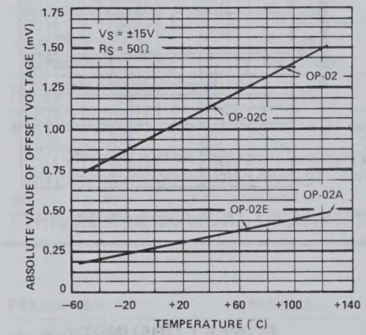
OUTPUT SHORT-CIRCUIT CURRENT vs TIME



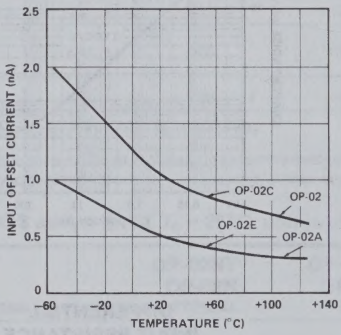
OPEN-LOOP GAIN vs TEMPERATURE



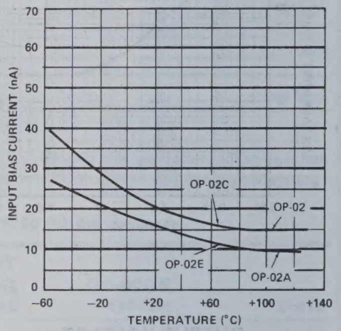
UNTRIMMED OFFSET VOLTAGE vs TEMPERATURE



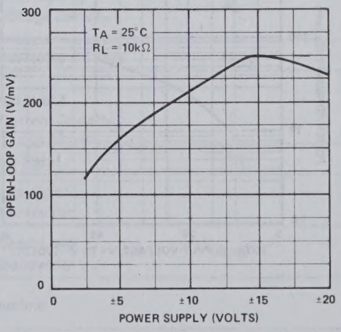
INPUT OFFSET CURRENT vs TEMPERATURE



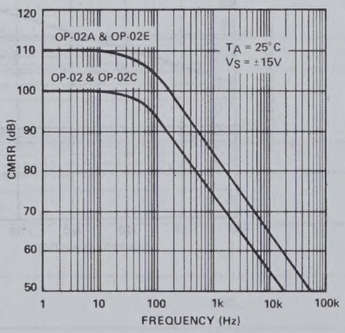
INPUT BIAS CURRENT vs TEMPERATURE



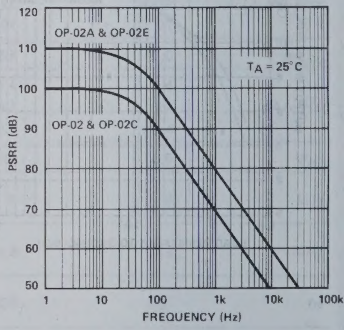
OPEN-LOOP GAIN vs POWER SUPPLY VOLTAGE



CMRR vs FREQUENCY

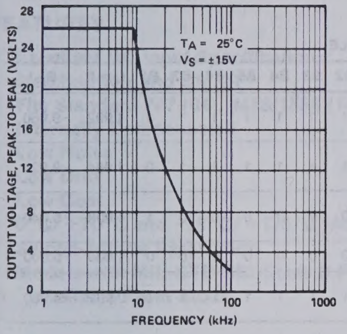


PSRR vs FREQUENCY

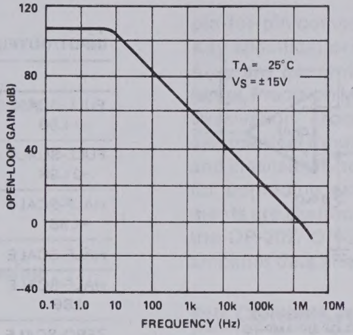


TYPICAL PERFORMANCE CHARACTERISTICS

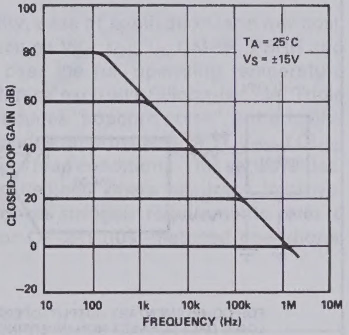
MAXIMUM UNDISTORTED OUTPUT vs FREQUENCY



OPEN-LOOP FREQUENCY RESPONSE

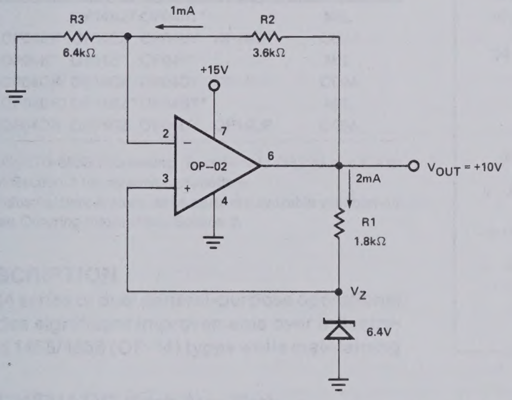


CLOSED-LOOP RESPONSE FOR VARIOUS GAIN CONFIGURATIONS



TYPICAL APPLICATIONS

HIGH-STABILITY VOLTAGE REFERENCE

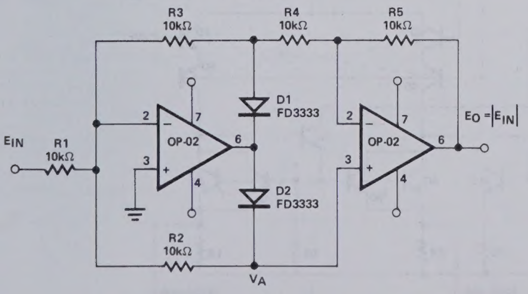


R3
6.4kΩ
1mA
R2
3.6kΩ
+15V
2
7
OP–02
6
3
4
V_{OUT} = +10V
2mA
R1
1.8kΩ
V_Z
6.4V

$$V_{OUT} = \left(1 + \frac{R_2}{R_3}\right) V_Z$$

FOR R2 = 3.6kΩ AND
R3 = 6.4kΩ,
$V_{OUT} = 1.5625V_Z$
IF V_Z = 6.4V, THEN
V_{OUT} = +10V

ABSOLUTE VALUE CIRCUIT



R3
10kΩ
R4
10kΩ
R5
10kΩ
D1
FD3333
D2
FD3333
E_{IN}
R1
10kΩ
2
7
OP-02
6
3
4
2
7
OP-02
6
3
4
$E_O = |E_{IN}|$
R2
10kΩ
V_A

DESIGN EQUATIONS

POSITIVE INPUT

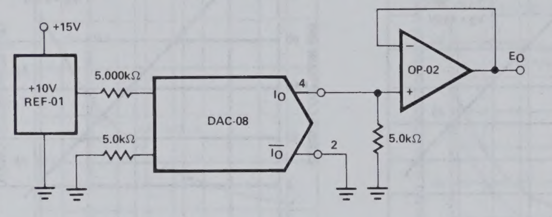
1. V_A = 0, D2 OFF, D1 ON
2. $E_O = \left(\frac{-E_{IN}R3}{R1}\right) \cdot \left(\frac{-R5}{R4}\right) = E_{IN}\frac{R3\ R5}{R1\ R4}$
3. With R1 = R3 = R4 = R5: $E_O = E_{IN}$
4. V_{OS} error included: $E_O = E_{IN} + 2V_{OS}$

NEGATIVE INPUT

1. D1 OFF, D2 ON
2. $\frac{-E_{IN}}{R1} = \frac{V_A}{R2} + \frac{V_A}{R3 + R4}$
3. $E_O = V_A\left(1 + \frac{R5}{R3 + R4}\right)$
4. With R3 = R4 = R5: $E_O = 1.5V_A$
5. $E_O = -\frac{(R2)\ (R3 + R4)\ (1.5)\ E_{IN}}{R1\ (R2 + R3 + R4)}$
6. With R1 = R2 = R3 = R4: $E_O = -E_{IN}$
7. V_{OS} error included:
   $E_O = -E_{IN} + 1.5V_{OS2} - 0.5V_{OS1}$
8. For both inputs: $E_O = +|E_{IN}|$

TYPICAL APPLICATIONS

DAC-08 OUTPUT AMPLIFIER


+15V
+10V
REF-01
5.000kΩ
5.0kΩ
DAC-08
I_O
4
$\overline{I_O}$
2
5.0kΩ
OP-02
−
+
E_O

FOR COMPLEMENTARY OUTPUT (OPERATION AS A NEGATIVE LOGIC DAC) CONNECT NON-INVERTING INPUT OF OP-AMP TO $\overline{I_O}$ (PIN 2), CONNECT I_O (PIN 4) TO GROUND.

INPUT/OUTPUT TABLE

	B1	B2	B3	B4	B5	B6	B7	B8	I_OmA	E_O
FULL-SCALE −1 LSB	1	1	1	1	1	1	1	1	1.992	−9.960
FULL-SCALE −2 LSB	1	1	1	1	1	1	1	0	1.984	−9.920
HALF-SCALE +LSB	1	0	0	0	0	0	0	1	1.008	−5.040
HALF-SCALE	1	0	0	0	0	0	0	0	1.000	−5.000
HALF-SCALE −LSB	0	1	1	1	1	1	1	1	0.992	−4.960
ZERO-SCALE +LSB	0	0	0	0	0	0	0	1	0.0008	−0.040
ZERO-SCALE	0	0	0	0	0	0	0	0	0.000	0.000

DUAL MATCHED HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

OP-04/OP-14

FEATURES

- Excellent DC Input Specifications
- Matched V_{OS} and CMRR
- Fits Standard 747 (04), 1458/1558 (14) Sockets
- Internally Compensated
- Low Noise
- Low Drift
- Low Cost
- 0° C/ +70° C and −55° C/ +125° C Models
- Silicon-Nitride Passivation
- Models with MIL-STD-883 Class B Processing Available From Stock

ORDERING INFORMATION†

$T_A = 25°C$ V_{OS} (mV)	HERMETIC TO-99 8-PIN	HERMETIC TO-100 10-PIN	HERMETIC DIP 8-PIN	HERMETIC DIP 14-PIN	PLASTIC DIP 8-PIN	OPERATING TEMPERATURE RANGE
0.75	OP14AJ*		OP14AZ*	OP04AY*		MIL
0.75	OP14EJ	OP04EK	OP14EZ	OP04EY	OP14EP	COM
2.0	OP14J*	OP04K*	OP14Z*	OP04Y*		MIL
2.0	OP14CJ	OP04CK	OP14CZ	OP04CY	OP14CP	COM
5.0	OP14BJ*	OP04BK*	OP14BZ*	OP04BY*		MIL
5.0	OP14DJ	OP04DK	OP14DZ	OP04DY	OP14DP	COM

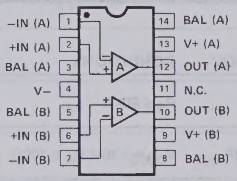
* Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

† All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

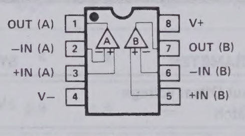
GENERAL DESCRIPTION

The OP-04/OP-14 series of dual general-purpose operational amplifiers provides significant improvements over industry-standard 747 and 1458/1558 (OP-14) types while maintaining pin-for-pin compatibility, ease of application, and low cost. Key specifications, such as V_{OS}, I_{OS}, I_B, CMRR, PSRR and A_{VO}, are guaranteed over the full operating temperature range. Precision Monolithics' exclusive Silicon-Nitride "Triple Passivation" process reduces "popcorn noise". A thermally-symmetrical input stage design provides low TCV_{OS}, TCI_{OS}, and insensitivity to output load conditions. This series is ideal for upgrading existing designs where accuracy improvements are desired. For more stringent requirements, refer to the OP-207, OP-220, or OP-221 dual-matched operational amplifier data sheets.

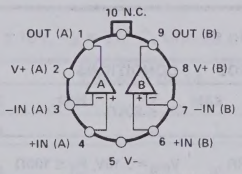
PIN CONNECTIONS


−IN (A) 1
+IN (A) 2
BAL (A) 3
V− 4
BAL (B) 5
+IN (B) 6
−IN (B) 7
14 BAL (A)
13 V+ (A)
12 OUT (A)
11 N.C.
10 OUT (B)
9 V+ (B)
8 BAL (B)
A
B

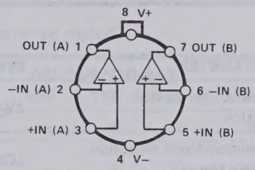
14-PIN HERMETIC DIP (Y-Suffix) OP-04


OUT (A) 1
−IN (A) 2
+IN (A) 3
V− 4
8 V+
7 OUT (B)
6 −IN (B)
5 +IN (B)
A
B

8-PIN HERMETIC DIP (Z-Suffix) OP-14 & EPOXY MINI-DIP (P-Suffix) OP-14

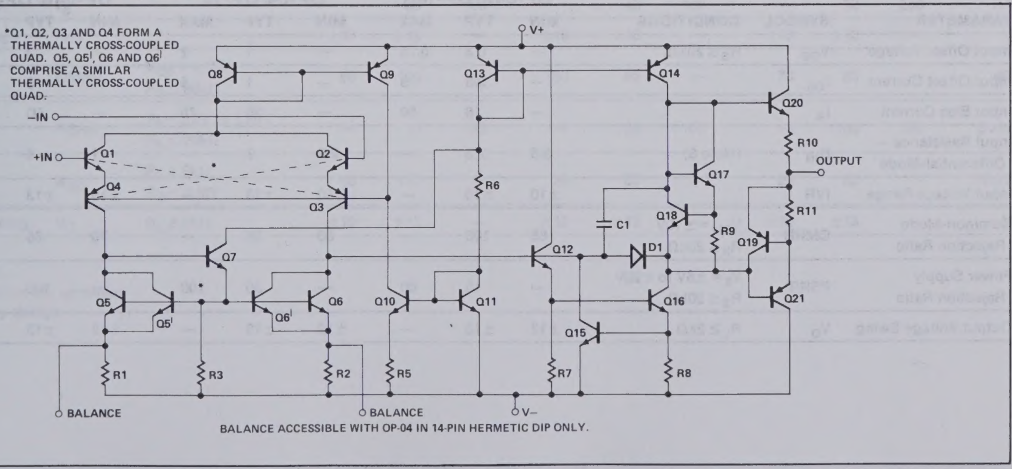

10 N.C.
OUT (A) 1
9 OUT (B)
V+ (A) 2
8 V+ (B)
−IN (A) 3
7 −IN (B)
+IN (A) 4
6 +IN (B)
5 V−
A
B

TO-100 (K-Suffix) OP-04


8 V+
OUT (A) 1
7 OUT (B)
−IN (A) 2
6 −IN (B)
+IN (A) 3
5 +IN (B)
4 V−

TO-99 (J-Suffix) OP-14

SIMPLIFIED SCHEMATIC (Each Amplifier)


V+
−IN
+IN
Q1
Q2
Q3
Q4
Q5
Q5'
Q6
Q6'
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q19
Q20
Q21
R1
R2
R3
R5
R6
R7
R8
R9
R10
R11
C1
D1
OUTPUT
BALANCE
BALANCE
V−

*Q1, Q2, Q3 AND Q4 FORM A THERMALLY CROSS-COUPLED QUAD. Q5, Q5', Q6 AND Q6' COMPRISE A SIMILAR THERMALLY CROSS-COUPLED QUAD.

BALANCE ACCESSIBLE WITH OP-04 IN 14-PIN HERMETIC DIP ONLY.

ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage	Supply Voltage
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	
J, K, Y, and Z Packages	−65°C to +150°C
P Package	−65°C to +125°C
Lead Temperature Range (Soldering, 60 sec)	300°C
Operating Temperature Range	
A, Plain, B-Suffix	−55°C to +125°C
E, C, D-Suffix	0°C to +70°C
DICE Junction Temperature (T_j)	−65°C to +150°C

	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
14-Pin Hermetic DIP (Y) OP-04	100°C	10.0mW/°C
TO-100 (K) OP-04	80°C	7.1mW/°C
TO-99 (J) OP-14	80°C	7.1mW/°C
8-Pin Hermetic DIP (Z) OP-14	75°C	6.7mW/°C
8-Pin Plastic DIP (P) OP-14	36°C	5.6mW/°C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.
2. Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

			OP-04A OP-04E OP-14A OP-14E			OP-04 OP-04C OP-14 OP-14C			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage Match	ΔV_{OS}	$R_S \leq 20k\Omega$	—	0.3	1	—	1	2	mV
Common-Mode Rejection Ratio Match	ΔCMRR	$V_{CM} = \pm 10V$, $R_S \leq 100\Omega$	94	106	—	94	106	—	dB

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$ for OP-04A, OP-14A, OP-04 and OP-14, $0°C \leq T_A \leq 70°C$ for OP-04E, OP-14E, OP-04C and OP-14C, unless otherwise noted.

			OP-04A OP-04E OP-14A OP-14E			OP-04 OP-04C OP-14 OP-14C			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage Match	ΔV_{OS}	$R_S \leq 20k\Omega$	—	0.5	1.5	—	1.5	3	mV
Common-Mode Rejection Ratio Match	ΔCMRR	$V_{CM} = \pm 10V$, $R_S \leq 100\Omega$	90	100	—	90	100	—	dB

ELECTRICAL CHARACTERISTICS (Each Amplifier) at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

			OP-04A/OP-14A			OP-04/OP-14			OP-04B/OP-14B			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	—	0.3	0.75	—	1	2	—	3	5	mV
Input Offset Current	I_{OS}		—	0.5	5	—	1	5	—	5	25	nA
Input Bias Current	I_B		—	18	50	—	20	75	—	30	100	nA
Input Resistance — Differential-Mode	R_{IN}	(Note 3)	3.8	7.5	—	2.3	7	—	1	5	—	MΩ
Input Voltage Range	IVR		±10	±13	—	±10	±13	—	±10	±13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20k\Omega$	85	100	—	80	95	—	70	85	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$ $R_S \leq 20k\Omega$	—	10	60	—	30	100	—	100	150	μV/V
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	±13	—	±12	±13	—	±12	±13	—	V

ELECTRICAL CHARACTERISTICS (Each Amplifier) at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted. (Continued)

			OP-04A/OP-14A			OP-04/OP-14			OP-04B/OP-14B			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	100	250	—	50	200	—	50	200	—	V/mV
Power Consumption (Note 2)	P_d	$V_O = 0V$	—	50	90	—	50	90	—	50	90	mW
Input Noise Voltage	$e_{np\text{-}p}$	0.1Hz to 10Hz	—	0.65	—	—	0.65	—	—	0.65	—	$\mu V_{p\text{-}p}$
Input Noise Voltage Density	e_n	$f_O = 10Hz$	—	25	—	—	25	—	—	25	—	$nV/\sqrt{Hz}$
		$f_O = 100Hz$	—	22	—	—	22	—	—	22	—	
		$f_O = 1000Hz$	—	21	—	—	21	—	—	21	—	
Input Noise Current	$i_{np\text{-}p}$	0.1Hz to 10Hz	—	12.8	—	—	12.8	—	—	12.8	—	$pA_{p\text{-}p}$
Input Noise Current Density	i_n	$f_O = 10Hz$	—	1.4	—	—	1.4	—	—	1.4	—	$pA/\sqrt{Hz}$
		$f_O = 100Hz$	—	0.7	—	—	0.7	—	—	0.7	—	
		$f_O = 1000Hz$	—	0.4	—	—	0.4	—	—	0.4	—	
Channel Separation	CS		100	—	—	100	—	—	80	—	—	dB
Slew Rate (Note 1)	SR	$R_L = 2k\Omega$, $C_L = 100pF$	0.25	0.5	—	0.25	0.5	—	0.25	0.5	—	V/μs
Large-Signal Bandwidth (Note 1)		$V_O = 20V_{p\text{-}p}$	4	8	—	4	8	—	4	8	—	kHz
Closed-Loop Bandwidth (Note 1)	BW	$A_{VCL} = +1.0$	0.8	1.3	—	0.8	1.3	—	0.8	1.3	—	MHz
Risetime (Note 1)	t_r	$A_V = +1$, $V_{IN} = 50mW$ $R_L = 2k\Omega$, $C_L = 50pF$	—	200	300	—	200	300	—	200	300	ns
Overshoot (Note 1)	OS	$A_V = +1$, $V_{IN} = 50mV$ $R_L = 2k\Omega$, $C_L = 50pF$	—	5	10	—	5	10	—	5	10	%

ELECTRICAL CHARACTERISTICS (Each Amplifier) at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

			OP-04A/OP-14A			OP-04/OP-14			OP-04B/OP-14B			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	—	0.4	1.5	—	1.2	3	—	3	6	mV
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	$R_S = 50\Omega$	—	2	8	—	4	10	—	8	20	μV/°C
Input Offset Current	I_{OS}		—	1	10	—	2	10	—	10	50	nA
Average Input Offset Current Drift (Note 1)	TCI_{OS}		—	7.5	120	—	15	250	—	70	500	pA/°C
Input Bias Current	I_B		—	30	60	—	40	100	—	50	200	nA
Input Voltage Range	IVR		±10	±13	—	±10	±13	—	±10	±13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20k\Omega$	80	100	—	80	95	—	70	85	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$ $R_S \leq 20k\Omega$	—	10	60	—	30	100	—	100	150	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	50	100	—	25	60	—	25	60	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	±13	—	±12	±13	—	±10	±13	—	V

NOTES:

1. Sample tested.
2. Power dissipation per amplifier.
3. Guaranteed by design.

ELECTRICAL CHARACTERISTICS (Each Amplifier) at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

			OP-04E/OP-14E			OP-04C/OP-14C			OP-04D/OP-14D			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	—	0.3	0.75	—	1	2	—	3	5	mV
Input Offset Current	I_{OS}		—	0.5	5	—	1	5	—	5	25	nA
Input Bias Current	I_B		—	18	50	—	20	75	—	30	100	nA
Input Resistance — Differential-Mode	R_{IN}	(Note 3)	3.8	7.5	—	2.3	7	—	1	5	—	MΩ
Input Voltage Range	IVR		±10	±13	—	±10	±13	—	±10	±13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20k\Omega$	85	100	—	80	95	—	70	85	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$ $R_S \leq 20k\Omega$	—	10	60	—	30	100	—	100	150	μV/V
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	±13	—	±12	±13	—	±12	±13	—	V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	100	250	—	50	200	—	25	150	—	V/mV
Power Consumption (Note 2)	P_d	$V_O = 0V$	—	50	90	—	50	90	—	50	90	mW
Input Noise Voltage	$e_{np\text{-}p}$	0.1Hz to 10Hz	—	0.65	—	—	0.65	—	—	0.65	—	$\mu V_{p\text{-}p}$
Input Noise Voltage Density	e_n	$f_O = 10Hz$ $f_O = 100Hz$ $f_O = 1000Hz$	— — —	25 22 21	— — —	— — —	25 22 21	— — —	— — —	25 22 21	— — —	$nV/\sqrt{Hz}$
Input Noise Current	$i_{np\text{-}p}$	0.1Hz to 10Hz	—	12.8	—	—	12.8	—	—	12.8	—	$pA_{p\text{-}p}$
Input Noise Current Density	i_n	$f_O = 10Hz$ $f_O = 100Hz$ $f_O = 1000Hz$	— — —	1.4 0.7 0.4	— — —	— — —	1.4 0.7 0.4	— — —	— — —	1.4 0.7 0.4	— — —	$pA/\sqrt{Hz}$
Channel Separation	CS		100	—	—	100	—	—	80	—	—	dB
Slew Rate (Note 1)	SR	$R_L = 2k\Omega$, $C_L = 100pF$	0.25	0.5	—	0.25	0.5	—	0.25	0.5	—	V/μs
Large-Signal Bandwidth (Note 1)		$V_O = 20V_{p\text{-}p}$	4	8	—	4	8	—	4	8	—	kHz
Closed-Loop Bandwidth (Note 1)	BW	$A_{VCL} = +1$	0.8	1.3	—	0.8	1.3	—	0.8	1.3	—	MHz
Risetime (Note 1)	t_r	$A_V = +1$, $V_{IN} = 50mV$ $R_L = 2k\Omega$, $C_L = 50pF$	—	200	300	—	200	300	—	200	300	ns
Overshoot (Note 1)	OS	$A_V = +1$, $V_{IN} = 50mV$ $R_L = 2k\Omega$, $C_L = 50pF$	—	5	10	—	5	10	—	5	10	%

NOTES:

1. Sample tested.
2. Power dissipation per amplifier.
3. Guaranteed by design.

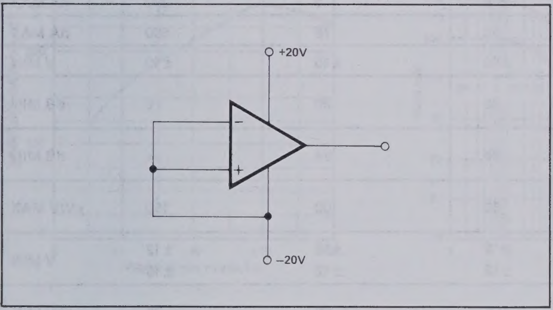
ELECTRICAL CHARACTERISTICS (Each Amplifier) at $V_S = \pm15V$, $0°C \le T_A \le +70°C$, unless otherwise noted.

			OP-04E/OP-14E			OP-04C/OP-14C			OP-04D/OP-14D			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \le 20k\Omega$	—	0.4	1.5	—	1.2	3	—	3	6	mV
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	$R_S = 50\Omega$	—	2	8	—	4	10	—	8	20	μV/°C
Input Offset Current	I_{OS}		—	1	10	—	2	10	—	10	50	nA
Average Input Offset Current Drift (Note 1)	TCI_{OS}		—	7.5	120	—	15	250	—	70	500	pA/°C
Input Bias Current	I_B		—	30	60	—	40	100	—	50	200	nA
Input Voltage Range	IVR		±10	±13	—	±10	±13	—	±10	±13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm10V$ $R_S \le 20k\Omega$	80	100	—	80	95	—	70	85	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm5V$ to $\pm20V$ $R_S \le 20k\Omega$	—	10	60	—	30	100	—	100	150	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$ $V_O = \pm10V$	50	100	—	25	60	—	15	25	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±12	±13	—	±12	±13	—	±10	±13	—	V

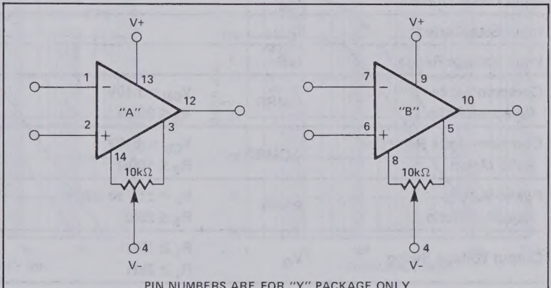
NOTES:

1. Sample tested.
2. Power dissipation per amplifier.
3. Guaranteed by design.

BURN-IN CIRCUIT (1/2 of OP-04, OP-14)



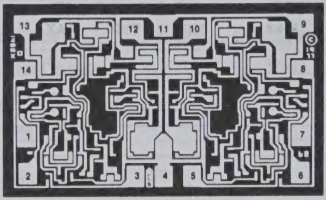
OFFSET ADJUST CIRCUIT



PIN NUMBERS ARE FOR "Y" PACKAGE ONLY.

DICE CHARACTERISTICS

OP-14



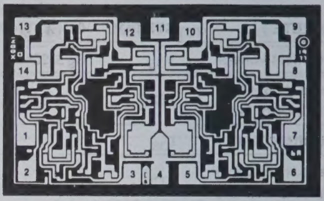
DIE SIZE 0.076 × 0.046 inch, 3496 sq. mils
(1.93 × 1.17 mm, 2.26 sq. mm)

For additional DICE information
refer to Section 2.

1. INVERTING INPUT (A)
2. NON-INVERTING INPUT (A)
3. BALANCE (A)
4. V−
5. BALANCE (B)
6. NON-INVERTING INPUT (B)
7. INVERTING INPUT (B)
8. BALANCE (B)
9. V+
10. OUTPUT (B)
11. V+
12. OUTPUT (A)
13. V+
14. BALANCE (A)

NOTE: 9, 11 and 13 are internally connected.

OP-04



1. INVERTING INPUT (A)
2. NON-INVERTING INPUT (A)
3. BALANCE (A)
4. V−
5. BALANCE (B)
6. NON-INVERTING INPUT (B)
7. INVERTING INPUT (B)
8. BALANCE (B)
9. V+ (B)
10. OUTPUT (B)
11. NO CONNECTIONS
12. OUTPUT (A)
13. V+ (A)
14. BALANCE (A)

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-04N OP-14N LIMIT	OP-04G OP-14G LIMIT	OP-14GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	0.75	2	6	mV MAX
Input Offset Voltage Match	ΔV_{OS}	$R_S \leq 20k\Omega$	1	2	—	mV MAX
Input Offset Current	I_{OS}		5	5	200	nA MAX
Input Bias Current	I_B		50	75	500	nA MAX
Input Voltage Range	IVR		±10	±10	±10	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20k\Omega$	85	80	70	dB MIN
Common-Mode Rejection Ratio Match	ΔCMRR	$V_{CM} = \pm 10V$ $R_S \leq 100\Omega$	94	94	—	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$ $R_S \leq 20k\Omega$	60	100	150	µV/V MAX
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$	±12 ±12	±12 ±12	±12 ±10	V MIN
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	100	50	25	V/mV MIN
Power Consumption (Both Amplifiers)	P_d	$V_{OUT} = 0$	170	170	180	mW MAX
Slew Rate	SR	$R_L = 2k\Omega$ $C_L = 100pF$	0.25	0.25	—	V/µs MIN
Channel Separation	CS		100	100	—	dB MIN

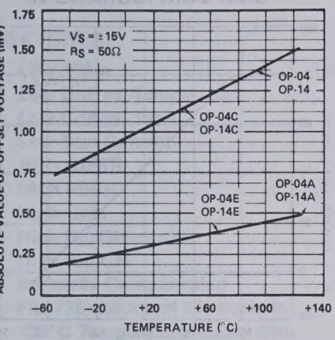
Note: Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

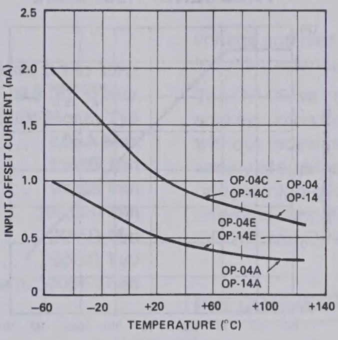
PARAMETER	SYMBOL	CONDITIONS	OP-04N OP-14N TYPICAL	OP-04G OP-14G TYPICAL	OP-14GR TYPICAL	UNITS
Risetime	t_r	$A_V = +1$ $V_{IN} = 50mV$ $R_L = 2k\Omega$ $C_L = 50pF$	200	200	200	ns
Overshoot	OS	$A_V = +1$ $V_{IN} = 50mV$ $R_L = 2k\Omega$ $C_L = 50pF$	5	5	5	%

TYPICAL PERFORMANCE CHARACTERISTICS (Each Amplifier)

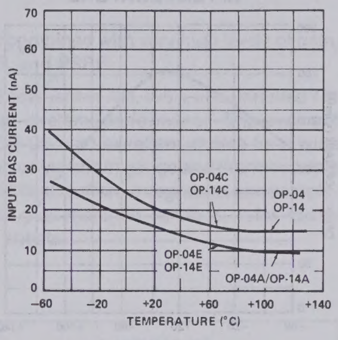
UNTRIMMED OFFSET VOLTAGE vs TEMPERATURE



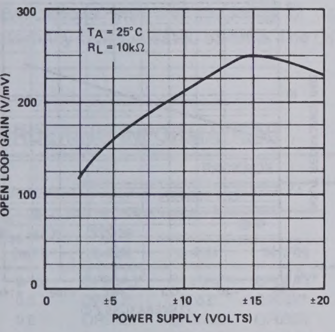
INPUT OFFSET CURRENT vs TEMPERATURE



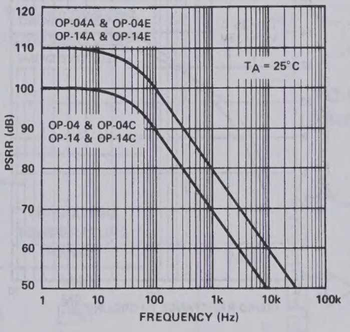
INPUT BIAS CURRENT vs TEMPERATURE



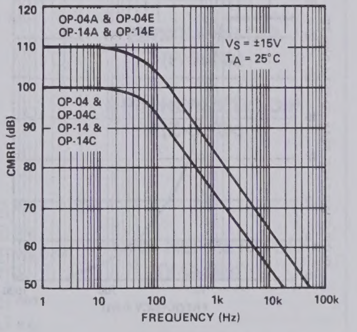
OPEN-LOOP GAIN vs POWER SUPPLY VOLTAGE



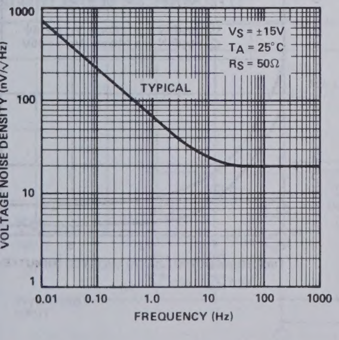
PSRR vs FREQUENCY



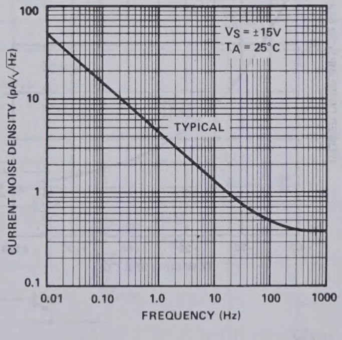
CMRR vs FREQUENCY



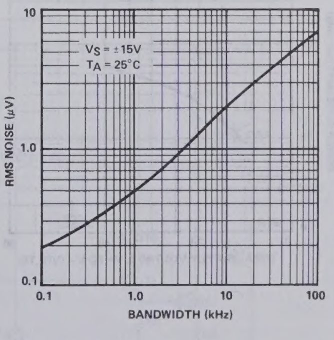
INPUT SPOT NOISE VOLTAGE vs FREQUENCY



INPUT SPOT NOISE CURRENT vs FREQUENCY

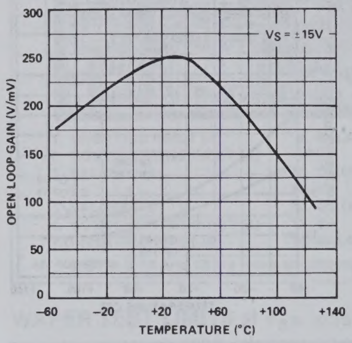


INPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)

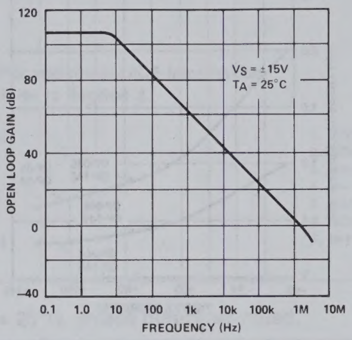


TYPICAL PERFORMANCE CHARACTERISTICS (Each Amplifier)

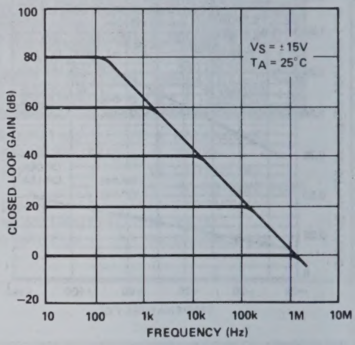
OPEN-LOOP GAIN vs TEMPERATURE



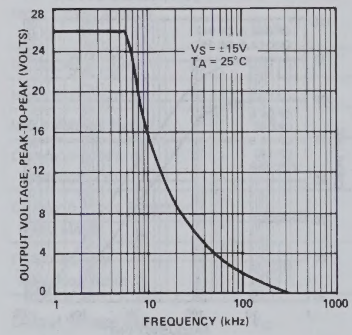
OPEN-LOOP FREQUENCY RESPONSE



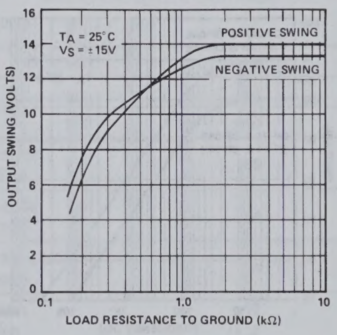
CLOSED-LOOP RESPONSE FOR VARIOUS GAIN CONFIGURATIONS



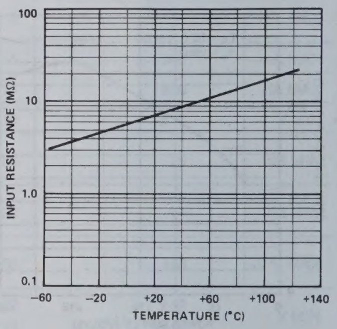
MAXIMUM UNDISTORTED OUTPUT vs FREQUENCY



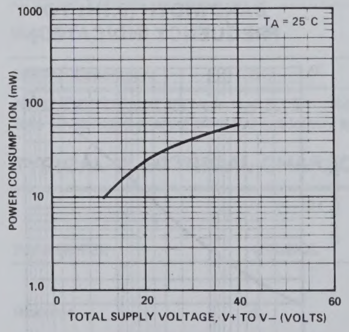
OUTPUT VOLTAGE vs LOAD RESISTANCE



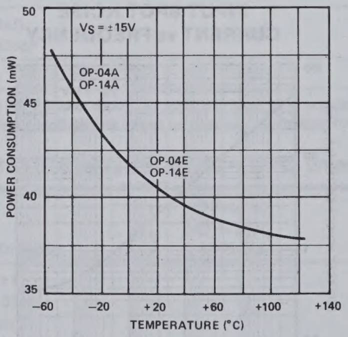
INPUT RESISTANCE vs TEMPERATURE



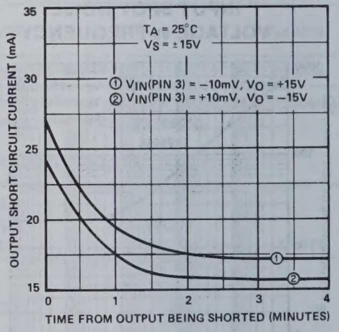
POWER CONSUMPTION vs POWER SUPPLY



POWER CONSUMPTION vs TEMPERATURE



OUTPUT SHORT-CIRCUIT CURRENT vs TIME



INSTRUMENTATION OPERATIONAL AMPLIFIER

OP-05

FEATURES

- **Low Noise** .... **0.6μVp-p Max, 0.1 to 10Hz**
- **Low Drift vs. Temperature** .... **0.5μV/°C Max**
- **Low Drift vs. Time** .... **0.2μV/Month Typ**
- **Low Bias Current** .... **2.0nA Max**
- **High CMRR** .... **114dB Min**
- **High PSRR** .... **100dB Min**
- **High Gain** .... **300,000 Min**
- **High R_{IN} Differential** .... **30MΩ Min**
- **High R_{IN} CM** .... **200GΩ Typ**
- **Internally Compensated** .... **Stable to 500pF Load**
- **Fits 725, 108A and 741 Sockets**
- **125°C Temperature Tested Dice**

GENERAL DESCRIPTION

The OP-05 series of monolithic instrumentation operational amplifiers combine excellent performance in low-signal-level applications with the simplicity of use of a fully-protected, internally-compensated op amp. The OP-05 has low input offset voltage and bias current combined with very high levels of gain, input impedance, CMRR, and PSRR.

The OP-05 is a direct replacement in 725, 108A, and unnulled 741 sockets allowing instant system performance improvement without redesign. The OP-05 is an excellent choice for a wide variety of applications including strain gauge and thermocouple bridges, high-gain active filters, buffers, integrators, and sample-and-hold amplifiers. For dual-matched versions, refer to the OP-207 and OP-10 data sheets.

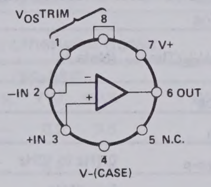
ORDERING INFORMATION†

T_A = 25°C V_{OS} MAX (mV)	PACKAGE HERMETIC TO-99 8-PIN	HERMETIC DIP 8-PIN	HERMETIC DIP 14-PIN	PLASTIC DIP 8-PIN	OPERATING TEMPERATURE RANGE
0.15	OP05AJ*	OP05AZ*	OP05AY*		MIL
0.5	OP05J*	OP05Z*	OP05Y*		MIL
0.5	OP05EJ	OP05EZ	OP05EY	OP-05EP	COM
1.3	OP05CJ	OP05CZ	OP05CY	OP05CP	COM

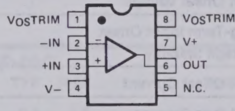
*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

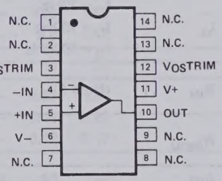
PIN CONNECTIONS


VOS TRIM
8
1
7 V+
−IN 2
6 OUT
+IN 3
5 N.C.
4
V−(CASE)

TO-99 (J-Suffix)


VOS TRIM 1
−IN 2
+IN 3
V− 4
8 VOS TRIM
7 V+
6 OUT
5 N.C.

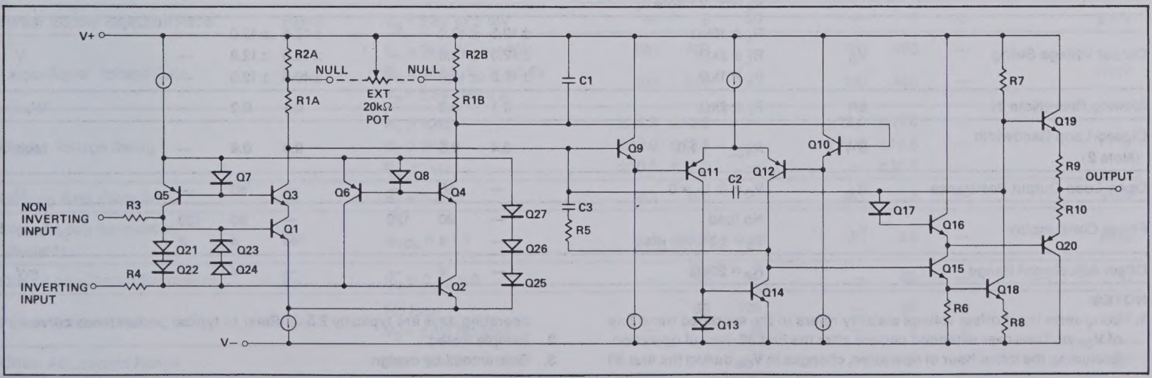
EPOXY MINI-DIP (P-Suffix) & 8-PIN HERMETIC DIP (Z-Suffix)


N.C. 1
N.C. 2
VOS TRIM 3
−IN 4
+IN 5
V− 6
N.C. 7
14 N.C.
13 N.C.
12 VOS TRIM
11 V+
10 OUT
9 N.C.
8 N.C.

14-PIN HERMETIC DIP (Y-Suffix)*

*This package not recommended for new designs.

SIMPLIFIED SCHEMATIC


V+
R2A
NULL
NULL
R2B
EXT 20kΩ POT
R1A
R1B
C1
R7
Q19
Q9
Q10
Q11
C2
Q12
R9
OUTPUT
Q7
Q8
Q5
Q3
Q6
Q4
NON INVERTING INPUT
R3
Q1
C3
R5
Q27
Q17
Q16
R10
Q20
Q21
Q23
Q22
Q24
R4
INVERTING INPUT
Q26
Q25
Q2
Q15
Q14
Q18
R6
R8
Q13
V−

ABSOLUTE MAXIMUM RATINGS (Note 3)

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±22V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	
J, Y, and Z Packages	−65°C to +150°C
P Package	−65°C to +125°C
Operating Temperature Range	
OP-05A, OP-05	−55°C to +125°C
OP-05E, OP-05C	0°C to +70°C
Lead Temperature Range (Soldering, 60 sec)	300°C
DICE Junction Temperature	−65°C to +150°C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
14-Pin Hermetic DIP (Y)	100°C	10.0mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C
8-Pin Plastic DIP (P)	36°C	5.6mW/°C

2. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
3. Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-05A MIN	OP-05A TYP	OP-05A MAX	OP-05 MIN	OP-05 TYP	OP-05 MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.07	0.15	—	0.2	0.5	mV
Long-Term Input Offset Voltage Stability	ΔV_{OS}/Time	(Note 1)	—	0.2	1.0	—	0.2	1.0	μV/Mo
Input Offset Current	I_{OS}		—	0.7	2.0	—	1.0	2.8	nA
Input Bias Current	I_B		—	±0.7	±2.0	—	±1.0	±3.0	nA
Input Noise Voltage (Note 2)	e_{np-p}	0.1Hz to 10Hz	—	0.35	0.6	—	0.35	0.6	μV_{p-p}
Input Noise Voltage Density (Note 2)	e_n	$f_O = 10Hz$ $f_O = 100Hz$ $f_O = 1000Hz$	— — —	10.3 10.0 9.6	18.0 13.0 11.0	— — —	10.3 10.0 9.6	18.0 13.0 11.0	$nV/\sqrt{Hz}$
Input Noise Current (Note 2)	i_{np-p}	0.1Hz to 10Hz	—	14	30	—	14	30	pA_{p-p}
Input Noise Current Density (Note 2)	i_n	$f_O = 10Hz$ $f_O = 100Hz$ $f_O = 1000Hz$	— — —	0.32 0.14 0.12	0.80 0.23 0.17	— — —	0.32 0.14 0.12	0.80 0.23 0.17	$pA/\sqrt{Hz}$
Input Resistance — Differential-Mode	R_{IN}	(Note 3)	30	80	—	20	60	—	MΩ
Input Resistance — Common-Mode	R_{INCM}		—	200	—	—	200	—	GΩ
Input Voltage Range	IVR		±13.5	±14.0	—	±13.5	±14.0	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm13.5V$	114	126	—	114	126	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm3V$ to $\pm18V$	—	4	10	—	4	10	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm10V$ $R_L \geq 500\Omega$, $V_O = \pm0.5V$ $V_S = \pm3V$ (Note 3)	300 150	500 500	— —	200 150	500 500	— —	V/mV
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0	— — —	±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0	— — —	V
Slewing Rate (Note 2)	SR	$R_L \geq 2k\Omega$	0.1	0.3	—	0.1	0.3	—	V/μs
Closed-Loop Bandwidth (Note 2)	BW	$A_{VCL} = +1.0$	0.4	0.6	—	0.4	0.6	—	MHz
Open-Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	60	—	—	60	—	Ω
Power Consumption	P_d	No load $V_S = \pm3V$, No load	— —	90 4	120 6	— —	90 4	120 6	mW
Offset Adjustment Range		$R_P = 20k\Omega$	—	4	—	—	4	—	mV

NOTES:

1. Long-term input offset voltage stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV. Refer to typical performance curve.
2. Sample tested.
3. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \le T_A \le +125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-05A MIN	OP-05A TYP	OP-05A MAX	OP-05 MIN	OP-05 TYP	OP-05 MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.10	0.24	—	0.3	0.7	mV
Average Input Offset Voltage Drift Without External Trim	TCV_{OS}	(Note 2)	—	0.3	0.9	—	0.7	2.0	μV/°C
With External Trim	TCV_{OSn}	$R_P = 20k\Omega$ (Note 3)	—	0.2	0.5	—	0.3	1.0	
Input Offset Current	I_{OS}		—	1.0	4.0	—	1.8	5.6	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 2)	—	5	25	—	8	50	pA/°C
Input Bias Current	I_B		—	±1	±4	—	±2	±6	nA
Average Input Bias Current Drift	TCI_B	(Note 2)	—	8	25	—	13	50	pA/°C
Input Voltage Range	IVR		±13.0	±13.5	—	±13.0	±13.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.0V$	110	123	—	110	123	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	5	20	—	5	20	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$, $V_O = \pm 10V$	200	400	—	150	400	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±12.0	±12.6	—	±12.0	±12.6	—	V

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-05E MIN	OP-05E TYP	OP-05E MAX	OP-05C MIN	OP-05C TYP	OP-05C MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.2	0.5	—	0.3	1.3	mV
Long-Term Input Offset Voltage Stability	$\Delta V_{OS}/Time$	(Notes 1, 2)	—	0.3	1.5	—	0.4	2.0	μV/Mo
Input Offset Current	I_{OS}		—	1.2	3.8	—	1.8	6.0	nA
Input Bias Current	I_B		—	±1.2	±4.0	—	±1.8	±7.0	nA
Input Noise Voltage (Note 2)	e_{np-p}	0.1Hz to 10Hz	—	0.35	0.6	—	0.38	0.65	μV_{p-p}
Input Noise Voltage Density (Note 2)	e_n	$f_O = 10Hz$	—	10.3	18.0	—	10.5	20.0	$nV/\sqrt{Hz}$
		$f_O = 100Hz$	—	10.0	13.0	—	10.2	13.5	
		$f_O = 1000Hz$	—	9.6	11.0	—	9.8	11.5	
Input Noise Current (Note 2)	i_{np-p}	0.1Hz to 10Hz	—	14	30	—	15	35	pA_{p-p}
Input Noise Current Density (Note 2)	i_n	$f_O = 10Hz$	—	0.32	0.80	—	0.35	0.90	$pA/\sqrt{Hz}$
		$f_O = 100Hz$	—	0.14	0.23	—	0.15	0.27	
		$f_O = 1000Hz$	—	0.12	0.17	—	0.13	0.18	
Input Resistance — Differential-Mode	R_{IN}	(Note 3)	15	50	—	8	33	—	MΩ
Input Resistance — Common-Mode	R_{INCM}		—	160	—	—	120	—	GΩ
Input Voltage Range	IVR		±13.5	±14.0	—	±13.0	±14.0	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.5V$	110	123	—	100	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	5	20	—	7	32	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$, $V_O = \pm 10V$	200	500	—	120	400	—	V/mV
		$R_L \ge 500\Omega$, $V_O = \pm 0.5V$ $V_S = \pm 3V$ (Note 3)	150	500	—	100	400	—	
Output Voltage Swing	V_O	$R_L \ge 10k\Omega$	±12.5	±13.0	—	±12.0	±13.0	—	V
		$R_L \ge 2k\Omega$	±12.0	±12.8	—	±11.5	±12.8	—	
		$R_L \ge 1k\Omega$	±10.5	±12.0	—	—	±12.0	—	
Slewing Rate (Note 2)	SR	$R_L = \ge 2k\Omega$	0.1	0.3	—	0.1	0.3	—	V/μs
Closed-Loop Bandwidth (Note 2)	BW	$A_{VCL} = +1.0$	0.4	0.6	—	0.4	0.6	—	MHz
Open-Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	60	—	—	60	—	Ω
Power Consumption	P_d	No load	—	90	120	—	95	150	mW
		$V_S = \pm 3V$, No load	—	4	6	—	4	8	
Offset Adjustment Range		$R_P = 20k\Omega$	—	4	—	—	4	—	mV

NOTE: See notes on previous page.

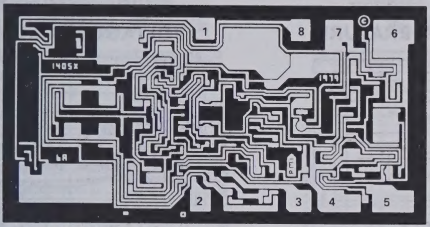
ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $0°C \le T_A \le +70°C$, unless otherwise noted.

			OP-05E			OP-05C			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.25	0.6	—	0.35	1.6	mV
Average Input Offset Voltage Drift Without External Trim	TCV_{OS}	(Note 2)	—	0.7	2.0	—	1.3	4.5	$\mu V/°C$
With External Trim	TCV_{OSn}	$R_P = 20k\Omega$ (Note 3)	—	0.2	0.6	—	0.4	1.5	
Input Offset Current	I_{OS}		—	1.4	5.3	—	2.0	8.0	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 2)	—	8	35	—	12	50	$pA/°C$
Input Bias Current	I_B		—	±1.5	±5.5	—	±2.2	±9.0	nA
Average Input Bias Current Drift	TCI_B	(Note 2)	—	13	35	—	18	50	$pA/°C$
Input Voltage Range	IVR		±13.0	±13.5	—	±13.0	±13.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm13.0V$	107	123	—	97	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm3V$ to $\pm18V$	—	7	32	—	10	51	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$, $V_O = \pm10V$	180	450	—	100	400	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±12.0	±12.6	—	±11.0	±12.6	—	V

NOTES:

1. Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5µV. Refer to typical performance curve.
2. Sample tested.
3. Guaranteed by design.

DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)



DIE SIZE 0.100 × 0.051 inch, 5100 sq. mils
(2.54 × 1.30 mm, 3.29 sq. mm)

1. BALANCE
2. INVERTING INPUT
3. NON-INVERTING INPUT
4. V−
5. NO CONNECTION
6. OUTPUT
7. V+
8. BALANCE

For additional DICE information refer to Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$ for OP-05N, OP-05G and OP-05GR devices; $T_A = 125°C$ for OP-05NT and OP-05GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-05NT LIMIT	OP-05N LIMIT	OP-05GT LIMIT	OP-05G LIMIT	OP-05GR LIMIT	UNITS
Input Offset Voltage	V_{OS}		0.25	0.15	0.7	0.5	1.3	mV MAX
Input Offset Current	I_{OS}		4.0	2.0	5.7	3.8	6.0	nA MAX
Input Bias Current	I_B		±4	±2	±6	±4	±7	nA MAX
Input Resistance Differential Mode	R_{IN}	(Note 2)	—	20	—	15	8	MΩ MIN
Input Voltage Range	IVR		±13.0	±13.5	±13.0	±13.5	±13.0	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.5V$ at +25° C $V_{CM} = \pm 13.0$ at +125° C	110	114	110	110	100	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	20	10	20	20	30	μV/V MAX
Output Voltage Swing	V_O	$R_L = 10k\Omega$ $R_L = 2k\Omega$ $R_L = 1k\Omega$	— ±12.0 —	±12.5 ±12.0 ±10.5	— ±12.0 —	±12.5 ±12.0 ±10.5	±12.0 ±11.5 —	V MIN
Large-Signal Voltage Gain	A_{VO}	$R_L = 2k\Omega$ $V_O = \pm 10V$	200	200	150	200	120	V/mV MIN
Differential Input Voltage			±30	±30	±30	±30	±30	V MAX
Power Consumption	P_d	$V_{OUT} = 0V$	—	120	—	120	150	mW MAX

NOTES:
1. For 25° C characteristics of NT & GT devices see N & G characteristics respectively.
2. Guaranteed by design.

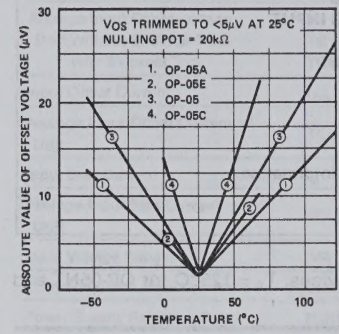
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25° C$, unless otherwise noted.

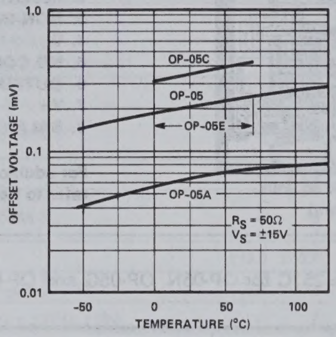
PARAMETER	SYMBOL	CONDITIONS	OP-05NT TYPICAL	OP-05N TYPICAL	OP-05GT TYPICAL	OP-05G TYPICAL	OP-05GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}	$R_S \leq 50\Omega$	0.3	0.3	0.7	0.7	1.2	μV/° C
Nulled Input Offset Voltage Drift	TCV_{OSn}	$R_S \leq 50\Omega$, $R_p = 20k\Omega$	0.2	0.2	0.3	0.3	0.4	μV/° C
Average Input Offset Current Drift	TCI_{OS}		5	5	8	8	12	pA/° C
Slew Rate	SR	$R_L \geq 2k\Omega$	0.3	0.3	0.3	0.3	0.3	V/μs
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$	0.6	0.6	0.6	0.6	0.6	MHz

TYPICAL PERFORMANCE CHARACTERISTICS

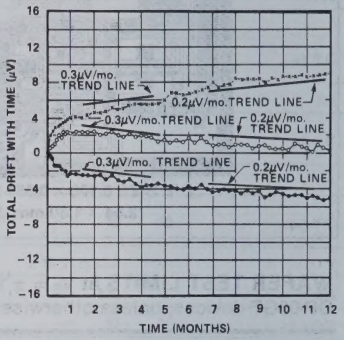
TRIMMED OFFSET VOLTAGE vs TEMPERATURE



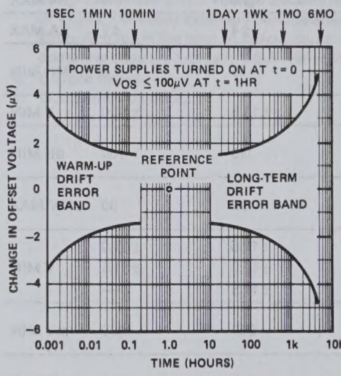
UNTRIMMED OFFSET VOLTAGE vs TEMPERATURE



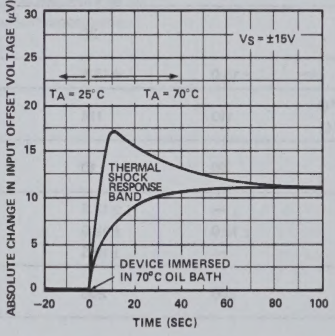
TYPICAL OFFSET VOLTAGE STABILITY vs TIME



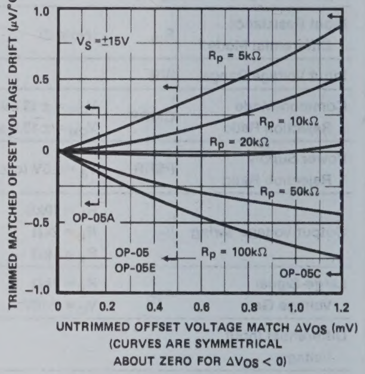
OFFSET VOLTAGE DRIFT WITH TIME



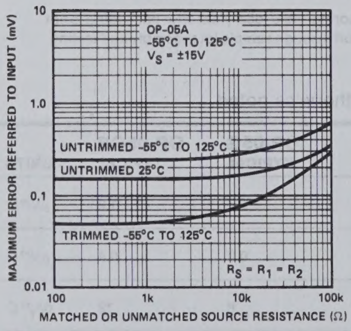
OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



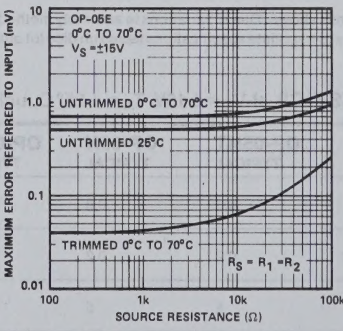
TRIMMED OFFSET VOLTAGE DRIFT



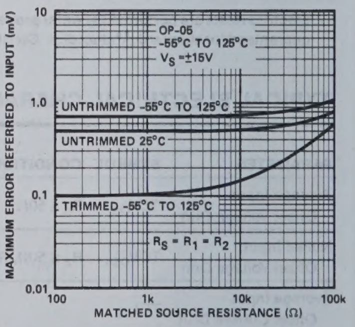
MAXIMUM ERROR vs SOURCE RESISTANCE



MAXIMUM ERROR vs SOURCE RESISTANCE

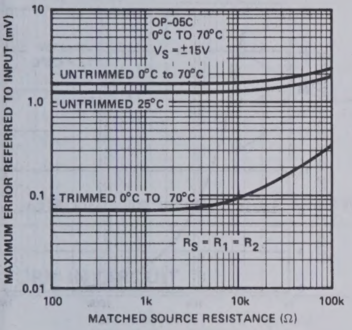


MAXIMUM ERROR vs SOURCE RESISTANCE

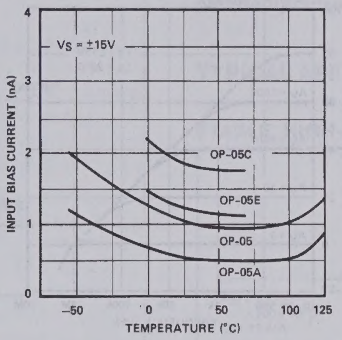


TYPICAL PERFORMANCE CHARACTERISTICS

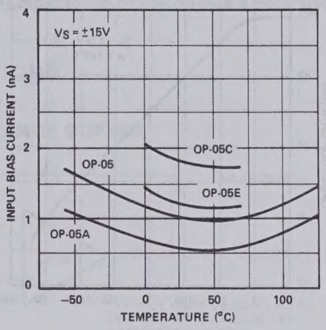
MAXIMUM ERROR vs SOURCE RESISTANCE



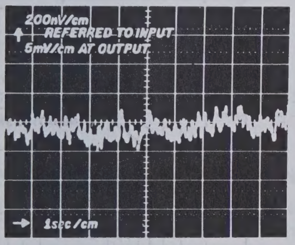
INPUT BIAS CURRENT vs TEMPERATURE



INPUT OFFSET CURRENT vs TEMPERATURE

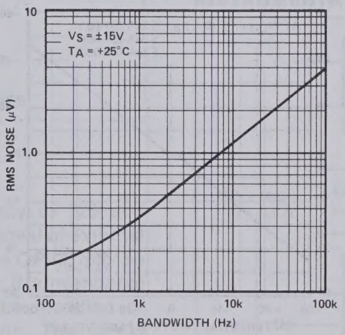


OP-05 LOW FREQUENCY NOISE

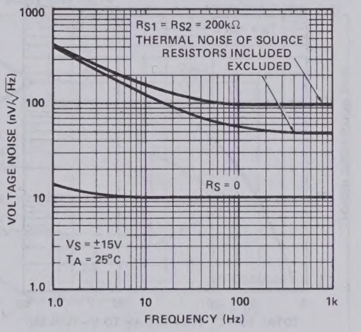


(SEE NOISE TEST CIRCUIT)

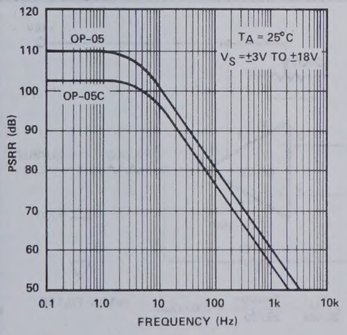
INPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



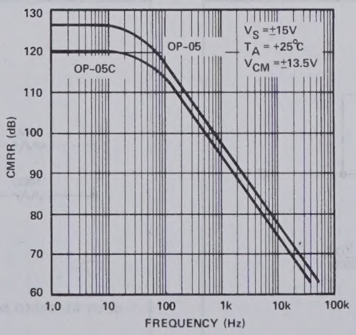
VOLTAGE NOISE DENSITY vs FREQUENCY



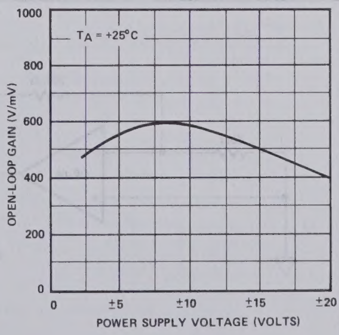
PSRR vs FREQUENCY



CMRR vs FREQUENCY

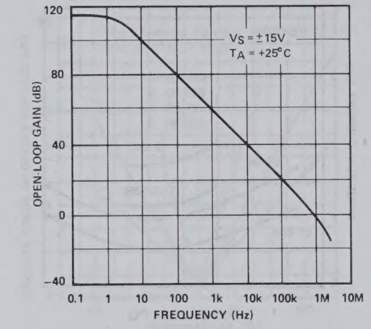


OPEN-LOOP GAIN vs POWER SUPPLY VOLTAGE

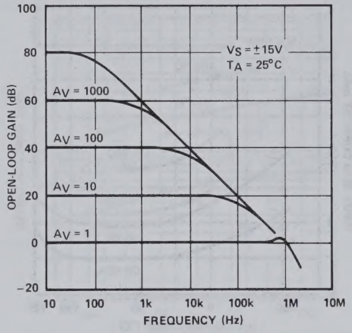


TYPICAL PERFORMANCE CHARACTERISTICS

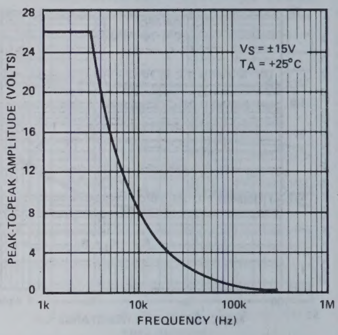
OPEN-LOOP GAIN vs FREQUENCY



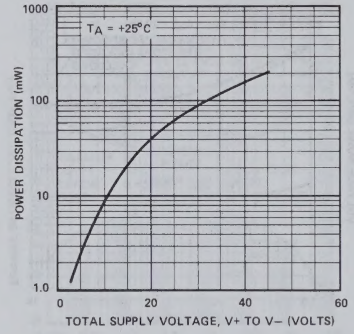
CLOSED-LOOP GAIN vs FREQUENCY



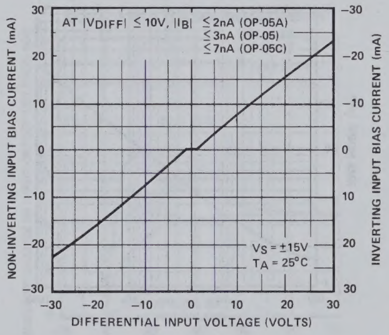
MAXIMUM OUTPUT SWING vs FREQUENCY



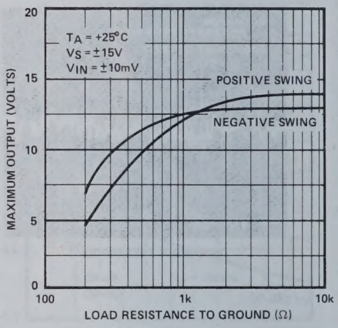
POWER CONSUMPTION vs POWER SUPPLY



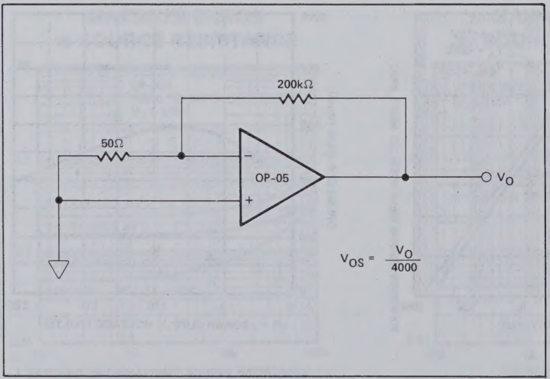
INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE



MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE

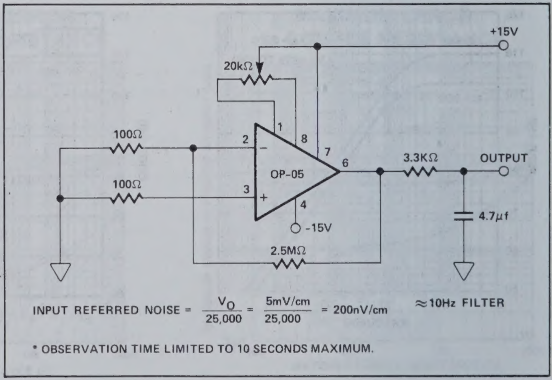


TYPICAL OFFSET VOLTAGE TEST CIRCUIT


200kΩ
50Ω
−
+
OP-05
V_O

$$V_{OS} = \frac{V_O}{4000}$$

TYPICAL LOW-FREQUENCY NOISE TEST CIRCUIT*

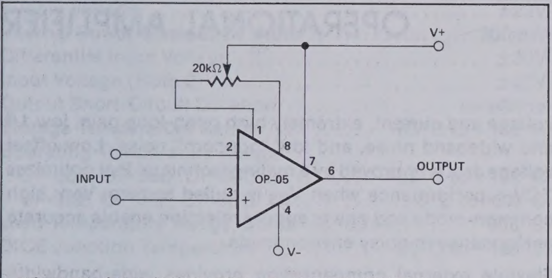

+15V
20kΩ
1
8
100Ω
2
−
7
6
3.3KΩ
OUTPUT
100Ω
3
+
OP-05
4
−15V
4.7μf
2.5MΩ

$$\text{INPUT REFERRED NOISE} = \frac{V_O}{25{,}000} = \frac{5mV/cm}{25{,}000} = 200nV/cm$$

≈10Hz FILTER

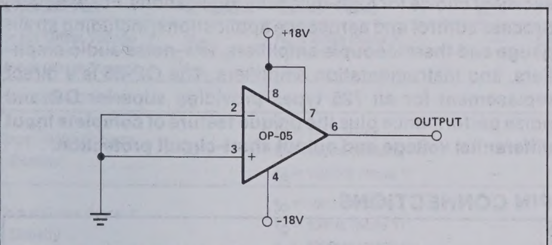
* OBSERVATION TIME LIMITED TO 10 SECONDS MAXIMUM.

OFFSET NULLING CIRCUIT


V+
20kΩ
1
8
2
7
6
OUTPUT
INPUT
OP-05
3
4
V-

NOTE: PIN OUTS SHOWN FOR J, P, AND Z PACKAGES.

BURN-IN CIRCUIT


+18V
8
2
7
OUTPUT
OP-05
6
3
4
-18V

NOTE: PIN OUTS SHOWN FOR J, P, AND Z PACKAGES.

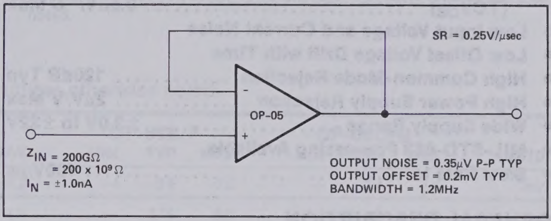
APPLICATIONS INFORMATION

OP-05 series devices may be fitted directly to 725 and 108/108A Series sockets with or without removal of external compensation components. Additionally, the OP-05 may be fitted to unnulled 741 series sockets. However, if conventional 741 nulling circuitry is in use, it should be modified or removed to enable proper OP-05 operation. The OP-05 provides stable operation with load capacitance of up to 500pF and ±10V swings; larger capacitances should be decoupled with a 50Ω resistor.

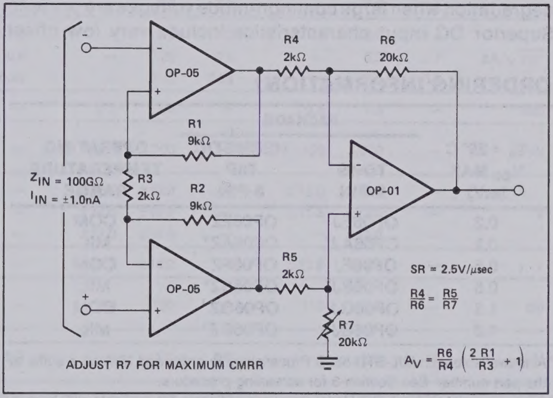
Offset stability can be degraded by stray thermoelectric voltages arising from dissimilar metals at the contacts to the input terminals. Best operation will be obtained when both input contacts are maintained at the same temperature, preferably close to the temperature of the device's package.

TYPICAL APPLICATIONS

STABLE, HIGH-IMPEDANCE BUFFER


SR = 0.25V/μsec
OP-05
Z_{IN} = 200GΩ
= 200 x 10^9Ω
I_N = ±1.0nA
OUTPUT NOISE = 0.35μV P-P TYP
OUTPUT OFFSET = 0.2mV TYP
BANDWIDTH = 1.2MHz

HIGH IMPEDANCE, HIGH COMMON-MODE REJECTION INSTRUMENTATION AMPLIFIER


OP-05
R4
2kΩ
R6
20kΩ
R1
9kΩ
Z_{IN} = 100GΩ
I_{IN} = ±1.0nA
R3
2kΩ
R2
9kΩ
OP-01
OP-05
R5
2kΩ
SR = 2.5V/μsec
$\frac{R4}{R6} = \frac{R5}{R7}$
R7
20kΩ
ADJUST R7 FOR MAXIMUM CMRR
$A_V = \frac{R6}{R4}\left(\frac{2\,R1}{R3} + 1\right)$

OP-06

HIGH-GAIN INSTRUMENTATION OPERATIONAL AMPLIFIER

FEATURES

- **Very High Voltage Gain .... 1,000V/mV Min**
- **Low Offset Voltage and Offset Current**
- **Low Drift vs. Temperature (TCV_{OS}) .... 0.8μV/°C Max**
- **Low Input Voltage and Current Noise**
- **Low Offset Voltage Drift with Time**
- **High Common-Mode Rejection .... 120dB Typ**
- **High Power Supply Rejection .... 2μV/V Max**
- **Wide Supply Range .... ±3.0V to ±22V**
- **MIL-STD-883 Processing Available**
- **Slew Rate to 100V/μs**

GENERAL DESCRIPTION

The OP-06 monolithic instrumentation operational amplifier is designed for accurate high-gain amplification of low level signals. High common-mode rejection reduces signal degradation when large common-mode voltages are present. Superior DC input characteristics include very low offset voltage and current, extremely high open-loop gain, low 1/f and wideband noise, and low "popcorn" noise. Low offset voltage drift is improved by a nulling technique that optimizes TCV_{OS} performance when V_{OS} is nulled to zero. Very high common-mode and power supply rejection enable accurate performance in noisy environments.

Flexible external compensation provides wide-bandwidth and high slew rate operation in high closed-loop gain applications. Excellent long-term stability, and compatibility with MIL-STD-883 processing, make the OP-06 an excellent choice for high-reliability applications. For example, process control and aerospace applications; including strain gauge and thermocouple amplifiers, low-noise audio amplifiers, and instrumentation amplifiers. The OP-06 is a direct replacement for all 725 types providing superior DC and noise performance plus the unique feature of **complete input differential voltage and output short-circuit protection.**

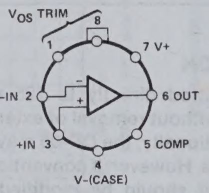
ORDERING INFORMATION†

$T_A = 25°C$ V_{OS} MAX (mV)	PACKAGE TO-99 8-PIN	PACKAGE HERMETIC DIP 8-PIN	OPERATING TEMPERATURE RANGE
0.2	OP06EJ	OP06EZ	COM
0.2	OP06AJ*	OP06AZ*	MIL
0.5	OP06FJ	OP06FZ	COM
0.5	OP06BJ*	OP06BZ*	MIL
1.3	OP06GJ	OP06GZ	COM
1.3	OP06CJ*	OP06CZ*	MIL

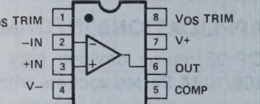
*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

PIN CONNECTIONS

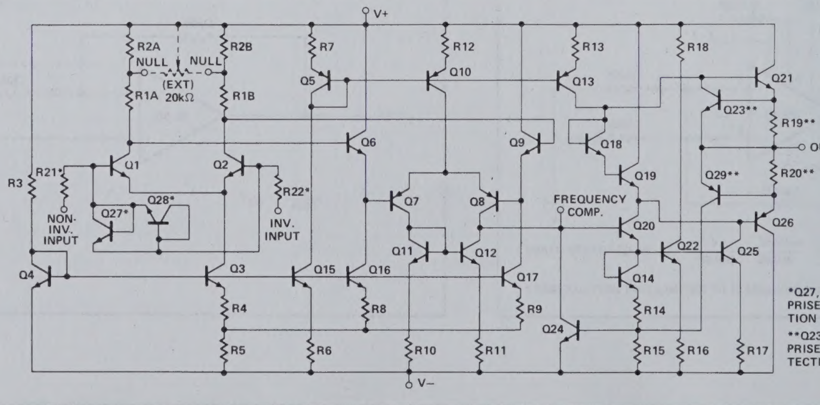

VOS TRIM
8
1
7 V+
–IN 2
6 OUT
+IN 3
5 COMP
4
V–(CASE)

TO-99 (J-Suffix)


VOS TRIM 1
–IN 2
+IN 3
V– 4
8 VOS TRIM
7 V+
6 OUT
5 COMP

8-PIN HERMETIC DIP (Z-Suffix)

SIMPLIFIED SCHEMATIC


V+
R2A
R2B
NULL
NULL
(EXT) 20kΩ
R1A
R1B
R7
R12
R13
R18
Q5
Q10
Q13
Q21
Q23**
R19**
OUTPUT
Q6
Q9
Q18
Q1
Q2
R3
R21*
R22*
NON-INV. INPUT
INV. INPUT
Q27*
Q28*
Q7
Q8
Q19
Q29**
R20**
FREQUENCY COMP.
Q20
Q26
Q11
Q12
Q22
Q25
Q4
Q3
Q15
Q16
Q17
Q14
R4
R8
R9
R14
Q24
R5
R6
R10
R11
R15
R16
R17
V–

*Q27, Q28, R21, R22, COMPRISE THE INPUT PROTECTION CIRCUIT.

**Q23, Q29, R19, R20 COMPRISE THE OUTPUT PROTECTION CIRCUIT.

ABSOLUTE MAXIMUM RATINGS (Note 3)

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±22V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
OP-06A, OP-06B, OP-06C	−55°C to +125°C
OP-06E, OP-06F, OP-06G	0°C to +70°C
Lead Temperature Range (Soldering, 60 sec)	300°C
DICE Junction Temperature	−65°C to +150°C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mV/°C

2. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
3. Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $T_A = 25°C$, unless otherwise noted.

			OP-06A/E			OP-06B/F			OP-06C/G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$ (Note 2)	—	0.06	0.2	—	0.2	0.5	—	0.4	1.3	mV
Input Offset Current	I_{OS}		—	0.3	2.0	—	0.75	5.0	—	2	13	nA
Input Bias Current	I_B		—	30	70	—	30	80	—	40	110	nA
Input Noise Voltage Density	e_n	$f_O = 10Hz$ (Note 1)	—	9.0	15.0	—	9.0	15.0	—	9.0	15.0	$nV/\sqrt{Hz}$
		$f_O = 100Hz$ (Note 1)	—	8.0	9.0	—	8.0	9.0	—	8.0	9.0	
		$f_O = 1000Hz$ (Note 1)	—	7.0	7.5	—	7.0	7.5	—	7.0	7.5	
Input Noise Current Density	i_n	$f_O = 10Hz$ (Note 1)	—	0.5	1.2	—	0.5	1.2	—	0.6	1.4	$pA/\sqrt{Hz}$
		$f_O = 100Hz$ (Note 1)	—	0.25	0.6	—	0.25	0.6	—	0.3	0.7	
		$f_O = 1000Hz$ (Note 1)	—	0.15	0.25	—	0.15	0.25	—	0.2	0.3	
Input Resistance	R_{IN}	(Note 3)	0.8	1.8	—	0.7	1.8	—	0.5	1.5	—	MΩ
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm10V$	1,000	3,000	—	1,000	3,000	—	500	3,000	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	±12.5	±13.0	—	±12.5	±13.0	—	±12.0	±13.0	—	V
		$R_L \geq 2k\Omega$	±12.0	±12.8	—	±12.0	±12.8	—	±11.5	±12.8	—	
		$R_L \geq 1k\Omega$	±11.0	±12.5	—	±11.0	±12.5	—	—	±12.0	—	
Input Voltage Range	IVR		±13.5	±14.0	—	±13.5	±14.0	—	±13.5	±14.0	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm13.5V$ $R_S \leq 20k\Omega$	114	120	—	114	120	—	110	115	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm3V$ to $\pm18V$ $R_S \leq 20k\Omega$	—	0.5	2.0	—	1.0	5.0	—	2.0	10	μV/V
Power Consumption	P_d		—	90	120	—	90	120	—	110	150	mW
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 500\Omega$, (Note 3) $V_O = \pm0.5V$ $V_S = \pm3V$	100	600	—	100	600	—	60	600	—	V/mV
Power Consumption	P_d	$V_S = \pm3V$	—	4	6	—	4	6	—	4	8	mW

NOTES:

1. Sample tested.
2. Thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can degrade drift performance. Both sides of the contacts should be kept at approximately the same temperature. All temperature gradients should be minimized.
3. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, −55°C ≤ T_A ≤ +125°C, unless otherwise noted.

				OP-06A			OP-06B			OP-06C		
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage (Without external trim)	V_{OS}	$R_S \leq 20\text{k}\Omega$ (Note 2)	—	0.08	0.28	—	0.3	0.7	—	0.5	1.6	mV
Average Input Offset Voltage Drift (Without external trim)	TCV_{OS}	$R_S = 50\Omega$ (Notes 1, 2)	—	0.3	0.8	—	0.7	2.0	—	1.4	4.5	μV/°C
Average Input Offset Voltage Drift (With external trim)	TCV_{OSn}	$R_S = 50\Omega$ (Notes 2, 3) $R_P = 20\text{k}\Omega$	—	0.2	0.6	—	0.28	1.0	—	0.5	1.5	μV/°C
Input Offset Current	I_{OS}	T_A MAX T_A MIN	— —	0.25 0.8	1.0 4.0	— —	0.6 2.0	4.0 18.0	— —	2.0 3.0	15 25	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 1)	—	3	20	—	8	90	—	14	150	pA/°C
Input Bias Current	I_B	T_A MAX T_A MIN	— —	22 40	60 120	— —	25 45	70 180	— —	35 45	110 180	nA
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.5\text{V}$ $R_S \leq 20\text{k}\Omega$	109	112	—	109	112	—	95	110	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3\text{V}$ to $\pm 18\text{V}$ $R_S \leq 20\text{k}\Omega$	—	1	5	—	2	8	—	3	15	μV/V
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10\text{V}$; $R_L \geq 2\text{k}\Omega$ T_A MAX T_A MIN	1,000 700	3,500 2,000	— —	1,000 700	3,500 1,800	— —	400 300	3,200 1,700	— —	V/mV
Output Voltage Swing	V_O	$R_L \geq 2\text{k}\Omega$	±12.0	±12.6	—	±12.0	±12.6	—	±11.0	±12.6	—	V

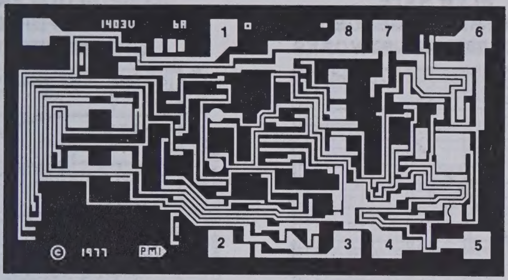
ELECTRICAL CHARACTERISTICS at V_S = ±15V, 0°C ≤ T_A ≤ 70°C, unless otherwise noted.

				OP-06E			OP-06F			OP-06G		
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage (Without external trim)	V_{OS}	$R_S \leq 20\text{k}\Omega$ (Note 2)	—	0.08	0.28	—	0.25	0.6	—	0.5	1.6	mV
Average Input Offset Voltage Drift (Without external trim)	TCV_{OS}	$R_S = 50\Omega$ (Notes 1, 2)	—	0.3	0.8	—	0.7	2.0	—	1.4	4.5	μV/°C
Average Input Offset Voltage Drift (With external trim)	TCV_{OSn}	$R_S = 50\Omega$ (Notes 2, 3) $R_P = 20\text{k}\Omega$	—	0.2	0.6	—	0.28	1.0	—	0.5	1.5	μV/°C
Input Offset Current	I_{OS}	T_A MAX T_A MIN	— —	0.25 0.8	1.0 4.0	— —	0.65 2.0	5.0 18.0	— —	2.0 3.0	15 25	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 1)	—	3	20	—	8	90	—	14	150	pA/°C
Input Bias Current	I_B	T_A MAX T_A MIN	— —	22 40	60 120	— —	30 45	80 180	— —	35 45	110 180	nA
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.5\text{V}$ $R_S \leq 20\text{k}\Omega$	109	112	—	109	112	—	95	110	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3\text{V}$ to $\pm 18\text{V}$ $R_S \leq 20\text{k}\Omega$	—	1.0	5.0	—	1.5	7.0	—	3.0	15	μV/V
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10\text{V}$; $R_L \geq 2\text{k}\Omega$ T_A MAX T_A MIN	1,000 800	3,500 2,000	— —	1,000 800	3,500 1,800	— —	400 300	3,200 1,700	— —	V/mV
Output Voltage Swing	V_O	$R_L \geq 2\text{k}\Omega$	±12.0	±12.6	—	±12.0	±12.6	—	±11.0	±12.6	—	V

NOTES:

1. Sample tested.
2. Thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can degrade drift performance. Both sides of the contacts should be kept at approximately the same temperature. All temperature gradients should be minimized.
3. Guaranteed by design.

DICE CHARACTERISTICS



DIE SIZE 0.094 × 0.050 inch, 4700sq. mils
(2.39 × 1.27 mm, 3.03 sq. mm)

1. **NULL**
2. **INVERTING INPUT**
3. **NONINVERTING INPUT**
4. **V−**
5. **COMPENSATION**
6. **OUTPUT**
7. **V+**
8. **NULL**

For additional DICE information refer to Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$ for OP-06N, OP-06G and OP-06GR devices; $T_A = 125°C$ for OP-06NT and OP-06GT devices, unless otherwise noted. (Note 2)

PARAMETER	SYMBOL	CONDITIONS	OP-06NT LIMIT	OP-06N LIMIT	OP-06GT LIMIT	OP-06G LIMIT	OP-06GR LIMIT	UNITS
nput Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	0.3	0.2	0.7	0.5	1.3	mV MAX
nput Offset Current	I_{OS}		1	2	4	5	13	nA MAX
nput Bias Current	I_B		60	70	70	80	110	nA MAX
nput Resistance Differential Mode	R_{IN}	(Note 1)	—	0.8	—	0.7	0.5	MΩ MIN
nput Voltage Range	IVR		±13.0	±13.5	±13.0	±13.5	±13.5	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.5$ $R_S \leq 20k\Omega$	108	114	108	114	110	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$ $R_S \leq 20k\Omega$	6	2	8	5	10	μV/V MAX
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	— ±12.0 —	±12.5 ±12.0 ±11.0	— ±12.0 —	±12.5 ±12.0 ±11.0	±12.0 ±11.5 —	V MIN
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	1000	1000	800	1000	500	V/mV MIN
Differential Input Voltage			±30	±30	±30	±30	±30	V MAX
Power Consumption ($V_{OUT} = 0V$)	P_d		—	120	—	120	150	mW MAX

Note: Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

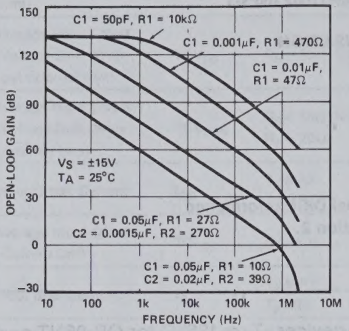
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-06NT TYPICAL	OP-06N TYPICAL	OP-06GT TYPICAL	OP-06G TYPICAL	OP-06GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}	$R_S \leq 50\Omega$	0.3	0.3	0.7	0.7	1.4	μV/°C
Nulled Input Offset Voltage Drift	TCV_{OSn}	$R_S \leq 50k\Omega$ $R_P = 20k\Omega$	0.2	0.2	0.28	0.28	0.5	μV/°C
Average Input Offset Current Drift	TCI_{OS}		3	3	8	8	14	pA/°C

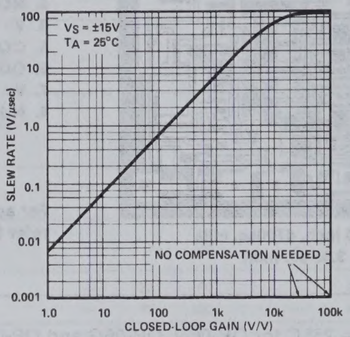
NOTES:
1. Guaranteed by design.
2. For +25°C specifications of OP-06NT and OP-06GT, see OP-06N and OP-06G respectively.

TYPICAL PERFORMANCE CHARACTERISTICS

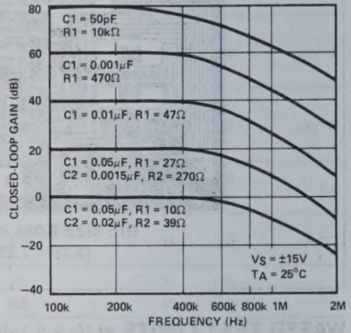
OPEN-LOOP RESPONSE FOR VALUES OF COMPENSATION



SLEW RATE USING RECOMMENDED COMPENSATION NETWORKS



CLOSED-LOOP FREQUENCY RESPONSE FOR VALUES OF COMPENSATION

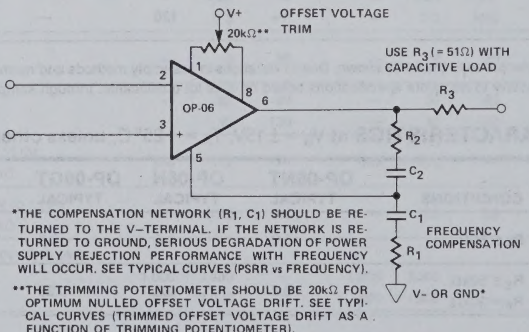


FREQUENCY COMPENSATION

COMPENSATION VALUES

Avcl	R_1 (Ω)	C_1 (μF)	R_2 (Ω)	C_2 (μF)
10000	10k	50pF	—	—
1000	470	0.001	—	—
100	47	0.01	—	—
10	27	0.05	270	0.0015
1	10	0.05	39	0.02

COMPENSATION CIRCUIT (J or Z PACKAGE)

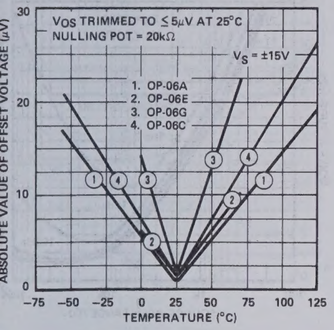

V+
20kΩ**
OFFSET VOLTAGE
TRIM
1
2
−
8
6
OP-06
3
+
5
USE R_3 (= 51Ω) WITH
CAPACITIVE LOAD
R_3
R_2
C_2
C_1
R_1
FREQUENCY
COMPENSATION
V− OR GND*

*THE COMPENSATION NETWORK (R_1, C_1) SHOULD BE RETURNED TO THE V−TERMINAL. IF THE NETWORK IS RETURNED TO GROUND, SERIOUS DEGRADATION OF POWER SUPPLY REJECTION PERFORMANCE WITH FREQUENCY WILL OCCUR. SEE TYPICAL CURVES (PSRR vs FREQUENCY).

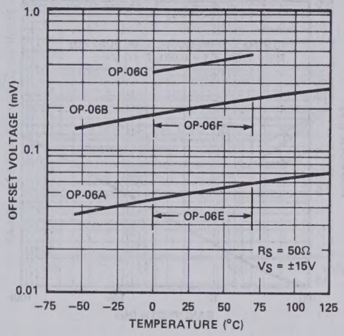
**THE TRIMMING POTENTIOMETER SHOULD BE 20kΩ FOR OPTIMUM NULLED OFFSET VOLTAGE DRIFT. SEE TYPICAL CURVES (TRIMMED OFFSET VOLTAGE DRIFT AS A FUNCTION OF TRIMMING POTENTIOMETER).

TYPICAL PERFORMANCE CHARACTERISTICS

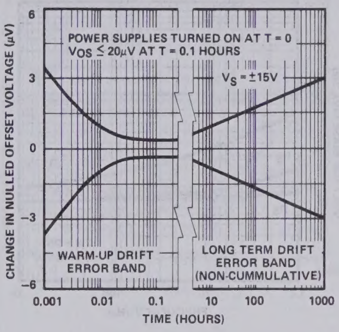
TRIMMED OFFSET VOLTAGE vs TEMPERATURE



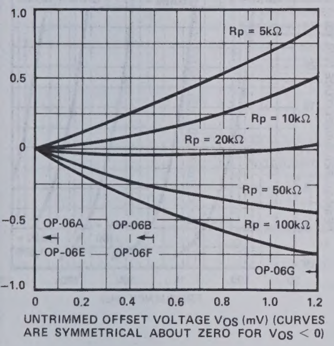
OFFSET VOLTAGE vs TEMPERATURE



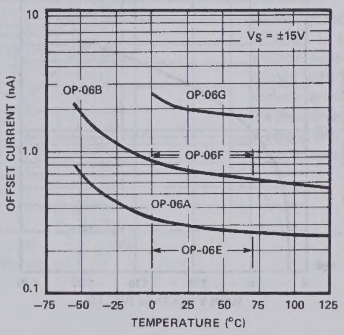
OFFSET VOLTAGE DRIFT WITH TIME



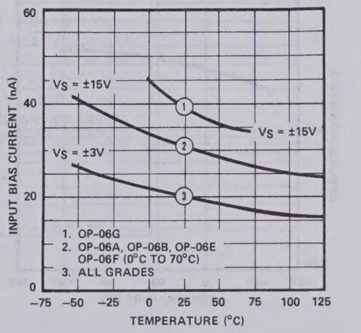
TRIMMED OFFSET VOLTAGE DRIFT AS A FUNCTION OF TRIMMING POTENTIOMETER (R_P) SIZE AND V_{OS}



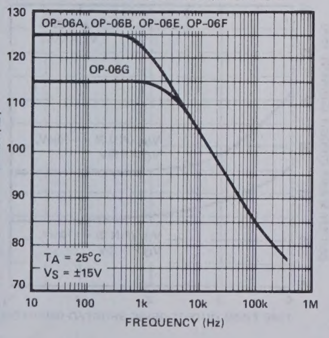
OFFSET CURRENT vs TEMPERATURE



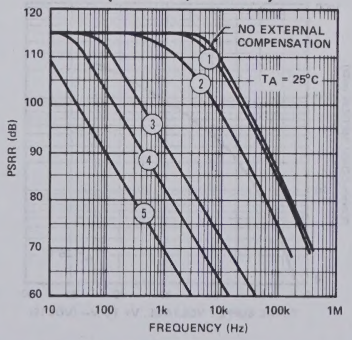
INPUT BIAS CURRENT vs TEMPERATURE



CMRR vs FREQUENCY

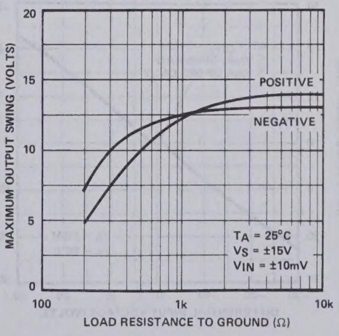


PSRR vs FREQUENCY (OP-06B, OP-06E)



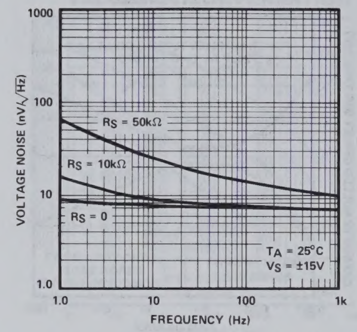
1. C1 = 0.001μF, R1 = 470Ω FROM PIN 5 TO V−
2. C1 = 0.1μF, R1 = 5Ω TO V−
3. C1 = 0.001μF, R1 = 470Ω FROM PIN 5 TO GND
4. C1 = 0.05μF, R1 = 10Ω, C2 = 0.02μF, R2 = 39Ω TO V−
5. C1 = 0.05μF, R1 = 10Ω, C2 = 0.02μF, R2 = 39Ω TO GND

MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE

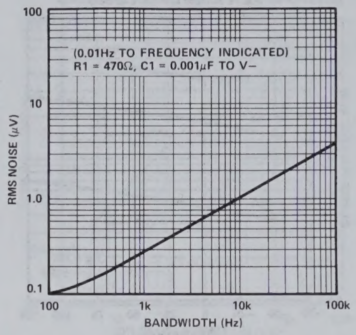


TYPICAL PERFORMANCE CHARACTERISTICS

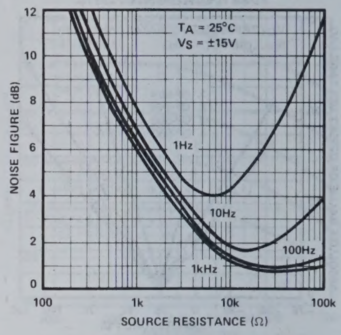
VOLTAGE NOISE DENSITY vs FREQUENCY



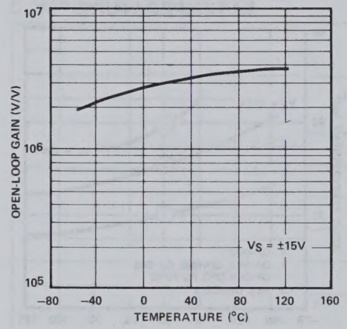
INPUT WIDEBAND NOISE vs BANDWIDTH



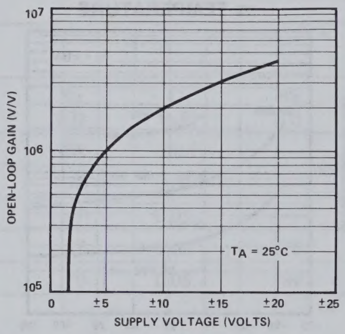
NOISE FIGURE vs SOURCE RESISTANCE



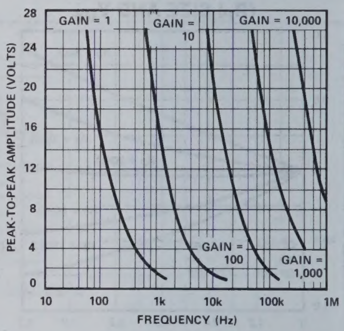
OPEN-LOOP GAIN vs TEMPERATURE



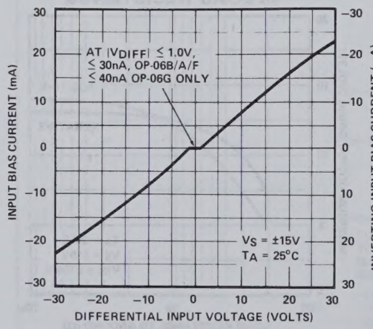
OPEN-LOOP GAIN vs SUPPLY VOLTAGE



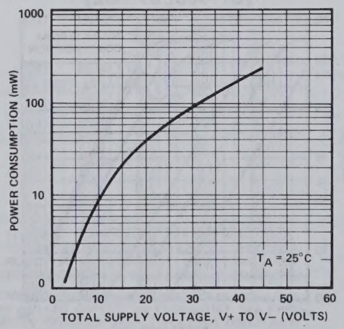
MAXIMUM OUTPUT SWING vs FREQUENCY



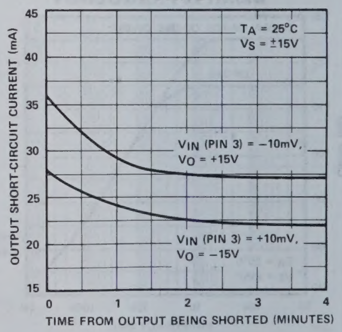
INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE



POWER CONSUMPTION vs SUPPLY VOLTAGE

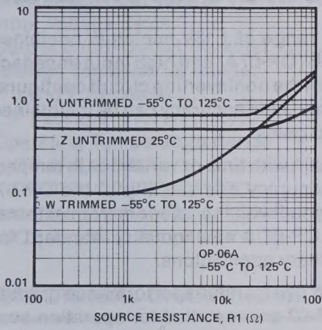


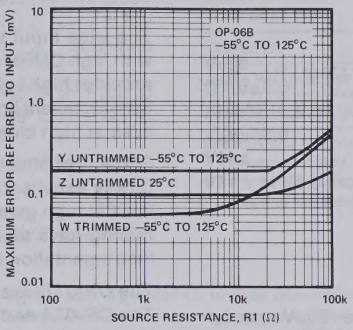
OUTPUT SHORT-CIRCUIT CURRENT

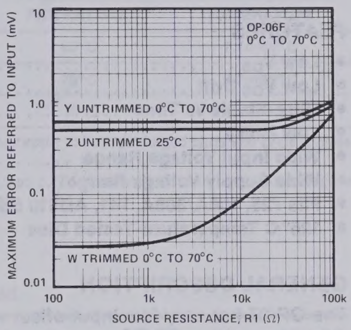


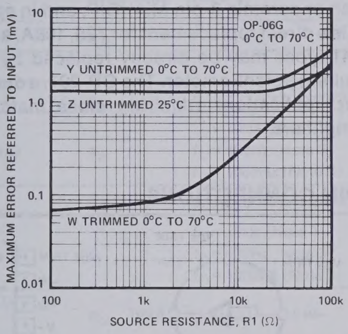
NOTE: For further information refer to AN-15, "Minimization of Noise in Operational Amplifier Applications".

;UARANTEED PERFORMANCE CHARACTERISTICS









These graphs depict maximum error referred to the input as a function of source resistance (R_1). Curves W are shown with V_{OS} trimmed at +25° C and include errors due to V_{OS} and I_{OS} over the indicated temperature range. Curves Y and Z plot maximum errors with V_{OS} not trimmed.

OP-07 ULTRA-LOW OFFSET VOLTAGE OPERATIONAL AMPLIFIER

FEATURES

- **Low V_{OS} .... $10\mu V$**
- **Low V_{OS} Drift .... $0.2\mu V/^\circ C$**
- **Ultra-Stable vs Time .... $0.2\mu V$/Month**
- **Low Noise .... $0.35\mu V_{p-p}$**
- **Wide Input Voltage Range .... ±14V**
- **Wide Supply Voltage Range .... ±3V to ±18V**
- **Fits 725, 108A/308A, 741, AD510 Sockets**
- **125°C Temperature-Tested Dice**

GENERAL DESCRIPTION

The OP-07 has very low input offset voltage ($25\mu V$ max for OP-07A) which is obtained by trimming at the wafer stage. These low offset voltages generally eliminate any need for external nulling. The OP-07 also features low input bias current (±2nA for OP-07A) and high open-loop gain (300V/mV for OP-07A). The low offsets and high open-loop gain make the OP-07 particularly useful for high-gain instrumentation applications.

ORDERING INFORMATION†

	PACKAGE			
$T_A = 25^\circ C$ V_{OS} MAX (μV)	TO-99 8-PIN	HERMETIC DIP 8-PIN	PLASTIC DIP 8-PIN	OPERATING TEMPERATURE RANGE
75	OP07AJ*	OP07AZ*		MIL
75	OP07EJ	OP07EZ	OP07EP	COM
75	OP07J*	OP07Z*		MIL
150	OP07CJ	OP07CZ	OP07CP	COM
150	OP07DJ		OP07DP	COM

*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

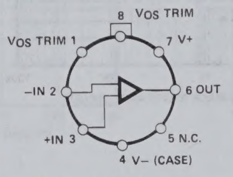
The wide input voltage range of ±13V minimum combined with high CMRR of 110dB (OP-07A) and high input impedace provides high accuracy in the noninverting circuit configuration. Excellent linearity and gain accuracy can be maintained even at high closed-loop gains.

Stability of offsets and gain with time or variations in temperture is excellent. The accuracy and stability of the OP-07, even at high gain, combined with the freedom from external nulling have made the OP-07 a new industry standard for instrumentation and military applications.

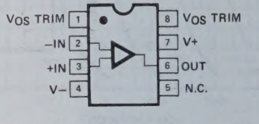
The OP-07 is available in five standard performance grades. The OP-07A and the OP-07 are specified for operation over the full military range of −55°C to +125°C; the OP-07 E, C, and D are specified for operation over the 0°C to +70°C range.

The OP-07 is available in hermetically-sealed TO-99 metal can or ceramic 8-pin Mini-DIP, and in epoxy 8-pin Mini-DIP. It is a direct replacement for 725, 108A, and OP-05 amplifiers; 741-types may be directly replaced by removing the 741's nulling potentiometer. The OP-207, a dual OP-07, is available for applications requiring close matching of two OP-07 amplifiers.

PIN CONNECTIONS

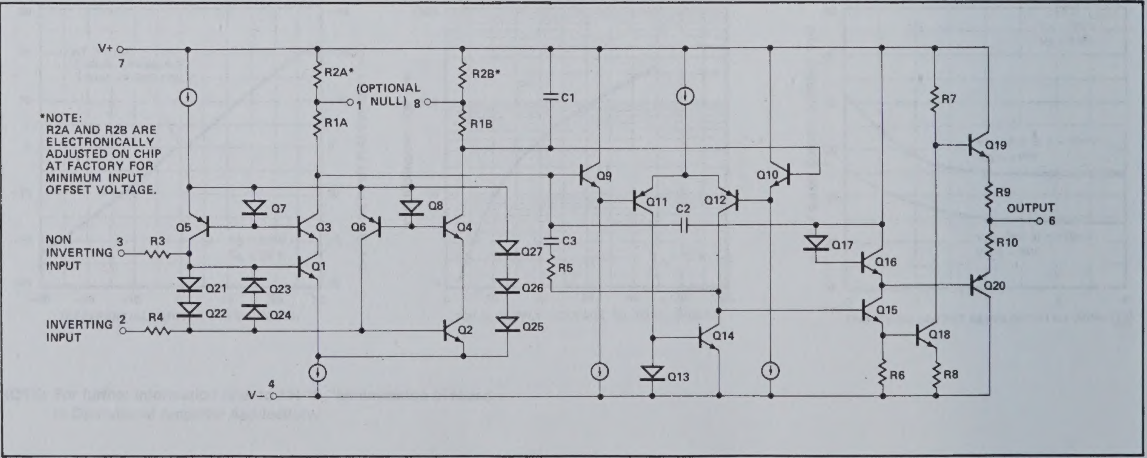

8 VOS TRIM
VOS TRIM 1
7 V+
−IN 2
6 OUT
+IN 3
5 N.C.
4 V− (CASE)

TO-99 (J-Suffix)


VOS TRIM 1
−IN 2
+IN 3
V− 4
8 VOS TRIM
7 V+
6 OUT
5 N.C.

**EPOXY MINI-DIP (P-Suffix)
8-PIN HERMETIC DIP
(Z-Suffix)**

SIMPLIFIED SCHEMATIC


V+ 7
R2A*
R2B*
(OPTIONAL NULL) 1 8
R1A
R1B
C1
R7
Q19
Q9
Q10
Q11
Q12
C2
Q7
Q8
Q5
Q3
Q6
Q4
R9
OUTPUT 6
C3
Q17
NON INVERTING INPUT 3
R3
Q1
Q27
R5
Q16
R10
Q21
Q23
Q26
Q20
Q22
Q24
Q15
INVERTING INPUT 2
R4
Q2
Q25
Q14
Q18
Q13
R6
R8
V− 4

*NOTE:
R2A AND R2B ARE ELECTRONICALLY ADJUSTED ON CHIP AT FACTORY FOR MINIMUM INPUT OFFSET VOLTAGE.

ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage .... ±22V
Internal Power Dissipation (Note 1) 500mW
Differential Input Voltage .... ±30V
Input Voltage (Note 3) .... ±22V
Output Short-Circuit Duration .... Indefinite
Storage Temperature Range
  J and Z Packages .... −65°C to +150°C
  P Package .... −65°C to +125°C
Operating Temperature Range
  OP-07A, OP-07 .... −55°C to +125°C
  OP-07E, OP-07C, OP-07D .... 0°C to +70°C
Lead Temperature Range (Soldering, 60 sec) ...... 300°C
DICE Junction Temperature (T_j) .... −65°C to +150°C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C
8-Pin Plastic DIP (P)	36°C	5.6mW/°C

2. Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.
3. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-07A MIN	OP-07A TYP	OP-07A MAX	OP-07 MIN	OP-07 TYP	OP-07 MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	10	25	—	30	75	μV
Long-Term Input Offset Voltage Stability	ΔV_{OS}/Time	(Note 2)	—	0.2	1.0	—	0.2	1.0	μV/Mo
Input Offset Current	I_{OS}		—	0.3	2.0	—	0.4	2.8	nA
Input Bias Current	I_B		—	±0.7	±2.0	—	±1.0	±3.0	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 3)	—	0.35	0.6	—	0.35	0.6	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10Hz$ (Note 3)	—	10.3	18.0	—	10.3	18.0	$nV/\sqrt{Hz}$
		$f_O = 100Hz$ (Note 3)	—	10.0	13.0	—	10.0	13.0	
		$f_O = 1000Hz$ (Note 3)	—	9.6	11.0	—	9.6	11.0	
Input Noise Current	i_{np-p}	0.1Hz to 10Hz (Note 3)	—	14	30	—	14	30	pA_{p-p}
Input Noise Current Density	i_n	$f_O = 10Hz$ (Note 3)	—	0.32	0.80	—	0.32	0.80	$pA/\sqrt{Hz}$
		$f_O = 100Hz$ (Note 3)	—	0.14	0.23	—	0.14	0.23	
		$f_O = 1000Hz$ (Note 3)	—	0.12	0.17	—	0.12	0.17	
Input Resistance — Differential-Mode	R_{IN}	(Note 4)	30	80	—	20	60	—	MΩ
Input Resistance — Common-Mode	R_{INCM}		—	200	—	—	200	—	GΩ
Input Voltage Range	IVR		±13	±14	—	±13	±14	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	110	126	—	110	126	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	4	10	—	4	10	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	300	500	—	200	500	—	V/mV
		$R_L \geq 500\Omega$, $V_O = \pm 0.5V$, $V_S = \pm 3V$ (Note 4)	150	400	—	150	400	—	
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	±12.5	±13.0	—	±12.5	±13.0	—	V
		$R_L \geq 2k\Omega$	±12.0	±12.8	—	±12.0	±12.8	—	
		$R_L \geq 1k\Omega$	±10.5	±12.0	—	±10.5	±12.0	—	
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 3)	0.1	0.3	—	0.1	0.3	—	V/μs
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$ (Note 3)	0.4	0.6	—	0.4	0.6	—	MHz
Open-Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	60	—	—	60	—	Ω
Power Consumption	P_d	$V_S = \pm 15V$, No Load	—	75	120	—	75	120	mW
		$V_S = \pm 3V$, No Load	—	4	6	—	4	6	
Offset Adjustment Range		$R_P = 20k\Omega$	—	±4	—	—	±4	—	mV

NOTES:

1. OP-07A grade V_{OS} is measured one minute after application of power. For all other grades V_{OS} is measured approximately 0.5 seconds after application of power.
2. Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV — refer to typical performance curves. Parameter is sample tested.
3. Sample tested.
4. Guaranteed by design.

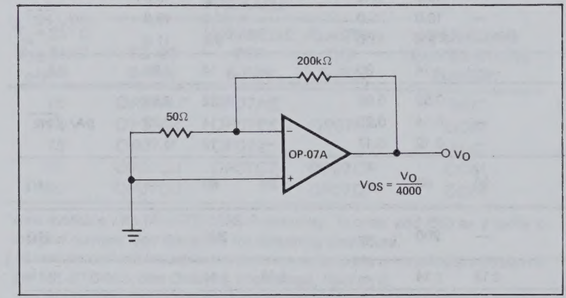
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$, unless otherwise noted.

			OP-07A			OP-07			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	25	60	—	60	200	μV
Average Input Offset Voltage Drift Without External Trim	TCV_{OS}	(Note 2)	—	0.2	0.6	—	0.3	1.3	μV/°C
With External Trim	TCV_{OSn}	$R_P = 20k\Omega$ (Note 1)	—	0.2	0.6	—	0.3	1.3	
Input Offset Current	I_{OS}		—	0.8	4	—	1.2	5.6	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 2)	—	5	25	—	8	50	pA/°C
Input Bias Current	I_B		—	±1	±4	—	±2	±6	nA
Average Input Bias Current Drift	TCI_B	(Note 2)	—	8	25	—	13	50	pA/°C
Input Voltage Range	IVR		±13	±13.5	—	±13	±13.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	106	123	—	106	123	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	5	20	—	5	20	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	200	400	—	150	400	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	±12.6	—	±12	±12.6	—	V

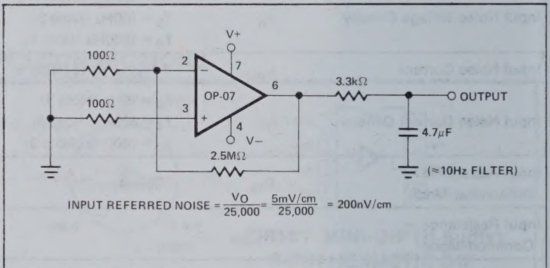
NOTES:

1. OP-07A grade V_{OS} is measured one minute after application of power. For all other grades V_{OS} is measured approximately 0.5 seconds after application of power.
2. Sample tested.
3. Guaranteed by design.

TYPICAL OFFSET VOLTAGE TEST CIRCUIT



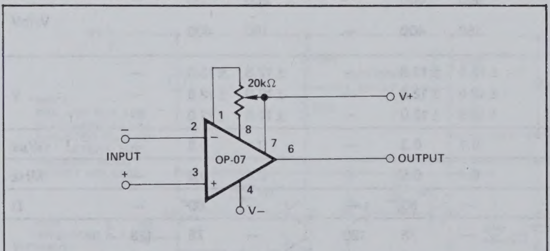
TYPICAL LOW-FREQUENCY NOISE TEST CIRCUIT



$$\text{INPUT REFERRED NOISE} = \frac{V_O}{25{,}000} = \frac{5mV/cm}{25{,}000} = 200nV/cm$$

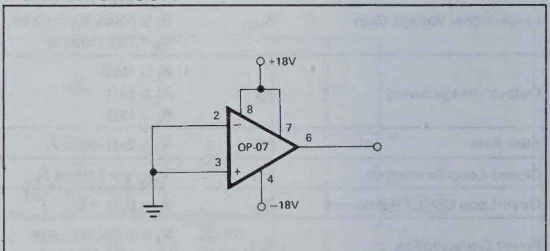
PINOUTS SHOWN FOR J, P, AND Z PACKAGES

OPTIONAL OFFSET NULLING CIRCUIT



PINOUTS SHOWN FOR J, P, AND Z PACKAGES

BURN-IN CIRCUIT



PINOUTS SHOWN FOR J, P, AND Z PACKAGES

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $T_A = 25°C$, unless otherwise noted.

			OP-07E			OP-07C			OP-07D			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}	(Note 1)	—	30	75	—	60	150	—	60	150	μV
Long-Term V_{OS} Stability	V_{OS}/Time	(Note 2)	—	0.3	1.5	—	0.4	2.0	—	0.5	3.0	μV/Mo
Input Offset Current	I_{OS}		—	0.5	3.8	—	0.8	6.0	—	0.8	6.0	nA
Input Bias Current	I_B		—	±1.2	±4.0	—	±1.8	±7.0	—	±2.0	±12	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 3)	—	0.35	0.6	—	0.38	0.65	—	0.38	0.65	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10Hz$	—	10.3	18.0	—	10.5	20.0	—	10.5	20.0	$nV/\sqrt{Hz}$
		$f_O = 100Hz$ (Note 3)	—	10.0	13.0	—	10.2	13.5	—	10.3	13.5	
		$f_O = 1000Hz$	—	9.6	11.0	—	9.8	11.5	—	9.8	11.5	
Input Noise Current	i_{np-p}	0.1Hz to 10Hz (Note 3)	—	14	30	—	15	35	—	15	35	pA_{p-p}
Input Noise Current Density	i_n	$f_O = 10Hz$	—	0.32	0.80	—	0.35	0.90	—	0.35	0.90	$pA/\sqrt{Hz}$
		$f_O = 100Hz$ (Note 3)	—	0.14	0.23	—	0.15	0.27	—	0.15	0.27	
		$f_O = 1000Hz$	—	0.12	0.17	—	0.13	0.18	—	0.13	0.18	
Input Resistance — Differential-Mode	R_{IN}	(Note 4)	15	50	—	8	33	—	7	31	—	MΩ
Input Resistance — Common-Mode	R_{INCM}		—	160	—	—	120	—	—	120	—	GΩ
Input Voltage Range	IVR		±13	±14	—	±13	±14	—	±13	±14	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm13V$	106	123	—	100	120	—	94	110	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm3V$ to $\pm18V$	—	5	20	—	7	32	—	7	32	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm10V$	200	500	—	120	400	—	120	400	—	V/mV
		$R_L \geq 500\Omega$ $V_O = \pm0.5V$ $V_S = \pm3V$ (Note 4)	150	400	—	100	400	—	—	400	—	
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	±12.5	±13.0	—	±12.0	±13.0	—	±12.0	±13.0	—	V
		$R_L \geq 2k\Omega$	±12.0	±12.8	—	±11.5	±12.8	—	±11.5	±12.8	—	
		$R_L \geq 1k\Omega$	±10.5	±12.0	—	—	±12.0	—	—	±12.0	—	
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 3)	0.1	0.3	—	0.1	0.3	—	0.1	0.3	—	V/μs
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$ (Note 3)	0.4	0.6	—	0.4	0.6	—	0.4	0.6	—	MHz
Open-Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	60	—	—	60	—	—	60	—	Ω
Power Consumption	P_d	$V_S = \pm15V$, No Load	—	75	120	—	80	150	—	80	150	mW
		$V_S = \pm3V$, No Load	—	4	6	—	4	8	—	4	8	
Offset Adjustment Range		$R_P = 20k\Omega$	—	±4	—	—	±4	—	—	±4	—	mV

NOTES:

1. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV — refer to typical performance curves. Parameter is sample tested.
3. Sample tested.
4. Guaranteed by design.

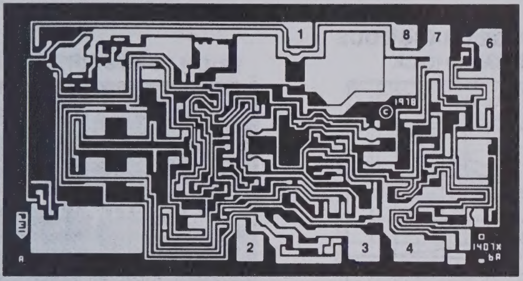
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $0°C \leq T_A \leq +70°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-07E MIN	OP-07E TYP	OP-07E MAX	OP-07C MIN	OP-07C TYP	OP-07C MAX	OP-07D MIN	OP-07D TYP	OP-07D MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	45	130	—	85	250	—	85	250	μV
Average Input Offset Voltage Drift Without External Trim	TCV_{OS}	(Note 3)	—	0.3	1.3	—	0.5	1.8	—	0.7	2.5	μV/°C
With External Trim	TCV_{OSn}	$R_P = 20k\Omega$ (Note 3)	—	0.3	1.3	—	0.4	1.6	—	0.7	2.5	μV/°C
Input Offset Current	I_{OS}		—	0.9	5.3	—	1.6	8.0	—	1.6	8.0	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 2)	—	8	35	—	12	50	—	12	50	pA/°C
Input Bias Current	I_B		—	±1.5	±5.5	—	±2.2	±9.0	—	±3.0	±14	nA
Average Input Bias Current Drift	TCI_B	(Note 2)	—	13	35	—	18	50	—	18	50	pA/°C
Input Voltage Range	IVR		±13.0	±13.5	—	±13.0	±13.5	—	±13.0	±13.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	103	123	—	97	120	—	94	106	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	7	32	—	10	51	—	10	51	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	180	450	—	100	400	—	100	400	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	±12.6	—	±11	±12.6	—	±11	±12.6	—	V

NOTES:

1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. Sample tested.
3. Guaranteed by design.

DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)



DIE SIZE 0.100 × 0.053 inch, 5300 sq. mils (2.54 × 1.35 mm, 3.42 sq. mm)

1. **BALANCE**
2. **INVERTING INPUT**
3. **NONINVERTING INPUT**
4. **V−**
6. **OUTPUT**
7. **V+**
8. **BALANCE**

For additional DICE information refer to Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$ for OP-07N, OP-07G and OP-07GR devices; $T_A = 125°C$ for OP-07NT and OP-07GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-07NT LIMIT	OP-07N LIMIT	OP-07GT LIMIT	OP-07G LIMIT	OP-07GR LIMIT	UNITS
Input Offset Voltage	V_{OS}		140	40	210	80	150	μV MAX
Input Offset Current	I_{OS}		4.0	2.0	5.6	2.8	6.0	nA MAX
Input Bias Current	I_B		±4	±2	±6	±3	±7	nA MAX
Input Resistance Differential-Mode	R_{IN}	(Note 2)	—	20	—	20	8	MΩ MIN
Input Voltage Range	IVR		±13	±13	±13	±13	±13	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	100	110	100	110	100	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	20	10	20	10	30	μV/V MAX
Output Voltage Swing	V_O	$R_L = 10k\Omega$ $R_L = 2k\Omega$ $R_L = 1k\Omega$	— ±12.0 —	±12.5 ±12.0 ±10.5	— ±12.0 —	±12.0 ±11.5 ±10.5	±12.0 ±11.5 —	V MIN
Large-Signal Voltage Gain	A_{VO}	$R_L = 2k\Omega$ $V_O = \pm 10V$	200	200	150	120	120	V/mV MIN
Differential Input Voltage			±30	±30	±30	±30	±30	V MAX
Power Consumption	P_d	$V_{OUT} = 0V$	—	120	—	120	150	mW MAX

NOTES:

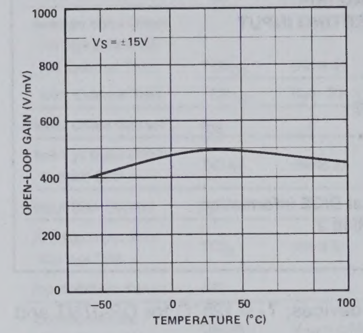
1. For 25° C characteristics of OP-07NT and OP-07GT, see OP-07N and OP-07G characteristics, respectively.
2. Guaranteed by design.

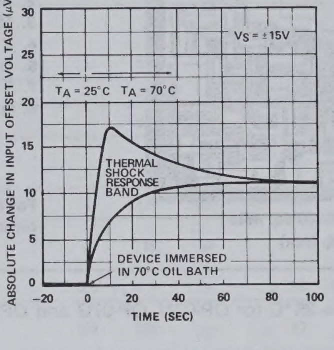
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

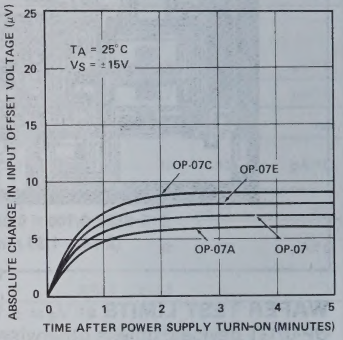
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25° C$, unless otherwise noted.

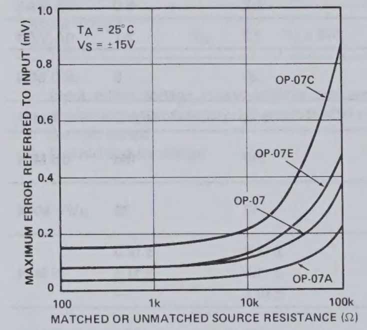
PARAMETER	SYMBOL	CONDITIONS	OP-07NT TYPICAL	OP-07N TYPICAL	OP-07GT TYPICAL	OP-07G TYPICAL	OP-07GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}	$R_S = 50\Omega$	0.2	0.2	0.3	0.3	0.7	μV/° C
Nulled Input Offset Voltage Drift	TCV_{OSn}	$R_S = 50\Omega$, $R_P = 20k\Omega$	0.2	0.2	0.3	0.3	0.7	μV/° C
Average Input Offset Current Drift	TCI_{OS}		5	5	8	8	12	pA/° C
Slew Rate	SR	$R_L \geq 2k\Omega$	0.3	0.3	0.3	0.3	0.3	V/μs
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$	0.6	0.6	0.6	0.6	0.6	MHz

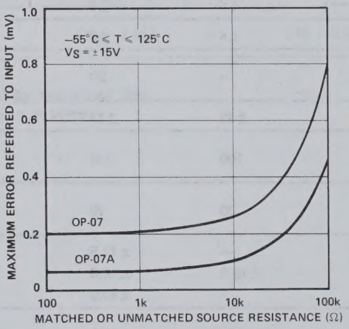
TYPICAL PERFORMANCE CHARACTERISTICS

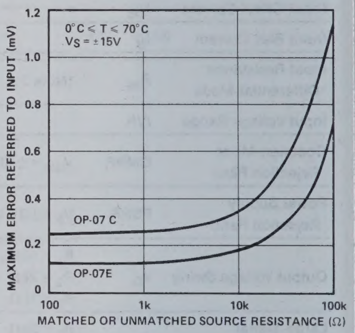

OPEN-LOOP GAIN vs TEMPERATURE

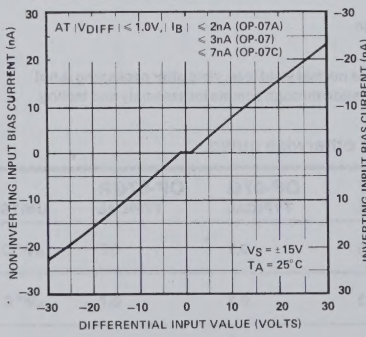

OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK

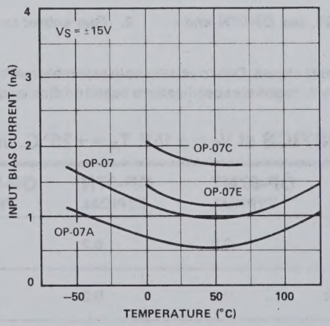

WARM-UP DRIFT

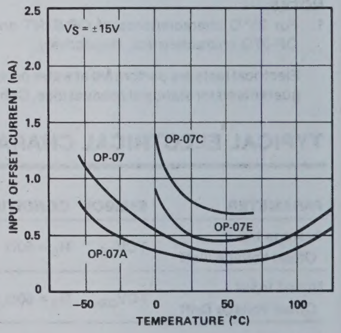

MAXIMUM ERROR vs SOURCE RESISTANCE


MAXIMUM ERROR vs SOURCE RESISTANCE


MAXIMUM ERROR vs SOURCE RESISTANCE

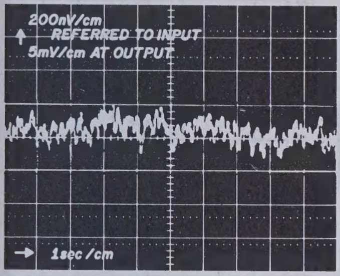

INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE


INPUT BIAS CURRENT vs TEMPERATURE

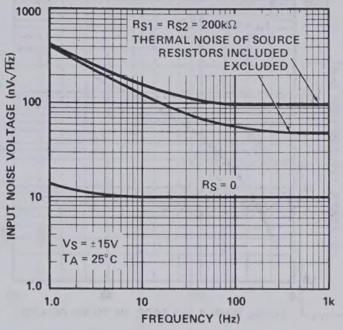

INPUT OFFSET CURRENT vs TEMPERATURE

TYPICAL PERFORMANCE CHARACTERISTICS

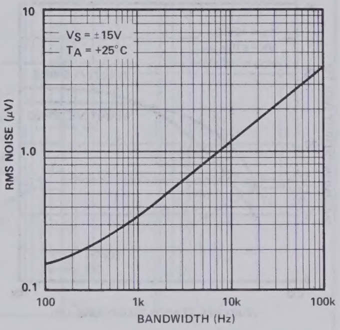
OP-07 LOW FREQUENCY NOISE



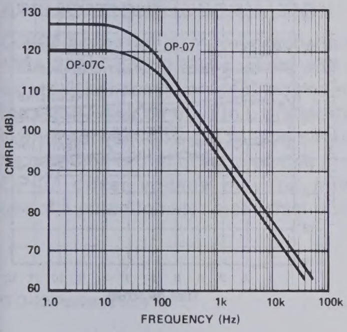
TOTAL INPUT NOISE VOLTAGE vs FREQUENCY



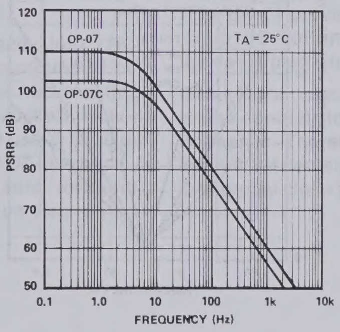
INPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



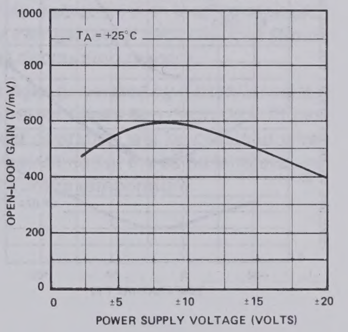
CMRR vs FREQUENCY



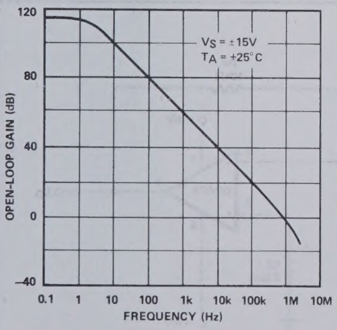
PSRR vs FREQUENCY



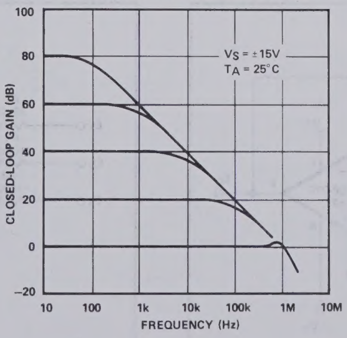
OPEN-LOOP GAIN vs POWER SUPPLY VOLTAGE



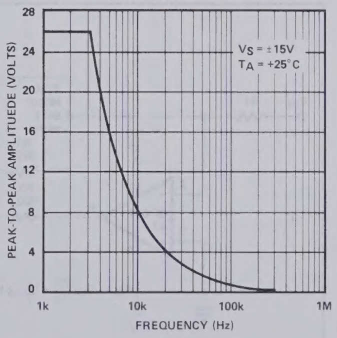
OPEN-LOOP FREQUENCY RESPONSE



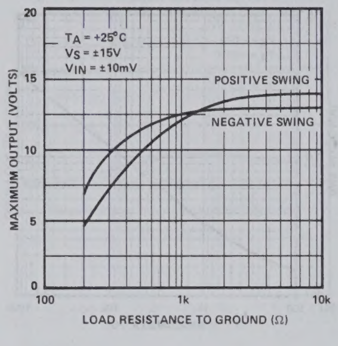
CLOSED-LOOP RESPONSE FOR VARIOUS GAIN CONFIGURATIONS

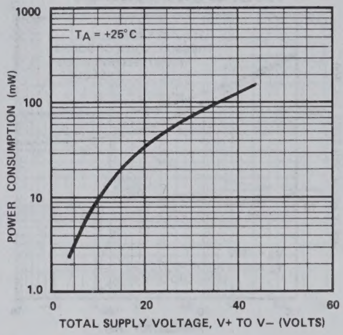


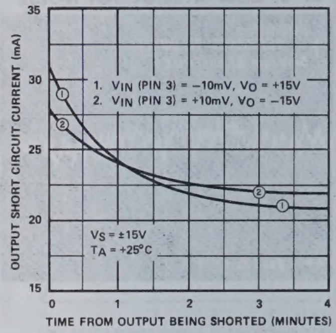
MAXIMUM OUTPUT SWING vs FREQUENCY

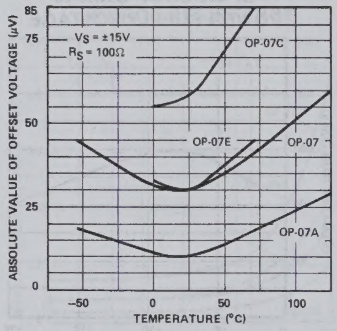


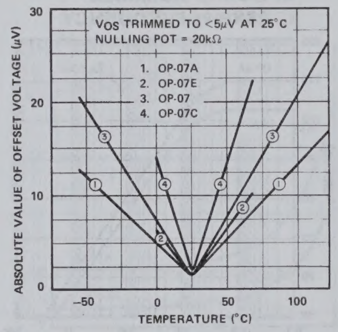
TYPICAL PERFORMANCE CHARACTERISTICS

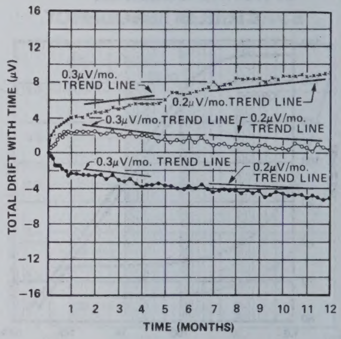

MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE


POWER CONSUMPTION vs POWER SUPPLY


OUTPUT SHORT-CIRCUIT CURRENT vs TIME

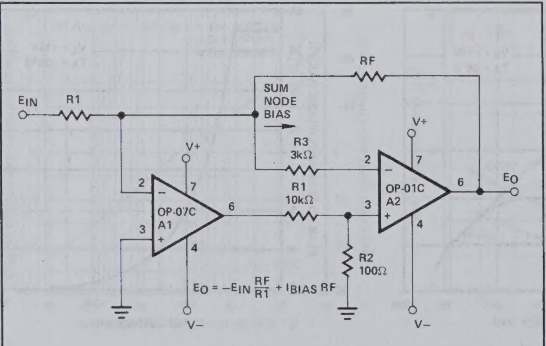

UNTRIMMED OFFSET VOLTAGE vs TEMPERATURE


TRIMMED OFFSET VOLTAGE vs TEMPERATURE


OFFSET VOLTAGE STABILITY vs TIME

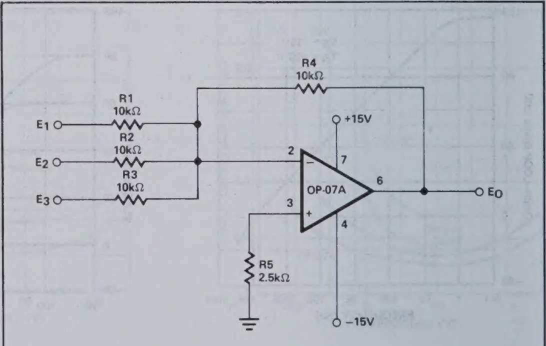
TYPICAL APPLICATIONS

HIGH SPEED, LOW V_{OS}, COMPOSITE AMPLIFIER


EIN
R1
RF
SUM NODE BIAS
R3 3kΩ
R1 10kΩ
R2 100Ω
V+
V−
OP-07C A1
OP-01C A2
2
3
4
6
7
EO
EO = −EIN RF/R1 + IBIAS RF

PINOUTS SHOWN FOR J, P, AND Z PACKAGES

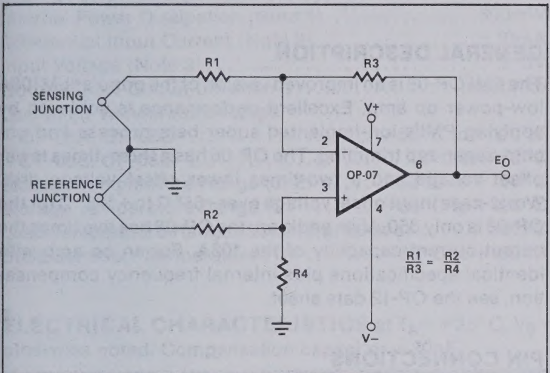
ADJUSTMENT-FREE PRECISION SUMMING AMPLIFIER


E1
E2
E3
R1 10kΩ
R2 10kΩ
R3 10kΩ
R4 10kΩ
R5 2.5kΩ
+15V
−15V
OP-07A
2
3
4
6
7
EO

PINOUTS SHOWN FOR J, P, AND Z PACKAGES

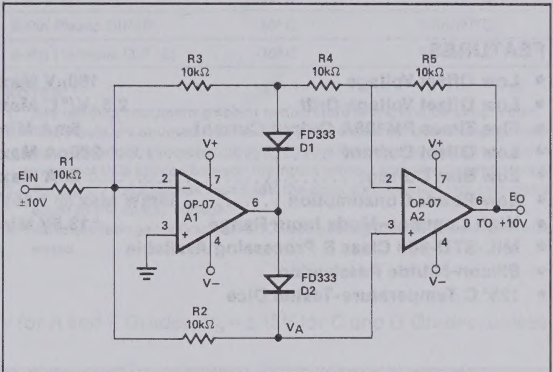
TYPICAL APPLICATIONS

HIGH-STABILITY THERMOCOUPLE AMPLIFIER


R1
R3
SENSING JUNCTION
V+
2
7
6
EO
OP-07
REFERENCE JUNCTION
3
4
R2
R1/R3 = R2/R4
R4
V–

PINOUTS SHOWN FOR J, P, AND Z PACKAGES

PRECISION ABSOLUTE-VALUE CIRCUIT


R3 10kΩ
R4 10kΩ
R5 10kΩ
FD333 D1
V+
R1 10kΩ
EIN ±10V
2
7
OP-07 A1
6
3
4
V–
FD333 D2
R2 10kΩ
VA
2
7
OP-07 A2
6
EO 0 TO +10V
3
4
V+
V–

PINOUTS SHOWN FOR J, P, AND Z PACKAGES

APPLICATIONS INFORMATION

OP-07 series units may be substituted directly into 725, 108A/308A* and OP-05 sockets with or without removal of external compensation or nulling components. Additionally, the OP-07 may be used in unnulled 741-type sockets. However, if conventional 741 nulling circuitry is in use, it should be modified or removed to enable proper OP-07 operation. OP-07 offset voltage may be nulled to zero through use of a potentiometer (see offset nulling circuit diagram).

The OP-07 provides stable operation with load capacitance of up to 500pF and ± 10V swings; larger capacitances should be decoupled with a 50Ω decoupling resistor.

Stray thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can degrade drift performance. Therefore, best operation will be obtained when both input contacts are maintained at the same temperature, preferably close to the package temperature.

*TO-99 Package only

OP-08 PRECISION LOW-INPUT-CURRENT OPERATIONAL AMPLIFIER

FEATURES

- **Low Offset Voltage .... 150μV Max**
- **Low Offset Voltage Drift .... 2.5μV/°C Max**
- **Five Times PM108A Output Current .... 5mA Min**
- **Low Offset Current .... 200pA Max**
- **Low Bias Current .... 2nA Max**
- **Low Power Consumption .... 18mW Max @ ±15V**
- **High Common-Mode Input Range .... ±13.5V Min**
- **MIL-STD-883 Class B Processing Available**
- **Silicon-Nitride Passivation**
- **125°C Temperature-Tested Dice**

ORDERING INFORMATION†

$T_A = 25°C$ V_{OS} MAX (mV)	PACKAGE HERMETIC TO-99 8-PIN	 HERMETIC DIP 8-PIN	 PLASTIC DIP 8-PIN	OPERATING TEMPERATURE RANGE
0.15	OP08AJ*	OP08AZ*		MIL
0.15	OP08EJ	OP08EZ	OP08EP	COM
1.0	OP08CJ*	OP08CZ*		MIL
1.0	OP08GJ	OP08GZ	OP08GP	COM

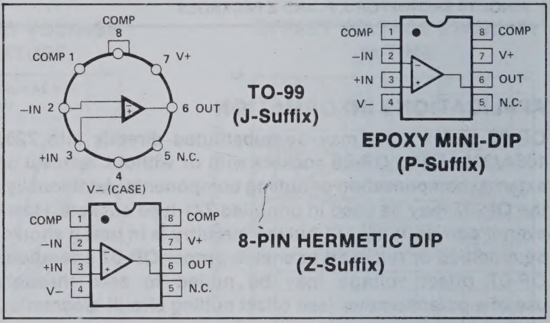
*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

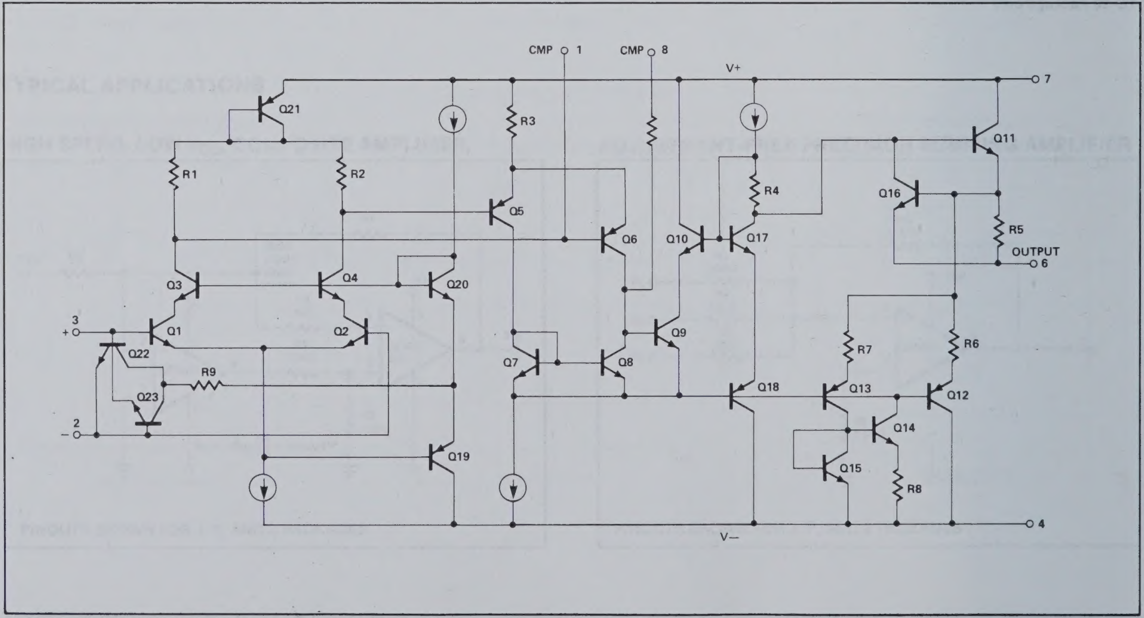
GENERAL DESCRIPTION

The PMI OP-08 is an improved version of the popular LM108A low-power op amp. Excellent performance is achieved by applying PMI's ion-implanted super-beta process and on-chip-zener-zap trimming. The OP-08 has a three-times lower offset voltage and a two-times lower offset voltage drift. Worst-case input offset voltage over −55°C to +125°C for the OP-08 is only 350μV. In addition, the OP-08 has five times the output current capability of the 108A. For an op amp with identical specifications plus internal frequency compensation, see the OP-12 data sheet.

PIN CONNECTIONS


COMP 8
COMP 1
7 V+
−IN 2
6 OUT
+IN 3
5 N.C.
4
V− (CASE)
TO-99
(J-Suffix)
COMP 1
−IN 2
+IN 3
V− 4
8 COMP
7 V+
6 OUT
5 N.C.
EPOXY MINI-DIP
(P-Suffix)
COMP 1
−IN 2
+IN 3
V− 4
8 COMP
7 V+
6 OUT
5 N.C.
8-PIN HERMETIC DIP
(Z-Suffix)

SIMPLIFIED SCHEMATIC


CMP 1
CMP 8
V+
7
Q21
R3
R1
R2
Q5
R4
Q11
Q16
R5
OUTPUT
6
Q6
Q10
Q17
Q3
Q4
Q20
3
+
Q1
Q2
Q9
Q22
R9
Q7
Q8
Q18
Q13
Q12
R7
R6
Q23
2
−
Q14
Q19
Q15
R8
4
V−

ABSOLUTE MAXIMUM RATINGS (Note 4)

Supply Voltage	
OP-08A, OP-08E (All DICE except GR)	±20V
OP-08C, OP-08G (GR DICE Only)	±18V
Internal Power Dissipation (Note 1)	500mW
Differential Input Current (Note 2)	±10mA
Input Voltage (Note 3)	±15V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	
OP-08A, OP-08C	−55° C to +125° C
OP-08E, OP-08G	0° C to +70° C
Storage Temperature Range (J, Z)	−65° C to +150° C
Storage Temperature Range (P)	−65° C to +125° C
Lead Temperature Range (Soldering, 60 sec)	300° C
DICE Junction Temperature (T_j)	−65° C to +150° C

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80° C	7.1mW/° C
8-Pin Plastic DIP (P)	36° C	5.6mW/° C
8-Pin Hermetic DIP (Z)	75° C	6.7mW/° C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.
2. The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs without some limiting resistance.
3. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
4. Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $T_A = +25° C$, $V_S = ±20V$ for A and E Grades, $V_S = ±15V$ for C and G Grades, unless otherwise noted. Compensation capacitor = 30pF.

			OP-08A/E			OP-08C/G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.07	0.15	—	0.25	1.0	mV
Input Offset Current	I_{OS}		—	0.05	0.20	—	0.08	0.50	nA
Input Bias Current	I_B		—	0.80	2.0	—	1.0	5.0	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	—	0.9	—	—	0.9	—	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10Hz$	—	22	—	—	22	—	$nV/\sqrt{Hz}$
		$f_O = 100Hz$	—	21	—	—	21	—	
		$f_O = 1000Hz$	—	20	—	—	20	—	
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	—	3	—	—	3	—	pA_{p-p}
Input Noise Current Density	i_n	$f_O = 10Hz$	—	0.15	—	—	0.15	—	$pA/\sqrt{Hz}$
		$f_O = 100Hz$	—	0.14	—	—	0.14	—	
		$f_O = 1000Hz$	—	0.13	—	—	0.13	—	
Input Resistance — Differential Mode	R_{IN}	(Note 1)	26	70	—	10	50	—	MΩ
Input Voltage Range	IVR	$V_S = ±15V$	±13.5	±14.0	—	±13.5	±14.0	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = ±13.5V$	104	120	—	84	116	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = ±5V$ to $±15V$	—	1	7	—	2	63	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 10k\Omega$, $V_O = ±10V$	80	300	—	40	250	—	V/mV
		$R_L \geq 2k\Omega$, $V_O = ±10V$, $V_S = ±15V$	50	150	—	—	100	—	
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$, $V_S = ±15V$	±13	±14	—	±13	±14	—	V
		$R_L \geq 2k\Omega$, $V_S = ±15V$	±10	±12	—	±10	±12	—	
Slew Rate	SR	$R_L \geq 2k\Omega$	—	0.12	—	—	0.12	—	V/μs
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$	—	0.8	—	—	0.8	—	MHz
Open-Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	200	—	—	200	—	Ω
Power Consumption	P_d	$V_S = ±15V$	—	9	18	—	12	24	mW
		$V_S = ±5V$	—	3	6	—	4	8	

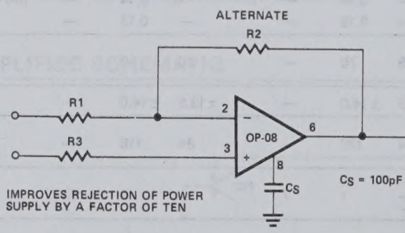
NOTE:

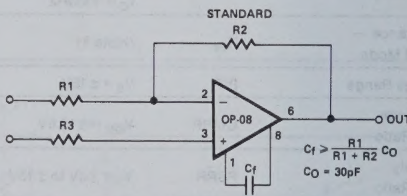
1. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ for C Grade and $V_S = \pm 20V$ for A Grade, $-55°C \le T_A \le +125°C$, unless otherwise noted.

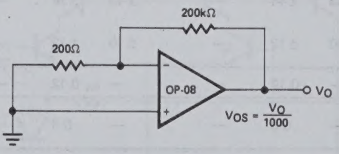
			OP-08A			OP-08C			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}		—	0.12	0.35	—	0.40	2.0	mV
Average Input Offset Voltage Drift	TCV_{OS}		—	0.50	2.5	—	1.5	10	μV/°C
Input Offset Current	I_{OS}		—	0.12	0.40	—	0.18	1.0	nA
Average Input Offset Current Drift	TCI_{OS}		—	0.50	2.5	—	1.0	5.0	pA/°C
Input Bias Current	I_B		—	1.2	3.0	—	1.8	10	nA
Input Voltage Range	IVR	$V_S = \pm 15V$	±13.5	±14.0	—	±13.5	±14.0	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.5V$	100	110	—	80	106	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 15V$	—	4	10	—	5	100	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 5k\Omega$, $V_O = \pm 10V$ $V_S = \pm 15V$	40	120	—	15	80	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 10k\Omega$, $V_S = \pm 15V$	±13	±14	—	±13	±14	—	V
		$R_L \ge 5k\Omega$, $V_S = \pm 15V$	±10	±12	—	±10	±12	—	
Power Consumption	P_d	$V_S = \pm 15V$	—	9	18	—	15	24	mW

COMPENSATION CIRCUITS

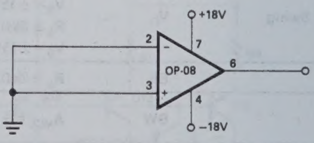

ALTERNATE
R2
R1
R3
2
3
6
8
OP-08
OUTPUT
C_S
C_S = 100pF
IMPROVES REJECTION OF POWER SUPPLY BY A FACTOR OF TEN


STANDARD
R2
R1
R3
2
3
6
8
1
C_f
OP-08
OUTPUT
$C_f > \frac{R1}{R1 + R2} C_O$
C_O = 30pF

OFFSET VOLTAGE TEST CIRCUIT


200kΩ
200Ω
OP-08
V_O
$V_{OS} = \frac{V_O}{1000}$

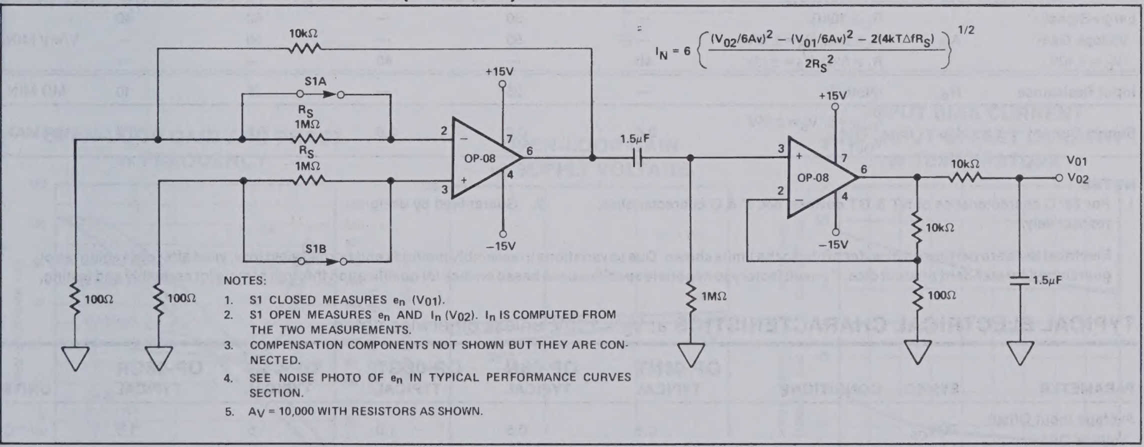
BURN-IN CIRCUIT


+18V
2
7
OP-08
6
3
4
−18V

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ for G Grade and $V_S = \pm 20V$ for E Grade, $0°C \le T_A \le +70°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-08E MIN	OP-08E TYP	OP-08E MAX	OP-08G MIN	OP-08G TYP	OP-08G MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.10	0.26	—	0.32	1.4	mV
Average Input Offset Voltage Drift	TCV_{OS}		—	0.50	2.5	—	1.5	10	μV/°C
Input Offset Current	I_{OS}		—	0.08	0.30	—	0.12	6.5	nA
Average Input Offset Current Drift	TCI_{OS}		—	0.50	2.5	—	2.0	50	pA/°C
Input Bias Current	I_B		—	1.0	2.6	—	1.4	6.5	nA
Input Voltage Range	IVR	$V_S = \pm 15V$	±13.5	±14.0	—	±13.5	±14.0	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.5V$	100	116	—	80	112	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 15V$	—	2	10	—	3	100	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$, $V_O = \pm 10V$	25	100	—	—	80	—	V/mV
		$R_L \ge 10k\Omega$, $V_O = \pm 10V$ $V_S = \pm 15V$	60	200	—	25	150	—	
Output Voltage Swing	V_O	$R_L \ge 10k\Omega$, $V_S = \pm 15V$	±13	±14	—	±13	±14	—	V
		$R_L \ge 2k\Omega$, $V_S = \pm 15V$	±10	±12	—	±10	±12	—	
Power Consumption	P_d	$V_S = \pm 15V$	—	9	18	—	15	24	mW

LOW-FREQUENCY NOISE TEST CIRCUIT (0.1 to 10Hz)

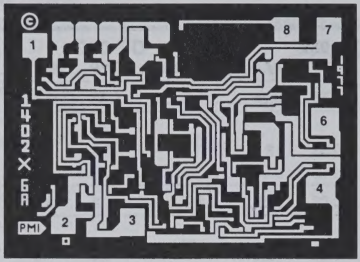


$$I_N = 6 \left\{ \frac{(V_{02}/6Av)^2 - (V_{01}/6Av)^2 - 2(4kT\Delta fR_S)}{2R_S{}^2} \right\}^{1/2}$$

NOTES:

1. S1 CLOSED MEASURES e_n (V_{01}).
2. S1 OPEN MEASURES e_n AND I_n (V_{02}). I_n IS COMPUTED FROM THE TWO MEASUREMENTS.
3. COMPENSATION COMPONENTS NOT SHOWN BUT THEY ARE CONNECTED.
4. SEE NOISE PHOTO OF e_n IN TYPICAL PERFORMANCE CURVES SECTION.
5. A_V = 10,000 WITH RESISTORS AS SHOWN.

DICE CHARACTERISTICS (125°C TESTED DICE AVAILABLE)



DIE SIZE 0.058 × 0.042 inch, 2436 sq. mils (1.47 × 1.07mm, 1.57 sq. mm)

1. COMPENSATION
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V−
6. OUTPUT
7. V+
8. COMPENSATION

For additional DICE information refer to Section 2.

WAFER TEST LIMITS at $V_S = \pm 20V$, $T_A = 25°C$ for OP-08N and OP-08G devices; $V_S = \pm 20V$, $T_A = 125°C$ for OP-08NT and OP-08GT devices; $V_S = \pm 15V$, $T_A = 25°C$ for OP-08GR devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-08NT LIMIT	OP-08N LIMIT	OP-08GT LIMIT	OP-08G LIMIT	OP-08GR LIMIT	UNITS
Input Offset Voltage	V_{OS}		0.35	0.15	0.6	0.3	1.0	mV MAX
Input Offset Current	I_{OS}		0.2	0.2	0.4	0.2	0.5	nA MAX
Input Bias Current	I_B		2	2	4	2	5	nA MAX
Input Voltage Range	IVR	$V_S = \pm 15V$	±13.5	±13.5	±13.5	±13.5	±13.5	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$ $V_S = \pm 15V$	100	104	100	104	84	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 15V$	10	7	10	7	63	µV/V MAX
Output Voltage Swing	V_O	$V_S = \pm 15V$						V MIN
		$R_L \geq 10k\Omega$	±13	±13	±13	±13	±13	
		$R_L \geq 2k\Omega$	—	±10	—	±10	±10	
		$R_L \geq 5k\Omega$	±10	—	±10	—	—	
Large-Signal Voltage Gain ($V_O = \pm 10V$)	A_{VO}	$R_L \geq 10k\Omega$	—	80	—	80	40	V/mV MIN
		$R_L \geq 2k\Omega$, $V_S = \pm 15V$	—	50	—	50	—	
		$R_L \geq 5k\Omega$, $V_S = \pm 15V$	40	—	40	—	—	
Input Resistance	R_{IN}	(Note 2)	—	25	—	25	10	MΩ MIN
Supply Current	I_{SY}	$I_{OUT} = 0$, $V_S = \pm 15V$ $V_{OUT} = 0$	0.6	0.6	0.6	0.6	0.8	mA MAX

NOTES:

1. For 25°C characteristics of NT & GT devices, see N & G characteristics, respectively.
2. Guaranteed by design.

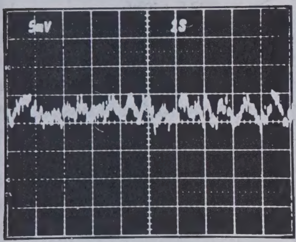
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-08NT TYPICAL	OP-08N TYPICAL	OP-08GT TYPICAL	OP-08G TYPICAL	OP-08GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}		0.5	0.5	1.0	1.0	1.5	µV/°C
Average Input Offset Current Drift	TCI_{OS}		0.5	0.5	0.5	0.5	1.0	pA/°C

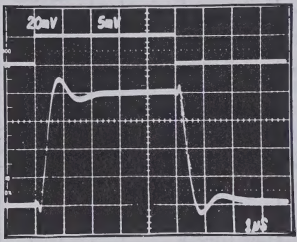
TYPICAL PERFORMANCE CHARACTERISTICS

LOW FREQUENCY NOISE

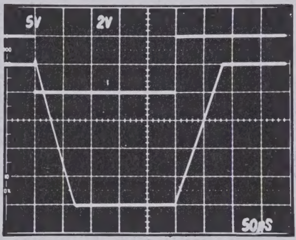


R_S = 0V, BW = 0.1Hz TO 10Hz
5mV/DIV AT READOUT
0.5μV/DIV REFERED TO INPUT

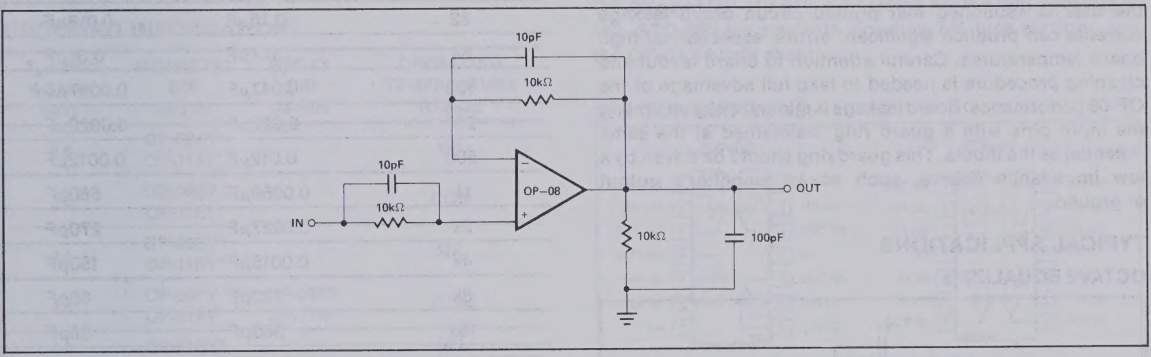
SMALL-SIGNAL TRANSIENT RESPONSE



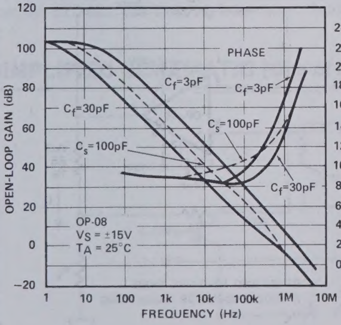
LARGE-SIGNAL TRANSIENT RESPONSE



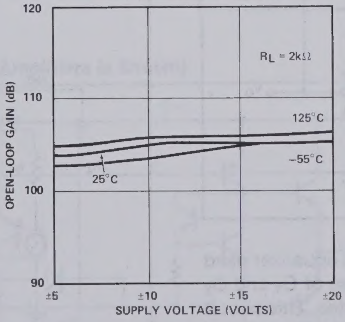
TRANSIENT RESPONSE TEST CIRCUIT



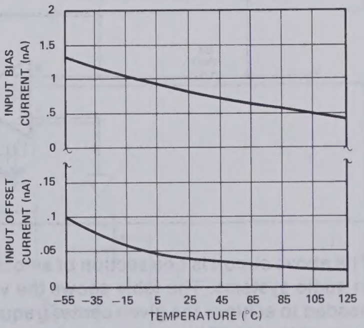
OPEN-LOOP GAIN AND PHASE vs FREQUENCY



OPEN-LOOP GAIN vs SUPPLY VOLTAGE

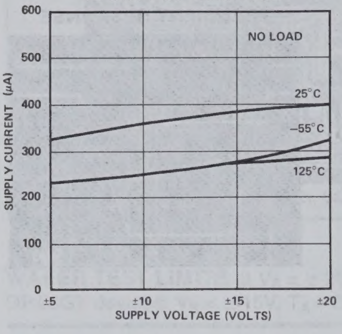


INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs TEMPERATURE

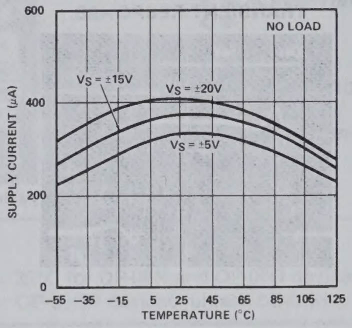


TYPICAL PERFORMANCE CHARACTERISTICS

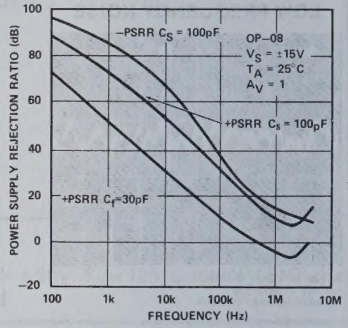
SUPPLY CURRENT vs SUPPLY VOLTAGE



SUPPLY CURRENT vs TEMPERATURE



POWER SUPPLY REJECTION RATIO (PSRR) vs FREQUENCY

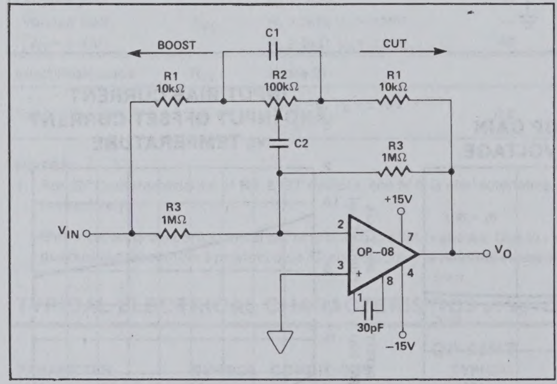


APPLICATIONS INFORMATION

The OP-08 series has very low input offset and bias currents; the user is cautioned that printed circuit board leakage currents can produce significant errors, especially at high board temperatures. Careful attention to board layout and cleaning procedure is needed to take full advantage of the OP-08 performance. Board leakage is minimized by encircling the input pins with a guard ring maintained at the same potential as the inputs. This guard ring should be driven by a low impedance source, such as an amplifier's output or ground.

TYPICAL APPLICATIONS

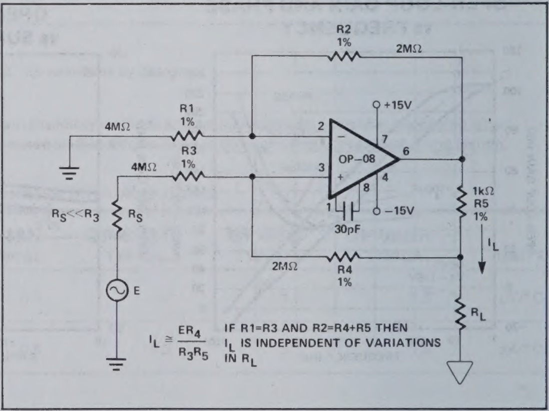
OCTAVE EQUALIZER


BOOST
C1
CUT
R1
10kΩ
R2
100kΩ
R1
10kΩ
C2
R3
1MΩ
+15V
VIN
R3
1MΩ
2
7
OP−08
VO
3
8
4
1
30pF
−15V

The above circuit is one section of an octave equalizer used in audio systems. The table shows the values of C_1 and C_2 needed to achieve the given center frequencies. This circuit is capable of 12dB boost or cut as determined by the position of R2.

f_O (Hz)	C_1	C_2
32	0.18μF	0.018μF
64	0.1μF	0.01μF
125	0.047μF	0.0047μF
250	0.022μF	0.0022μF
500	0.012μF	0.0012μF
1k	0.0056μF	560pF
2k	0.0027μF	270pF
4k	0.0015μF	150pF
8k	680pF	68pF
16k	360pF	36pF

BILATERAL CURRENT SOURCE


R2
1%
2MΩ
R1
1%
4MΩ
+15V
2
7
6
R3
1%
4MΩ
OP−08
3
8
4
1
30pF
−15V
RS<<R3
RS
1kΩ
R5
1%
IL
2MΩ
R4
1%
E
RL

$$I_L \cong \frac{ER_4}{R_3R_5}$$

IF R1=R3 AND R2=R4+R5 THEN I_L IS INDEPENDENT OF VARIATIONS IN R_L

QUAD MATCHED 741-TYPE OPERATIONAL AMPLIFIERS

OP-09/OP-11

FEATURES

- **Guaranteed V_{OS} .... 500μV Max**
- **Guaranteed Matched CMRR .... 94dB Min**
- **Guaranteed Matched V_{OS} .... 750μV Max**
- **RC/RM4136 Direct Replacement (OP-09)**
- **LM148/LM348 Direct Replacement (OP-11)**
- **Low Noise**
- **Silicon-Nitride Passivation**
- **Internal Frequency Compensation**
- **Low Crossover Distortion**
- **Continuous Short-Circuit Protection**
- **Low Input Bias Current**

GENERAL DESCRIPTION

The OP-09 and OP-11 provide four matched 741-type operational amplifiers in a single 14-pin DIP package. The OP-11 is pin compatible with the LM148, LM348, RM4156, and HA4741 amplifiers. The OP-09 is pin compatible with the RM4136 and RC4136. The amplifiers are matched for common-mode rejection ratio and offset voltage which is very important in designing instrumentation amplifiers. In addition, the amplifier is designed to have equal positive-going and negative-going slew rates. This is an important consideration for good audio system performance.

Each of the four amplifiers has the proven OP-02 advantages of low noise, low drift, and excellent long-term stability. Precision Monolithics' exclusive Silicon-Nitride "Triple Passivation" process reduces "popcorn noise", provides high reliability, and assures long-term stability of parameters.

The OP-09 and OP-11 are ideal for use in designs requiring minimum space and cost while maintaining OP-02-type performance.

OP-09's and OP-11's with processing per the requirements of MIL-STD-883 are available. For dual-741-type versions, see the OP-04/14 data sheet.

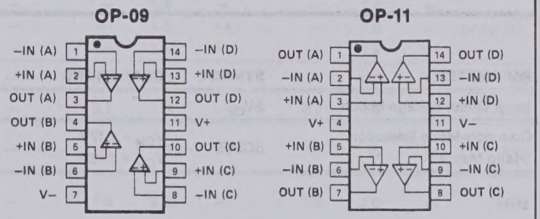
ORDERING INFORMATION†

$T_A = 25°C$ V_{OS} MAX (mV)	HERMETIC DIP 14-PIN	EPOXY DIP 14-PIN	OPERATING TEMPERATURE RANGE
0.5	OP-09AY* OP-11AY*		MIL
0.5	OP-09EY OP-11EY		COM
2.5	OP-09BY* OP-11BY*		MIL
2.5	OP-09FY OP-11FY	OP-09FP OP-11FP	COM
5.0	OP-11CY*		MIL
5.0	OP-11GY	OP-11GP	COM

*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

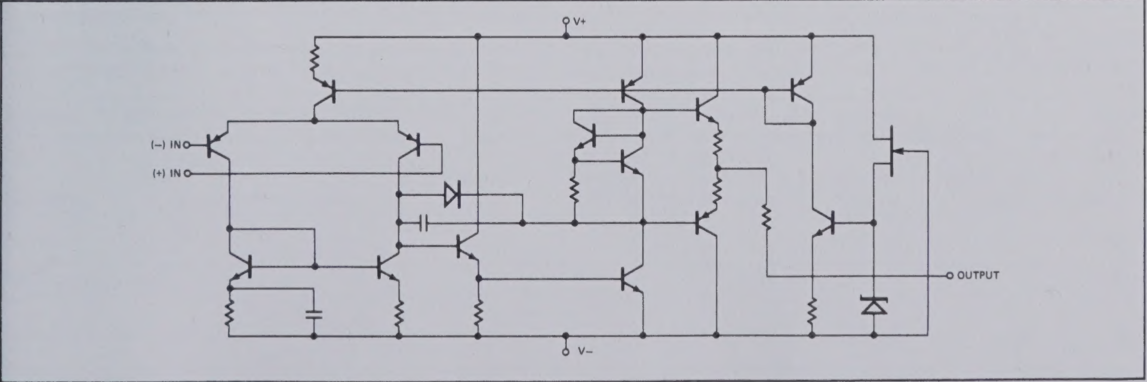
†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

PIN CONNECTIONS



14-PIN HERMETIC DIP
(Y-Suffix)
EPOXY DIP
(P-Suffix)

SIMPLIFIED SCHEMATIC (One of Four Amplifiers is Shown)



ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage .... ±22V
OP-09GR and OP-11GR (Only) .... ±18V
Internal Power Dissipation (Note 1)
Y-Package 800mW
P-Package 500mW
Differential Input Voltage .... ±30V
Input Voltage .... Supply Voltage
Output Short-Circuit Duration .... Continuous
(One Amplifier Only)
Storage Temperature Range
Y-Package .... −65°C to +150°C
P-Package .... −65°C to +125°C
Lead Temperature Range (Soldering, 60 sec) ...... 300°C
DICE Junction Temperature (T_j) ..... −65°C to +150°C

Operating Temperature Range
OP-09A, OP-09B .... −55°C to +125°C
OP-09E, OP-09F .... 0°C to +70°C
OP-11A, OP-11B, OP-11C .... −55°C to +125°C
OP-11E, OP-11F, OP-11G .... 0°C to +70°C

NOTES:

1. See table for maximum ambient temperature and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
14-Pin Hermetic DIP (Y)	70°C	10.0mW/°C
14-Pin Plastic DIP (P)	42°C	6mW/°C

2. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

MATCHING CHARACTERISTICS at $V_S = \pm15V$, $T_A = +25°C$, $R_S \leq 100\Omega$, unless otherwise noted.

			OP-09A, OP-09E OP-11A, OP-11E			OP-09B, OP-09F OP-11B, OP-11F			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage Match	ΔV_{OS}		—	0.5	0.75	—	0.8	2.0	mV
Common-Mode Rejection Ratio Match	ΔCMRR	$V_{CM} = \pm12V$	—	1	20	—	1	20	µV/V
		$V_{CM} = \pm12V$	94	120	—	94	120	—	dB

MATCHING CHARACTERISTICS at $V_S = \pm15V$, $-55°C \leq T_A \leq +125°C$ for OP-09A, OP-09B, OP-11A and OP-11B, $0°C \leq T_A \leq +70°C$ for OP-09E, OP-09F, OP-11E and OP-11F, $R_S \leq 100\Omega$, unless otherwise noted.

			OP-09A, OP-09E OP-11A, OP-11E			OP-09B, OP-09F OP-11B, OP-11F			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage Match	ΔV_{OS}		—	0.6	1.0	—	1.0	2.5	mV
Common-Mode Rejection Ratio Match	ΔCMRR	$V_{CM} = \pm12V$	—	3.2	20	—	3.2	20	µV/V
		$V_{CM} = \pm12V$	94	110	—	94	110	—	dB

ELECTRICAL CHARACTERISTICS (Each Amplifier) at $V_S = \pm 15V$ $T_A = 25°C$, unless otherwise noted.

			OP-09A/E OP-11A/E			OP-09B/F OP-11B/F			OP-11C/G			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$	—	0.3	0.5	—	0.6	2.5	—	1.2	5.0	mV
Input Offset Current	I_{OS}		—	5.5	20	—	25	50	—	75	200	nA
Input Bias Current	I_B		—	180	300	—	300	500	—	300	500	nA
Input Resistance Differential Mode	R_{IN}	(Note 3)	0.2	0.4	—	0.2	0.4	—	0.2	0.4	—	MΩ
Input Voltage Range	IVR		±12	±13	—	±12	±13	—	±12	±13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 12V$, $R_S \leq 10k\Omega$	100	120	—	100	120	—	70	100	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5$ to $\pm 15V$, $R_S \leq 10k\Omega$	—	4	32	—	4	32	—	10	100	μV/V
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±11	±13	—	±11	±13	—	±11	±13	—	V
Large-Signal Voltage Gain	A_{VO}	$R_L \leq 2k\Omega$, $V_O = \pm 10V$	100	650	—	100	650	—	50	500	—	V/mV
Power Consumption (Note 1)	P_d	$V_O = 0V$	—	105	180	—	123	180	—	210	340	mW
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	—	0.7	—	—	0.7	—	—	0.7	—	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10Hz$	—	18	—	—	18	—	—	18	—	$nV/\sqrt{Hz}$
		$f_O = 100Hz$	—	14	—	—	14	—	—	14	—	
		$f_O = 1000Hz$	—	12	—	—	12	—	—	12	—	
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	—	17	—	—	17	—	—	17	—	pA_{p-p}
Input Noise Current Density	i_n	$f_O = 10Hz$	—	1.8	—	—	1.8	—	—	1.8	—	$pA/\sqrt{Hz}$
		$f_O = 100Hz$	—	1.5	—	—	1.5	—	—	1.5	—	
		$f_O = 1000Hz$	—	1.2	—	—	1.2	—	—	1.2	—	
Channel Separation	CS		100	130	—	100	130	—	—	130	—	dB
Slew Rate (Note 3)	SR		0.7	1.0	—	0.7	1.0	—	0.7	1.0	—	V/μs
Large-Signal Bandwidth (Note 3)		$V_O = 20V_{p-p}$	11	16	—	11	16	—	11	16	—	kHz
Closed-Loop Bandwidth (Note 3)	BW	$A_{VCL} = +1.0$	1.5	2.0	—	1.5	2.0	—	1.5	2.0	—	MHz
Risetime (Note 2)	t_r	$A_V = +1$, $V_{IN} = 50mV$	—	80	120	—	80	120	—	80	120	ns
Overshoot (Note 2)	O_S		—	15	25	—	15	25	—	15	25	%

NOTES:
1. Total dissipation for all four amplifiers in package.
2. Sample tested.
3. Guaranteed by design.

ELECTRICAL CHARACTERISTICS (Each Amplifier) at $V_S = \pm 15V$, $-55°C \le T_A \le +125°C$, unless otherwise noted.

			OP-09A OP-11A			OP-09B OP-11B			OP-11C			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}	$R_S \le 10k\Omega$	—	0.4	1.0	—	1.0	3.5	—	1.5	6.0	mV
Average Input Offset Voltage Drift (Note 2)	TCV_{OS}	$R_S \le 10k\Omega$	—	2.0	10	—	4.0	15	—	4.0	—	μV/°C
Input Offset Current	I_{OS}		—	20	40	—	40	80	—	250	300	nA
Average Input Offset Current Drift (Note 2)	TCI_{OS}		—	0.1	0.3	—	0.3	0.6	—	0.3	0.6	nA/°C
Input Bias Current	I_B		—	200	375	—	400	650	—	400	800	nA
Input Voltage Range	IVR		±12	±13	—	±12	±13	—	±12	±13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 12V$, $R_S \le 10k\Omega$	100	120	—	100	120	—	70	100	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5$ to $\pm 15V$, $R_S \le 10k\Omega$	—	4	32	—	4	32	—	10	100	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$, $V_O = \pm 10V$	50	250	—	50	250	—	25	100	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±11	±13	—	±11	±13	—	±11	±13	—	V
Power Consumption (Note 1)	P_d	$V_O = 0V$	—	115	200	—	115	200	—	250	400	mW

ELECTRICAL CHARACTERISTICS (Each Amplifier) at $V_S = \pm 15V$, $0°C \le T_A \le +70°C$, unless otherwise noted.

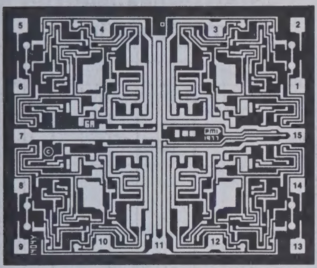
			OP-09E OP-11E			OP-09F OP-11F			OP-11G			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}	$R_S \le 10k\Omega$	—	0.4	0.8	—	0.8	3.0	—	1.5	6.0	mV
Average Input Offset Voltage Drift	TCV_{OS}	$R_S \le 10k\Omega$	—	2.0	10	—	4.0	15	—	4.0	—	μV/°C
Input Offset Current	I_{OS}		—	14	30	—	40	60	—	250	300	nA
Average Input Offset Current Drift (Note 2)	TCI_{OS}		—	0.1	0.3	—	0.3	0.6	—	0.3	0.6	nA/°C
Input Bias Current	I_B		—	200	350	—	400	550	—	400	800	nA
Input Voltage Range	IVR		±12	±13	—	±12	±13	—	±12	±13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 12V$, $R_S \le 10k\Omega$	100	120	—	100	120	—	70	100	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5$ to $\pm 15V$, $R_S \le 10k\Omega$	—	4	32	—	4	32	—	10	100	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$, $V_O = \pm 10V$	50	250	—	50	250	—	25	100	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±11	±13	—	±11	±13	—	±11	±13	—	V
Power Consumption (Note 1)	P_d	$V_O = 0V$	—	115	200	—	115	200	—	250	400	mW

NOTES:

1. Total dissipation for all four amplifiers in package.
2. Sample tested.

DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)

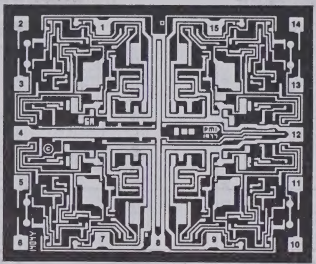
OP-09



1. INVERTING INPUT (A)
2. NONINVERTING INPUT (A)
3. OUTPUT (A)
4. OUTPUT (B)
5. NONINVERTING INPUT (B)
6. INVERTING INPUT (B)
7. V−
8. INVERTING INPUT (C)
9. NONINVERTING INPUT (C)
10. OUTPUT (C)
11. V+
12. OUTPUT (D)
13. NONINVERTING INPUT (D)
14. INVERTING INPUT (D)
15. V+

DIE SIZE 0.085 × 0.070 inch, 5950 sq. mils
(2.16 × 1.78 mm, 3.84 sq. mm)

OP-11



1. OUTPUT (A)
2. INVERTING INPUT (A)
3. NONINVERTING INPUT (A)
4. V−
5. NONINVERTING INPUT (B)
6. INVERTING INPUT (B)
7. OUTPUT (B)
8. V+
9. OUTPUT (C)
10. INVERTING INPUT (C)
11. NONINVERTING INPUT (C)
12. V+
13. NONINVERTING INPUT (D)
14. INVERTING INPUT (D)
15. OUTPUT (D)

DIE SIZE 0.085 × 0.070 inch, 5950 sq. mils
(2.16 × 1.78 mm, 3.84 sq. mm)

NOTE:
Either or both V+ pads may be used without any change in performance.

For additional DICE information refer to Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$ for OP-09/11N, OP-09/11G and OP-09/11GR devices; $T_A = 125°C$ for OP-09/11NT and OP-09/11GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-09NT OP-11NT LIMIT	OP-09N OP-11N LIMIT	OP-09GT OP-11GT LIMIT	OP-11G LIMIT	OP-09GR OP-11GR LIMIT	UNITS
nput Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$	1.0	0.5	3.5	2.5	5.0	mV MAX
nput Offset Current	I_{OS}		20	20	50	50	200	nA MAX
nput Bias Current	I_B		300	300	500	500	500	nA MAX
nput Voltage Range	IVR		±12	±12	±12	±12	±12	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 12V$ $R_S \leq 10k\Omega$	100	100	100	100	70	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 15V$ $R_S \leq 10k\Omega$	32	32	32	32	100	μV/V MAX
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$ $R_L = 2k\Omega$	±11 ±11	±12 ±11	±11 ±11	±12 ±11	±11 ±11	V MIN
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	50	100	50	100	50	V/mV MIN
Power Consumption (Four Amplifiers)	P_d	$V_{OUT} = 0$ No Load	200	180	200	180	340	mW MAX

NOTE: For 25° C characteristics of NT & GT devices, see N & G characteristics, respectively.

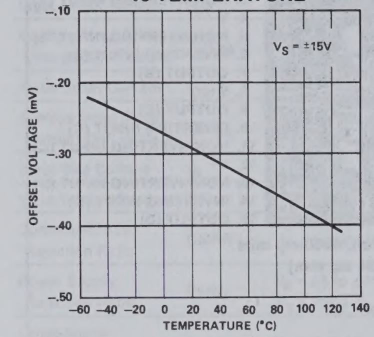
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

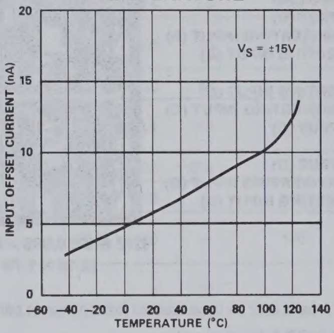
PARAMETER	SYMBOL	CONDITIONS	OP-09NT OP-11NT TYPICAL	OP-09N OP-11N TYPICAL	OP-09GT OP-11GT TYPICAL	OP-11G TYPICAL	OP-09GR OP-11GR TYPICAL	UNITS
Slew Rate	SR	$A_V = 1$ $R_L \geq 2k\Omega$	1	1	1	1	1	V/μs
Unity Gain Bandwidth	GBW		2	2	2	2	2	MHz
Channel Separation	CS	$A_V = 100$ f = 10kHz $R_S = 1k\Omega$	130	130	130	130	130	dB

TYPICAL PERFORMANCE CHARACTERISTICS

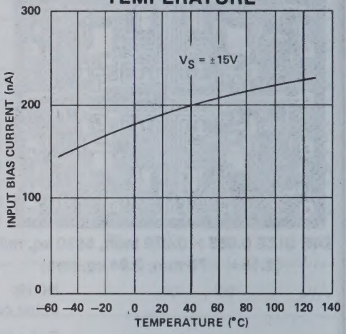
INPUT OFFSET VOLTAGE vs TEMPERATURE



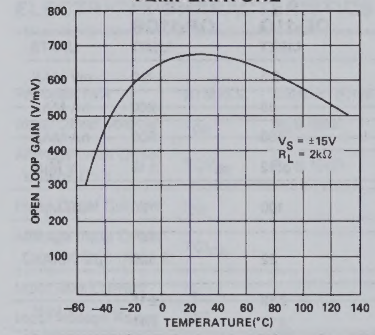
OFFSET CURRENT vs TEMPERATURE



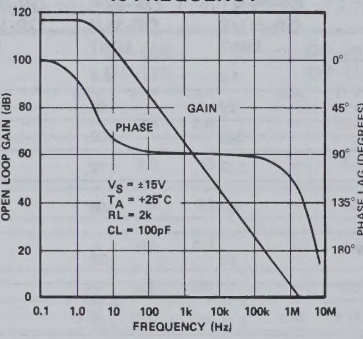
BIAS CURRENT vs TEMPERATURE



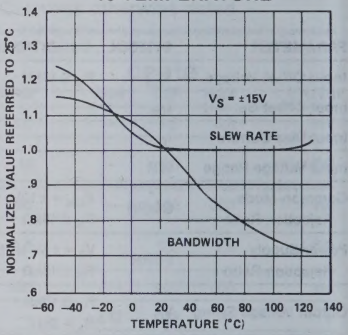
OPEN-LOOP GAIN vs TEMPERATURE



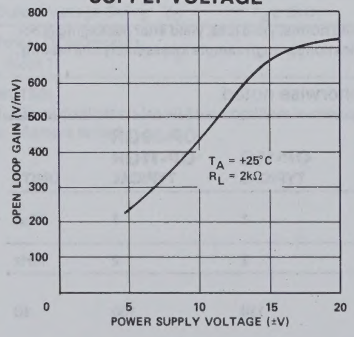
OPEN-LOOP GAIN AND PHASE vs FREQUENCY



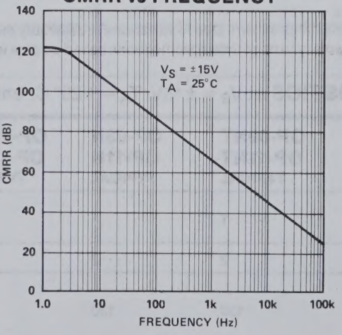
NORMALIZED SLEW RATE AND BANDWIDTH vs TEMPERATURE



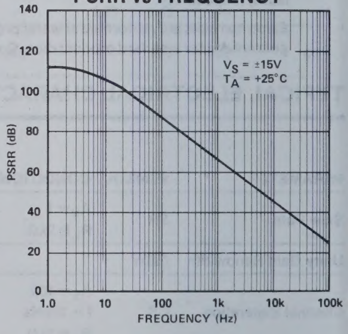
OPEN-LOOP GAIN vs SUPPLY VOLTAGE



CMRR vs FREQUENCY

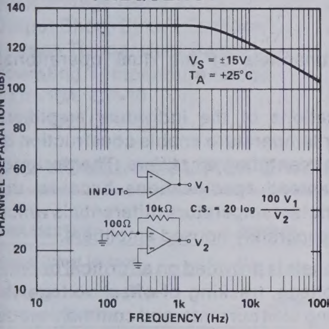


PSRR vs FREQUENCY

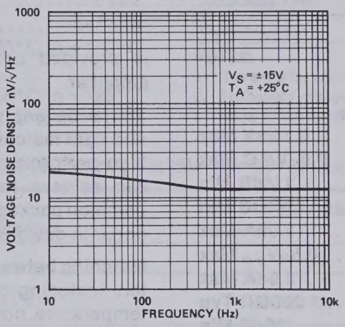


TYPICAL PERFORMANCE CHARACTERISTICS

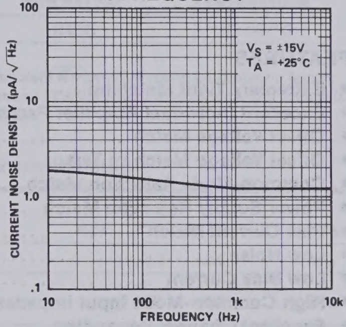
CHANNEL SEPARATION vs FREQUENCY



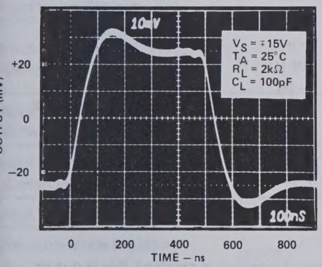
NOISE VOLTAGE DENSITY vs FREQUENCY



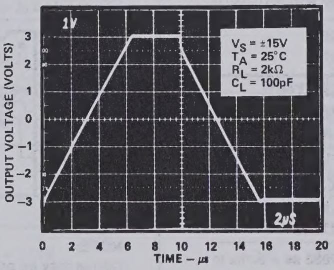
NOISE CURRENT DENSITY vs FREQUENCY



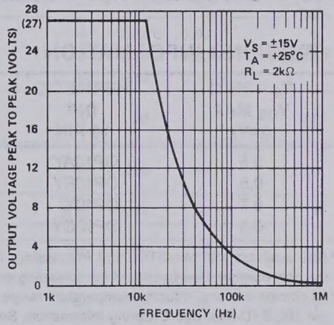
TRANSIENT RESPONSE



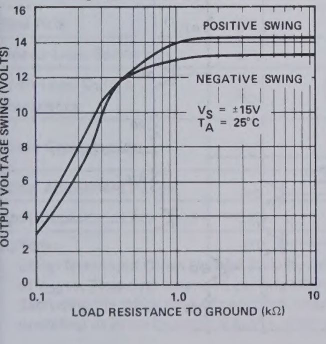
VOLTAGE FOLLOWER PULSE RESPONSE



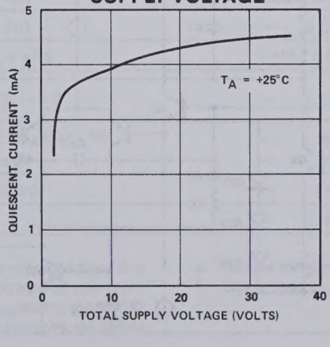
MAXIMUM OUTPUT SWING vs FREQUENCY



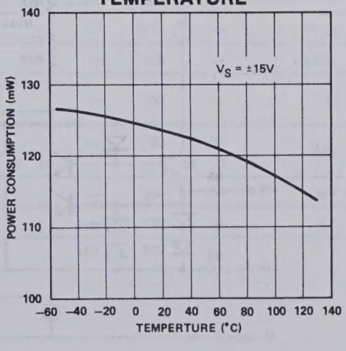
OUTPUT VOLTAGE vs LOAD RESISTANCE



QUIESCENT CURRENT vs SUPPLY VOLTAGE



POWER CONSUMPTION vs TEMPERATURE



OP-10

DUAL MATCHED INSTRUMENTATION OPERATIONAL AMPLIFIER

FEATURES

- **Extremely Tight Matching**
- **Excellent Individual Amplifier Parameters**
- **Offset Voltage Match .... 0.18mV Max**
- **Offset Voltage Match vs Temp. .... 0.8μV/°C Max**
- **Common-Mode Rejection Match .... 114dB Min**
- **Power Supply Rejection Match .... 100dB Min**
- **Bias Current Match .... 3.0nA Max**
- **Low Noise .... 0.6μV_{p-p} Max**
- **Low Bias Current .... 3.0nA Max**
- **High Common-Mode Input Impedance .... 200GΩ Typ**
- **Excellent Channel Separation .... 126dB Min**

GENERAL DESCRIPTION

The OP-10 series of dual-matched instrumentation operational amplifiers consists of two independent monolithic high-performance operational amplifiers in a single 14-pin Dual-in-Line package. Tight matching of critical parameters is provided between channels of the dual operational amplifier.

The excellent specifications of the individual amplifiers and tight matching over temperature enable construction of high-performance instrumentation amplifiers. The designer can achieve the guaranteed specifications because the common package eliminates temperature differentials which occur in designs using separately housed amplifiers.

Matching between channels is provided on all critical paramters including offset voltage, tracking of offset voltage vs. temperature, noninverting bias currents, and common-mode and power-supply rejection ratios. The individual amplifiers feature extremely low offset voltage, offset voltage drift, low noise voltage, low bias current, internal compensation and input/output protection.

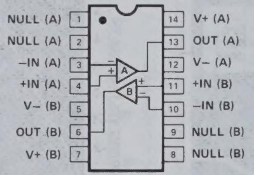
ORDERING INFORMATION†

T_A = 25°C V_{OS} MAX (mV)	HERMETIC DIP 14-PIN	OPERATING TEMPERATURE RANGE
0.5	OP10AY*	MIL
0.5	OP10EY	COM
0.5	OP10Y*	MIL
0.5	OP10CY	COM

*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

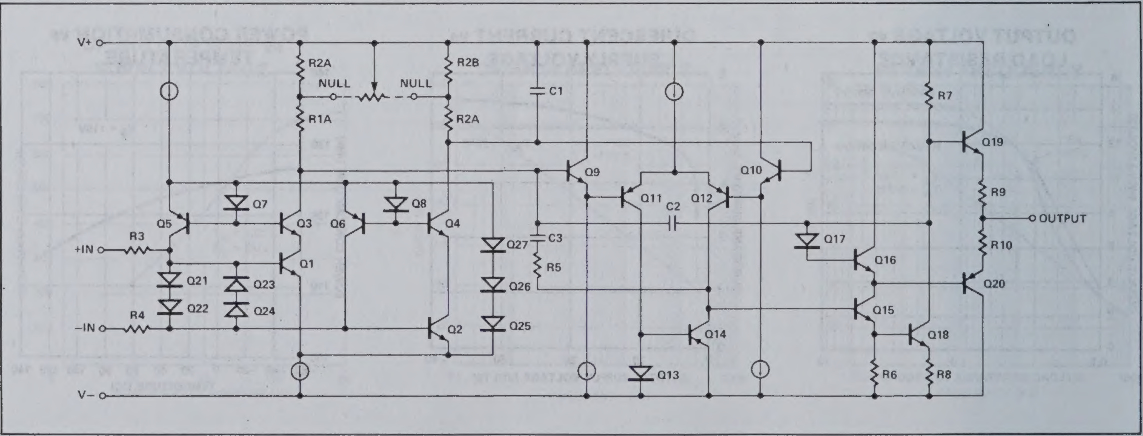
PIN CONNECTIONS



14-PIN CERAMIC DIP (Y-Suffix)

NOTE:
Device may be operated even if insertion is reversed; this is due to inherent symmetry of pin locations of amplifiers A and B.

SIMPLIFIED SCHEMATIC (1/2 OP-10)



ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... ±22V
nternal Power Dissipation (Note 1) 500mW
Differential Input Voltage .... ±30V
nput Voltage (Note 2) .... ±22V
Output Short-Circuit Duration .... Indefinite
Storage Temperature Range .... −65° C to +150° C
Operating Temperature Range
OP-10A, OP-10 .... −55° C to +125° C
OP-10E, OP-10C .... 0° C to +70° C
DICE Junction Temperature (T_j) .... −65° C to +150° C
Lead Temperature Range (Soldering, 60 sec) ...... 300° C

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
Dual-In-Line (Y)	106° C	11.3mW/° C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.
2. For supply voltages less than +22V, the absolute maximum input voltage is equal to the supply voltage.

INDIVIDUAL AMPLIFIER CHARACTERISTICS at $V_S = \pm15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-10A MIN	OP-10A TYP	OP-10A MAX	OP-10 MIN	OP-10 TYP	OP-10 MAX	UNITS
nput Offset Voltage	V_{OS}		—	0.2	0.5	—	0.2	0.5	mV
Long-Term Input Offset Voltage Stability	ΔV_{OS}/Time	(Notes 1, 2)	—	0.25	1.0	—	0.25	1.0	μV/Mo
nput Offset Current	I_{OS}		—	1.0	2.8	—	1.0	2.8	nA
nput Bias Current	I_B		—	±1	±3	—	±1	±3	nA
nput Noise Voltage	$e_{np\text{-}p}$	(Note 2) 0.1Hz to 10Hz	—	0.35	0.6	—	0.35	0.6	$\mu V_{p\text{-}p}$
nput Noise Voltage Density	e_n	$f_O = 10Hz$ (Note 2) $f_O = 100Hz$ $f_O = 1000Hz$	— — —	10.3 10.0 9.6	18.0 13.0 11.0	— — —	10.3 10.0 9.6	18.0 13.0 11.0	$nV/\sqrt{Hz}$
nput Noise Current	$i_{np\text{-}p}$	(Note 2) 0.1Hz to 10Hz	—	14	30	—	14	30	$pA_{p\text{-}p}$
nput Noise Current Density	i_n	$f_O = 10Hz$ (Note 2) $f_O = 100Hz$ $f_O = 1000Hz$	— — —	0.32 0.14 0.12	0.80 0.23 0.17	— — —	0.32 0.14 0.12	0.80 0.23 0.17	$pA/\sqrt{Hz}$
nput Resistance — Differential-Mode	R_{IN}	(Note 3)	20	60	—	20	60	—	MΩ
nput Resistance — Common-Mode	R_{INCM}		—	200	—	—	200	—	GΩ
nput Voltage Range	IVR		±13	±14	—	±13	±14	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm13V$	110	126	—	110	126	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm3V$ to $\pm18V$	—	4	10	—	—	10	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm10V$ $R_L \geq 500\Omega$, $V_O = \pm5V$ $V_S = \pm3V$ (Note 3)	200 150 —	500 500 —	— — —	200 150 —	500 500 —	— — —	V/mV
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0	— — —	±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0	— — —	V
Slew Rate	SR	$R_L \geq 2k\Omega$	—	0.17	—	—	0.17	—	V/μs
Closed-Loop Bandwidth	BW	$A_{VCL} = +1.0$	—	0.6	—	—	0.6	—	MHz
Open-Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	60	—	—	60	—	Ω
Power Consumption	P_d	Each Amplifier $V_S = \pm3V$	— —	90 4	120 6	— —	90 4	120 6	mW
Offset Adjustment Range		$R_P = 20k\Omega$	—	±4	—	—	±4	—	mV
nput Capacitance	C_{IN}		—	8	—	—	8	—	pF

NOTES:

1. Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV — refer to typical performance curves.
2. Sample tested.
3. Guaranteed by design.

INDIVIDUAL AMPLIFIER CHARACTERISTICS at $V_S = \pm15V$, $-55°C \leq T_A \leq +125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-10A MIN	OP-10A TYP	OP-10A MAX	OP-10 MIN	OP-10 TYP	OP-10 MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.3	0.7	—	0.3	0.7	mV
Average Input Offset Voltage Drift Without External Trim	TCV_{OS}	(Note 2)	—	0.7	2.0	—	0.7	2.0	μV/°C
With External Trim	TCV_{OSn}	$R_P = 20k\Omega$ (Note 3)	—	0.3	1.0	—	0.3	1.0	μV/°C
Input Offset Current	I_{OS}		—	1.8	5.6	—	1.8	5.6	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 2)	—	8	50	—	8	50	pA/°C
Input Bias Current	I_B		—	±2	±6	—	±2	±6	nA
Average Input Bias Current Drift	TCI_B	(Note 2)	—	13	50	—	13	50	pA/°C
Input Voltage Range	IVR		±13.0	±13.5	—	±13.0	±13.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm13V$	106	123	—	106	123	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm3V$ to $\pm18V$	—	5	20	—	5	20	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm10V$	150	400	—	150	400	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12.0	±12.6	—	±12.0	±12.6	—	V

MATCHING CHARACTERISTICS at $V_S = \pm15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-10A MIN	OP-10A TYP	OP-10A MAX	OP-10 MIN	OP-10 TYP	OP-10 MAX	UNITS
Input Offset Voltage	ΔV_{OS}		—	0.07	0.18	—	0.12	0.5	mV
Average Noninverting Bias Current	I_B+		—	±1.0	±3.0	—	±1.3	±4.5	nA
Noninverting Offset Current	$I_{OS}+$		—	0.8	2.8	—	1.1	4.5	nA
Inverting Offset Current	$I_{OS}-$		—	0.8	2.8	—	1.1	4.5	nA
Common-Mode Rejection Ratio Match	ΔCMRR	$V_{CM} = \pm13V$	114	123	—	106	120	—	dB
Power Supply Rejection Ratio Match	ΔPSRR	$V_S = \pm3V$ to $\pm18V$	—	3	10	—	4	20	μV/V
Channel Separation	CS	(Note 2)	126	140	—	126	140	—	dB

MATCHING CHARACTERISTICS at $V_S = \pm15V$, $-55°C \leq T_A \leq +125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-10A MIN	OP-10A TYP	OP-10A MAX	OP-10 MIN	OP-10 TYP	OP-10 MAX	UNITS
Input Offset Voltage Match	ΔV_{OS}		—	0.1	0.3	—	0.2	0.9	mV
Input Offset Voltage Tracking Without External Trim	$TC\Delta V_{OS}$	(Note 2)	—	0.45	1.3	—	0.9	2.5	μV/°C
With External Trim	$TC\Delta V_{OSn}$	$R_P = 20k\Omega$ (Note 3) Channel A only	—	0.3	0.8	—	0.4	1.2	μV/°C

NOTES:

1. Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV — refer to typical performance curves.
2. Sample tested.
3. Guaranteed by design.

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \le T_A \le +125°C$, unless otherwise noted. (Continued)

			OP-10A			OP-10			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Average Noninverting Bias Current	I_B+		—	±2.0	±6.0	—	±2.4	±8.0	nA
Average Drift of Noninverting Bias Current	TCI_B+	(Note 2)	—	10	40	—	15	—	pA/°C
Noninverting Offset Current	$I_{OS}+$		—	2.0	6.5	—	2.4	9.0	nA
Average Drift of Noninverting Offset Current	$TCI_{OS}+$	(Note 2)	—	12	50	—	18	—	pA/°C
Inverting Offset Current	$I_{OS}-$		—	2.0	6.5	—	2.4	9.0	nA
Common-Mode Rejection Ratio Match	ΔCMRR	$V_{CM} = \pm 13V$	108	120	—	103	117	—	dB
Power Supply Rejection Ratio Match	ΔPSRR	$V_S = \pm 3V$ to $\pm 18V$	—	6	20	—	7	32	μV/V

INDIVIDUAL AMPLIFIER CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

			OP-10E			OP-10C			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.2	0.5	—	0.2	0.5	mV
Long-Term Input Offset Voltage Stability	ΔV_{OS}/Time	(Notes 1, 2)	—	0.3	1.5	—	0.5	—	μV/Mo
Input Offset Current	I_{OS}		—	1.2	3.8	—	1.8	6.0	nA
Input Bias Current	I_B		—	±1.2	±4.0	—	±1.8	±7.0	nA
Input Noise Voltage	e_{np-p}	(Note 2) 0.1Hz to 10Hz	—	0.35	0.6	—	0.38	0.65	μV_{p-p}
Input Noise Voltage Density	e_n	f_O = 10Hz	—	10.3	18.0	—	10.5	20.0	$nV/\sqrt{Hz}$
		(Note 2) f_O = 100Hz	—	10.0	13.0	—	10.2	13.5	
		f_O = 1000Hz	—	9.6	11.0	—	9.8	11.5	
Input Noise Current	i_{np-p}	(Note 2) 0.1Hz to 10Hz	—	14	30	—	15	35	pA_{p-p}
Input Noise Current Density	i_n	f_O = 10Hz	—	0.32	0.80	—	0.35	0.90	$pA/\sqrt{Hz}$
		(Note 2) f_O = 100Hz	—	0.14	0.23	—	0.15	0.27	
		f_O = 1000Hz	—	0.12	0.17	—	0.13	0.18	
Input Resistance — Differential-Mode	R_{IN}	(Note 3)	15	50	—	8	33	—	MΩ
Input Resistance — Common-Mode	R_{INCM}		—	160	—	—	120	—	GΩ
Input Voltage Range	IVR		±13	±14	—	±13	±14	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	106	123	—	100	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	4	20	—	10	32	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$, $V_O = \pm 10V$	200	500	—	120	400	—	V/mV
		$R_L \ge 500\Omega$, $V_O = \pm 0.5V$	150	500	—	100	400	—	
		$V_S = \pm 3V$ (Note 3)	—	—	—	—	—	—	
Output Voltage Swing	V_O	$R_L \ge 10k\Omega$	±12.5	±13.0	—	±12.0	±13.0	—	V
		$R_L \ge 2k\Omega$	±12.0	±12.8	—	±11.5	±12.8	—	
		$R_L \ge 1k\Omega$	±10.5	±12.0	—	—	±12.0	—	

NOTES:

1. Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV — refer to typical performance curves.
2. Sample tested.
3. Guaranteed by design.

INDIVIDUAL AMPLIFIER CHARACTERISTICS at $V_S = \pm 15V$, $0°C \le T_A \le +70°C$, unless otherwise noted. (Continued)

			OP-10E			OP-10C			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Slewing Rate	SR	$R_L \ge 2k\Omega$	—	0.17	—	—	0.17	—	V/μs
Closed-Loop Bandwidth	BW	$A_{VCL} = +1.0$	—	0.6	—	—	0.6	—	MHz
Open-Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	60	—	—	60	—	Ω
Power Consumption	P_d	Each Amplifier $V_S = \pm 3V$	— —	90 4	120 6	— —	95 4	150 8	mW
Offset Adjustment Range		$R_P = 20k\Omega$	—	±4	—	—	±4	—	mV
Input Capacitance	C_{IN}		—	8	—	—	8	—	pF

INDIVIDUAL AMPLIFIER CHARACTERISTICS at $V_S = \pm 15V$, $0°C \le T_A \le +70°C$, unless otherwise noted.

			OP-10E			OP-10C			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}		—	0.25	0.6	—	0.35	1.6	mV
Average Input Offset Voltage Drift									
Without External Trim	TCV_{OS}	(Note 2)	—	0.7	2.0	—	1.2	4.5	μV/°C
With External Trim	TCV_{OSn}	$R_P = 20k\Omega$ (Note 3)	—	0.3	1.0	—	0.4	1.5	μV/°C
Input Offset Current	I_{OS}		—	1.4	5.3	—	2.0	8.0	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 2)	—	8	50	—	12	50	pA/°C
Input Bias Current	I_B		—	±1.5	±5.5	—	±2.2	±9.0	nA
Average Input Bias Current Drift	TCI_B	(Note 2)	—	13	50	—	18	50	pA/°C
Input Voltage Range	IVR		±13.0	±13.5	—	±13.0	±13.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	103	123	—	97	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	7	32	—	10	51	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$, $V_O = \pm 10V$	100	400	—	100	400	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±12.0	±12.6	—	±11.0	±12.6	—	V

NOTES:

1. Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV — refer to typical performance curves.
2. Sample tested.
3. Guaranteed by design.

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

			OP-10E			OP-10C			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage Match	ΔV_{OS}		—	0.12	0.5	—	0.3	—	mV
Average Noninverting Bias Current	I_B^+		—	±1.3	±4.5	—	±2.0	—	nA
Noninverting Offset Current	I_{OS}^+		—	1.1	4.5	—	1.8	—	nA
Inverting Offset Current	I_{OS}^-		—	1.1	4.5	—	1.8	—	nA
Common-Mode Rejection Ratio Match	ΔCMRR	$V_{CM} = \pm 13V$	106	120	—	—	117	—	dB
Power Supply Rejection Ratio Match	ΔPSRR	$V_S = \pm 3V$ to $\pm 18V$	—	4	20	—	5	—	µV/V
Channel Separation	CS	(Note 1)	126	140	—	120	137	—	dB

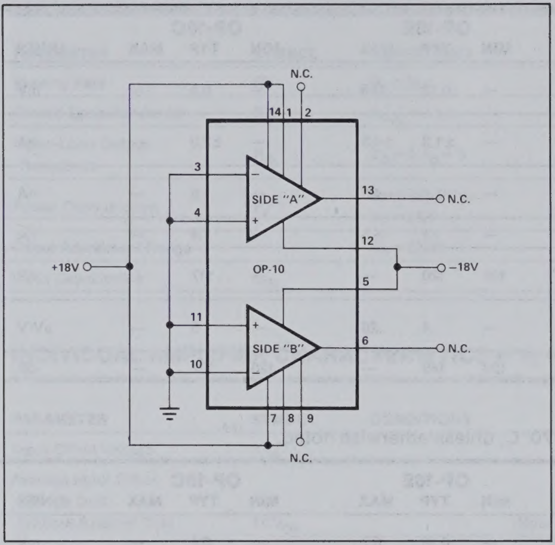
MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $0°C \le T_A \le +70°C$, unless otherwise noted.

			OP-10E			OP-10C			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage Match	ΔV_{OS}		—	0.18	0.7	—	0.4	—	mV
Input Offset Voltage Tracking Without External Trim	$TC\Delta V_{OS}$	(Note 1)	—	0.9	2.3	—	1.3	—	µV/°C
With External Trim	$TC\Delta V_{OSn}$	$R_L = 20k\Omega$ Channel A Only (Note 2)	—	0.3	0.9	—	0.6	—	µV/°C
Average Noninverting Bias Current	I_B^+		—	±2.0	±6.0	—	±2.8	—	nA
Average Drift of Noninverting Bias Current	TCI_B^+	(Note 1)	—	12	40	—	18	—	pA/°C
Noninverting Offset Current	I_B^+		—	2.0	6.0	—	2.8	—	nA
Average Drift of Noninverting Offset Current	TCI_{OS}^+	(Note 1)	—	15	50	—	20	—	pA/°C
Input Offset Current	I_{OS}^-		—	2.0	6.0	—	2.8	—	nA
Common-Mode Rejection Ratio Match	ΔCMRR	$V_{CM} = \pm 13V$	103	117	—	—	114	—	dB
Power Supply Rejection Ratio Match	ΔPSRR	$V_S = \pm 3V$ to $\pm 18V$	—	6	32	—	8	—	µV/V

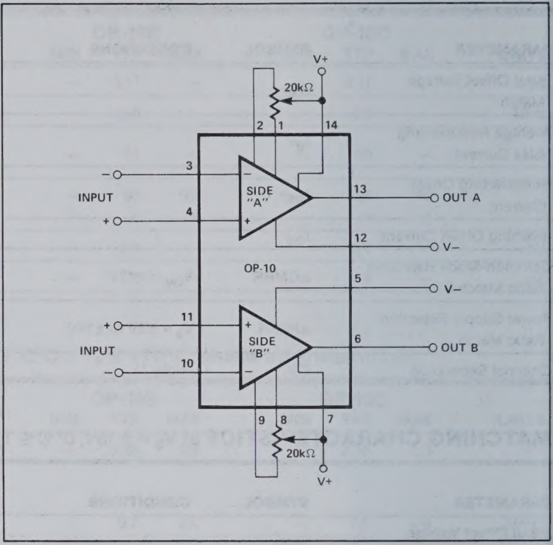
NOTES:

1. Sample tested.
2. Guaranteed by design.

BURN-IN CIRCUIT

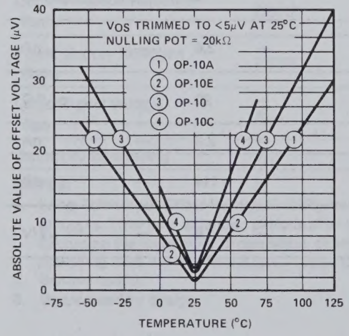

N.C.
14
1
2
3
4
SIDE "A"
13
N.C.
12
+18V
OP-10
−18V
5
11
SIDE "B"
6
N.C.
10
7
8
9
N.C.

OFFSET NULLING CIRCUIT

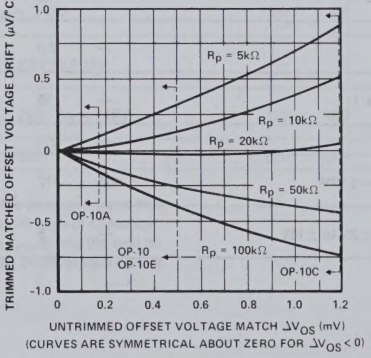

V+
20kΩ
2
1
14
3
INPUT
4
SIDE "A"
13
OUT A
12
V−
OP-10
5
V−
11
INPUT
SIDE "B"
6
OUT B
10
9
8
7
20kΩ
V+

TYPICAL PERFORMANCE CHARACTERISTICS

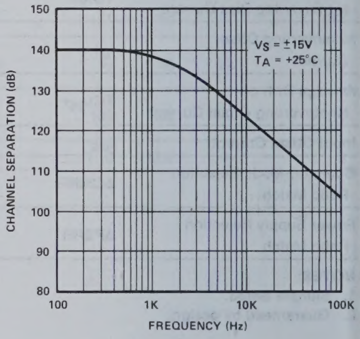
MATCHING CHARACTERISTICS TRIMMED OFFSET VOLTAGE MATCH vs TEMPERATURE



MATCHING CHARACTERISTICS TRIMMED MATCHED OFFSET VOLTAGE DRIFT AS A FUNCTION OF TRIMMING POT (R_P) SIZE AND ΔV_{OS}

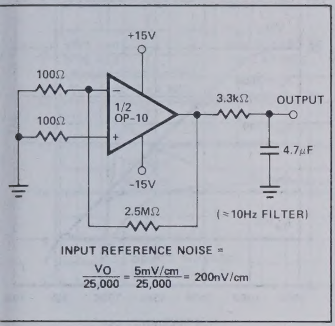


MATCHING CHARACTERISTICS CHANNEL SEPARATION vs FREQUENCY



TYPICAL PERFORMANCE CHARACTERISTICS

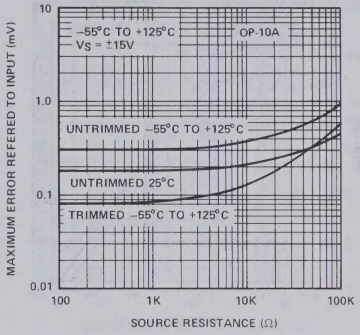
TYPICAL LOW-FREQUENCY NOISE TEST CIRCUIT



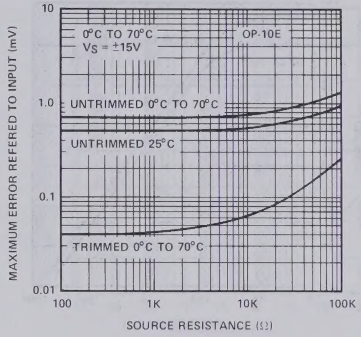
INPUT REFERENCE NOISE =

$$\frac{V_O}{25{,}000} = \frac{5\text{mV/cm}}{25{,}000} = 200\text{nV/cm}$$

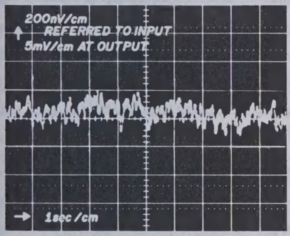
MATCHING CHARACTERISTIC MAXIMUM INPUT ERROR vs SOURCE RESISTANCE



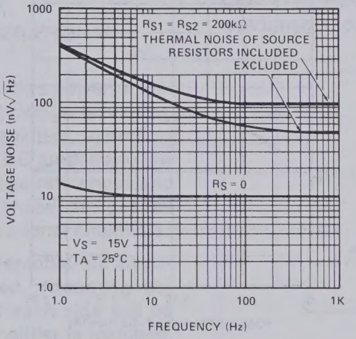
MATCHING CHARACTERISTIC MAXIMUM INPUT ERROR vs SOURCE RESISTANCE



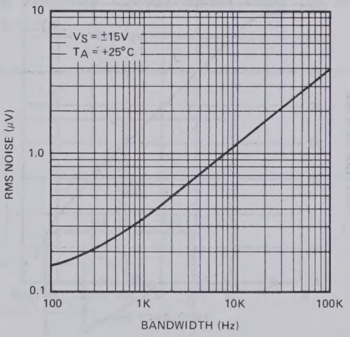
OP-10 LOW FREQUENCY NOISE



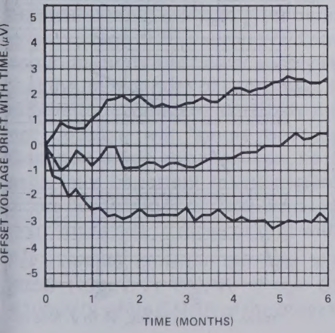
VOLTAGE NOISE DENSITY vs FREQUENCY



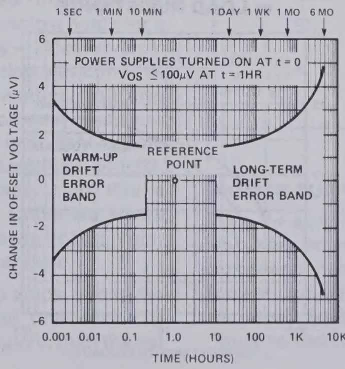
INPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



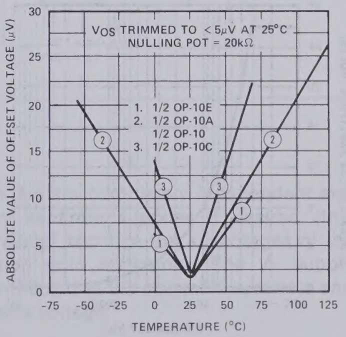
TYPICAL OFFSET VOLTAGE STABILITY vs TIME



OFFSET VOLTAGE DRIFT WITH TIME

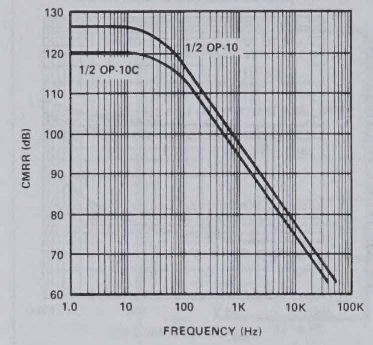


TRIMMED OFFSET VOLTAGE vs TEMPERATURE

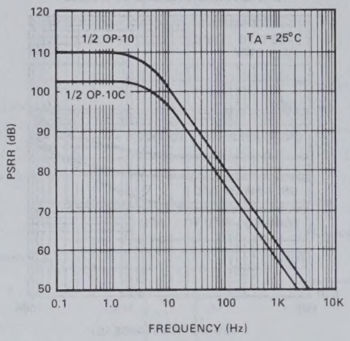


TYPICAL PERFORMANCE CHARACTERISTICS EACH AMPLIFIER

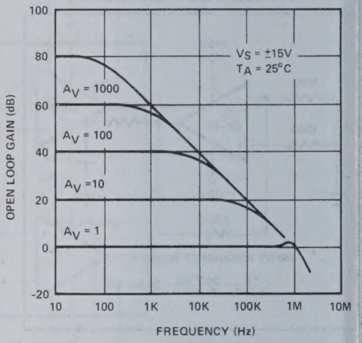
CMRR vs FREQUENCY



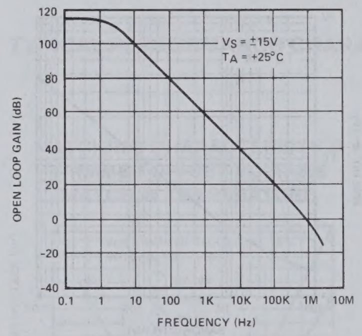
PSRR vs FREQUENCY



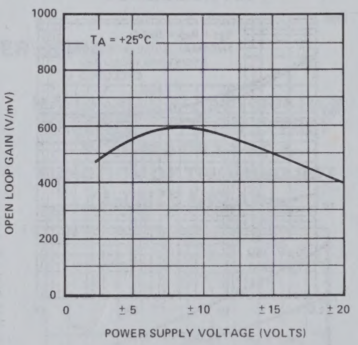
CLOSED-LOOP GAIN vs FREQUENCY



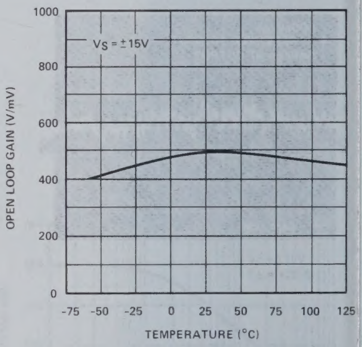
OPEN-LOOP GAIN vs FREQUENCY



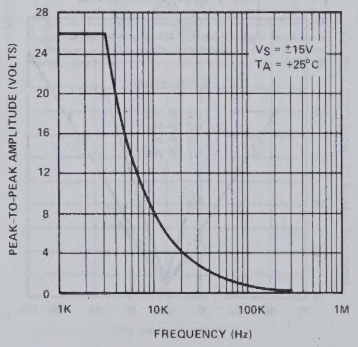
OPEN-LOOP GAIN vs POWER SUPPLY VOLTAGE



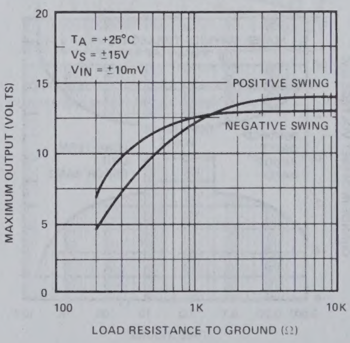
OPEN-LOOP GAIN vs TEMPERATURE



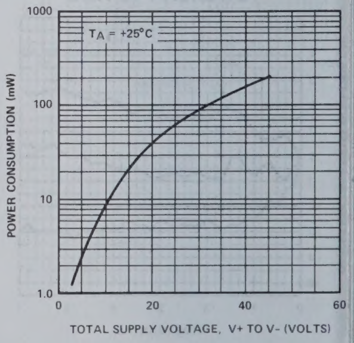
MAXIMUM OUTPUT SWING vs FREQUENCY



MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE

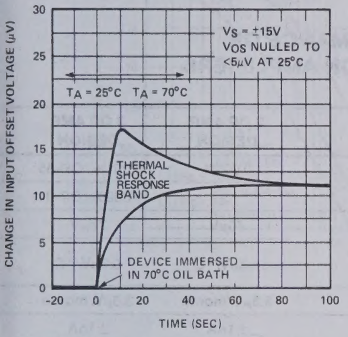


POWER CONSUMPTION vs POWER SUPPLY

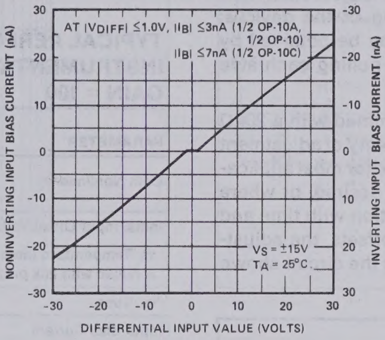


TYPICAL PERFORMANCE CHARACTERISTICS

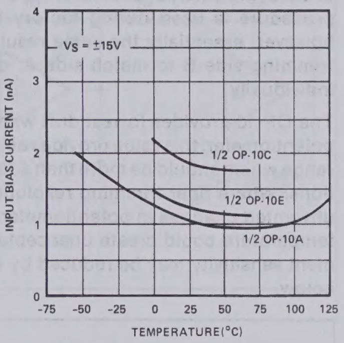
OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE



INPUT BIAS CURRENT vs TEMPERATURE



APPLICATIONS INFORMATION

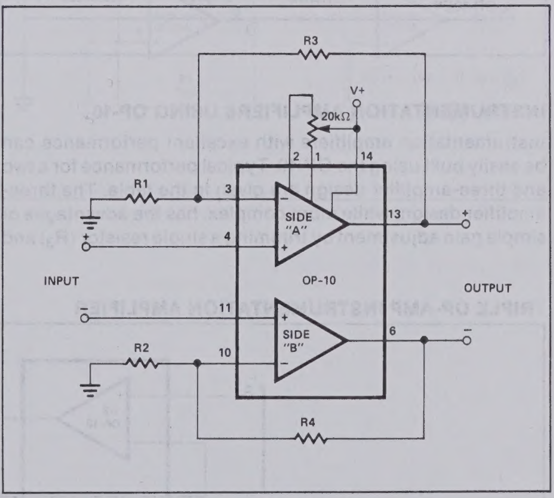
SPECIAL NOTES ON THE APPLICATION OF DUAL-MATCHED OPERATIONAL AMPLIFIERS

ADVANTAGES OF DUAL MATCHED OPERATIONAL AMPLIFIERS

Dual matched operational amplifiers provide a powerful tool for the solution of some difficult circuit design problems. Circuits include true instrumentation amplifiers, extremely low drift, high common-mode rejection DC amplifiers, low DC drift active filters, dual tracking voltage references and many other demanding applications. These designs all require good matching between two operational amplifiers.

The adjacent circuit, a differential-in, differential-out amplifier, shows how errors can be reduced. Assuming the resistors used are matched, the gain of each side will be identical; if the offset voltage of each amplifier is matched, then the net differential voltage at the amplifiers output will be zero. Note that the output offset error of this amplifier is not a function of the offset voltage of the individual amplifiers, but only a function of the **difference** between the amplifiers' offset voltages. This error-cancellation principle holds for a number of input-referred error parameters — offset voltage, offset voltage drift, inverting and noninverting bias currents, common-mode and power supply rejection ratios. Note also that the impedances of each input, both common-mode and differential-mode, are extremely high, an important feature not possible with single operational amplifier circuits. Common-mode rejection can be made very high; this is especially important in instrumentation amplifiers where errors due to large common-mode voltages can be far greater than errors due to noise or drift with temperature.

For example, consider the case of two op amps, each with 80dB (100μV/V) CMRR. If the CMRR of one device is +100μV/V while CMRR of the other is −100μV/V, then the net CMRR will be 200μV/V, a 6dB degradation. The matching of CMRR increases the effective CMRR when used as an instrumentation input stage.



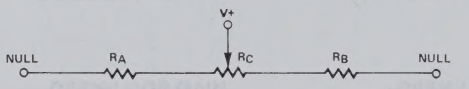
POWER SUPPLIES

The V+ supply terminals are completely independent and may be powered by separate supplies if desired (this approach, however, would sacrifice the advantages of the power supply rejection ratio matching). The V− supply terminals are both connected to the common substrate and must be tied to the same voltage.

OFFSET TRIMMING

Offset trimming terminals are provided for each amplifier of the OP-10. Guaranteed performance over temperature is obtained by trimming only one side (side A) to match the offset of the other; a net differential offset of zero results. This procedure is used during factory testing of the devices; however, essentially the same results may be obtained by trimming side B to match side A, or by nulling each side individually.

The OP-10 provides lowest drift when trimmed with a 20kΩ potentiometer; this value provides about ±4mV of adjustment range which should be more than adequate for most applications. Where finer trimming resolution is desired, or where unwanted changes in potentiometer position with time and temperature could create unacceptable offsets, the adjustment sensitivity may be reduced by using the circuit shown below.


V+
NULL
R_A
R_C
R_B
NULL

Model	Null Range	Fixed Resistors R_A, R_B	Potentiometer R_C
OP-10AY, OP-10Y, OP-10EY	±1.2mV	5.1kΩ	10.0kΩ

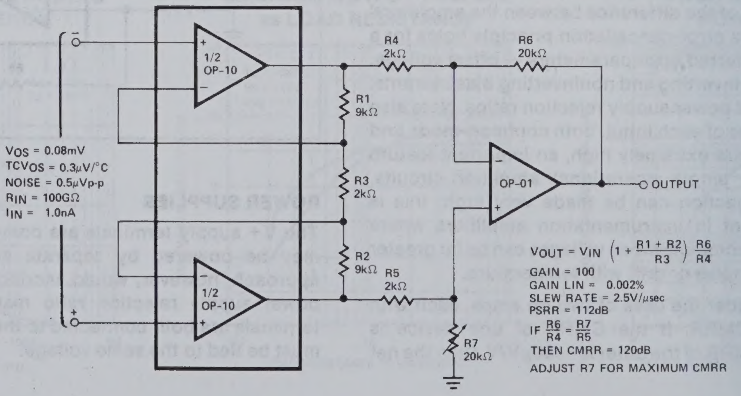
INSTRUMENTATION AMPLIFIERS USING OP-10

Instrumentation amplifiers with excellent performance can be easily built using the OP-10. Typical performance for a two and three-amplifier design are given in the table. The three-amplifier design, while more complex, has the advantages of simple gain adjustment by trimming a single resistor (R_3) and wide common-mode voltage capability at any gain, plus improved gain linearity. Slew rate, small-signal bandwidth, and full power bandwidth are also superior. Speed will be improved by using an OP-01 for the output stage.

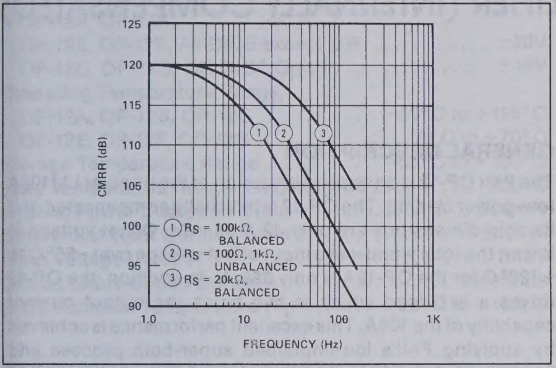
TYPICAL PERFORMANCE OF INSTRUMENTATION AMPLIFIERS GAIN = 100

PARAMETER	2 OP AMP DESIGN	3 OP AMP DESIGN
Gain Nonlinearity	0.004%	0.001% (OP-05) 0.002% (OP-01)
Initial Input Offset Voltage	70μV	75μV
vs. Temperature (amplifier A nulled with 20k pot)	0.3μV/°C	0.3μV/°C
vs. Time	3.5μV/month	3.5μV/month
Input Bias Current	±1nA	±1nA
vs. Temperature	10pA/°C	10pA/°C
Input Offset Current	0.8nA	0.8nA
vs. Temperature	12pA/°C	12pA/°C
Input Impedance		
Differential	80GΩ	100GΩ
Common-Mode	100GΩ	100GΩ
Input Noise Voltage (0.1 to 10Hz)	$0.5\mu V_{p-p}$	$0.5\mu V_{p-p}$
Input Noise Current (0.1 to 10Hz)	$14pA_{p-p}$	$14pA_{p-p}$
Common-Mode Rejection	120dB	120dB
Power Supply Rejection	112dB	112dB
Frequency Response		
Small-Signal (−3dB)	6.0Hz	26kHz (OP-05) 85kHz (OP-01)
Full Power	2.5Hz	4.3kHz (OP-05) 43kHz (OP-01)
Slew Rate	0.17V/μs	0.17V/μsec (OP-05) 4.0V/μsec (OP-01)

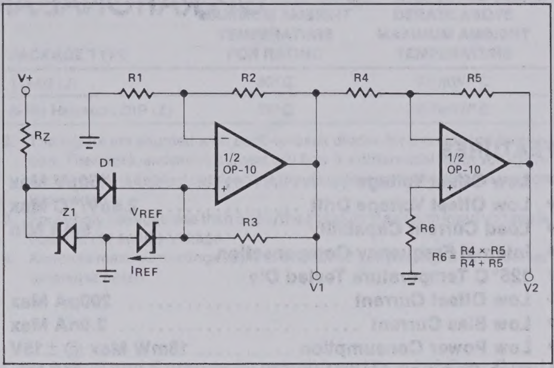
TRIPLE OP-AMP INSTRUMENTATION AMPLIFIER


−
+
1/2 OP-10
1/2 OP-10
V_{OS} = 0.08mV
TCV_{OS} = 0.3μV/°C
NOISE = 0.5μVp-p
R_{IN} = 100GΩ
I_{IN} = 1.0nA
R4 2kΩ
R6 20kΩ
R1 9kΩ
R3 2kΩ
R2 9kΩ
R5 2kΩ
R7 20kΩ
OP-01
OUTPUT
$V_{OUT} = V_{IN}\left(1 + \frac{R1 + R2}{R3}\right)\frac{R6}{R4}$
GAIN = 100
GAIN LIN = 0.002%
SLEW RATE = 2.5V/μsec
PSRR = 112dB
IF $\frac{R6}{R4} = \frac{R7}{R5}$
THEN CMRR = 120dB
ADJUST R7 FOR MAXIMUM CMRR

CMRR vs FREQUENCY INSTRUMENTATION AMPLIFIER (3 OP-AMP DESIGN)



PRECISION DUAL TRACKING VOLTAGE REFERENCES USING OP-10


V+
R1
R2
R4
R5
RZ
D1
1/2 OP-10
1/2 OP-10
Z1
VREF
R3
R6
IREF
V1
V2
R6 = R4 × R5 / R4 + R5

PRECISION DUAL TRACKING VOLTAGE REFERENCES USING OP-10

Precision dual tracking voltage references using a single reference source are easily constructed using OP-10. These references exhibit low noise, excellent stability vs. temperature and time, and have excellent power supply rejection.

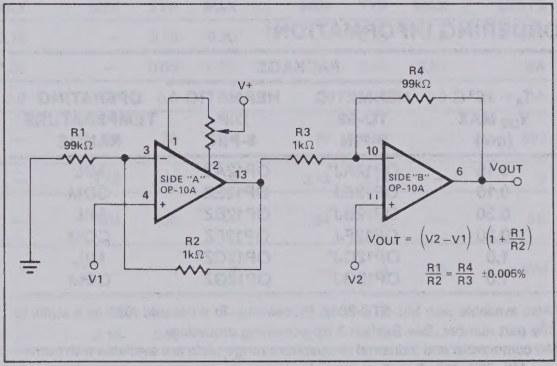
In the circuit shown, R_3 should be adjusted to set I_{REF} to operate V_{REF} at its minimum temperature coefficient current. Proper circuit start-up is assured by R_Z, Z_1, and D_1.

$V_{Z1} \leq V_{REF} + 2V$ $\qquad$ $V1 = V_{REF}\left(1 + \frac{R2}{R1}\right)$

$I_{REF} = (V1 - V_{REF})/R3$ $\qquad$ $V2 = V1\left(\frac{-R5}{R4}\right)$

Output Impedance (ΔI_L:1.0mA-5.0mA) ...... $0.25 \times 10^{-3}\Omega$

INSTRUMENTATION AMPLIFIER (2 OP-AMP DESIGN)


R4 99kΩ
V+
R1 99kΩ
R3 1kΩ
3
1
2
4
13
10
11
6
SIDE "A" OP-10A
SIDE "B" OP-10A
R2 1kΩ
V1
V2
VOUT

$V_{OUT} = (V2 - V1)\left(1 + \frac{R1}{R2}\right)$

$\frac{R1}{R2} = \frac{R4}{R3}$ ±0.005%

OP-12 PRECISION LOW-INPUT-CURRENT OPERATIONAL AMPLIFIER (INTERNALLY COMPENSATED)

FEATURES

- **Low Offset Voltage .... 150µV Max**
- **Low Offset Voltage Drift .... 2.5µV/°C Max**
- **Load Current Capability .... 5mA Min**
- **Internal Frequency Compensation**
- **125°C Temperature Tested Die**
- **Low Offset Current .... 200pA Max**
- **Low Bias Current .... 2.0nA Max**
- **Low Power Consumption .... 18mW Max @ ±15V**
- **High Common-Mode Input Range .... ±13V Min**
- **MIL-STD-883 Class B Processing Available**
- **Silicon-Nitride Passivation**

ORDERING INFORMATION†

$T_A = 25°C$ V_{OS} MAX (mV)	PACKAGE HERMETIC TO-99 8-PIN	HERMETIC DIP 8-PIN	OPERATING TEMPERATURE RANGE
0.15	OP12AJ*	OP12AZ*	MIL
0.15	OP12EJ	OP12EZ	COM
0.30	OP12BJ*	OP12BZ*	MIL
0.30	OP12FJ	OP12FZ	COM
1.0	OP12CJ*	OP12CZ*	MIL
1.0	OP12GJ	OP12GZ	COM

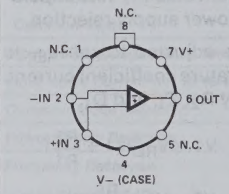
*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

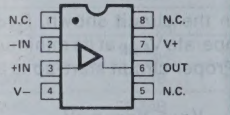
GENERAL DESCRIPTION

The PMI OP-12 is an improved version of the popular LM108A low-power op amp. The OP-12 is internally compensated and its chip dimensions are only 42 X 58 mils. Offset voltage is lower; the total worst-case input offset voltage over −55°C to +125°C for the OP-12A is only 350µV. In addition, the OP-12 drives a 2kΩ load which is five times the output current capability of the 108A. This excellent performance is achieved by applying PMI's ion-implanted super-beta process and on-chip zener-zap trimming capabilities. The internal compensation makes this op amp ideal for hybrid assembly applications.

PIN CONNECTIONS

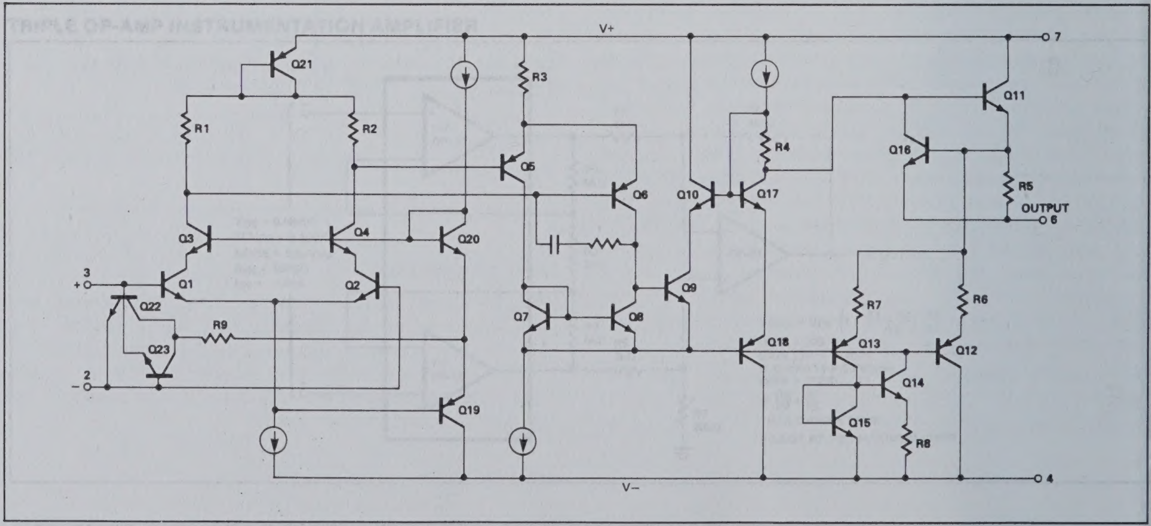


TO-99 (J-Suffix)



8-PIN HERMETIC MINI-DIP (Z-Suffix)

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 4)

Supply Voltage
  OP-12A, OP-12B,
  OP-12E, OP-12F, All DICE except GR .... ±20V
  OP-12C, OP-12G, GR DICE Only .... ±18V
Operating Temperature Range
  OP-12A, OP-12B, OP-12C .... −55°C to +125°C
  OP-12E, OP-12F, OP-12G .... 0°C to +70°C
Storage Temperature Range .... −65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) ...... 300°C
Internal Power Dissipation (Note 1) 500mW
Differential Input Current (Note 2) .... ±10mA
Input Voltage (Note 3) .... ±15V
Output Short-Circuit Duration .... Indefinite
DICE Junction Temperature (T_j) .... −65°C to +150°C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C

2. The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is provided.
3. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
4. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 20V$ and $T_A = 25°C$ for A, B, E and F grades, $V_S = \pm 15V$, and $T_A = 25°C$ for C and G grades, unless otherwise noted.

			OP-12A/E			OP-12B/F			OP-12C/G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.07	0.15	—	0.18	0.30	—	0.25	1.0	mV
Input Offset Current	I_{OS}		—	0.05	0.20	—	0.05	0.20	—	0.08	0.50	nA
Input Bias Current	I_B		—	0.8	2.0	—	0.8	2.0	—	1.0	5.0	nA
Input Resistance — Differential-Mode	R_{IN}	(Note 1)	26	70	—	26	70	—	10	50	—	MΩ
Input Voltage Range	IVR	$V_S = \pm 15V$	±13	±14	—	±13	±14	—	±13	±14	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	104	120	—	104	120	—	84	116	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 15V$	—	1	7	—	1	7	—	4	63	μV/V
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$, $V_S = \pm 15V$	±13	±14	—	±13	±14	—	±13	±14	—	V
		$R_L \geq 2k\Omega$, $V_S = \pm 15V$	±10	±12	—	±10	±12	—	±10	±12	—	
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 10k\Omega$ $V_O = \pm 10V$	80	300	—	80	300	—	40	250	—	V/mV
		$R_L \geq 2k\Omega$ $V_O = \pm 10V$	50	150	—	50	150	—	—	100	—	
Power Consumption	P_d	$V_S = \pm 15V$, No Load	—	9	18	—	9	18	—	12	24	mW
		$V_S = \pm 5V$, No Load	—	3	6	—	3	6	—	4	8	
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	—	0.9	—	—	0.9	—	—	0.9	—	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10Hz$	—	22	—	—	22	—	—	22	—	$nV/\sqrt{Hz}$
		$f_O = 100Hz$	—	21	—	—	21	—	—	21	—	
		$f_O = 1000Hz$	—	20	—	—	20	—	—	20	—	
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	—	3	—	—	3	—	—	3	—	pA_{p-p}
Input Noise Current Density	i_n	$f_O = 10Hz$	—	0.15	—	—	0.15	—	—	0.15	—	$pA/\sqrt{Hz}$
		$f_O = 100Hz$	—	0.14	—	—	0.14	—	—	0.14	—	
		$f_O = 1000Hz$	—	0.13	—	—	0.13	—	—	0.13	—	
Slew Rate	SR	$R_L \geq 2k\Omega$	—	0.12	—	—	0.12	—	—	0.12	—	V/μs
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$	—	0.80	—	—	0.80	—	—	0.80	—	MHz
Open-Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	200	—	—	200	—	—	200	—	Ω

NOTE:
1. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, for C grade, $V_S = \pm20V$ for A and B grades, $-55°C \le T_A \le +125°C$, unless otherwise noted.

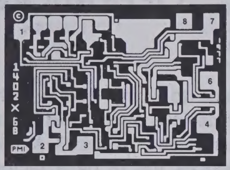
			OP-12A			OP-12B			OP-12C			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}		—	0.12	0.35	—	0.28	0.60	—	0.40	2.0	mV
Average Input Offset Voltage Drift	TCV_{OS}		—	0.50	2.5	—	1.0	3.5	—	1.5	10	μV/°C
Input Offset Current	I_{OS}		—	0.12	0.40	—	0.12	0.40	—	0.18	1.0	nA
Average Input Offset Current Drift	TCI_{OS}		—	0.50	2.5	—	0.50	2.5	—	1.0	5.0	pA/°C
Input Bias Current	I_B		—	1.2	3.0	—	1.2	3.0	—	1.8	10	nA
Input Voltage Range	IVR	$V_S = \pm15V$	±13	±14	—	±13	±14	—	±13	±14	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm13V$	100	116	—	100	116	—	80	112	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm5$ to $\pm15V$	—	4	10	—	4	10	—	6	100	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 5k\Omega$ $V_O = \pm10V$	40	120	—	40	120	—	15	80	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 10k\Omega$, $V_S = \pm15V$	±13	±14	—	±13	±14	—	±13	±14	—	V
		$R_L \ge 5k\Omega$, $V_S = \pm15V$	±10	±13	—	±10	±13	—	±10	±12	—	
Power Consumption	P_d	$V_S = \pm15V$, No Load	—	9	18	—	9	18	—	15	24	mW

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$ for G grade, $V_S = \pm20V$ for E and F grades, $0°C \le T_A \le 70°C$, unless otherwise noted.

			OP-12E			OP-12F			OP-12G			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}		—	0.10	0.26	—	0.23	0.45	—	0.32	1.4	mV
Average Input Offset Voltage Drift	TCV_{OS}		—	0.50	2.5	—	1.0	3.5	—	1.5	10	μV/°C
Input Offset Current	I_{OS}		—	0.08	0.30	—	0.11	0.60	—	0.12	0.70	nA
Average Input Offset Current Drift	TCI_{OS}		—	0.50	2.5	—	1.0	5.0	—	1.0	5.0	pA/°C
Input Bias Current	I_B		—	1.0	2.6	—	1.2	5.2	—	1.4	6.5	nA
Input Voltage Range	IVR	$V_S = \pm15V$	±13	±14	—	±13	±14	—	±13	±14	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm13V$	100	116	—	100	116	—	80	112	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm5$ to $\pm15V$	—	4	10	—	4	10	—	6	100	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 10k\Omega$ $V_O = \pm10V$	60	200	—	60	200	—	25	150	—	V/mV
		$R_L \ge 2k\Omega$ $V_O = \pm10V$	25	100	—	25	100	—	—	80	—	
Output Voltage Swing	V_O	$R_L \ge 10k\Omega$ $V_S = \pm15V$	±13	±14	—	±13	±14	—	±13	±14	—	V
		$R_L \ge 5k\Omega$ $V_S = \pm15V$	±10	±12	—	±10	±12	—	±10	±12	—	
Power Consumption	P_d	$V_S = \pm15V$, No Load	—	9	18	—	9	18	—	15	24	mW

For typical performance characteristics, see OP-08 data sheet. Assume $C_C = 30pF$.

DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)



DIE SIZE 0.058 × 0.042 inch, 2436 sq. mils
(1.47 × 1.07 mm, 1.57 sq. mm)

1. NO CONNECTION
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V−
6. OUTPUT
7. V+
8. NO CONNECTION

For additional DICE information refer to Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$ for OP-12N, OP-12G and OP-12GR devices; $T_A = 125°C$ for OP-12NT and OP-12GT devices, unless otherwise noted. (Note 2)

PARAMETER	SYMBOL	CONDITIONS	OP-12NT LIMIT	OP-12N LIMIT	OP-12GT LIMIT	OP-12G LIMIT	OP-12GR LIMIT	UNITS
Input Offset Voltage	V_{OS}		0.15	0.3	0.6	0.3	1	mV MAX
Input Offset Current	I_{OS}		0.2	0.2	0.2	0.2	0.5	nA MAX
Input Bias Current	I_B		2	2	2	2	5	nA MAX
Input Voltage Range	IVR		±13	±13	±13	±13	±13	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	100	104	100	104	84	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 15V$	10	7	10	7	63	μV/V MAX
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	±13	±13	±13	±13	±13	V MIN
		$R_L \geq 2k\Omega$	—	±10	—	±10	±10	
		$R_L \geq 5k\Omega$	±10	—	±10	—	—	
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 10k\Omega$, $V_O = \pm 10V$	80	80	80	80	40	V/mV MIN
		$R_L \geq 2k\Omega$, $V_O = \pm 10V$	—	50	—	50	—	
		$R_L \geq 5k\Omega$, $V_O = \pm 10V$	40	—	40	—	—	
Input Resistance	R_{IN}	(Note 1)	26	26	26	26	10	MΩ MIN
Supply Current	I_{SY}	$I_{OUT} = 0$ $V_{OUT} = 0$	0.6	0.6	0.6	0.6	0.8	mA MAX

NOTES:
1. Guaranteed by design.
2. For 25°C specifications of OP-12NT and OP-12GT, see OP-12N and OP-12G, respectively.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-12NT TYPICAL	OP-12N TYPICAL	OP-12GT TYPICAL	OP-12G TYPICAL	OP-12GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}		0.5	0.5	1.0	1.0	1.5	μV/°C
Average Input Offset Current Drift	TCI_{OS}		0.5	0.5	1.0	1.0	1.0	pA/°C

OP-15/OP-16/OP-17

PRECISION JFET-INPUT OPERATIONAL AMPLIFIERS

FEATURES (All Devices)

- **Significant Performance Advantages over LF155, 156 and 157 Devices.**
- **Low Input Offset Voltage .... $500\mu V$ Max**
- **Low Input Offset Voltage Drift .... $2.0\mu V/°C$**
- **Minimum Slew Rate Guaranteed on All Models**
- **Temperature-Compensated Input Bias Currents**
- **Guaranteed Input Bias Current @ 125°C**
- **Bias Current Specified WARMED UP Over Temperature**
- **Internal Compensation**
- **Low Input Noise Current .... $0.01pA/\sqrt{Hz}$**
- **High Common-Mode Rejection Ratio 100dB**
- **Models With MIL-STD-883 Class B Processing Available**
- **125°C Temperature Tested DICE**

OP-15

- **156 Speed With 155 Dissipation .... (80mW Typ)**
- **Wide Bandwidth 6MHz**
- **High Slew Rate .... $13V/\mu s$**
- **Fast Settling to ±0.1% 1200ns**

OP-16

- **Higher Slew Rate .... $25V/\mu s$**
- **Faster Settling to ±0.1% 900ns**
- **Wider Bandwidth 8MHz**

OP-17

- **Highest Slew Rate .... $60V/\mu s$**
- **Fastest Settling to ±0.1% 600ns**
- **Highest Gain Bandwidth Product 30MHz**

GENERAL DESCRIPTION

The PMI BIFET series of devices offer clear advantages over industry-generic BIFET's and are superior in both cost and performance to many dielectrically-isolated and hybrid op-amps. All devices offer offset voltages as low as 0.5mV with TCV_{OS} guaranteed to $5\mu V/°C$. A unique input bias cancellation circuit reduces the I_B by a factor of 10 over conventional designs. In addition, PMI specifies I_B and I_{OS} with the devices warmed up and operating at 25°C ambient.

These devices were designed to provide real precision performance along with high speed. Although they can be nulled, the design objective was to provide low offset-voltage without nulling. Systems generally become more cost effective as the number of trim circuits is decreased. PMI achieves this performance by use of an improved BIFET process coupled with on-chip, zener-zap offset trimming.

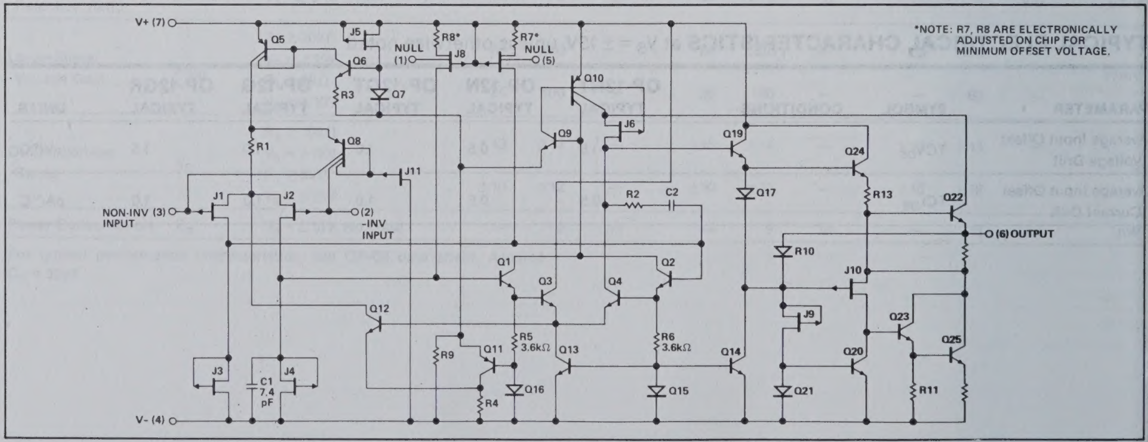
The OP-15 provides an excellent combination of high speed and low input offset voltage. In addition, the OP-15 offers the speed of the 156A op amp with the power dissipation of a 155A. The combination of a low input offset voltage of $500\mu V$, slew rate of $13V/\mu s$, and settling time of 1200ns to 0.1% makes the OP-15 an op amp of both precision and speed. The additional features of low supply current coupled with an input bias current of 9nA at 125°C ambient (not junction) temperature makes the OP-15 ideal for a wide range of applications.

The OP-16 features a slew rate of $25V/\mu s$ and a settling time of 900ns to 0.1% which represents a significant improvement in speed over the 156. Also, the OP-16 has all the DC features of the OP-15.

The OP-17 has a slew rate of $60V/\mu s$ and is the best choice for applications requiring high closed-loop gain with high speed. Applications include high-speed amplifiers for current output DACs, active filters, sample-and-hold buffers, and photocell amplifiers.

See the OP-215 data sheet for a dual configuration of the OP-15.

SIMPLIFIED SCHEMATIC



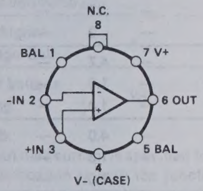
ORDERING INFORMATION†

T_A = 25° C V_{OS} MAX (mV)	PACKAGE TO-99 8-PIN	PACKAGE 8-PIN HERMETIC DIP	OPERATING TEMPERATURE RANGE
0.5	OP15AJ* OP16AJ* OP17AJ*	OP15AZ* OP16AZ* OP17AZ*	MIL
0.5	OP15EJ OP16EJ OP17EJ	OP15EZ OP16EZ OP17EZ	COM
1.0	OP15BJ* OP16BJ* OP17BJ*	OP15BZ* OP16BZ* OP17BZ*	MIL
1.0	OP15FJ OP16FJ OP17FJ	OP15FZ OP16FZ OP17FZ	COM
3.0	OP15CJ* OP16CJ* OP17CJ*	OP15CZ* OP16CZ* OP17CZ*	MIL
3.0	OP15GJ OP16GJ OP17GJ	OP15GZ OP16GZ OP17GZ	COM

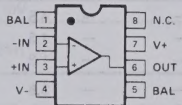
Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

PIN CONNECTIONS



TO-99 (J-Suffix)



8-PIN HERMETIC DIP (Z-Suffix)

ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage
- All Devices Except C, G (Packaged) & GR Grades . . ±22V
- C, G (Packaged) & GR Grades .... ±18V

Internal Power Dissipation (Note 1) 500mW

Operating Temperature
- A, B, & C Grades .... −55° C to +125° C
- E, F & G Grades .... 0° C to +70° C

Maximum Junction Temperature .... +150° C

DICE Junction Temperature (T_j) .... −65° C to +150° C

Differential Input Voltage
- All Devices Except C, G (Packaged) & GR Grades . . ±40V
- C, G (Packaged) & GR Grades .... ±30V

Input Voltage (Note 3)
- All Devices Except C, G (Packaged) & GR Grades . . ±20V
- C, G (Packaged) & GR Grades .... ±16V

Input Voltage
- OP-15A, OP-15B, OP-15E, OP-15F .... ±20V
- OP-15C, OP-15G .... ±16V
- OP-16A, OP-16B, OP-16E, OP-16F .... ±20V
- OP-16C, OP-16G .... ±16V
- OP-17A, OP-17B, OP-17E, OP-17F .... ±20V
- OP-17C, OP-17G .... ±16V

Output Short-Circuit Duration .... Indefinite

Storage Temperature Range .... −65° C to +150° C

Lead Temperature Range (Soldering, 60 sec) .... +300° C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80° C	7.1mW/° C
Hermetic 8-Pin Dip (Z)	75° C	6.7mW/° C

2. Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.
3. Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS		OP-15A/E OP-16A/E OP-17A/E MIN	TYP	MAX	OP-15B/F OP-16B/F OP-17B/F MIN	TYP	MAX	OP-15C/G OP-16C/G OP-17C/G MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$		—	0.2	0.5	—	0.4	1.0	—	0.5	3.0	mV
Input Offset Current	I_{OS}	$T_j = 25°C$ (Note 1)	OP-15	—	3	10	—	6	20	—	12	50	pA
		Device Operating		—	5	22	—	10	40	—	20	100	
		$T_j = 25°C$ (Note 1)	OP-016/OP-17	—	3	10	—	6	20	—	12	50	
		Device Operating		—	5	25	—	10	50	—	20	125	
Input Bias Current	I_B	$T_j = 25°C$ (Note 1)	OP-15	—	±15	±50	—	±30	±100	—	±60	±200	pA
		Device Operating		—	±18	±110	—	±40	±200	—	±80	±400	
		$T_j = 25°C$ (Note 1)	OP-16/OP-17	—	±15	±50	—	±30	±100	—	±60	±200	
		Device Operating		—	±20	±130	—	±40	±250	—	±80	±500	
Input Resistance	R_{IN}			—	10^{12}	—	—	10^{12}	—	—	10^{12}	—	Ω
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm10V$		100	240	—	75	220	—	50	200	—	V/mV
Output Voltage Swing	V_O	$R_L = 10k\Omega$		±12	±13	—	±12	±13	—	±12	±13	—	V
		$R_L = 2k\Omega$		±11	±12.7	—	±11	±12.7	—	±11	±12.7	—	
Supply Current	I_{SY}		OP-15	—	2.7	4.0	—	2.7	4.0	—	2.8	5.0	mA
			OP-16/OP-17	—	4.6	7.0	—	4.6	7.0	—	4.8	8.0	
Slew Rate	SR	$A_{VCL} = +1$ (Note 3)	OP-15	10	13	—	7.5	11	—	5	9	—	V/μs
			OP-16	18	25	—	12	21	—	9	17	—	
		$A_{VCL} = +5$ (Note 3)	OP-17	45	60	—	35	50	—	25	40	—	
Gain Bandwidth Product	GBW	(Note 3)	OP-15	4.0	6.0	—	3.5	5.7	—	3.0	5.4	—	MHz
			OP-16	6.0	8.0	—	5.5	7.6	—	5.0	7.2	—	
			OP-17	20	30	—	15	28	—	11	26	—	
Closed-Loop Bandwidth	CLBW	$A_{VCL} = +1$	OP-15	—	14	—	—	13	—	—	12	—	MHz
			OP-16	—	19	—	—	18	—	—	17	—	
		$A_{VCL} = +5$	OP-17	—	11	—	—	10	—	—	9	—	
Settling Time	t_S	to 0.01%	OP-15	—	4.5	—	—	4.5	—	—	4.7	—	μs
		to 0.05% (Note 2)		—	1.5	—	—	1.5	—	—	1.6	—	
		to 0.10%		—	1.2	—	—	1.2	—	—	1.3	—	
		to 0.01%	OP-16	—	3.8	—	—	3.8	—	—	4.0	—	
		to 0.05% (Note 2)		—	1.2	—	—	1.2	—	—	1.3	—	
		to 0.10%		—	0.9	—	—	0.9	—	—	1.0	—	
		to 0.01%	OP-17	—	1.5	—	—	1.5	—	—	1.6	—	
		to 0.05% (Note 4)		—	0.7	—	—	0.7	—	—	0.8	—	
		to 0.10%		—	0.6	—	—	0.6	—	—	0.7	—	
Input Voltage Range	IVR			±10.5	—	—	±10.5	—	—	±10.3	—	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm10.5V$		86	100	—	86	100	—	—	—	—	dB
		$V_{CM} = \pm10.3V$		—	—	—	—	—	—	82	96	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm10V$ to $\pm18V$		—	10	51	—	10	51	—	—	—	μV/V
		$V_S = \pm10V$ to $\pm15V$		—	—	—	—	—	—	—	10	80	
Input Noise Voltage Density	e_n	$f_O = 100Hz$		—	20	—	—	20	—	—	20	—	$nV/\sqrt{Hz}$
		$f_O = 1000Hz$		—	15	—	—	15	—	—	15	—	
Input Noise Current Density	i_n	$f_O = 100Hz$		—	0.01	—	—	0.01	—	—	0.01	—	$pA/\sqrt{Hz}$
		$f_O = 1000Hz$		—	0.01	—	—	0.01	—	—	0.01	—	
Input Capacitance	C_{IN}			—	3	—	—	3	—	—	3	—	pF

NOTES:

1. Input bias current is specified for two different conditions. The $T_j = 25°C$ specification is with the junction at ambient temperature; the Device Operating specification is with the device operating in a warmed-up condition at 25° C ambient. The warmed-up bias current value is correlated to the junction temperature value via the curves of I_B vs T_j and I_B vs T_A. PMI has a bias current compensation circuit which gives improved bias current over the standard JFET input op amps. I_B and I_{OS} are measured at $V_{CM} = 0$.
2. Settling time is defined here for a unity gain inverter connection using 2kΩ resistors. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within a specified percent of its final value from the time a 10V step input is applied to the inverter. See settling time test circuit.
3. Sample tested.
4. Settling time is defined here for a $A_V = -5$ connection with $R_F = 2k\Omega$. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 2V step input is applied to the inverter. See settling time test circuit.

ELECTRICAL CHARACTERISTICS $V_S = \pm15V, -55°C \le T_A \le 125°C$, unless otherwise noted.

ARAMETER	SYMBOL	CONDITIONS		OP-15A OP-16A OP-17A MIN	TYP	MAX	OP-15B OP-16B OP-17B MIN	TYP	MAX	OP-15C OP-16C OP-17C MIN	TYP	MAX	UNITS
nput Offset Voltage	V_{OS}	$R_S = 50\Omega$		—	0.4	0.9	—	0.7	2.0	—	0.9	4.5	mV
verage Input Offset Voltage Drift		(Note 2)											
Without External Trim	TCV_{OS}			—	2	5	—	3	10	—	4	15	µV/°C
With External Trim	TCV_{OSn}	$R_P = 100k\Omega$		—	2	—	—	3	—	—	4	—	
nput Offset Current (Note 1)	I_{OS}	$T_j = 125°C$	OP-15	—	0.6	4.0	—	0.8	6.0	—	1.0	9.0	nA
		$T_A = 125°C$ Device Operating		—	0.8	7.0	—	1.2	11	—	1.5	17	
		$T_j = 125°C$	OP-16/OP-17	—	0.6	4.0	—	0.8	6.0	—	1.0	9.0	
		$T_A = 125°C$ Device Operating		—	1.0	8.5	—	1.3	14.5	—	1.7	22	
nput Bias Current (Note 1)	I_B	$T_j = 125°C$	OP-15	—	±1.2	±5.0	—	±1.5	±7.5	—	±1.8	±10	nA
		$T_A = 125°C$ Device Operating		—	±1.7	±9.0	—	±2.2	±14	—	±2.7	±19	
		$T_j = 125°C$	OP-16/OP-17	—	±1.2	±5.0	—	±1.5	±7.5	—	±1.8	±10	
		$T_A = 125°C$ Device Operating		—	±2.0	±11	—	±2.5	±18	—	±3.0	±25	
nput Voltage Range	IVR			±10.4	—	—	±10.4	—	—	±10.25	—	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm10.4V$		85	97	—	85	97	—	—	—	—	dB
		$V_{CM} = \pm10.25V$		—	—	—	—	—	—	80	93	—	
ower Supply Rejection Ratio	PSRR	$V_S = \pm10V$ to $\pm18V$		—	15	57	—	15	57	—	—	—	µV/V
		$V_S = \pm10V$ to $\pm15V$		—	—	—	—	—	—	—	23	100	
arge-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$ $V_O = \pm10V$		35	120	—	30	110	—	25	100	—	V/mV
utput Voltage Swing	V_O	$R_L \ge 10k\Omega$		±12	±13	—	±12	±13	—	±12	±13	—	V

NOTES:

1. Input bias current is specified for two different conditions. The $T_j = 25°C$ specification is with the junction at ambient temperature; the Device Operating specification is with the device operating in a warmed-up condition at 25°C ambient. The warmed-up bias current value is correlated to the junction temperature value via the curves of I_B vs T_j and I_B vs T_A. PMI has a bias current compensation circuit which gives improved bias current over the standard JFET input op amps. I_B and I_{OS} are measured at $V_{CM} = 0$.
2. Sample tested.

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $-0°C \le T_A \le 70°C$, unless otherwise noted.

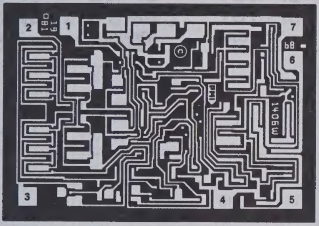
					OP-15E OP-16E OP-17E			OP-15F OP-16F OP-17F			OP-15G OP-16G OP-17G		
PARAMETER	**SYMBOL**	**CONDITIONS**		**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$		—	0.3	0.75	—	0.55	1.5	—	0.7	3.8	mV
Average Input Offset Voltage Drift											(Note 2)		
Without External Trim	TCV_{OS}			—	2	5	—	3	10	—	4	15	µV/°C
With External Trim	TCV_{OSn}	$R_P = 100k\Omega$		—	2	—	—	3	—	—	4	—	
Input Offset Current (Note 1)	I_{OS}	$T_j = 70°C$	OP-15	—	0.04	0.30	—	0.06	0.45	—	0.08	0.65	nA
		$T_A = 70°C$ Device Operating		—	0.06	0.55	—	0.08	0.80	—	0.10	1.2	
		$T_j = 70°C$	OP-16/OP-17	—	0.04	0.30	—	0.06	0.45	—	0.08	0.65	
		$T_A = 70°C$ Device Operating		—	0.07	0.70	—	0.10	1.1	—	0.15	1.7	
Input Bias Current (Note 1)	I_B	$T_j = 70°C$	OP-15	—	±0.10	±0.40	—	±0.12	±0.60	—	±0.14	±0.80	nA
		$T_A = 70°C$ Device Operating		—	±0.13	±0.75	—	±0.16	±1.1	—	±0.19	±1.5	
		$T_j = 70°C$	OP-16/OP-17	—	±0.10	±0.40	—	±0.12	±0.60	—	±0.14	±0.80	
		$T_A = 70°C$ Device Operating		—	±0.15	±0.90	—	±0.20	±1.4	—	±0.25	±2.0	
Input Voltage Range	IVR			±10.4	—	—	±10.4	—	—	±10.25	—	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10.4V$		85	98	—	85	98	—	—	—	—	dB
		$V_{CM} = \pm 10.25V$		—	—	—	—	—	—	80	94	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 18V$		—	13	57	—	13	57	—	—	—	µV/V
		$V_S = \pm 10V$ to $\pm 15V$		—	—	—	—	—	—	—	20	100	
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$ $V_O = \pm 10V$		65	200	—	50	180	—	35	160	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 10k\Omega$		±12	±13	—	±12	±13	—	±12	±13	—	V

NOTES:

1. Input bias current is specified for two different conditions. The $T_j = 25°C$ specification is with the junction at ambient temperature; the Device Operating specification is with the device operating in a warmed-up condition at 25°C ambient. The warmed-up bias current value is correlated to the junction temperature value via the curves of I_B vs T_j and I_B vs T_A. PMI has a bias current compensation circuit which gives improved bias current over the standard JFET input op amps. I_B and I_{OS} are measured at $V_{CM} = 0$.
2. Sample tested.

DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)

OP-15/OP-16

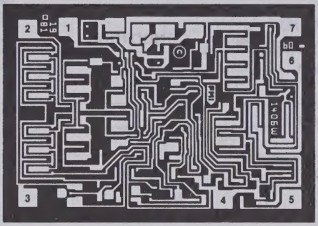


DIE SIZE 0.064 × 0.045 inch, 2880 sq. mils
(1.63 × 1.14mm, 1.86 sq. mm)

1. BALANCE
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V−
5. BALANCE
6. OUTPUT
7. V+

For additional DICE information refer to Section 2.

OP-17



DIE SIZE 0.064 × 0.045 inch, 2880 sq. mils
(1.63 × 1.14mm, 1.86 sq. mm)

1. BALANCE
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V−
5. BALANCE
6. OUTPUT
7. V+

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$ for OP-15/16/17N, OP-15/16/17G and OP-15/16/17GR devices; $T_A = 125°C$ for OP-15/16/17NT and OP-15/16/17GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-15NT OP-16NT OP-17NT LIMIT	OP-15N OP-16N OP-17N LIMIT	OP-15GT OP-16GT OP-17GT LIMIT	OP-15G OP-16G OP-17G LIMIT	OP-15GR OP-16GR OP-17GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	0.9	0.5	2.0	1.0	3.0	mV MAX
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$ $R_L = 2k\Omega$	35	100	30	75	50	V/mV MIN
Input Voltage Range	IVR		±10.4	±10.5	±10.4	±10.5	±10.3	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm IVR$	85	86	85	86	82	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 20V$ $V_S = \pm 10V$ to $\pm 15V$	57 —	51 —	57 —	51 —	— 80	μV/V MAX
Output Voltage Swing	V_O	$R_L = 10k\Omega$ $R_L = 2k\Omega$	±12 —	±12 ±11	±12 —	±12 ±11	±12 ±11	V MIN
Supply Current	I_{SY}	OP-15 OP-16, OP-17	— —	4 7	— —	4 7	5 8	mA MAX
Input Bias Current	I_B	OP-15 OP-16, OP-17	±9 ±11	— —	±14 ±18	— —	— —	nA MAX
Input Offset Current	I_{OS}	OP-15 OP-16, OP-17	7.0 8.5	— —	11.0 14.5	— —	— —	nA MAX

NOTE: For 25° C characteristics of OP-15/16/17NT and OP-15/16/17GT, see OP-15/16/17N and OP-15/16/17G characteristics, respectively.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

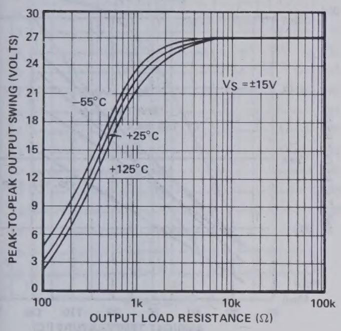
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS		OP-15NT OP-16NT OP-17NT TYPICAL	OP-15N OP-16N OP-17N TYPICAL	OP-15GT OP-16GT OP-17GT TYPICAL	OP-15G OP-16G OP-17G TYPICAL	OP-15GR OP-16GR OP-17GR TYPICAL	UNITS
Average Input Offset Drift Unnulled	TCV_{OS}			2	2	3	3	4	μV/°C
Average Input Offset Drift Nulled	TCV_{OSn}	$R_P = 100k\Omega$		2	2	3	3	4	μV/°C
Input Offset Current	I_{OS}			3	3	3	3	3	pA
Input Bias Current	I_B			±15	±15	±15	±15	±15	pA
Slew Rate	SR	$A_{VCL} = +1$	OP-15	13	13	11	11	9	V/μs
			OP-16	25	25	21	21	17	
		$A_{VCL} = +5$	OP-17	60	60	50	50	40	
Settling Time (see settling time test circuits)	t_S	to 0.01%	OP-15	4.5	4.5	4.5	4.5	4.7	μs
		to 0.05%		1.5	1.5	1.5	1.5	1.6	
		to 0.10%		1.2	1.2	1.2	1.2	1.3	
		to 0.01%	OP-16	3.8	3.8	3.8	3.8	4.0	
		to 0.05%		1.2	1.2	1.2	1.2	1.3	
		to 0.10%		0.9	0.9	0.9	0.9	1.0	
		to 0.01%	OP-17	1.5	1.5	1.5	1.5	1.6	
		to 0.05%		0.7	0.7	0.7	0.7	0.8	
		to 0.10%		0.6	0.6	0.6	0.6	0.7	
Gain Bandwidth Product	GBW		OP-15	6.0	6.0	5.7	5.7	5.4	MHz
			OP-16	8.0	8.0	7.6	7.6	7.2	
			OP-17	30	30	28	28	26	
Closed-Loop Bandwidth	CLBW	$A_{VCL} = +1$	OP-15	14	14	13	13	12	MHz
			OP-16	19	19	18	18	17	
		$A_{VCL} = +5$	OP-17	11	11	10	10	9	
Input Noise Voltage Density	e_n	f = 100Hz		20	20	20	20	20	$nV/\sqrt{Hz}$
		f = 1000Hz		15	15	15	15	15	
Input Noise Current Density	i_n	f = 100Hz		0.01	0.01	0.01	0.01	0.01	$pA/\sqrt{Hz}$
		f = 1000Hz		0.01	0.01	0.01	0.01	0.01	
Input Capacitance	C_{IN}			3	3	3	3	3	pF

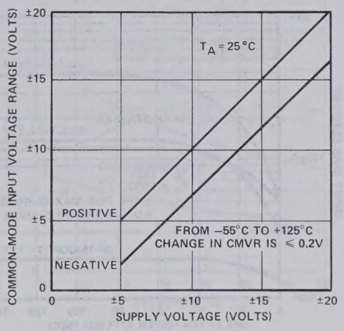
NOTE: For 25°C characteristics of OP-15/16/17NT and OP-15/16/17GT, see OP-15/16/17N and OP-15/16/17G characteristics, respectively.

TYPICAL PERFORMANCE CHARACTERISTICS (OP-15/OP-16/OP-17)

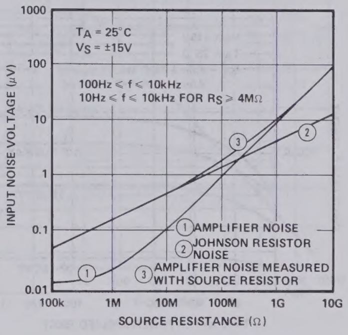
MAXIMUM OUTPUT SWING vs LOAD RESISTANCE



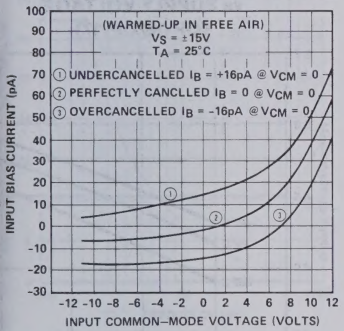
COMMON-MODE INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE



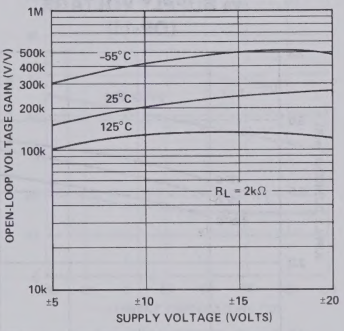
VOLTAGE NOISE vs SOURCE RESISTANCE



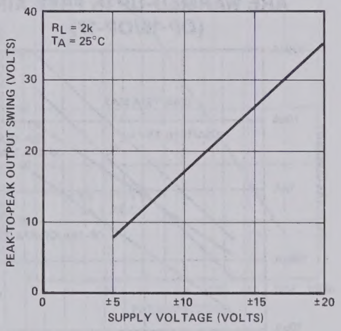
INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE



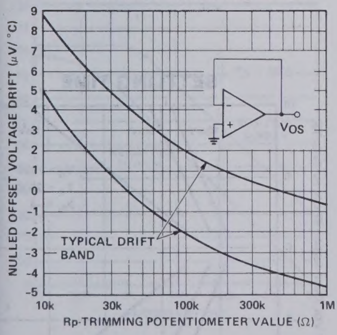
OPEN-LOOP VOLTAGE GAIN vs SUPPLY VOLTAGE



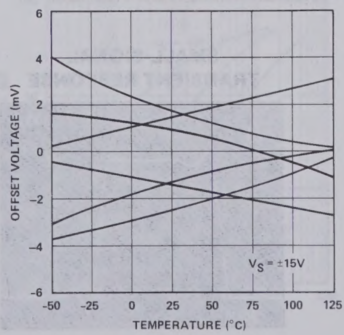
OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE



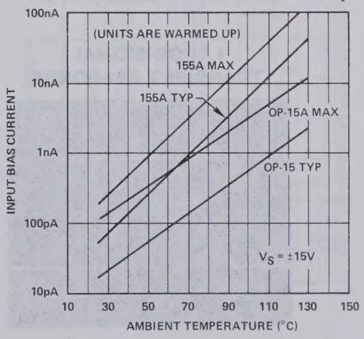
NULLED OFFSET VOLTAGE DRIFT vs POTENTIOMETER SIZE



OFFSET VOLTAGE DRIFT vs TEMPERATURE OF REPRESENTATIVE UNITS

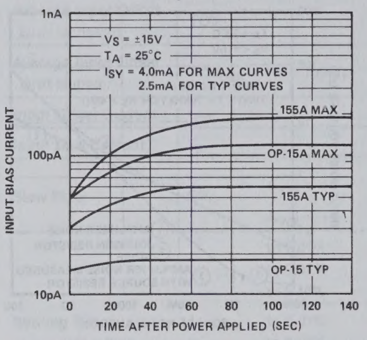


INPUT BIAS CURRENT vs AMBIENT TEMPERATURE (UNITS ARE WARMED-UP IN FREE AIR)

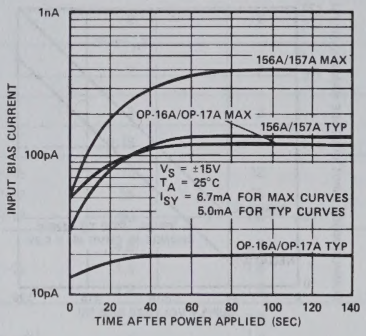


TYPICAL PERFORMANCE CHARACTERISTICS (OP-15/OP-16/OP-17)

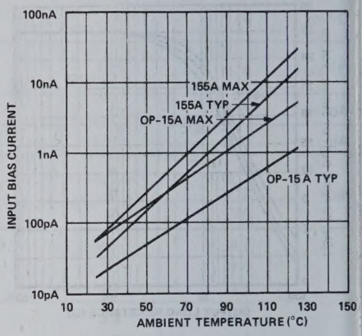
BIAS CURRENT vs TIME IN FREE AIR (OP-15)



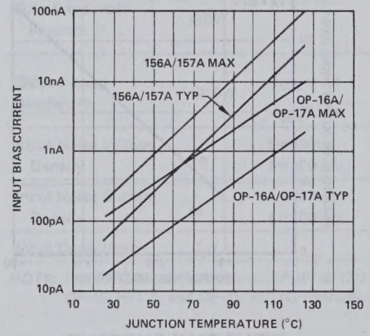
BIAS CURRENT vs TIME IN FREE AIR (OP-16/OP-17)



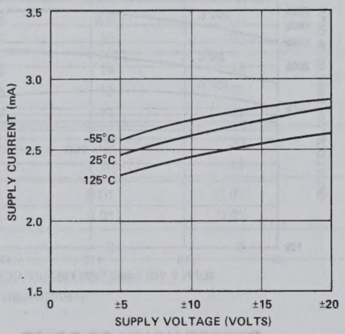
INPUT BIAS CURRENT vs AMBIENT TEMPERATURE (UNITS ARE WARMED-UP IN FREE AIR) (OP-15)



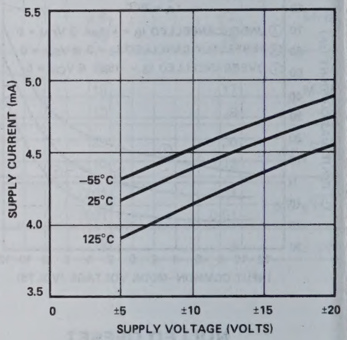
INPUT BIAS CURRENT vs AMBIENT TEMPERATURE (UNITS ARE WARMED-UP IN FREE AIR) (OP-16/OP-17)



SUPPLY CURRENT vs SUPPLY VOLTAGE (OP-15)

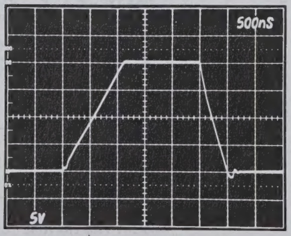


SUPPLY CURRENT vs SUPPLY VOLTAGE (OP-16/OP-17)

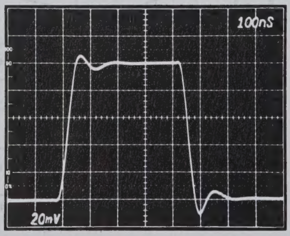


TYPICAL PERFORMANCE CHARACTERISTICS (OP-15)

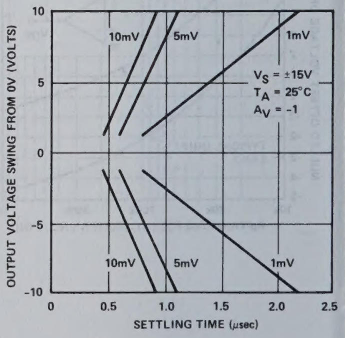
LARGE-SIGNAL TRANSIENT RESPONSE



SMALL-SIGNAL TRANSIENT RESPONSE

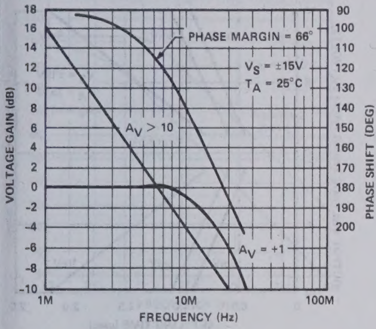


SETTLING TIME

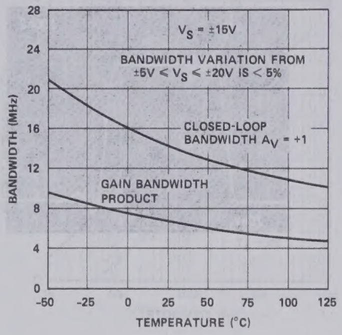


TYPICAL PERFORMANCE CHARACTERISTICS (OP-15)

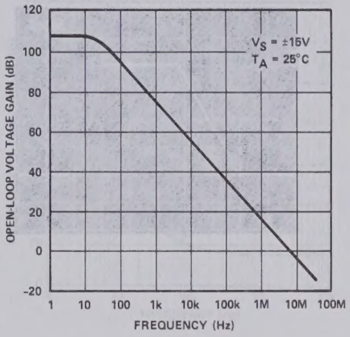
CLOSED-LOOP BANDWIDTH AND PHASE SHIFT vs FREQUENCY



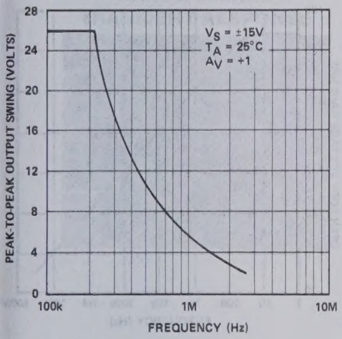
BANDWIDTH vs TEMPERATURE



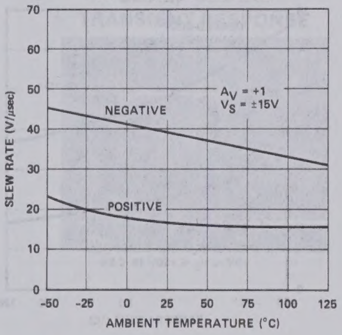
OPEN-LOOP GAIN vs FREQUENCY



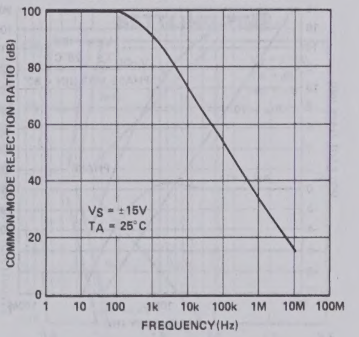
MAXIMUM OUTPUT SWING vs FREQUENCY



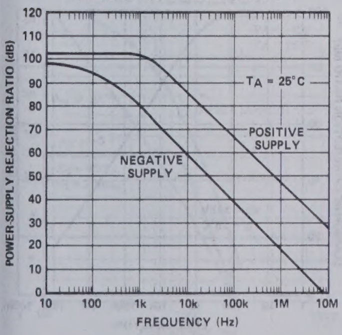
SLEW RATE vs TEMPERATURE



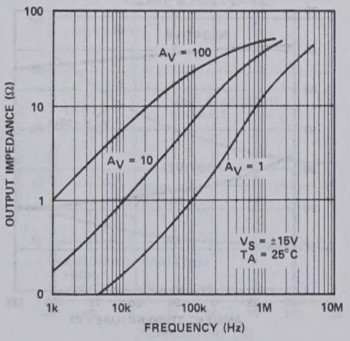
COMMON-MODE REJECTION RATIO vs FREQUENCY



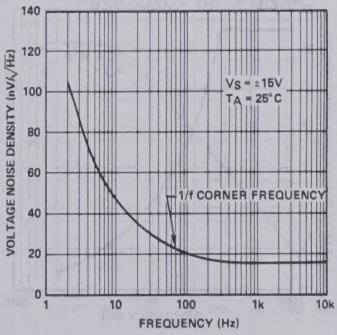
POWER-SUPPLY REJECTION RATIO vs FREQUENCY



OUTPUT IMPEDANCE vs FREQUENCY

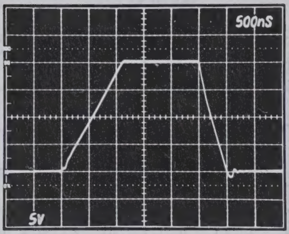


VOLTAGE NOISE DENSITY vs FREQUENCY

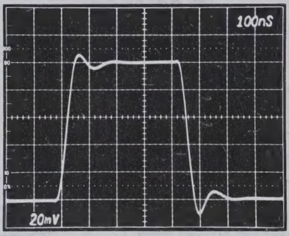


TYPICAL PERFORMANCE CHARACTERISTICS (OP-16)

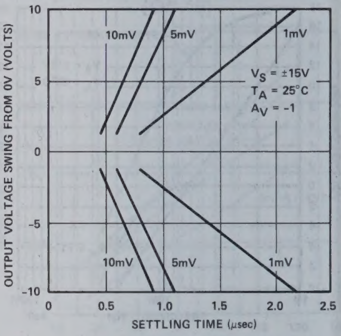
LARGE-SIGNAL TRANSIENT RESPONSE



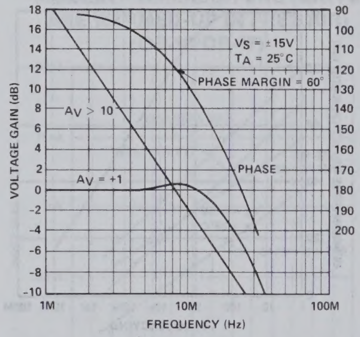
SMALL-SIGNAL TRANSIENT RESPONSE



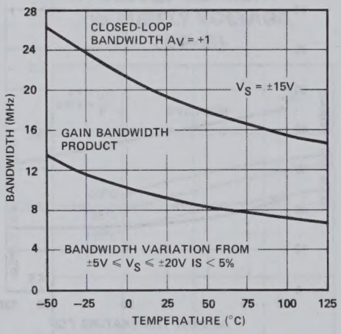
SETTLING TIME



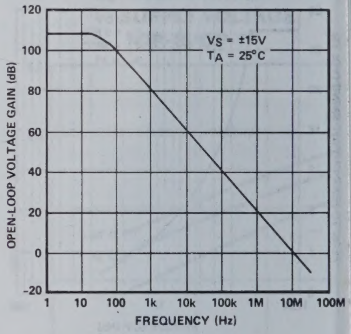
CLOSED-LOOP BANDWIDTH AND PHASE SHIFT vs FREQUENCY



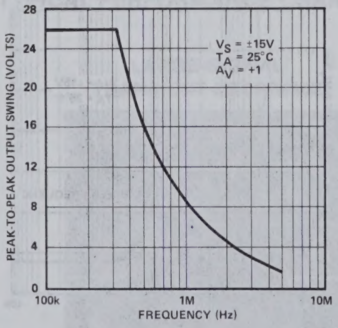
BANDWIDTH vs TEMPERATURE



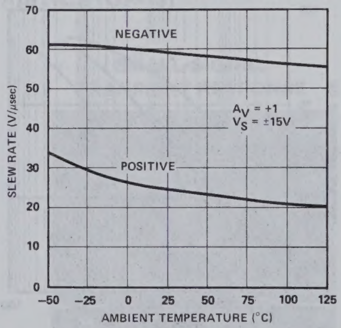
OPEN-LOOP GAIN vs FREQUENCY



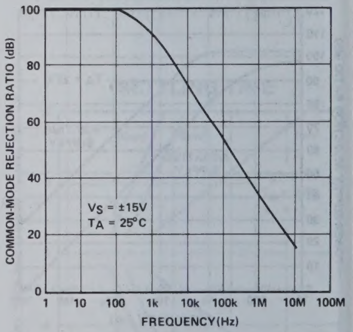
MAXIMUM OUTPUT SWING vs FREQUENCY



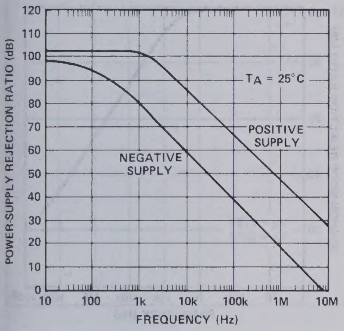
SLEW RATE vs TEMPERATURE

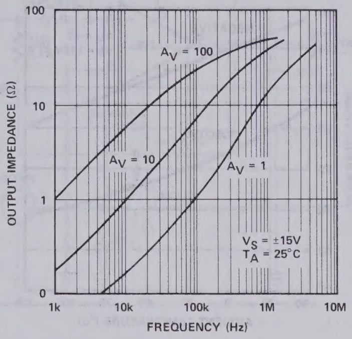


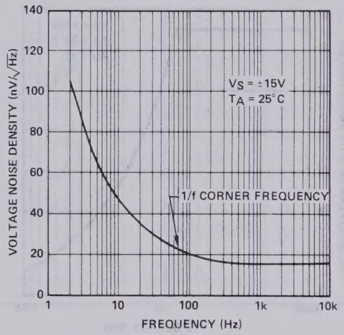
COMMON-MODE REJECTION RATIO vs FREQUENCY



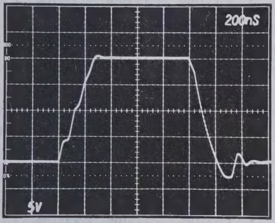
TYPICAL PERFORMANCE CHARACTERISTICS (OP-16)

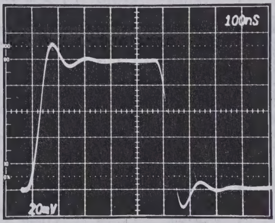

POWER-SUPPLY REJECTION RATIO vs FREQUENCY

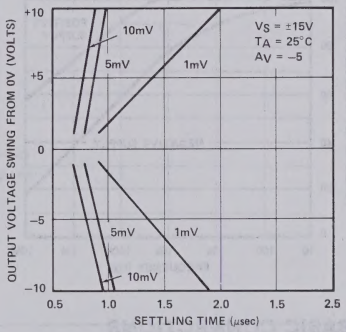

OUTPUT IMPEDANCE vs FREQUENCY

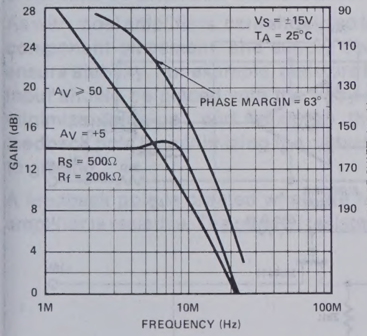

VOLTAGE NOISE DENSITY vs FREQUENCY

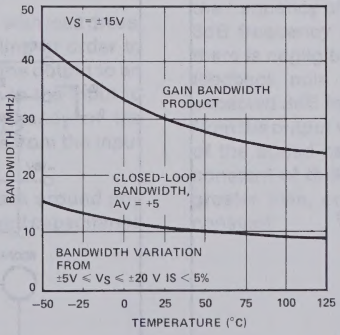
TYPICAL PERFORMANCE CHARACTERISTICS (OP-17)

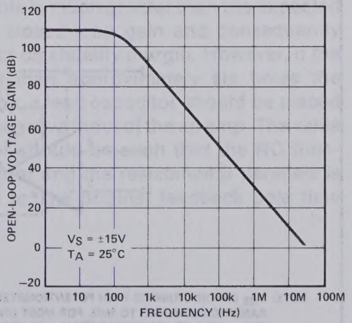

LARGE-SIGNAL TRANSIENT RESPONSE


SMALL-SIGNAL TRANSIENT RESPONSE

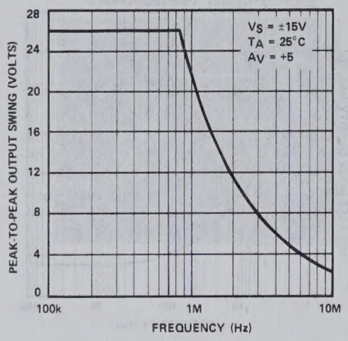

SETTLING TIME

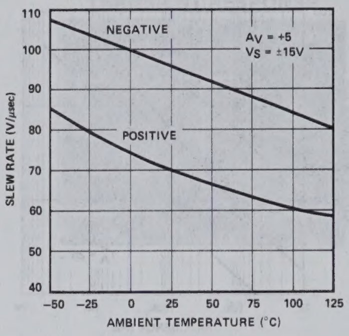

CLOSED-LOOP BANDWIDTH AND PHASE SHIFT vs FREQUENCY

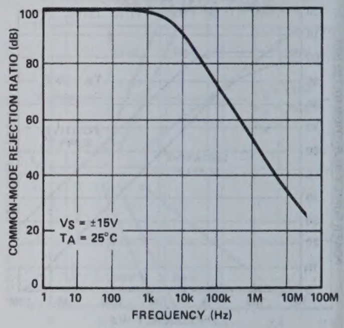

BANDWIDTH vs TEMPERATURE

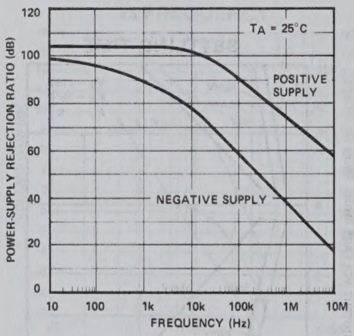

OPEN-LOOP FREQUENCY RESPONSE

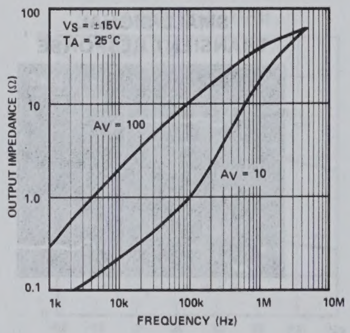
TYPICAL PERFORMANCE CHARACTERISTICS (OP-17)

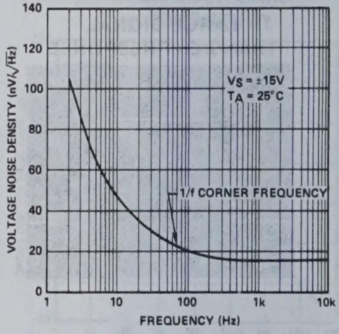

MAXIMUM OUTPUT SWING vs FREQUENCY


SLEW RATE vs TEMPERATURE


COMMON-MODE REJECTION RATIO vs FREQUENCY

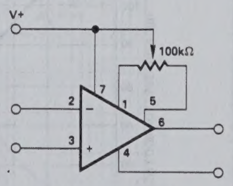

POWER-SUPPLY REJECTION RATIO vs FREQUENCY


OUTPUT IMPEDANCE vs FREQUENCY


VOLTAGE NOISE vs FREQUENCY

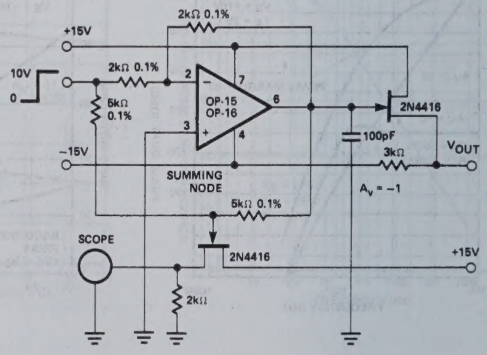
BASIC CONNECTIONS

INPUT OFFSET VOLTAGE NULLING

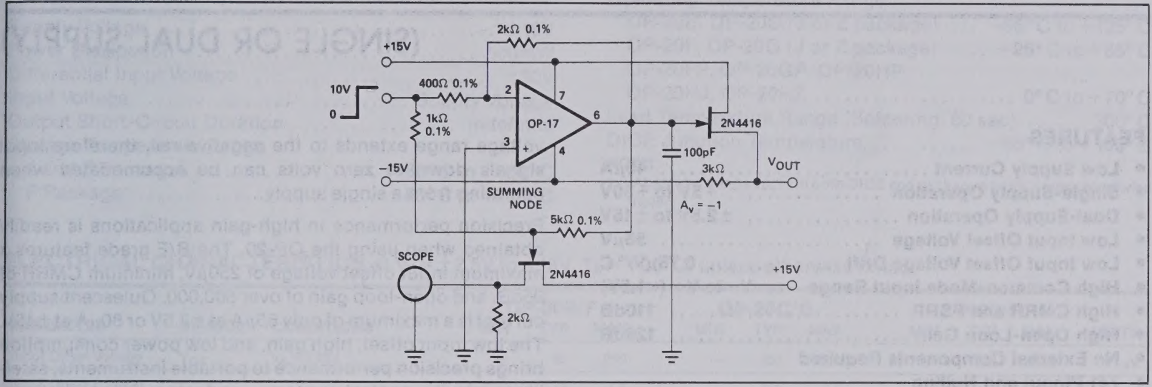

V+
100kΩ
7
1
5
2
−
3
+
4
6

NOTE: V_{OS} CAN BE TRIMMED WITH POTENTIOMETERS RANGING FROM 10kΩ TO 1MΩ. FOR MOST UNITS TCV_{OS} WILL BE MINIMUM WHEN V_{OS} IS ADJUSTED WITH A 100kΩ POTENTIOMETER.

SETTLING-TIME TEST CIRCUIT — OP-15/OP-16

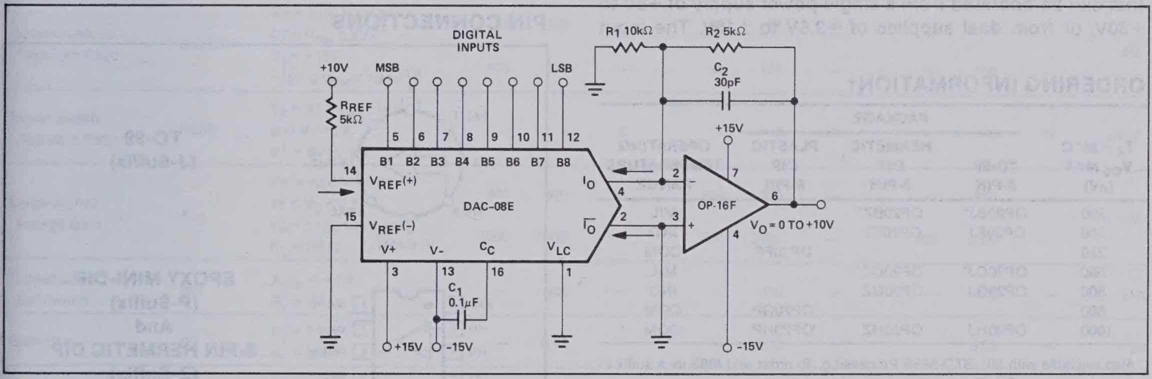

2kΩ 0.1%
+15V
10V
0
2kΩ 0.1%
5kΩ
0.1%
2
7
OP-15
OP-16
6
3
4
2N4416
100pF
−15V
3kΩ
VOUT
SUMMING NODE
Av = −1
5kΩ 0.1%
SCOPE
2N4416
+15V
2kΩ

SETTLING-TIME TEST CIRCUIT — OP-17


+15V
2kΩ 0.1%
10V
0
400Ω 0.1%
1kΩ
0.1%
2
7
OP-17
6
3
4
2N4416
100pF
3kΩ
VOUT
Av = −1
−15V
SUMMING
NODE
5kΩ 0.1%
SCOPE
2N4416
+15V
2kΩ

TYPICAL APPLICATIONS

CURRENT-TO-VOLTAGE AMPLIFIER OUTPUT


DIGITAL
INPUTS
+10V
MSB
LSB
RREF
5kΩ
5 6 7 8 9 10 11 12
B1 B2 B3 B4 B5 B6 B7 B8
14
VREF(+)
DAC-08E
15
VREF(−)
V+
V-
CC
VLC
IO
I̅O̅
4
2
3
13
16
1
C1
0.1µF
+15V
−15V
R1 10kΩ
R2 5kΩ
C2
30pF
+15V
2
7
OP-16F
6
3
4
VO = 0 TO +10V
-15V

APPLICATIONS INFORMATION

DYNAMIC OPERATING CONSIDERATIONS

As with most amplifiers, care should be taken with lead dress, component placement, and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3dB frequency of the closed-loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3dB frequency, a lead capacitor should be placed from the output to the negative input of the op amp. The value of the added capacitor should be such that the RC time-constant of this capacitor and the resistance it parallels is greater than, or equal to, the original feedback pole time constant.

OP-20

MICROPOWER OPERATIONAL AMPLIFIER (SINGLE OR DUAL SUPPLY)

FEATURES

- **Low Supply Current 40μA**
- **Single-Supply Operation .... +5V to +30V**
- **Dual-Supply Operation .... ±2.5V to ±15V**
- **Low Input Offset Voltage 55μV**
- **Low Input Offset Voltage Drift .... 0.75μV/°C**
- **High Common-Mode Input Range ... V− to V+ (−1.5V)**
- **High CMRR and PSRR 110dB**
- **High Open-Loop Gain 126dB**
- **No External Components Required**
- **741 Pinout and Nulling**

GENERAL DESCRIPTION

The OP-20 is a monolithic micropower operational amplifier that can be operated from a single power supply of +5V to +30V, or from dual supplies of ±2.5V to ±15V. The input voltage range extends to the negative rail, therefore input signals down to zero volts can be accomodated when operating from a single supply.

Precision performance in high-gain applications is readily obtained when using the OP-20. The B/F grade features a maximum input offset voltage of 250μV, minimum CMRR of 95dB, and open-loop gain of over 500,000. Quiescent supply current is a maximum of only 55μA at ±2.5V or 80μA at ±15V. The low input offset, high gain, and low power consumption brings precision performance to portable instruments, satellites, missile control systems, and many other battery-powered applications.

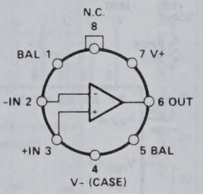
ORDERING INFORMATION†

T_A = 25°C V_{OS} MAX (μV)	PACKAGE TO-99 8-PIN	HERMETIC DIP 8-PIN	PLASTIC DIP 8-PIN	OPERATING TEMPERATURE RANGE
250	OP20BJ*	OP20BZ*		MIL
250	OP20FJ	OP20FZ		IND
250			OP20FP	COM
500	OP20CJ*	OP20CZ*		MIL
500	OP20GJ	OP20GZ		IND
500			OP20GP	COM
1000	OP20HJ	OP20HZ	OP20HP	COM

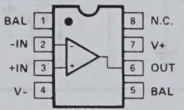
*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

PIN CONNECTIONS

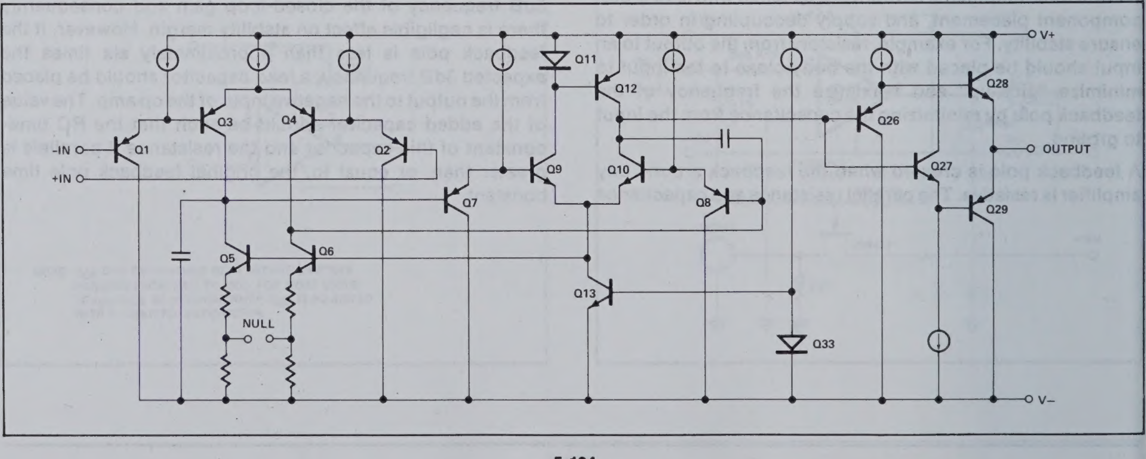


TO-99 (J-Suffix)



EPOXY MINI-DIP (P-Suffix) And 8-PIN HERMETIC DIP (Z-Suffix)

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage .... ±18V
Power Dissipation 500mW
Differential Input Voltage .... ±30V
Input Voltage .... Supply Voltage
Output Short-Circuit Duration .... Indefinite
Storage Temperature Range
  J and Z Packages .... −65° C to +150° C
  P Package .... −65° C to +125° C

Operating Temperature Range
  OP-20B, OP-20C (J or Z package) ... −55° C to +125° C
  OP-20F, OP-20G (J or Z package) .... −25° C to +85° C
  OP-20FP, OP-20GP, OP-20HP
  OP-20HJ, OP-20HZ .... 0° C to +70° C
Lead Temperature Range (Soldering, 60 sec) ...... 300° C
DICE Junction Temperature .... −65° C to +150° C

NOTE:
1. Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 2.5V$ to $\pm 15V$, $T_A = +25° C$, unless otherwise noted.

			OP-20B/F			OP-20C/G			OP-20H			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$V_S = \pm 15V$	—	55	250	—	150	500	—	300	1000	μV
Input Offset Current	I_{OS}		—	0.15	1.5	—	0.2	2.5	—	0.3	4.0	nA
Input Bias Current	I_B		—	12	25	—	14	30	—	16	40	nA
Input Voltage Range	IVR	V+ = +5V, V− = 0V	0/3.5	—	—	0/3.5	—	—	0/3.5	—	—	V
		$V_S = \pm 15V$	−15/13.5	—	—	−15/13.5	—	—	−15/13.5	—	—	
Common-Mode Rejection Ratio	CMRR	V+ = +5V, V− = 0V $0V \le V_{CM} \le 3.5V$	95	105	—	90	95	—	85	90	—	dB
		$V_S = \pm 15V$ $-15V \le V_{CM} \le 13.5V$	100	110	—	94	105	—	90	100	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$ and V− = 0V, V+ = 5V to 30V	—	4	6	—	6	10	—	10	32	μV/V
Large-Signal Voltage Gain	A_{VO}	V+ = +5V, V− = 0V $1V \le V_O \le 3.5V$	300	500	—	200	500	—	—	500	—	V/mV
		$V_S = \pm 15V$, $V_O = \pm 10V$ $R_L = 25k\Omega$	1000	2000	—	800	2000	—	500	1000	—	
Closed-Loop Bandwidth	BW	$A_{VCL} = +1.0$, $R_L = 10k\Omega$	—	100	—	—	100	—	—	100	—	kHz
Slew Rate	SR	$V_S = \pm 15V$ $R_L = 25k\Omega$	—	0.05	—	—	0.05	—	—	0.05	—	V/μs
Supply Current	I_{SY}	$V_S = \pm 2.5V$, No Load	—	40	55	—	44	63	—	45	70	μA
		$V_S = \pm 15V$, No Load	—	55	80	—	57	85	—	60	95	

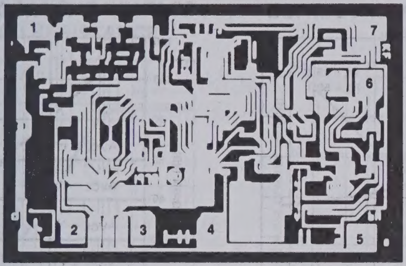
ELECTRICAL CHARACTERISTICS at $V_S = \pm 2.5V$ to $\pm 15V$, $-55°C \le T_A \le +125°C$ for OP-20BJ/BZ and OP-20CJ/CZ, $-25°C \le T_A \le +85°C$ for OP-20FJ/FZ and OP-20GJ/GZ, and $0°C \le T_A \le +70°C$ for OP-20FP, OP-20GP, OP-20HP, OP-20HZ and OP-20HJ, unless otherwise noted.

			OP-20B/F			OP-20C/G			OP-20H			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Average Input Offset Voltage Drift (Note 1)	TCV_{OS} TCV_{OSn}	Unnulled Nulled, $R_P = 10k\Omega$	—	0.75	1.5	—	1.0	3.0	—	1.5	7.0	µV/°C
Input Offset Voltage	V_{OS}	$V_S = \pm 15V$	—	155	400	—	250	800	—	500	1700	µV
Input Offset Current	I_{OS}		—	0.5	2.5	—	1.0	3.5	—	1.5	5.0	nA
Input Bias Current	I_B		—	12	27	—	14	33	—	16	45	nA
Input Voltage Range	IVR	$V+ = +5V$, $V- = 0V$	0/3.2	—	—	0/3.2	—	—	0/3.2	—	—	V
		$V_S = \pm 15V$	−15/13.2	—	—	−15/13.2	—	—	−15/13.2	—	—	
Common-Mode Rejection Ratio	CMRR	$V+ = +5V$, $V- = 0V$ $0V \le V_{CM} \le 3.2V$	90	100	—	85	90	—	80	85	—	dB
		$V_S = \pm 15V$ $-15V \le V_{CM} \le 13.2V$	96	110	—	90	105	—	85	100	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$	—	4	10	—	6	18	—	10	32	µV/V
		$V- = 0V$, $V+ = 5V$ to $30V$	—	4	10	—	6	18	—	10	57	
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $V_O = \pm 10V$ $R_L = 50k\Omega$	500	700	—	400	600	—	250	400	—	V/mV
Output Voltage Swing	V_O	$V+ = 5V$, $V- = 0V$, $R_L = 50k\Omega$	0.8/4.0	—	—	0.9/3.9	—	—	1.0/3.8	—	—	V
		$V_S = \pm 15V$, $R_L = 50k\Omega$	±14.0	—	—	±13.9	—	—	±13.9	—	—	
Supply Current	I_{SY}	$V_S = \pm 2.5V$, No Load or +5V, 0V	—	50	65	—	53	75	—	55	85	µA
		$V_S = \pm 15V$, No Load	—	64	95	—	68	100	—	72	115	

NOTE:

1. Sample tested.

DICE CHARACTERISTICS



DIE SIZE 0.068 × 0.045 inch, 3060 sq. mils
(1.73 × 1.14 mm, 1.97 sq. mm)

1. BALANCE
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V−
5. BALANCE
6. OUTPUT
7. V+

For additional DICE information refer to Section 2.

WAFER TEST LIMITS at $V_S = \pm15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-20N LIMIT	OP-20G LIMIT	OP-20GR LIMIT	UNITS
Input Offset Voltage	V_{OS}		300	600	1000	μV MAX
Input Offset Current	I_{OS}		1.5	2.5	4.0	nA MAX
Input Bias Current	I_B		25	30	40	nA MAX
Input Voltage Range	IVR	$V+ = +5V$, $V- = 0V$ $V_S = \pm15V$	0/3.5 −15/13.5	0/3.5 −15/13.5	0/3.5 −15/13.5	V MIN
Common-Mode Rejection Ratio	CMRR	$V+ = +5V$, $V- = 0V$, $0V \leq V_{CM} \leq +3.5V$ $V_S = \pm15V$, $-15V \leq V_{CM} \leq \pm13.5V$	95 100	90 94	85 90	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm2.5V$ to $\pm15V$ $V- = 0V$, $V+ = +5V$ to $+30V$	6	10	32	μV/V MAX
Large-Signal Voltage Gain	A_{VO}	$R_L = 25k\Omega$ $V_O = \pm10V$	1000	800	500	V/mV MIN
Output Voltage Swing	V_O	$R_L = 10k\Omega$, $V+ = +5V$, $V- = 0V$ $R_L = 25k\Omega$, $V_S = \pm15V$	0.7/4.1 ±14.1	0.8/4.1 ±14.1	0.9/4.0 ±14.0	V MIN
Supply Current	I_{SY}	$V_S = \pm2.5V$, No Load $V_S = \pm15V$, No Load	55 80	63 85	70 95	μA MAX

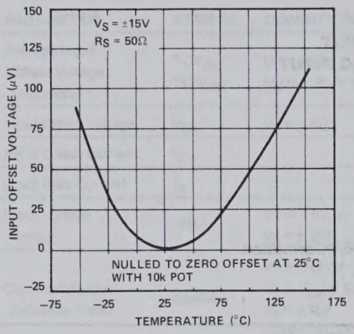
Note: Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $T_A = +25°C$, unless otherwise noted.

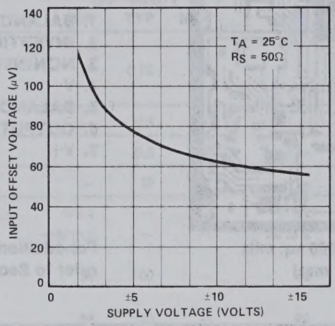
PARAMETER	SYMBOL	CONDITIONS	OP-20N TYPICAL	OP-20G TYPICAL	OP-20GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS} TCV_{OSn}	Unnulled Nulled, $R_P = 10k\Omega$	1.0 1.0	1.5 1.5	2.5 2.5	μV/°C
Large-Signal Voltage Gain	A_{VO}	$R_L = 25k\Omega$	2000	2000	1000	V/mV

TYPICAL PERFORMANCE CHARACTERISTICS

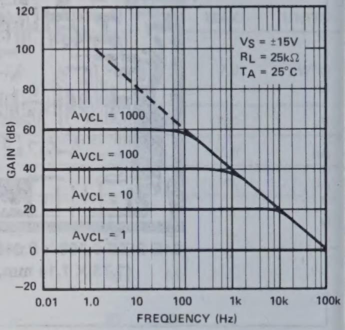
TRIMMED OFFSET VOLTAGE vs TEMPERATURE



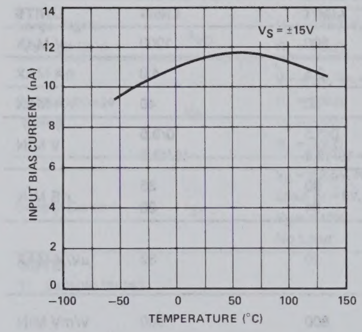
INPUT OFFSET VOLTAGE vs POWER SUPPLY VOLTAGE



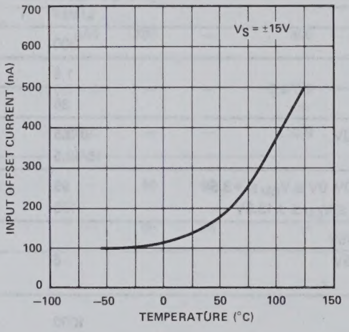
CLOSED-LOOP GAIN vs FREQUENCY



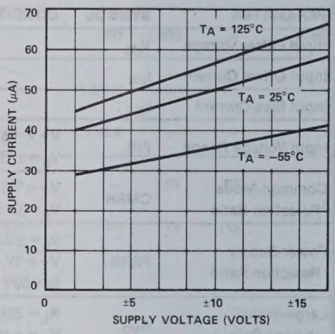
INPUT BIAS CURRENT vs TEMPERATURE



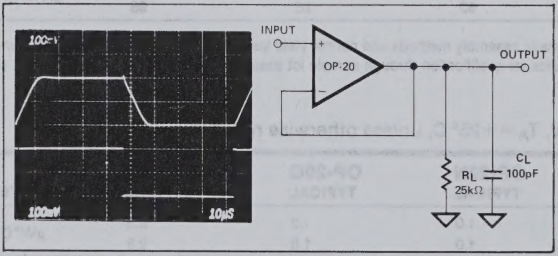
INPUT OFFSET CURRENT vs TEMPERATURE



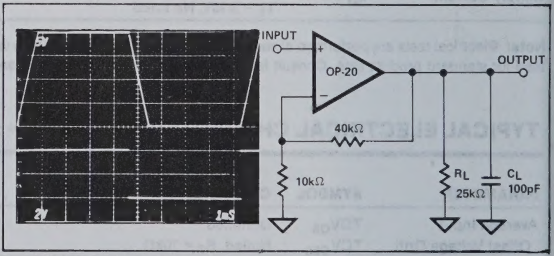
SUPPLY CURRENT vs SUPPLY VOLTAGE



SMALL-SIGNAL TRANSIENT RESPONSE

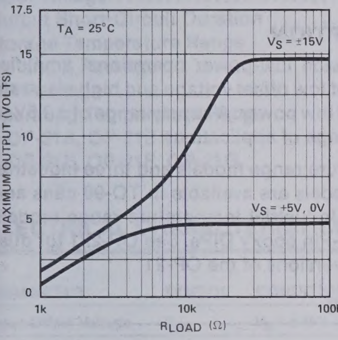

100mV
10μS
INPUT
OUTPUT
OP-20
+
−
RL
25kΩ
CL
100pF

LARGE-SIGNAL TRANSIENT RESPONSE

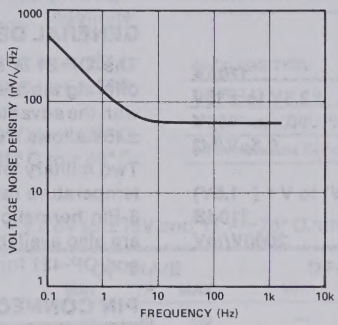

5V
2V
1mS
INPUT
OUTPUT
OP-20
+
−
40kΩ
10kΩ
RL
25kΩ
CL
100pF

TYPICAL PERFORMANCE CHARACTERISTICS

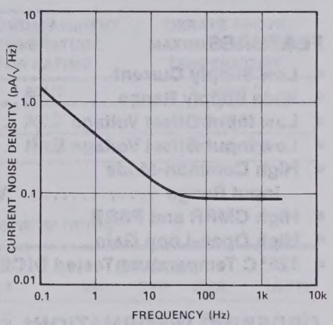
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



VOLTAGE NOISE DENSITY vs FREQUENCY

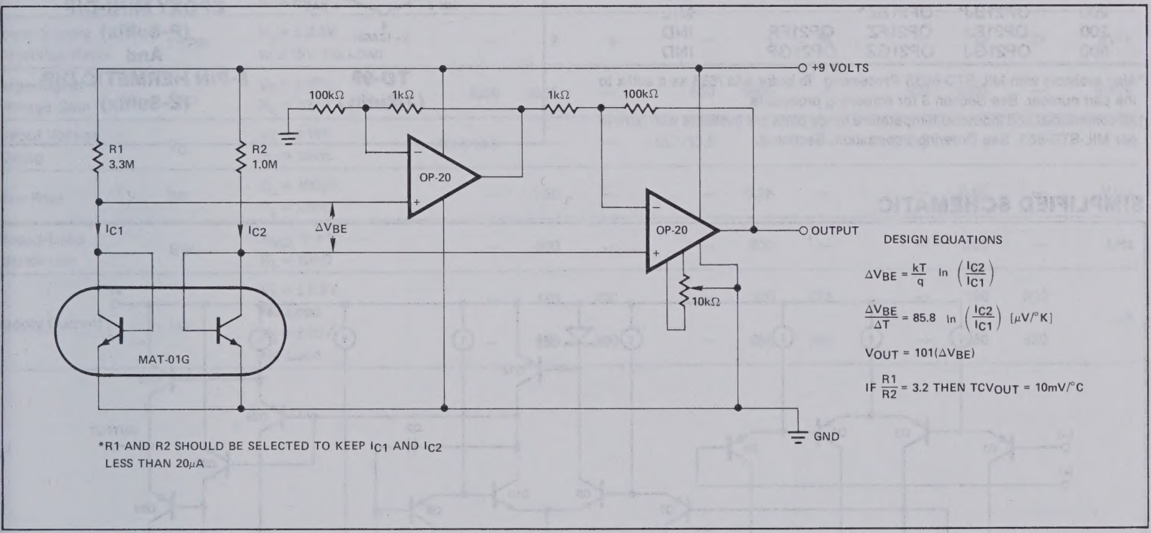


CURRENT NOISE DENSITY vs FREQUENCY



TYPICAL APPLICATIONS

TEMPERATURE SENSOR


+9 VOLTS
100kΩ
1kΩ
1kΩ
100kΩ
R1
3.3M
R2
1.0M
OP-20
OP-20
I_{C1}
I_{C2}
ΔV_{BE}
OUTPUT
10kΩ
MAT-01G
GND

DESIGN EQUATIONS

$$\Delta V_{BE} = \frac{kT}{q} \ln\left(\frac{I_{C2}}{I_{C1}}\right)$$

$$\frac{\Delta V_{BE}}{\Delta T} = 85.8 \ln\left(\frac{I_{C2}}{I_{C1}}\right) \ [\mu V/°K]$$

$$V_{OUT} = 101(\Delta V_{BE})$$

IF $\frac{R1}{R2} = 3.2$ THEN $TCV_{OUT} = 10mV/°C$

*R1 AND R2 SHOULD BE SELECTED TO KEEP I_{C1} AND I_{C2} LESS THAN 20μA

OP-21 LOW-POWER OPERATIONAL AMPLIFIER

FEATURES

- **Low Supply Current 170µA**
- **Wide Supply Range .... ±2.5V to ±15V**
- **Low Input Offset Voltage 40µV**
- **Low Input Offset Voltage Drift .... 0.5µV/°C**
- **High Common-Mode Input Range .... V− (+0.5V) to V+ (−1.5V)**
- **High CMRR and PSRR 110dB**
- **High Open-Loop Gain 2000V/mV**
- **125°C Temperature Tested DICE**

ORDERING INFORMATION†

T_A = 25°C V_{OS} MAX (µV)	PACKAGE TO-99 8-PIN	HERMETIC DIP 8-PIN	PLASTIC DIP 8-PIN	OPERATING TEMPERATURE RANGE
100	OP21AJ*	OP21AZ*		MIL
100	OP21EJ	OP21EZ	OP21EP	IND
200	OP21BJ*	OP21BZ*		MIL
200	OP21FJ	OP21FZ	OP21FP	IND
500	OP21GJ	OP21GZ	OP21GP	IND

*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

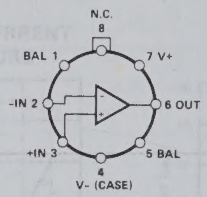
†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

GENERAL DESCRIPTION

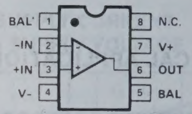
The OP-21 is a precision low-power operational amplifier offering the benefits of low offset voltage and high slew rate with the advantages of low power. A supply range of ±2.5V to ±15V allows a wide range of applications.

Two military temperature range models and three industrial temperature range models are available in TO-99 cans and 8-Pin hermetic DIPs. Industrial temperature range models are also available in 8-Pin epoxy DIPs. See OP-221 for dual and OP-421 for quad versions of the OP-21.

PIN CONNECTIONS

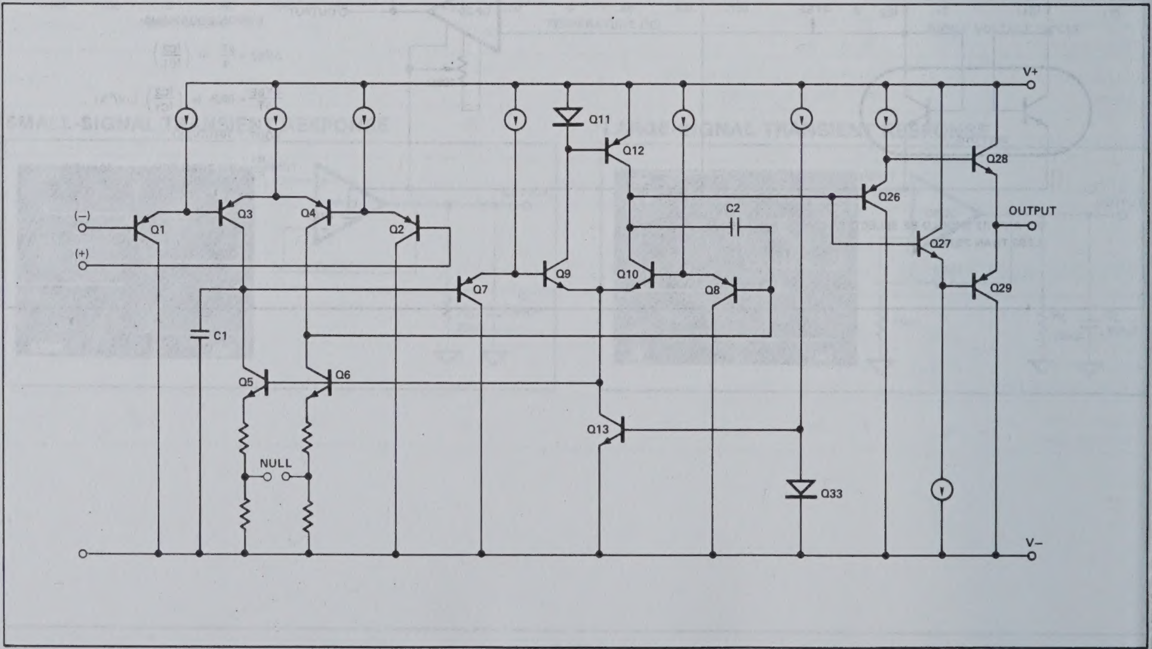


TO-99
(J-Suffix)



EPOXY MINI-DIP
(P-Suffix)
And
8-PIN HERMETIC DIP
(Z-Suffix)

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage .... ±18V
Power Dissipation (Note 1) 500mW
Differential Input Voltage .... ±30V
Input Voltage .... Supply Voltage
Output Short-Circuit Duration .... Indefinite
Storage Temperature Range
J and Z Packages .... −65° C to +125° C
P Package .... −65° C to +125° C
Operating Temperature Range
OP-21A, OP-21B .... −55° C to +125° C
OP-21E, OP-21F, OP-21G .... −25° C to +85° C
DICE Junction Temperature (T_j) .... −65° C to +150° C
Lead Temperature Range (Soldering, 60 sec) ...... 300° C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.
2. Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80° C	7.1mW/° C
8-Pin Plastic DIP (P)	36° C	5.6mW/° C
8-Pin Hermetic DIP (Z)	75° C	6.7mW/° C

ELECTRICAL CHARACTERISTICS at $V_S = \pm 2.5V$ to $\pm 15V$ and $T_A = +25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-21A/E MIN	OP-21A/E TYP	OP-21A/E MAX	OP-21B/F MIN	OP-21B/F TYP	OP-21B/F MAX	OP-21G MIN	OP-21G TYP	OP-21G MAX	UNITS
Input Offset Voltage	V_{OS}	$V_S = \pm 15V$	—	40	100	—	150	200	—	300	500	µV
Input Offset Current	I_{OS}	$V_{CM} = 0$	—	0.6	4	—	0.8	5	—	1.2	6	nA
Input Bias Current	I_B	$V_{CM} = 0$	—	50	100	—	60	120	—	70	150	nA
Input Voltage Range	IVR	$V_S = \pm 15V$	−14.5/13.5	—	—	−14.5/13.5	—	—	−14.5/13.5	—	—	V
Common-Mode Rejection Ratio	CMRR	$V_S = \pm 15V$, No Load $-14.5V \le V_{CM} \le 13.5V$	100	110	—	90	105	—	84	100	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$, No Load	—	2	6	—	4	10	—	10	32	µV/V
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $R_L = 10k\Omega$, $V_O \pm 10V$	1000	2000	—	500	1500	—	500	1000	—	V/mV
Output Voltage Swing	V_O	$V_S = \pm 15V$, $R_L = 10k\Omega$	−13.7/14.0	—	—	−13.7/13.9	—	—	−13.6/13.8	—	—	V
Slew Rate	SR	$C_L = 100pF$, $R_L = 25k\Omega$	—	0.25	—	—	0.25	—	—	0.25	—	V/µs
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$, $R_L = 10k\Omega$	—	600	—	—	600	—	—	600	—	kHz
Supply Current	I_{SY}	$V_S = \pm 2.5V$, No Load	—	170	230	—	180	275	—	190	300	µA
		$V_S = \pm 15V$, No Load	—	230	300	—	235	360	—	250	420	

ELECTRICAL CHARACTERISTICS at $V_S = \pm 2.5V$ to $\pm 15V$, $-55°C \le T_A \le +125°C$ for OP-21A and OP-21B, $-25°C \le T_A \le +85°C$ for OP-21E, OP-21F and OP-21G, unless otherwise noted.

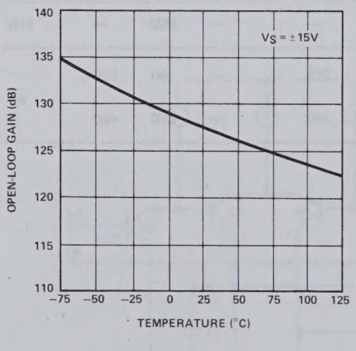
PARAMETER	SYMBOL	CONDITIONS	OP-21A/E MIN	OP-21A/E TYP	OP-21A/E MAX	OP-21B/F MIN	OP-21B/F TYP	OP-21B/F MAX	OP-21G MIN	OP-21G TYP	OP-21G MAX	UNITS
Average Input Offset Voltage Drift (Note 1)	TCV_{OS} TCV_{OSn}	Unnulled Nulled	—	0.5	1.0	—	1.0	2.0	—	2.5	5.0	μV/°C
Input Offset Voltage	V_{OS}	$V_{CM} = 0$	—	75	200	—	200	500	—	500	1000	μV
Input Offset Current	I_{OS}	$V_{CM} = 0$	—	1.5	5	—	2.0	6	—	2.0	8	nA
Input Bias Current	I_B		—	50	110	—	60	130	—	70	165	nA
Input Voltage Range	IVR		−14.3/13.2	—	—	−14.3/13.2	—	—	−14.3/13.2	—	—	V
Common-Mode Rejection Ratio	CMRR	No Load, $V_S = \pm 15V$, $-14.5V \le V_{CM} \le 13.2V$	96	105	—	86	100	—	80	95	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$, No Load	—	4	10	—	6	18	—	18	57	μV/V
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $R_L = 20k\Omega$, $V_O = \pm 10V$	500	1500	—	250	1300	—	250	1000	—	V/mV
Output Voltage Swing	V_O	$V_S = \pm 15V$, $R_L = 20k\Omega$	−13.5/13.8	—	—	−13.5/13.7	—	—	−13.5/13.6	—	—	V
Supply Current	I_{SY}	$V_S = \pm 2.5V$, No Load	—	205	275	—	215	330	—	230	360	μA
		$V_S = \pm 15V$, No Load	—	275	360	—	285	430	—	300	500	

NOTE:

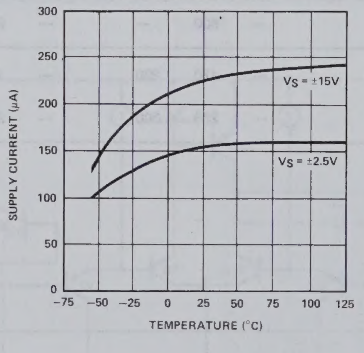
1. Sample tested.

TYPICAL PERFORMANCE CHARACTERISTICS

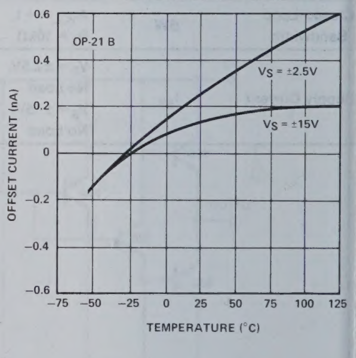
OPEN-LOOP GAIN vs TEMPERATURE



SUPPLY CURRENT vs TEMPERATURE

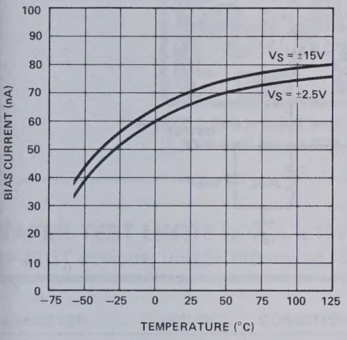


OFFSET CURRENT vs TEMPERATURE

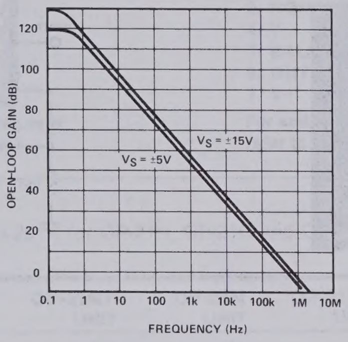


TYPICAL PERFORMANCE CHARACTERISTICS

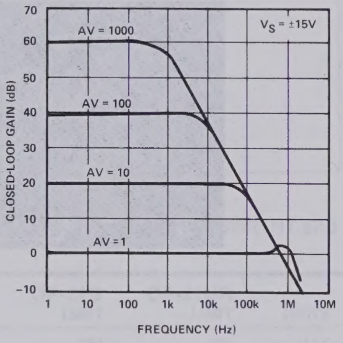
BIAS CURRENT vs TEMPERATURE



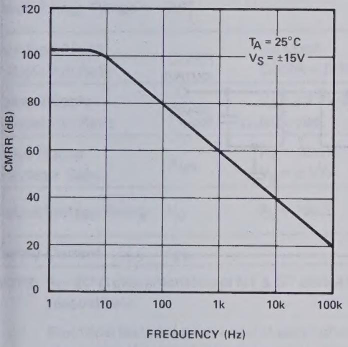
OPEN-LOOP GAIN vs FREQUENCY



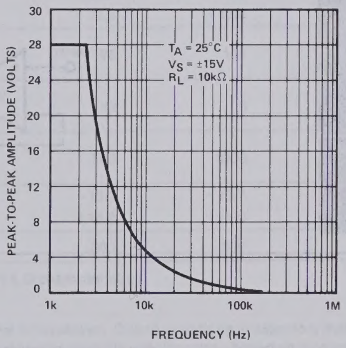
CLOSED-LOOP GAIN vs FREQUENCY



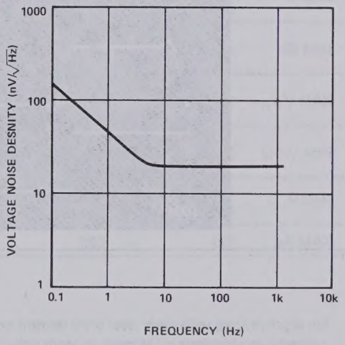
CMRR vs FREQUENCY



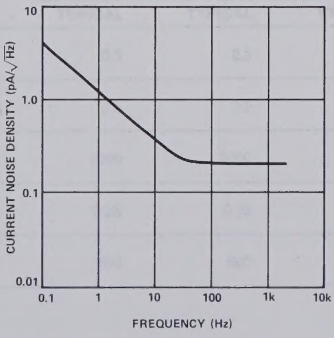
MAXIMUM OUTPUT SWING vs FREQUENCY



VOLTAGE NOISE DENSITY vs FREQUENCY

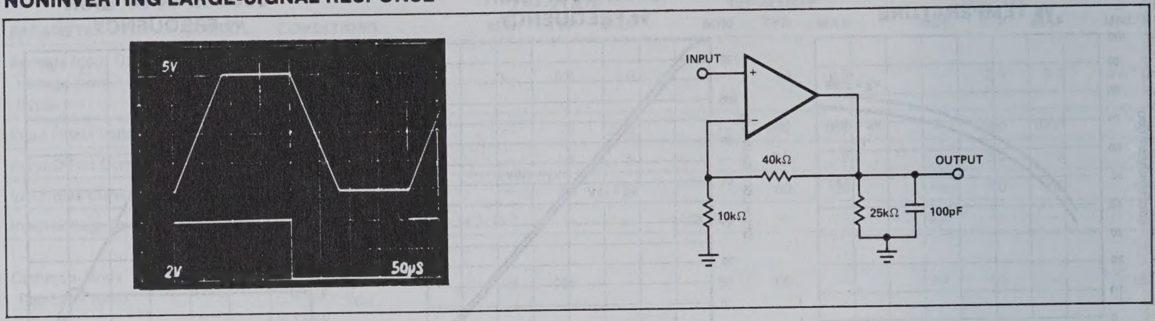


CURRENT NOISE DENSITY vs FREQUENCY

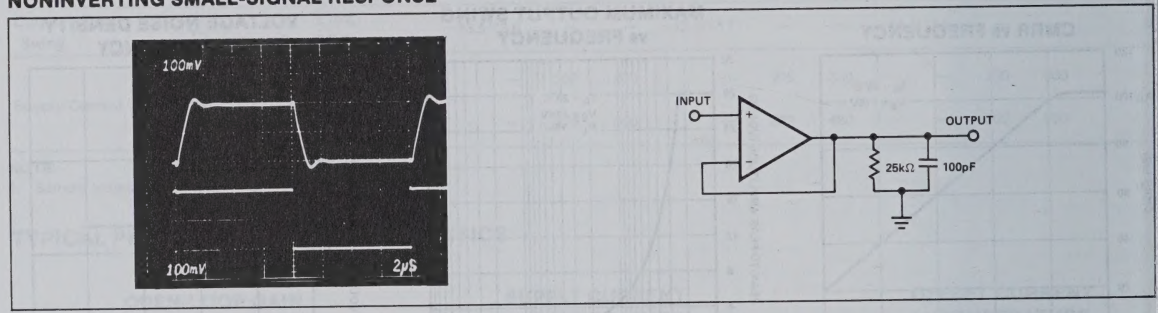


TYPICAL PERFORMANCE CHARACTERISTICS

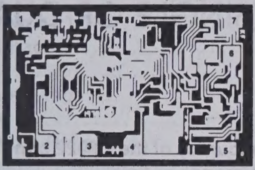
NONINVERTING LARGE-SIGNAL RESPONSE



NONINVERTING SMALL-SIGNAL RESPONSE



DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)



DIE SIZE 0.068 × 0.045 inch, 3060sq. mils
(1.73 × 1.14 mm, 1.974 sq. mm)

1. **BALANCE**
2. **INVERTING INPUT**
3. **NONINVERTING INPUT**
4. **V−**
5. **BALANCE**
6. **OUTPUT**
7. **V+**

For additional DICE information refer to Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$ for OP-21N, OP-21G and OP-21GR devices; $T_A = 125°C$ for OP-21NT and OP-21GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-21NT LIMIT	OP-21N LIMIT	OP-21GT LIMIT	OP-21G LIMIT	OP-21GR LIMIT	UNITS
Input Offset Voltage	V_{OS}		200	100	500	200	500	μV MAX
Input Offset Current	I_{OS}	$V_{CM} = 0$	4	4	5	5	6	nA MAX
Input Bias Current	I_B	$V_{CM} = 0$	100	100	120	120	150	nA MAX
Input Voltage Range	IVR		−14.3 +13.5	−14.5 +13.5	−14.3 +13.5	−14.5 +13.5	−14.5 +13.5	V MIN
Common-Mode Rejection Ratio	CMRR	No Load CMVR = IVR	96	100	86	90	84	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$ No Load	10	6	18	10	32	μV/V MAX
Large-Signal Voltage Gain	A_{VO}	$R_L = 10k\Omega$, $V_O = \pm 10V$	500	1000	250	500	500	V/mV MIN
Output Voltage Swing	V_O	$R_L = 10k\Omega$	−13.5 +13.8	−13.7 +14.0	−13.5 +13.8	−13.7 +13.9	−13.6 +13.8	V MIN
Supply Current	I_{SY}		300	300	360	360	420	μA MAX

NOTE: For 25° C characteristics of NT & GT devices, see N & G characteristics respectively.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25° C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-21NT TYPICAL	OP-21N TYPICAL	OP-21GT TYPICAL	OP-21G TYPICAL	OP-21GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}	Unnulled	0.5	0.5	1	1	2.5	μV/° C
Nulled Input Offset Voltage Drift	TCV_{OSn}	Nulled, $R_p = 10k\Omega$	0.5	0.5	1	1	2.5	μV/° C
Large-Signal Voltage Gain	A_{VO}	$R_L = 10k\Omega$	2000	2000	1500	1500	1000	V/mV
Slew Rate	SR	$R_L = 25k\Omega$ $C_L = 100pF$	0.25	0.25	0.25	0.25	0.25	V/μs
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$ $R_L = 10k\Omega$	600	600	600	600	600	kHz

OP-22

PROGRAMMABLE MICROPOWER OPERATIONAL AMPLIFIER

(SINGLE OR DUAL SUPPLY)

FEATURES

- **Programmable Supply Current .... 1µA to 400µA**
- **Single Supply Operation .... +3V to +30V**
- **Dual Supply Operation .... ±1.5V to ±15V**
- **Low Input Offset Voltage 100µV**
- **Low Input Offset Voltage Drift .... 0.75µV/°C**
- **High Common-Mode Input Range ... V− to V+ (−1.5V)**
- **High CMRR and PSRR 115dB**
- **High Open-Loop Gain 1800V/mV**
- **±30V Input Overvoltage Protection**
- **Unity-Gain Stable**
- **LM4250 Pinout and Nulling**

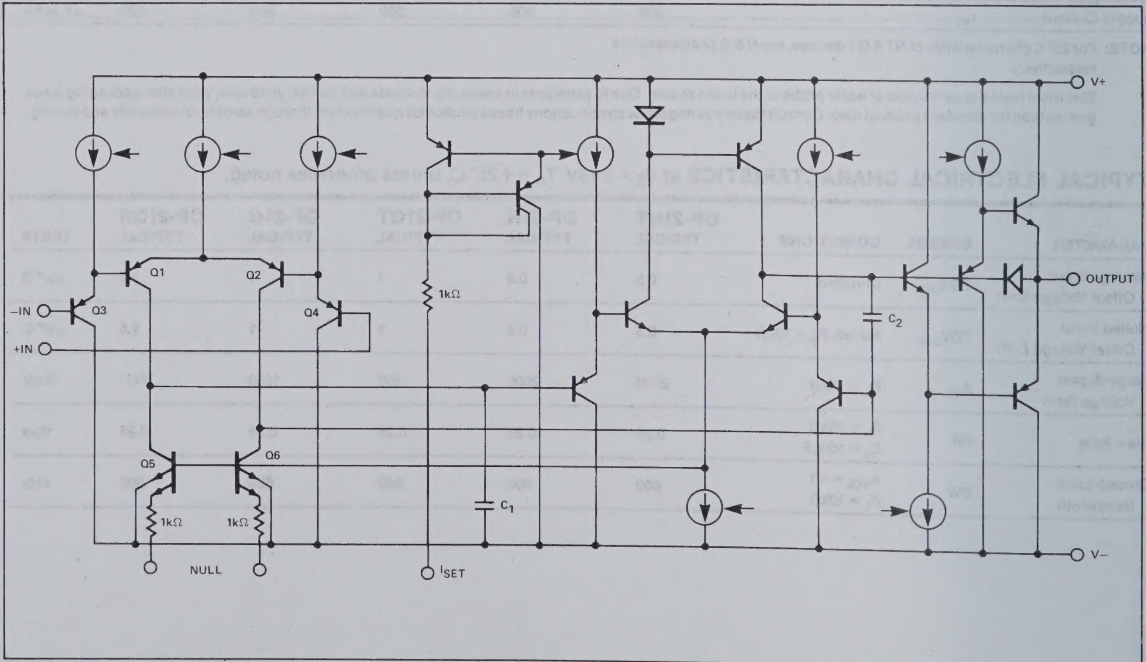
GENERAL DESCRIPTION

The OP-22 is a monolithic micropower operational amplifier designed to provide excellent accuracy in high-gain applications. Offsets are very low which generally eliminates any need for external nulling of V_{OS}. The OP-22 is internally compensated and unity-gain stable. It also features high open-loop gain, CMRR, and PSRR. This assures good gain accuracy and rejection of power supply variations even when used in circuits with high closed-loop gain. The low offsets and high gain accuracy of the OP-22 bring precision performance to the micropower field.

The OP-22 is a versatile op amp designed for operation from battery or solar-cell power sources. Supply current is programmable over a range of 1µA to 400µA with a single external resistor. Input voltage range is very wide and extends down to the negative rail, thus the common-mode input voltage range includes ground when operating from a single supply voltage. This ability to provide high DC performance over a wide input range is particularly useful in single-battery applications. In addition, the OP-22 is characterized over a wide supply range of ±1.5V to ±15V, or +3V to +30V for single supply.

The OP-22 pin-out and offset nulling are identical to the LM4250 and many other micropower operational amplifiers. This functional commonality allows easy upgrading of system performance. By selection of set resistor value, the circuit designer can readily use the OP-22 in place of such amplifiers as the LM108, LM112, LM4250, µA776, and ICL8021 in high-gain, low-frequency applications.

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage .... ±18V
Power Dissipation (Note 1) 500mW
Differential Input Voltage .... ±30V
Input Voltage .... Supply Voltage
Storage Temperature Range
  J and Z Packages .... −65°C to +150°C
Operating Temperature Range
  OP-22A, OP-22B (J or Z package) ... −55°C to +125°C
  OP-22E, OP-22F (J or Z package) .... −25°C to +85°C
  OP-22HJ, OP-22HZ .... 0°C to +70°C
Lead Temperature Range (Soldering, 60 sec.) ..... 300°C
DICE Junction Temperature .... −65°C to +150°C

NOTES:

1. See table for maximum ambient temperature rating.
2. Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

	MAXIMUM AMBIENT TEMPERATURE $V_S = \pm15V$ and $I_{SET} = 10\mu A$	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	124°C	—
8-Pin Hermetic DIP (Z)	124°C	—

ELECTRICAL CHARACTERISTICS at $V_S = \pm1.5V$ to $\pm15V$, $1\mu A \le I_{SET} \le 10\mu A$, $T_A = +25°C$, unless otherwise noted.

			OP-22A/E			OP-22B/F			OP-22H			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		—	100	300	—	200	500	—	400	1000	μV
Input Offset Current	I_{OS}		—	0.2	1	—	0.3	2	—	0.5	3	nA
Input Bias Current	I_B	$I_{SET} = 1\mu A$	—	2.6	5	—	3.0	7.5	—	4.0	10	nA
		$I_{SET} = 10\mu A$	—	19	30	—	24	35	—	30	50	
Input Voltage Range	IVR	$V+ = +5V$, $V- = 0V$.	0/3.5	—	—	0/3.5	—	—	0/3.5	—	—	V
		$V_S = \pm15V$	−15/+13.5	—	—	−15/+13.5	—	—	−15/+13.5	—	—	
Common-Mode Rejection Ratio	CMRR	$V_S = \pm15V$ $-15V \le V_{CM} \le +13.5V$	100	115	—	95	105	—	85	95	—	dB
Power Supply Rejection Ratio (Note 1)	PSRR	$V_S = \pm1.5V$ to $\pm15V$; and $V- = 0V$, $V+ = 3V$ to $30V$.	—	1.8	6	—	6	18	—	10	32	dB
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm15V$, $I_{SET} = 1\mu A$, $R_L = 100k\Omega$.	1000	1800	—	500	900	—	250	500	—	V/mV
		$V_S = \pm15V$, $I_{SET} = 10\mu A$, $R_L = 10k\Omega$.	1000	1800	—	500	900	—	300	500	—	V/mV
Output Voltage Swing	V_O	$V_S = \pm1.5V$, $I_{SET} = 1\mu A$, $R_L = 100k\Omega$ & $I_{SET} = 10\mu A$, $R_L = 10k\Omega$.	±0.8	±0.82	—	±0.8	±0.82	—	±0.75	±0.8	—	V
		$V_S = \pm15V$, $I_{SET} = 1\mu A$, $R_L = 100k\Omega$ & $I_{SET} = 10\mu A$, $R_L = 10k\Omega$.	±14	±14.2	—	±14	±14.2	—	±13.5	±14	—	V
Closed-Loop Bandwidth	BW	$A_{VCL} = +1.0$, $V_S = \pm15V$, $I_{SET} = 10\mu A$, $R_L = 10k\Omega$.	—	250	—	—	250	—	—	250	—	kHz
Slew Rate	SR	$V_S = \pm15V$, $I_{SET} = 10\mu A$, $R_L = 10k\Omega$.	—	0.08	—	—	0.08	—	—	0.08	—	V/μs
Supply Current No Load	I_{SY}	$V_S = \pm15V$, $I_{SET} = 1\mu A$.	—	15	17	—	16	19	—	18	21	μA
		$V_S = \pm15V$, $I_{SET} = 10\mu A$.	—	150	170	—	160	190	—	180	210	
		$V_S = \pm1.5V$, $I_{SET} = 1\mu A$.	—	10.5	12.5	—	14	16	—	17	20	
		$V_S = \pm1.5V$, $I_{SET} = 10\mu A$.	—	105	125	—	140	160	—	170	200	

NOTE:

1. Sample tested for single-supply operation, 100% tested for dual-supply operation.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 1.5V$ to $\pm 15V$, $1\mu A \le I_{SET} \le 10\mu A$, $-55°C \le T_A \le +125°C$ for OP-22AJ/AZ and OP-22BJ/BZ, $-25°C \le T_A \le +85°C$ for OP-22EJ/EZ and OP-22FJ/FZ, and $0°C \le T_A \le +70°C$ for OP-22HJ and OP-22HZ, unless otherwise noted.

			OP-22A/E			OP-22B/F			OP-22H			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	Unnulled	—	0.75	1.5	—	1.0	2.0	—	1.5	3.0	µV/°C
Input Offset Voltage	V_{OS}	—	—	175	400	—	350	600	—	500	1200	µV
Input Offset Current	I_{OS}	—	—	0.2	1	—	0.3	2	—	0.5	3	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 1)	—	2	10	—	3	15	—	5	25	pA/°C
Input Bias Current	I_B	$I_{SET} = 1\mu A$ $I_{SET} = 10\mu A$	— —	2.8 21	5 30	— —	3.3 27	7.5 35	— —	4.5 34	10 50	nA
Input Voltage Range	IVR	$V+ = +5V$, $V- = 0V$ $V_S = \pm 15V$	0/3.2 −15/+13.2	— —	— —	0/3.2 −15/+13.2	— —	— —	0/3.2 −15/+13.2	— —	— —	V
Common-Mode Rejection Ratio	CMRR	$V_S = \pm 15V$ $-15V \le V_{CM} \le +13.2V$	90	115	—	86	105	—	80	90	—	dB
Power Supply Rejection Ratio (Note 2)	PSRR	$V_S = \pm 1.5V$ to $\pm 15V$ & $V- = 0V$, $V+ = 3V$ to $30V$	—	3.2	10	—	10	32	—	32	56	µV/V
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $I_{SET} = 1\mu A$, $R_L = 100k\Omega$. $V_S = \pm 15V$, $I_{SET} = 10\mu A$, $R_L = 10k\Omega$.	400 500	900 1000	— —	250 250	500 500	— —	100 150	250 300	— —	V/mV
Output Voltage Swing	V_O	$V_S = \pm 1.5V$, $I_{SET} = 1\mu A$, $R_L = 100k\Omega$ & $I_{SET} = 10\mu A$, $R_L = 10k\Omega$.	±0.65	±0.75	—	±0.65	±0.75	—	±0.6	±0.7	—	V
		$V_S = \pm 15V$, $I_{SET} = 1\mu A$, $R_L = 100k\Omega$ & $I_{SET} = 10\mu A$, $R_L = 10k\Omega$.	±13.6	±13.8	—	±13.6	±13.8	—	±13.0	±13.5	—	V
Supply Current No Load	I_{SY}	$V_S = \pm 15V$, $I_{SET} = 1\mu A$. $V_S = \pm 15V$, $I_{SET} = 10\mu A$. $V_S = \pm 1.5V$, $I_{SET} = 1\mu A$. $V_S = \pm 1.5V$, $I_{SET} = 10\mu A$.	— — — —	16 160 12 120	18 180 14 140	— — — —	17 170 15 150	20 200 18 180	— — — —	20 200 19 190	25 250 25 250	µA

NOTES:

1. Sample tested.
2. 100% tested for dual supply operation, sample tested for single supply operation.

ORDERING INFORMATION†

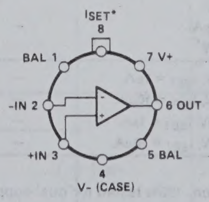
	PACKAGE		
$T_A = 25°C$ V_{OS} MAX (µV)	TO-99 8-PIN	HERMETIC DIP 8-PIN	OPERATING TEMPERATURE RANGE
300	OP22AJ*	OP22AZ*	MIL
300	OP22EJ	OP22EZ	IND
500	OP22BJ*	OP22BZ*	MIL
500	OP22FJ	OP22FZ	IND
1000	OP22HJ	OP22HZ	COM

*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

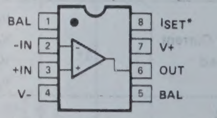
†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

PIN CONNECTIONS

* NOTE: DO NOT SHORT PIN 8 TO V– OR GROUND. SEE APPLICATIONS INFORMATION.

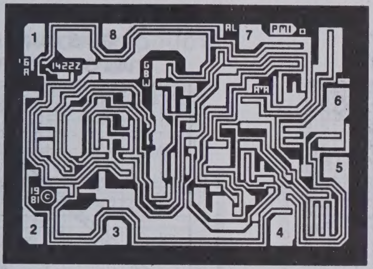


TO-99 (J-Suffix)



8-PIN HERMETIC DIP (Z-Suffix)

DICE CHARACTERISTICS



DIE SIZE 0.069 × 0.049 inch, 3381 sq. mils (1.75 × 1.24 mm, 2.18 sq. mm)

1. **BALANCE**
2. **INVERTING INPUT**
3. **NONINVERTING INPUT**
4. **V−**
5. **BALANCE**
6. **OUTPUT**
7. **V+**
8. **I_{SET}**

For additional DICE information refer to Section 2.

WAFER TEST LIMITS at $V_S = \pm 1.5V$ to $\pm 15V$, $1\mu A \le I_{SET} \le 10\mu A$, $T_A = 25°C$, unless otherwise noted.

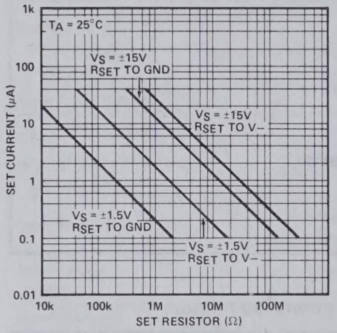
PARAMETER	SYMBOL	CONDITIONS	OP-22N LIMIT	OP-22G LIMIT	OP-22GR LIMIT	UNITS
Input Offset Voltage	V_{OS}		300	500	1000	μV MAX
Input Offset Current	I_{OS}		1	2	3	nA MAX
Input Bias Current	I_B	$I_{SET} = 1\mu A$ $I_{SET} = 10\mu A$	5 30	7.5 35	10 50	nA MAX
Input Voltage Range	IVR	$V+ = +5V$, $V- = 0V$ $V_S = \pm 15V$	0/3.5 −15/+13.5	0/3.5 −15/+13.5	0/3.5 −15/+13.5	V MIN
Common-Mode Rejection Ratio	CMRR	$V_S = \pm 15V$, $-15V \le V_{CM} \le +13.5V$	100	95	85	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 1.5V$ to $\pm 15V$ $V- = 0V$, $V+ = 3V$ to $30V$	6	18	32	μV/V MIN
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $I_{SET} = 1\mu A$, $R_L = 100k\Omega$.	1000	500	250	V/mV MIN
		$V_S = \pm 15V$, $I_{SET} = 10\mu A$, $R_L = 10k\Omega$.	1000	500	300	
Output Voltage Swing	V_O	$V_S = \pm 1.5V$, $I_{SET} = 1\mu A$, $R_L = 100k\Omega$ & $I_{SET} = 10\mu A$, $R_L = 10k\Omega$.	±0.8	±0.8	±0.75	V MIN
		$V_S = \pm 15V$, $I_{SET} = 1\mu A$, $R_L = 100k\Omega$ & $I_{SET} = 10\mu A$, $R_L = 10k\Omega$.	±14	±14	±13.5	
Supply Current No Load	I_{SY}	$V_S = \pm 15V$, $I_{SET} = 1\mu A$. $V_S = \pm 15V$, $I_{SET} = 10\mu A$. $V_S = \pm 1.5V$, $I_{SET} = 1\mu A$. $V_S = \pm 1.5V$, $I_{SET} = 10\mu A$.	17 170 12.5 125	19 190 16 160	21 210 20 200	μA MAX

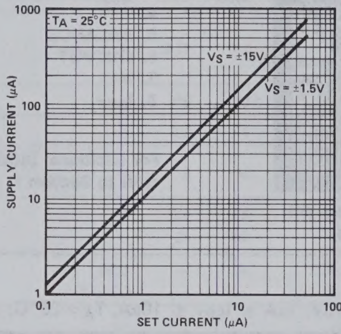
Note: Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

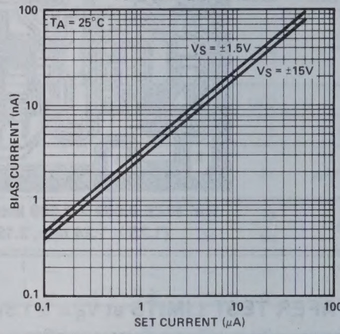
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 1.5V$ to $\pm 15V$, $1\mu A \le I_{SET} \le 10\mu A$, $T_A = +25°C$, unless otherwise noted.

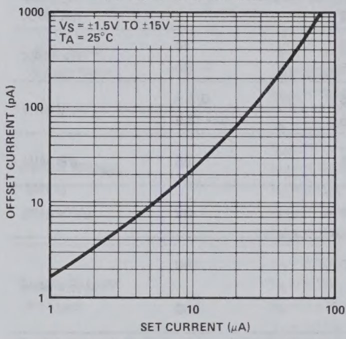
PARAMETER	SYMBOL	CONDITIONS	OP-22N TYPICAL	OP-22G TYPICAL	OP-22GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}	Unnulled	1.0	1.5	2.5	μV/°C
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$ $I_{SET} = 1\mu A$, $R_L = 100k\Omega$ & $I_{SET} = 10\mu A$, $R_L = 10k\Omega$	1800	900	500	V/mV

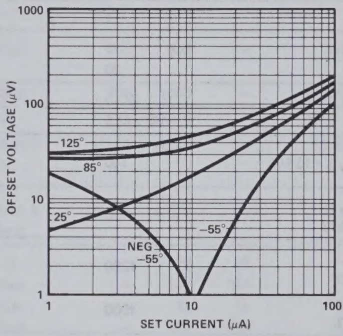
TYPICAL PERFORMANCE CHARACTERISTICS

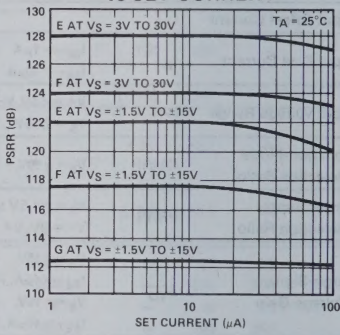

SET CURRENT vs SET RESISTOR

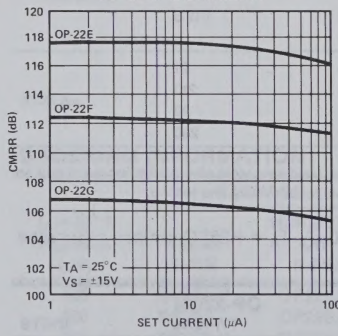

SUPPLY CURRENT vs SET CURRENT

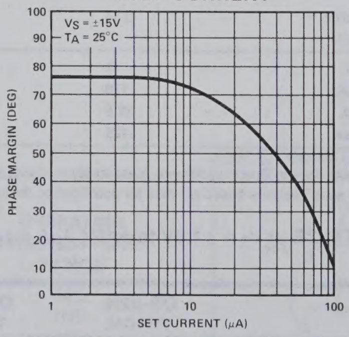

BIAS CURRENT vs SET CURRENT

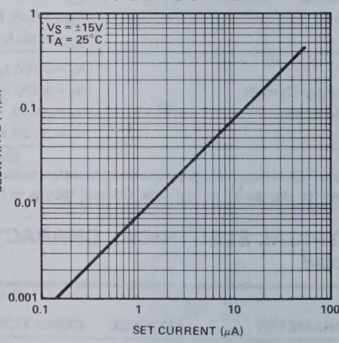

OFFSET CURRENT vs SET CURRENT


OFFSET VOLTAGE vs SET CURRENT


POWER SUPPLY REJECTION vs SET CURRENT

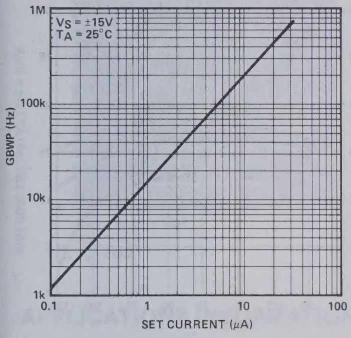

COMMON-MODE REJECTION vs SET CURRENT


PHASE MARGIN vs SET CURRENT

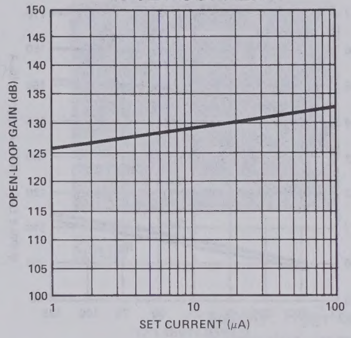

SLEW RATE vs SET CURRENT

TYPICAL PERFORMANCE CHARACTERISTICS

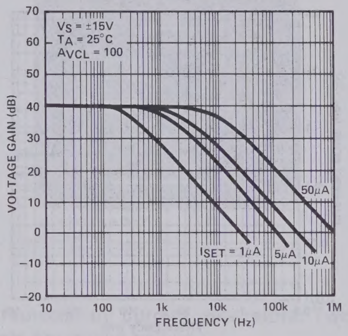
GAIN-BANDWIDTH PRODUCT vs SET CURRENT



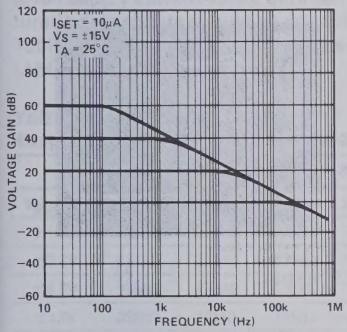
OPEN-LOOP GAIN vs SET CURRENT



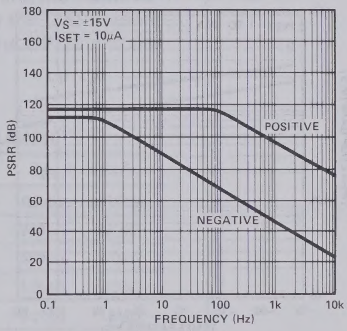
FREQUENCY RESPONSE vs SET CURRENT



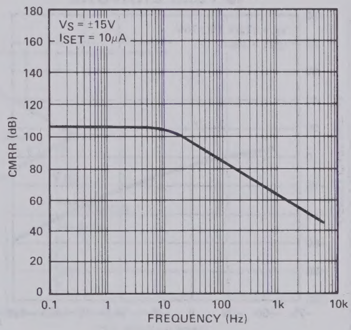
CLOSED-LOOP FREQUENCY RESPONSE



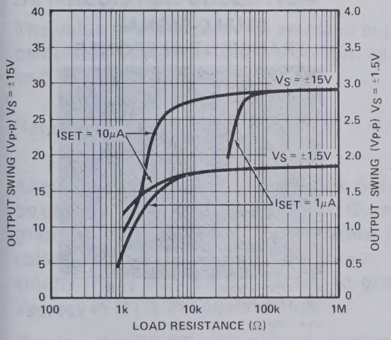
POWER SUPPLY REJECTION vs FREQUENCY



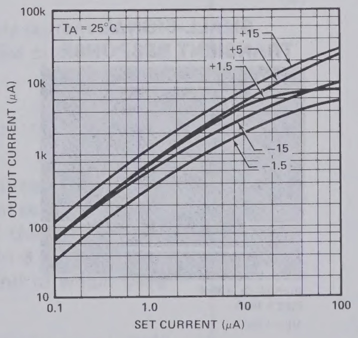
COMMON-MODE REJECTION vs FREQUENCY



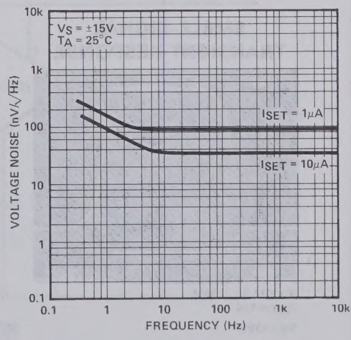
PEAK-TO-PEAK OUTPUT SWING vs LOAD RESISTANCE



MAXIMUM OUTPUT CURRENT vs SET CURRENT AT $V_S = \pm 15V, +5$ AND ± 1.5

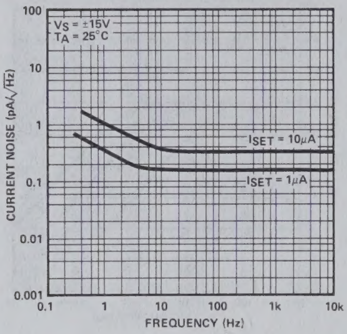


VOLTAGE NOISE vs FREQUENCY

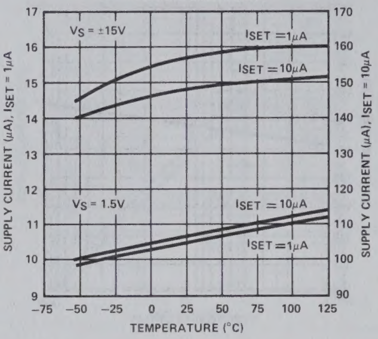


TYPICAL PERFORMANCE CHARACTERISTICS

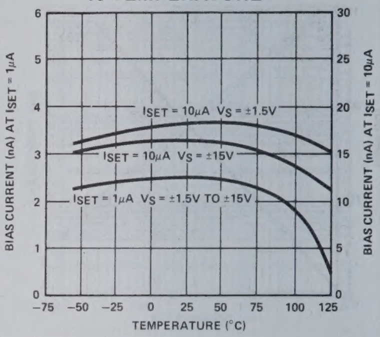
CURRENT NOISE vs FREQUENCY



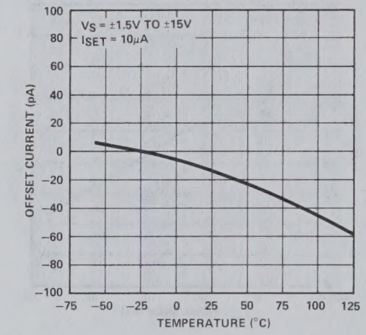
SUPPLY CURRENT vs TEMPERATURE



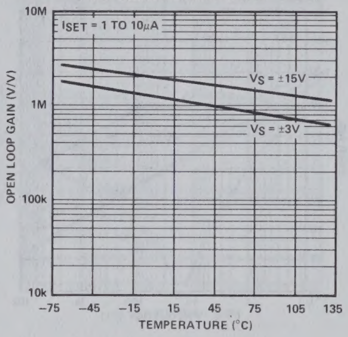
BIAS CURRENT vs TEMPERATURE



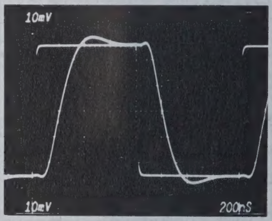
OFFSET CURRENT vs TEMPERATURE



OPEN-LOOP GAIN vs TEMPERATURE

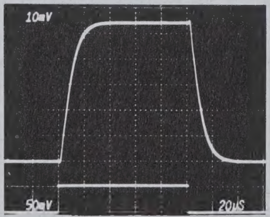


SMALL-SIGNAL TRANSIENT RESPONSE



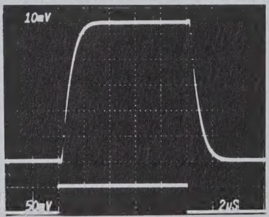
$A_V = +1$, $C_L = 30pF$
$I_{SET} = 50\mu A$
$V_S = \pm15V$

SMALL-SIGNAL TRANSIENT RESPONSE



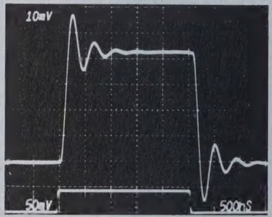
$A_V = +1$, $C_L = 30pF$
$I_{SET} = 1\mu A$
$V_S = \pm15V$

SMALL-SIGNAL TRANSIENT RESPONSE



$A_V = +1$, $C_L = 30pF$
$I_{SET} = 10\mu A$
$V_S = \pm15V$

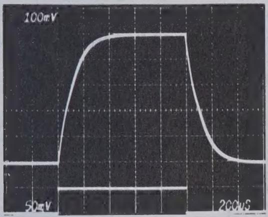
SMALL-SIGNAL TRANSIENT RESPONSE



$A_V = +1$, $C_L = 30pF$
$I_{SET} = 100\mu A$
$V_S = \pm15V$

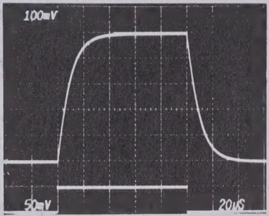
TYPICAL PERFORMANCE CHARACTERISTICS

SMALL-SIGNAL TRANSIENT RESPONSE



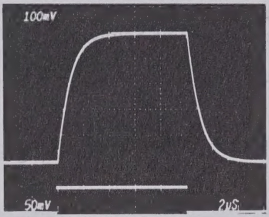
$A_V = +10$, $C_L = 30pF$
$I_{SET} = 1\mu A$
$V_S = \pm 15V$

SMALL-SIGNAL TRANSIENT RESPONSE



$A_V = +10$, $C_L = 30pF$
$I_{SET} = 10\mu A$
$V_S = \pm 15V$

SMALL-SIGNAL TRANSIENT RESPONSE



$A_V = +10$, $C_L = 30pF$
$I_{SET} = 100\mu A$
$V_S = \pm 15V$

APPLICATIONS INFORMATION

OP-22 series units may be inserted directly into LM4250, µA776 and ICL8021 sockets with or without removal of external nulling components. The value of set resistor for a given supply current varies between types and the manufacturer's data sheets should be consulted for this information. Table 1 compares set resistor values for the OP-22 and the LM4250. (R_{SET} connected to V−).

TABLE 1
Supply Current vs. Set Resistor for OP-22 and LM4250

	$I_{SY} = 10\mu A$		$I_{SY} = 30\mu A$		$I_{SY} = 100\mu A$	
V_{SUPPLY}	OP-22	LM4250	OP-22	LM4250	OP-22	LM4250
±1.5V	2.2MΩ	1.3MΩ	680kΩ	430kΩ	220kΩ	120kΩ
±3.0V	6.8MΩ	2.7MΩ	2.2MΩ	910kΩ	680kΩ	270kΩ
±5.0V	13MΩ	4.7MΩ	4.3MΩ	1.5MΩ	1.3MΩ	470kΩ
±12V	33MΩ	12MΩ	11MΩ	3.9MΩ	3.3MΩ	1.2MΩ
±15V	43MΩ	15MΩ	15MΩ	5.1MΩ	4.3MΩ	1.5MΩ
I_{SET}	0.67µA	1.8µA	2.0µA	6.0µA	6.7µA	20µA

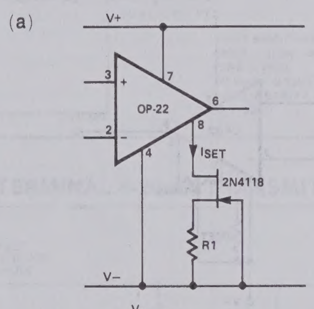
SET-RESISTOR SELECTION

The value of set resistor for selected supply current may be calculated using the "Supply current vs. Set current" curve and the formula;

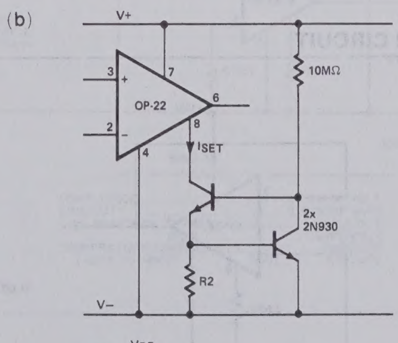
$$R_{SET} = \frac{(V_{SUPPLY} - 2V_{BE})}{I_{SET}} \quad \text{(1)}$$

Alternatively, the "Supply Current vs. Set Current" graph may be used in conjunction with the "Set Current vs. Set Resistor" graph. V_{SUPPLY} in formula (1) refers to the total supply voltage with R_{SET} connected between pin 8 and negative supply. R_{SET} may be connected to ground in which case V_{SUPPLY} in (1) is the positive supply.

Biasing the OP-22 with a fixed resistor produces a supply current approximately proportional to supply voltage. In applications where a constant drain is required with varying supply, R_{SET} can be replaced by current generators. Two suggested arrangements are shown below:



$I_{SET} \approx \frac{V_P}{2R1}$, $I_{DSS} \gg I_{SET}$

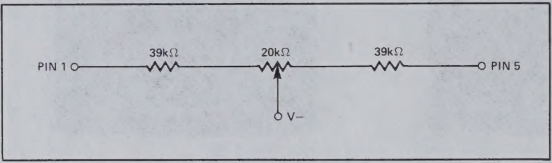


$I_{SET} \approx \frac{V_{BE}}{R2}$

CAUTION: Shorting of pin 8 to negative supply or ground will cause excessive I_{SET} which in turn will cause excessive supply current to flow. I_{SET} should always be limited.

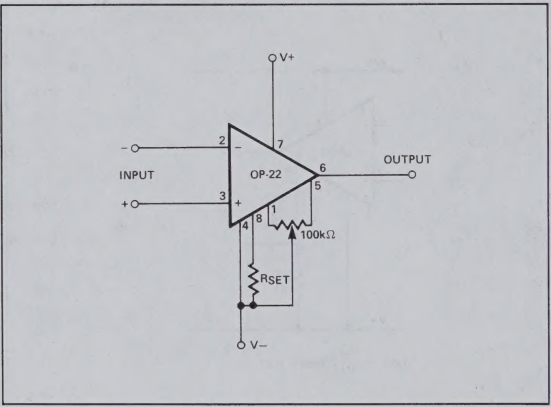
OFFSET VOLTAGE ADJUSTMENT

The offset voltage can be trimmed to zero using a 100kΩ potentiometer (see offset nulling circuit). Adjustment range is approximately ±5mV. Resolution of the nulling can be increased by using a smaller pot in conjunction with fixed resistors as shown below.

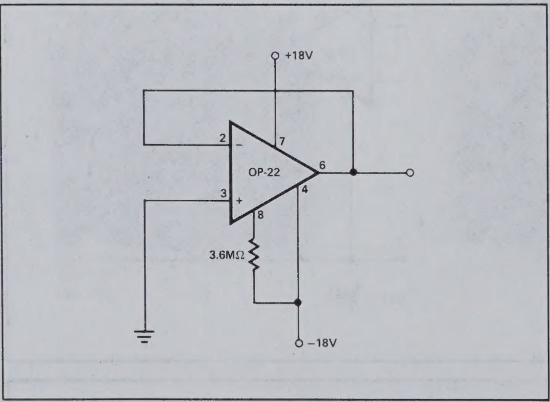

PIN 1
39kΩ
20kΩ
39kΩ
PIN 5
V−

This arrangement has a ±500μV adjustment range. Offset nulling of the OP-22 has negligible effect on the value of TCV_{OS}.

OFFSET NULLING CIRCUIT


V+
−
INPUT
+
2
3
7
OP-22
6
OUTPUT
5
1
4
8
100kΩ
RSET
V−

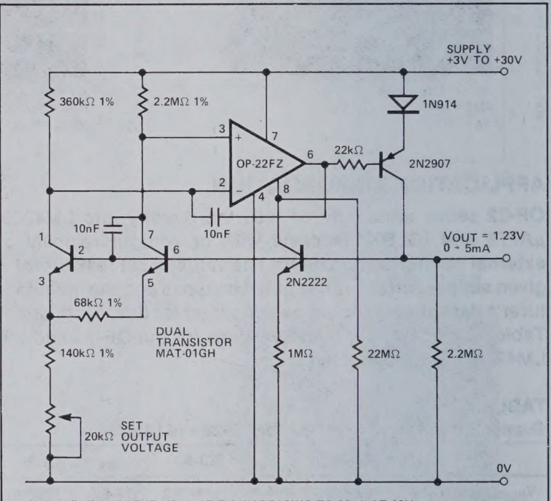
BURN-IN CIRCUIT


+18V
2
7
OP-22
6
3
4
8
3.6MΩ
−18V

APPLICATIONS CIRCUITS

A micropower bandgap voltage reference operating at a quiescent current of 15μA may be constructed using an OP-22 and a MAT-01 dual transistor (see Figure 1). The circuit provides a 1.23V reference with better performance than micropower I.C. shunt regulators and has the advantages of being a series regulator.

MICROPOWER 1.23 VOLT BANDGAP REFERENCE


SUPPLY
+3V TO +30V
360kΩ 1%
2.2MΩ 1%
1N914
3
7
OP-22FZ
6
22kΩ
2N2907
2
4
8
10nF
10nF
1
2
7
6
3
5
VOUT = 1.23V
0 → 5mA
2N2222
68kΩ 1%
DUAL
TRANSISTOR
MAT-01GH
140kΩ 1%
1MΩ
22MΩ
2.2MΩ
20kΩ
SET
OUTPUT
VOLTAGE
0V

QUIESCENT CURRENT, 15μA AT 5V INCREASING TO 20μA AT 10V.
OUTPUT VOLTAGE TEMPERATURE COEFFICIENT (OVER 0° TO 70°C), 20ppm/°C TYP.
LINE REGULATION, 0.01%/VOLT.
LOAD REGULATION, 0.001% /mA.

Figure 1

GATED MICROPOWER AMPLIFIER

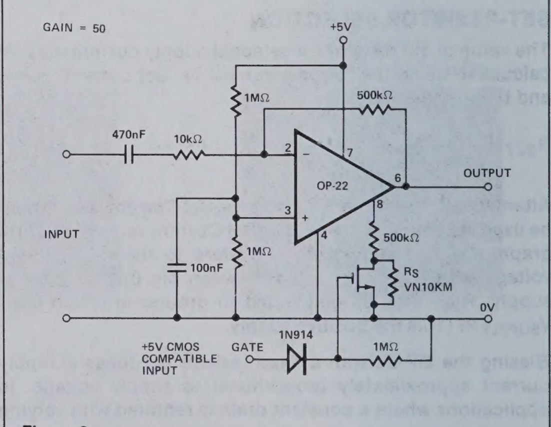
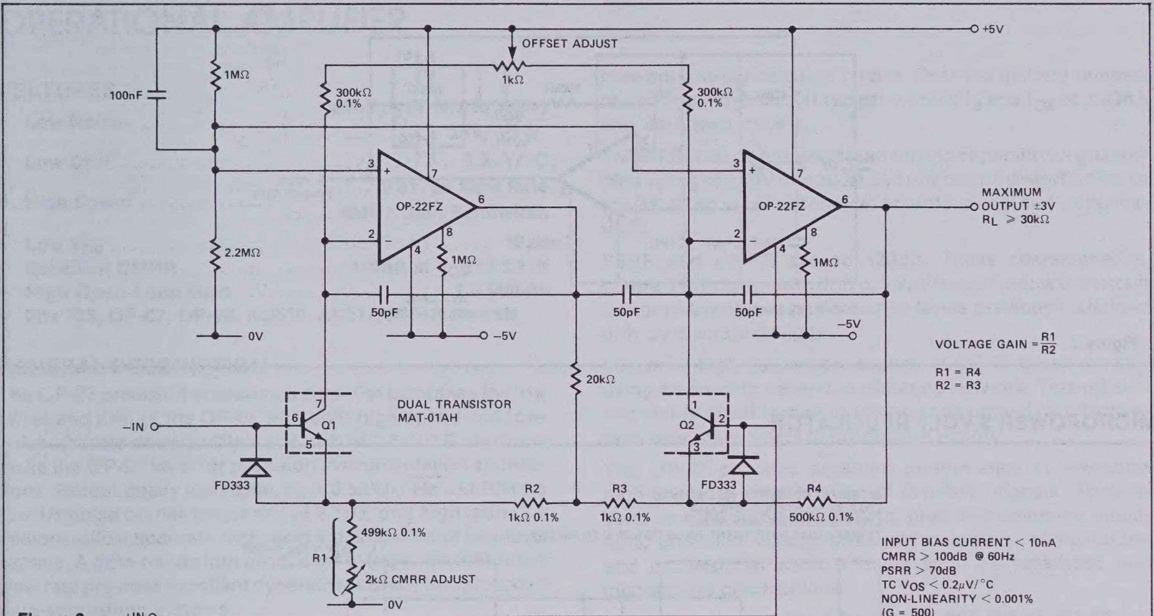

GAIN = 50
+5V
1MΩ
500kΩ
470nF
10kΩ
2
7
OP-22
6
OUTPUT
3
8
INPUT
4
500kΩ
1MΩ
100nF
RS
VN10KM
0V
1N914
+5V CMOS
COMPATIBLE
INPUT
GATE
1MΩ

Figure 2

MICROPOWER INSTRUMENTATION AMPLIFIER

POWER DRAIN ≤ 3mW WITH ±5 VOLT SUPPLIES


+5V
OFFSET ADJUST
1kΩ
1MΩ
100nF
300kΩ 0.1%
300kΩ 0.1%
OP-22FZ
OP-22FZ
3
2
7
6
4
8
1MΩ
1MΩ
MAXIMUM OUTPUT ±3V
$R_L \geq 30k\Omega$
2.2MΩ
50pF
50pF
50pF
0V
−5V
−5V
VOLTAGE GAIN = $\frac{R1}{R2}$
R1 = R4
R2 = R3
20kΩ
DUAL TRANSISTOR MAT-01AH
−IN
Q1
Q2
FD333
FD333
R2 1kΩ 0.1%
R3 1kΩ 0.1%
R4 500kΩ 0.1%
499kΩ 0.1%
R1
2kΩ CMRR ADJUST
0V
+IN

INPUT BIAS CURRENT < 10nA
CMRR > 100dB @ 60Hz
PSRR > 70dB
TC V_{OS} < 0.2μV/°C
NON-LINEARITY < 0.001%
(G = 500)

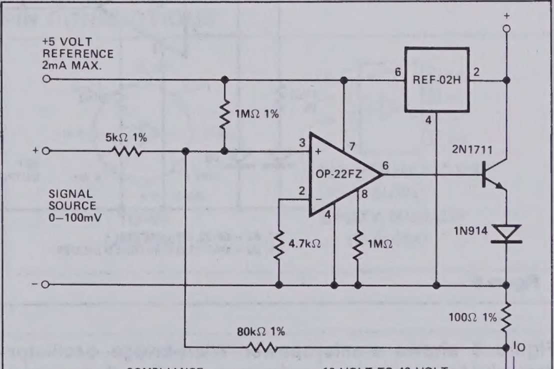
Figure 3

In Figure 2, the OP-22 is used as a gated amplifier where power consumption and bandwidth are controllable. R_S can be selected for a specific lower-power operation or omitted so the amplifier can be completely shut down.

A micropower instrumentation amplifier that consumes less than 3mW with ±5V supplies is shown in Figure 3. Offset voltage drift is better than 0.2μV/°C and common-mode input range is ±3V with CMRR of over 100dB at 60Hz.

Process control systems use two-wire 4-20mA current transmitters when sending analog signals through noisy environments. The "zero" or "offset" current of 4mA may be used to power the transmitter signal conditioning amplifiers and/or excite a d.c. transducer. This allows remote signal conditioning without having a remote power source. Power is provided at the receiving end where the signal current is monitored by a precision 50Ω resistor. The 4-20mA transmitter shown in Figure 4 has high stability, excellent linearity, and generates the 4-20mA current output. A 5V reference is available for powering transducers and micropower amplifiers at a maximum current of 2mA.

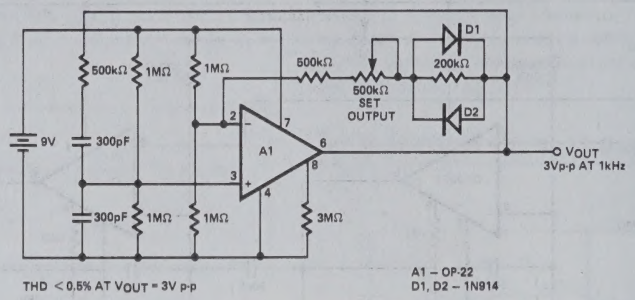
TWO TERMINAL 4-20mA TRANSMITTER


+5 VOLT REFERENCE 2mA MAX.
+
REF-02H
6
2
4
1MΩ 1%
5kΩ 1%
+
SIGNAL SOURCE 0–100mV
OP-22FZ
3
2
7
6
4
8
2N1711
1N914
4.7kΩ
1MΩ
−
100Ω 1%
80kΩ 1%
I_O
−

COMPLIANCE .... 10 VOLT TO 40 VOLT
LINEARITY .... 0.002% OF SPAN
LINE REJECTION, OFFSET 0.002%/VOLT
SPAN 0.005%/VOLT
TEMPERATURE COEFFICIENTS, OFFSET .... 0.002%/°C
(−25°C TO +85°C) SPAN .... 0.001%/°C

Figure 4

MICROPOWER WIEN-BRIDGE OSCILLATOR ($P_d < 500\mu W$)


500kΩ
1MΩ
1MΩ
500kΩ
500kΩ SET OUTPUT
200kΩ
D1
D2
9V
300pF
300pF
1MΩ
1MΩ
3MΩ
A1
2
3
4
6
7
8
VOUT
3Vp-p AT 1kHz

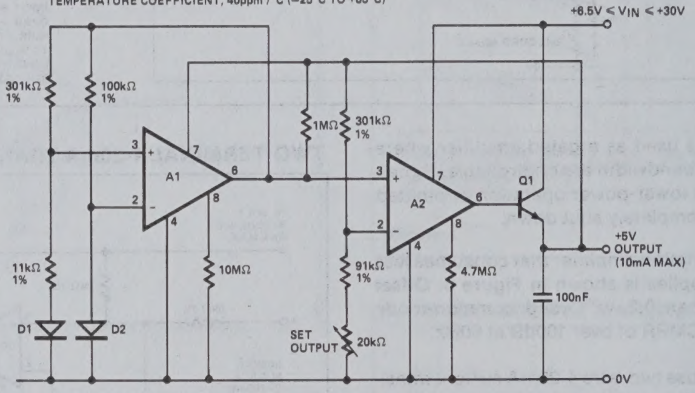
THD < 0.5% AT V_{OUT} = 3V p-p

A1 – OP-22
D1, D2 – 1N914

Figure 5

MICROPOWER 5 VOLT REGULATOR

QUIESCENT CURRENT ≈ 50µA AT 9V
LOAD REGULATION, 0.001% / mA
LINE REGULATION, 0.01% / VOLT
TEMPERATURE COEFFICIENT, 40ppm /°C (−25°C TO +85°C)


+6.5V ≤ VIN ≤ +30V
301kΩ 1%
100kΩ 1%
1MΩ
301kΩ 1%
A1
A2
Q1
2
3
4
6
7
8
11kΩ 1%
D1
D2
10MΩ
91kΩ 1%
SET OUTPUT
20kΩ
4.7MΩ
100nF
+5V OUTPUT (10mA MAX)
0V

A1, A2 – OP-22, Q1 – 2N2222
D1, D2 – MAT-01 OR MATCHED DIODES

Figure 6

Figure 5 shows a micropower Wien-bridge oscillator designed for battery-powered instrumentation. Output level is controlled by nonlinear elements D1 and D2. When adjusted for 3V p-p output, the distortion level is below 0.5% at 1kHz.

The 5 volt regulator in Figure 6 is intended for instrumentation requiring good power efficiency. Low-power 3-terminal IC regulators typically draw 2mA to 5mA quiescent current compared to only 50µA with this discrete implementation. Maximum load current is 10mA as shown, and can be increased by changing Q1 to a power transistor and proportionately increasing the set current of A2.

LOW-NOISE PRECISION OPERATIONAL AMPLIFIER

OP-27

FEATURES

- **Low Noise** .... **80nV$_{p-p}$ (0.1Hz to 10Hz)**, **3nV/$\sqrt{Hz}$**
- **Low Drift** .... **0.2μV/°C**
- **High Speed** .... **2.8V/μs Slew Rate**, **8MHz Gain Bandwidth**
- **Low V$_{OS}$** **10μV**
- **Excellent CMRR** .... **126dB at V$_{CM}$ of ±11V**
- **High Open-Loop Gain** .... **1.8 Million**
- **Fits 725, OP-07, OP-05, AD510, AD517, 5534A sockets**

GENERAL DESCRIPTION

The OP-27 precision operational amplifier combines the low offset and drift of the OP-07 with both high-speed and low-noise. Offsets down to 25μV and drift of 0.6μV/°C maximim make the OP-27 ideal for precision instrumentation applications. Exceptionally low noise, $e_n = 3.5nV/\sqrt{Hz}$, at 10Hz, a low 1/f noise corner frequency of 2.7Hz, and high gain (1.8 million), allow accurate high-gain amplification of low-level signals. A gain-bandwidth product of 8MHz and a 2.8V/μsec slew rate provides excellent dynamic accuracy in high-speed data-acquisition systems.

A low input bias current of ±10nA is achieved by use of a bias-current-cancellation circuit. Over the military temperature range, this circuit typically holds I_B and I_{OS} to ±20nA and 15nA respectively.

The output stage has good load driving capability. A guaranteed swing of ±10V into 600Ω and low output distortion make the OP-27 an excellent choice for professional audio applications.

PSRR and CMRR exceed 120dB. These characteristics, coupled with long-term drift of 0.2μV/month, allow the circuit designer to achieve performance levels previously attained only by discrete designs.

Low cost, high-volume production of OP-27 is achieved by using an on-chip zener-zap trimming network. This reliable and stable offset trimming scheme has proved its effectiveness over many years of production history.

The OP-27 provides excellent performance in low-noise high-accuracy amplification of low-level signals. Applications include stable integrators, precision summing amplifiers, precision voltage-threshold detectors, comparators, and professional audio circuits such as tape-head and microphone preamplifiers.

The OP-27 is a direct replacement for 725, OP-06, OP-07 and OP-05 amplifiers; 741 types may be directly replaced by removing the 741's nulling potentiometer.

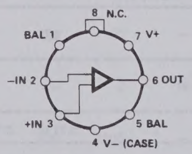
ORDERING INFORMATION†

$T_A = 25°C$ V_{OS} MAX (μV)	PACKAGE HERMETIC TO-99 8-PIN	PACKAGE HERMETIC DIP 8-PIN	PACKAGE PLASTIC DIP 8-PIN	OPERATING TEMPERATURE RANGE
25	OP27AJ*	OP27AZ*		MIL
25	OP27EJ	OP27EZ	OP27EP	IND/COM
60	OP27BJ*	OP27BZ*		MIL
60	OP27FJ	OP27FZ	OP27FP	IND/COM
100	OP27CJ*	OP27CZ*		MIL
100	OP27GJ	OP27GZ	OP27GP	IND/COM

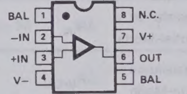
*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

PIN CONNECTIONS

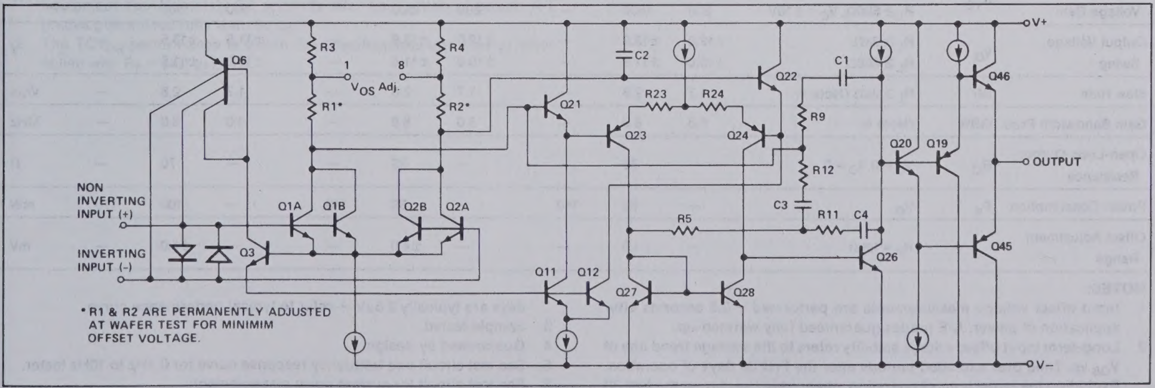


TO-99
(J-Suffix)



8-PIN HERMETIC DIP
(Z-Suffix)
EPOXY MINI-DIP
(P-Suffix)

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 4)

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	500mW
Input Voltage (Note 3)	±22V
Output Short-Circuit Duration	Indefinite
Differential Input Voltage (Note 2)	±0.7V
Differential Input Current (Note 2)	±25mA
Storage Temperature Range	−65° C to +150° C
Operating Temperature Range	
OP-27A, OP-27B, OP-27C (J, Z)	−55° C to +125° C
OP-27E, OP-27F, OP-27G (J, Z)	−25° C to +85° C
OP-27E, OP-27F, OP-27G (P)	0° C to +70° C
Lead Temperature Range (Soldering, 60 sec)	300° C
DICE Junction Temperature	−65° C to +150° C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80° C	7.1mW/° C
8-Pin Hermetic DIP (Z)	75° C	6.7mW/° C
8-Pin Plastic DIP (P)	62° C	5.6mW/° C

2. The OP-27's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.
3. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
4. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

			OP-27A/E			OP-27B/F			OP-27C/G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	10	25	—	20	60	—	30	100	µV
Long-Term V_{OS} Stability	V_{OS}/Time	(Note 2)	—	0.2	1.0	—	0.3	1.5	—	0.4	2.0	µV/Mo
Input Offset Current	I_{OS}		—	7	35	—	9	50	—	12	75	nA
Input Bias Current	I_B		—	±10	±40	—	±12	±55	—	±15	±80	nA
Input Noise Voltage	$e_{np\text{-}p}$	0.1Hz to 10Hz (Notes 3, 5)	—	0.08	0.18	—	0.08	0.18	—	0.09	0.25	µVp-p
Input Noise Voltage Density	e_n	$f_O = 10Hz$ (Note 3)	—	3.5	5.5	—	3.5	5.5	—	3.8	8.0	
		$f_O = 30Hz$ (Note 3)	—	3.1	4.5	—	3.1	4.5	—	3.3	5.6	nV/√Hz
		$f_O = 1000Hz$ (Note 3)	—	3.0	3.8	—	3.0	3.8	—	3.2	4.5	
Input Noise Current Density	i_n	$f_O = 10Hz$ (Notes 3,6)	—	1.7	4.0	—	1.7	4.0	—	1.7	—	
		$f_O = 30Hz$ (Notes 3,6)	—	1.0	2.3	—	1.0	2.3	—	1.0	—	pA/√Hz
		$f_O = 1000Hz$ (Notes 3, 6)	—	0.4	0.6	—	0.4	0.6	—	0.4	0.6	
Input Resistance — Differential-Mode	R_{IN}	(Note 4)	1.5	6	—	1.2	5	—	0.8	4	—	MΩ
Input Resistance — Common-Mode	R_{INCM}		—	3	—	—	2.5	—	—	2	—	GΩ
Input Voltage Range	IVR		±11.0	±12.3	—	±11.0	±12.3	—	±11.0	±12.3	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 11V$	114	126	—	106	123	—	100	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4V$ to $\pm 18V$	—	1	10	—	1	10	—	2	20	µV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	1000	1800	—	1000	1800	—	700	1500	—	V/mV
		$R_L \geq 600\Omega$, $V_O = \pm 10V$	800	1500	—	800	1500	—	600	1500	—	
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12.0	±13.8	—	±12.0	±13.8	—	±11.5	±13.5	—	V
		$R_L \geq 600\Omega$	±10.0	±11.5	—	±10.0	±11.5	—	±10.0	±11.5	—	
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 4)	1.7	2.8	—	1.7	2.8	—	1.7	2.8	—	V/µs
Gain Bandwidth Prod.	GBW	(Note 4)	5.0	8.0	—	5.0	8.0	—	5.0	8.0	—	MHz
Open-Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	70	—	—	70	—	—	70	—	Ω
Power Consumption	P_d	V_O	—	90	140	—	90	140	—	100	170	mW
Offset Adjustment Range		$R_P = 10k\Omega$	—	±4.0	—	—	±4.0	—	—	±4.0	—	mV

NOTES:

1. Input offset voltage measurements are performed ~ 0.5 seconds after application of power. A/E grades guaranteed fully warmed-up.
2. Long-term input offset voltage stability refers to the average trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2.5µV — refer to typical performance curve.
3. Sample tested.
4. Guaranteed by design.
5. See test circuit and frequency response curve for 0.1Hz to 10Hz tester.
6. See test circuit for current noise measurement.

ELECTRICAL CHARACTERISTICS for $V_S = \pm 15V$, $-55°C \le T_A \le +125°C$, unless otherwise noted.

			OP-27A			OP-27B			OP-27C			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	30	60	—	50	200	—	70	300	μV
Average Input Offset Drift	TCV_{OS} TCV_{OSn}	(Note 2)	—	0.2	0.6	—	0.3	1.3	—	0.4	1.8	μV/°C
Input Offset Current	I_{OS}		—	15	50	—	22	85	—	30	135	nA
Input Bias Current	I_B		—	±20	±60	—	±28	±95	—	±35	±150	nA
Input Voltage Range	IVR		±10.3	±11.5	—	±10.3	±11.5	—	±10.2	±11.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$	108	122	—	100	119	—	94	116	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	2	16	—	2	20	—	4	51	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$, $V_O = \pm 10V$	600	1200	—	500	1000	—	300	800	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±11.5	±13.5	—	±11.0	±13.2	—	±10.5	±13.0	—	V

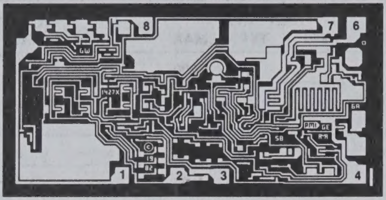
ELECTRICAL CHARACTERISTICS for $V_S = \pm 15V$, $-25°C \le T_A \le +85°C$ for OP-27J and OP-27Z, $0°C \le T_A \le +70°C$ for OP-27P, unless otherwise noted.

			OP-27E			OP-27F			OP-27G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		—	20	50	—	40	140	—	55	220	μV
Average Input Offset Drift	TCV_{OS} TCV_{OSn}	(Note 2)	—	0.2	0.6	—	0.3	1.3	—	0.4	1.8	μV/°C
Input Offset Current	I_{OS}		—	10	50	—	14	85	—	20	135	nA
Input Bias Current	I_B		—	±14	±60	—	±18	±95	—	±25	±150	nA
Input Voltage Range	IVR		±10.5	±11.8	—	±10.5	±11.8	—	±10.5	±11.8	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$	110	124	—	102	121	—	96	118	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	2	15	—	2	16	—	2	32	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$, $V_O = \pm 10V$	750	1500	—	700	1300	—	450	1000	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±11.7	±13.6	—	±11.4	±13.5	—	±11.0	±13.3	—	V

NOTES:

1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. A/E grades guaranteed fully warmed-up.
2. The TCV_{OS} performance is within the specifications unnulled or when nulled with $R_P = 8k\Omega$ to $20k\Omega$.

DICE CHARACTERISTICS



DIE SIZE 0.054 × 0.108 inch, 5832 sq. mils
(1.37 × 2.74mm, 3.76 sq. mm)

1. NULL
2. (–) INPUT
3. (+) INPUT
4. V–
6. OUTPUT
7. V+
8. NULL

For additional DICE information refer to Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$ for OP-27N, OP-27G, and OP-27GR devices; $T_A = 125°C$ for OP-27NT and OP-27GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-27NT LIMIT	OP-27N LIMIT	OP-27GT LIMIT	OP-27G LIMIT	OP-27GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	60	35	200	60	100	μV MAX
Input Offset Current	I_{OS}		50	35	85	50	75	nA MAX
Input Bias Current	I_B		±60	±40	±95	±55	±80	nA MAX
Input Voltage Range	IVR		±10.3	±11	±10.3	±11	±11	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = IVR$	108	114	100	106	100	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4V$ to $\pm 18V$	—	10	—	10	20	μV/V MAX
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	600	1000	500	1000	700	V/mV MIN
		$R_L \geq 600\Omega$, $V_O = \pm 10V$	—	800	—	800	600	
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±11.5	±12.0	±11.0	±12.0	±11.5	V MIN
		$R_L \geq 600\Omega$	—	±10.0	—	±10.0	±10.0	
Power Consumption	P_d	$V_O = 0$	—	140	—	140	170	mW MAX

Note: Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

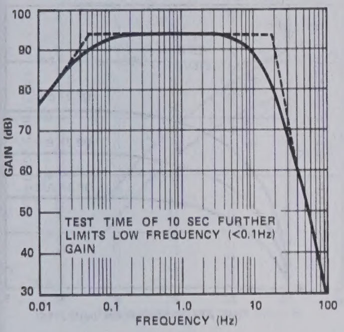
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-27N TYPICAL	OP-27G TYPICAL	OP-27GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS} or TCV_{OSn}	Nulled or Unnulled $R_P = 8k\Omega$ to $20k\Omega$	0.2	0.3	0.4	μV/°C
Average Input Offset Current Drift	TCI_{OS}		80	130	180	pA/°C
Average Input Bias Current Drift	TCI_B		100	160	200	pA/°C
Input Noise Voltage Density	e_n	$f_O = 10Hz$	3.5	3.5	3.8	$nV/\sqrt{Hz}$
		$f_O = 30Hz$	3.1	3.1	3.3	
		$f_O = 1000Hz$	3.0	3.0	3.2	
Input Noise Current Density	i_n	$f_O = 10Hz$	1.7	1.7	1.7	$pA/\sqrt{Hz}$
		$f_O = 30Hz$	1.0	1.0	1.0	
		$f_O = 1000Hz$	0.4	0.4	0.4	
Input Noise Voltage	$e_{np\text{-}p}$	0.1Hz to 10Hz	0.08	0.08	0.09	μVp-p
Slew Rate	SR	$R_L \geq 2k\Omega$	2.8	2.8	2.8	V/μs
Gain Bandwidth Product	GBW		8	8	8	MHz

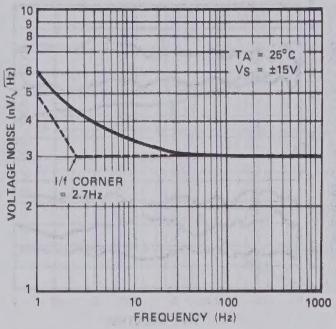
NOTE:
1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

TYPICAL PERFORMANCE CHARACTERISTICS

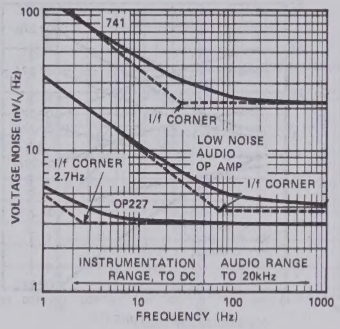
0.1Hz TO 10Hz$_{p-p}$ NOISE TESTER FREQUENCY RESPONSE



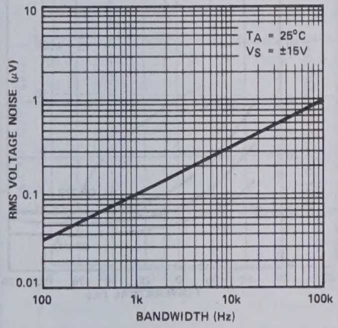
VOLTAGE NOISE DENSITY vs FREQUENCY



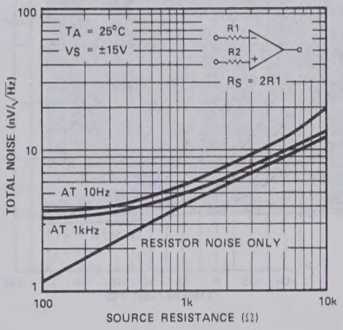
A COMPARISON OF OP AMP VOLTAGE NOISE SPECTRA



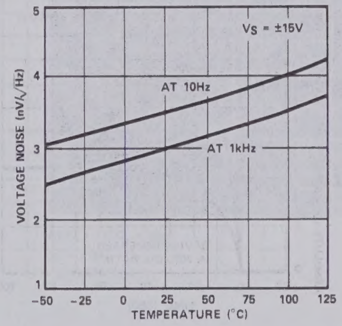
INPUT WIDEBAND VOLTAGE NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



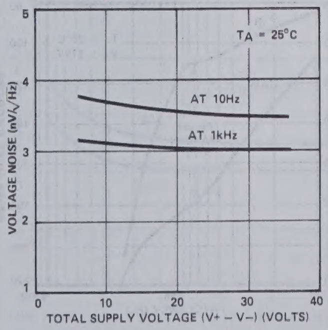
TOTAL NOISE vs SOURCE RESISTANCE



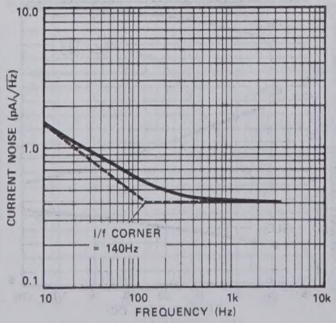
VOLTAGE NOISE DENSITY vs TEMPERATURE



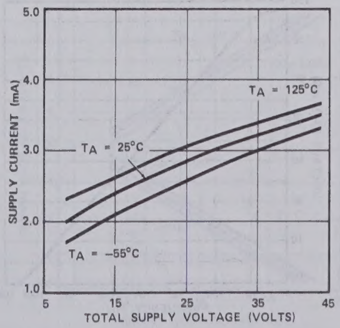
VOLTAGE NOISE DENSITY vs SUPPLY VOLTAGE



CURRENT NOISE DENSITY vs FREQUENCY

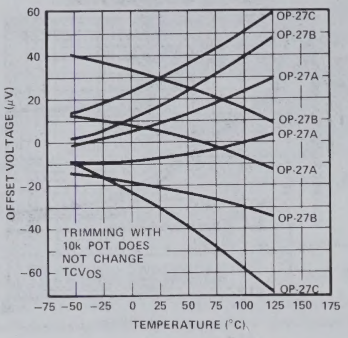


SUPPLY CURRENT vs SUPPLY VOLTAGE

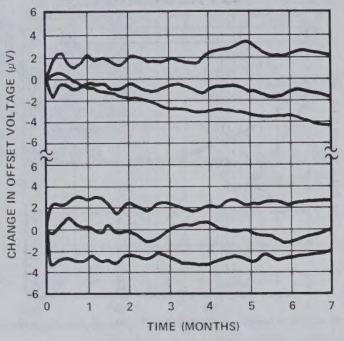


TYPICAL PERFORMANCE CHARACTERISTICS

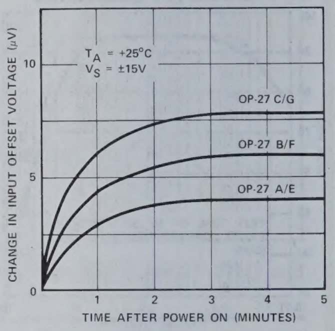
OFFSET VOLTAGE DRIFT OF EIGHT REPRESENTATIVE UNITS vs TEMPERATURE



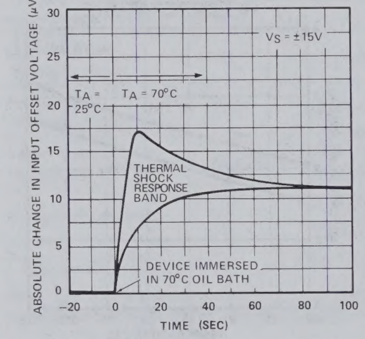
LONG-TERM OFFSET VOLTAGE DRIFT OF SIX REPRESENTATIVE UNITS



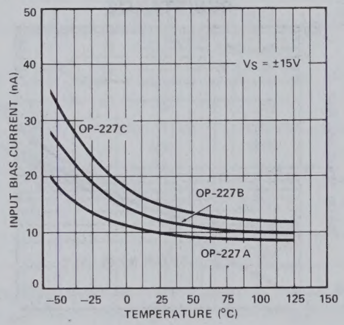
WARM-UP OFFSET VOLTAGE DRIFT



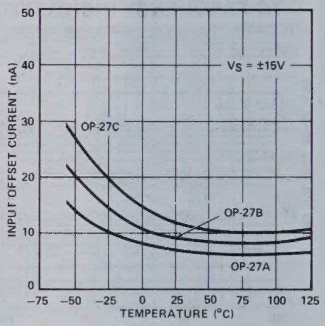
OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



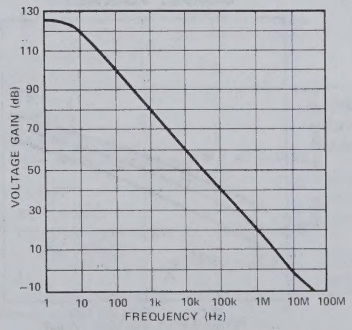
INPUT BIAS CURRENT vs TEMPERATURE



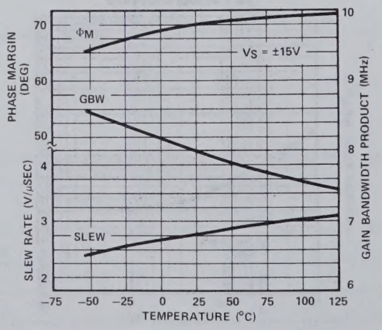
INPUT OFFSET CURRENT vs TEMPERATURE



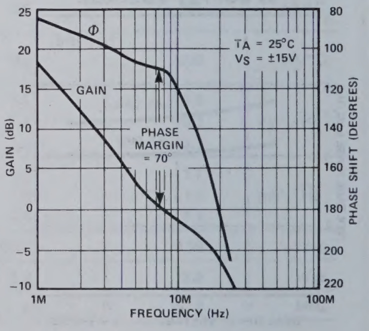
OPEN-LOOP GAIN vs FREQUENCY



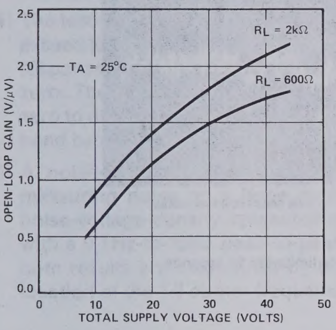
SLEW RATE, GAIN-BANDWIDTH PRODUCT, PHASE MARGIN vs TEMPERATURE

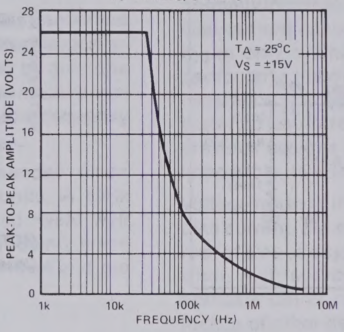


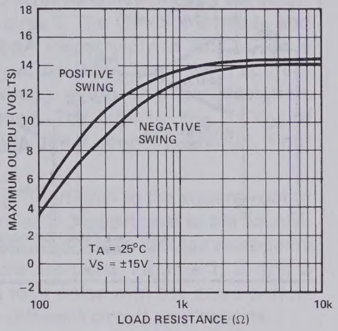
GAIN, PHASE SHIFT vs FREQUENCY

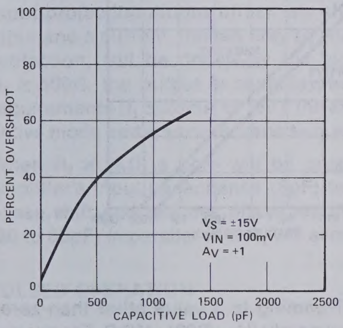


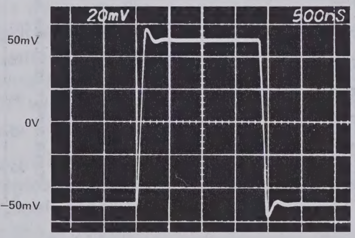
TYPICAL PERFORMANCE CHARACTERISTICS


OPEN-LOOP VOLTAGE GAIN vs SUPPLY VOLTAGE

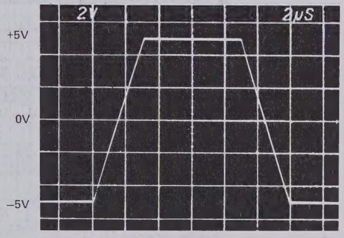

MAXIMUM OUTPUT SWING vs FREQUENCY


MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE

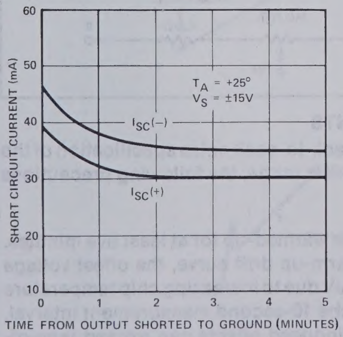

SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD

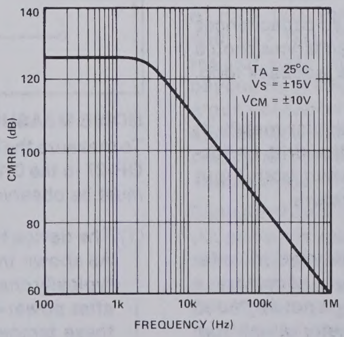

SMALL-SIGNAL TRANSIENT RESPONSE

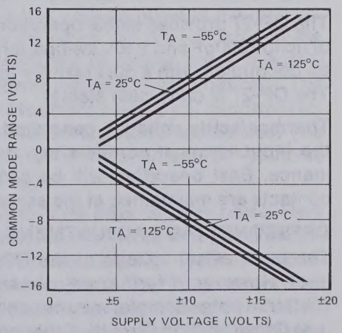
AVCL = +1
VS = ±15V
TA = 25°C


LARGE-SIGNAL TRANSIENT RESPONSE

AVCL = +1, CL = 15pF
VS = ±15V
TA = 25°C

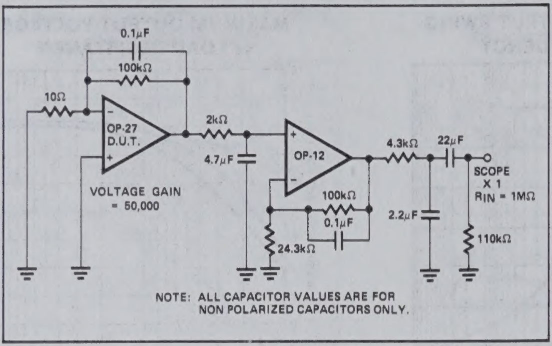

SHORT-CIRCUIT CURRENT vs TIME


CMRR vs FREQUENCY


COMMON-MODE INPUT RANGE vs SUPPLY VOLTAGE

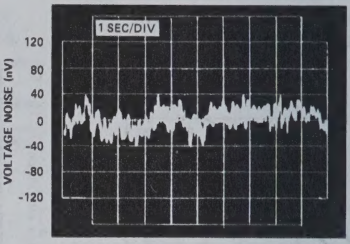
TYPICAL PERFORMANCE CHARACTERISTICS

VOLTAGE NOISE TEST CIRCUIT (0.1Hz-TO-10Hz)



NOTE: ALL CAPACITOR VALUES ARE FOR NON POLARIZED CAPACITORS ONLY.

LOW-FREQUENCY NOISE

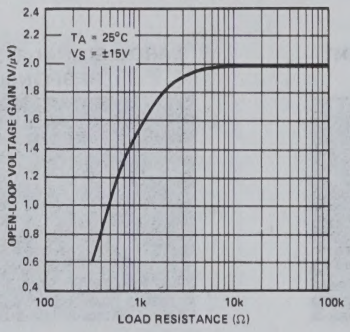


0.1Hz TO 10Hz PEAK-TO-PEAK NOISE

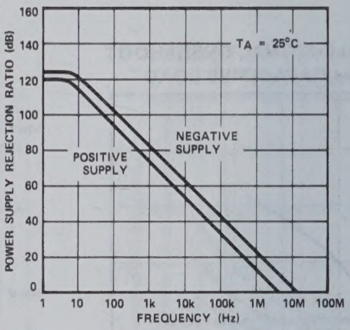
NOTE:

Observation time limited to 10 seconds.

OPEN-LOOP VOLTAGE GAIN vs LOAD RESISTANCE



PSRR vs FREQUENCY



APPLICATIONS INFORMATION

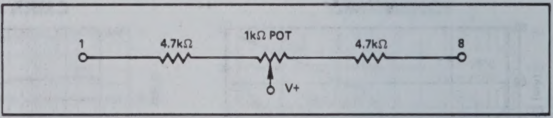
OP-27 Series units may be inserted directly into 725, OP-06, OP-07 and OP-05 sockets with or without removal of external compensation or nulling components. Additionally, the OP-27 may be fitted to unnulled 741-type sockets; however, if conventional 741 nulling circuitry is in use, it should be modified or removed to ensure correct OP-27 operation. OP-27 offset voltage may be nulled to zero (or other desired setting) using a potentiometer (see Offset Nulling Circuit).

The OP-27 provides stable operation with load capacitances of up to 2000pF and ±10V swings; larger capacitances should be decoupled with a 50Ω resistor inside the feedback loop. The OP-27 is unity-gain stable.

Thermoelectric voltages generated by dissimilar metals at the input terminal contacts can degrade the drift performance. Best operation will be obtained when both input contacts are maintained at the same temperature.

OFFSET VOLTAGE ADJUSTMENT

The input offset voltage of the OP-27 is trimmed at wafer level. However, if further adjustment of V_{OS} is necessary, a 10kΩ trim potentiometer may be used. TCV_{OS} is not degraded (see Offset Nulling Circuit). Other potentiometer values from 1kΩ to 1MΩ can be used with a slight degradation (0.1 to 0.2μV/°C) of TCV_{OS}. Trimming to a value other than zero creates a drift of approximately (V_{OS}/300) μV/°C. For example, the change in TCV_{OS} will be 0.33μV/°C if V_{OS} is adjusted to 100μV. The offset-voltage adjustment range with a 10kΩ potentiometer is ±4mV. If smaller adjustment range is required, the nulling sensitivity can be reduced by using a smaller pot in conjuction with fixed resistors. For example, the network below will have a ±280μV adjustment range.



NOISE MEASUREMENTS

To measure the 80nV peak-to-peak noise specification of the OP-27 in the 0.1Hz to 10Hz range, the following precautions must be observed:

(1) The device has to be warmed-up for at least five minutes. As shown in the warm-up drift curve, the offset voltage typically changes 4μV due to increasing chip temperature after power-up. In the 10-second measurement interval, these temperature-induced effects can exceed tens-of-nanovolts.

(2) For similar reasons, the device has to be well-shielded from air currents. Shielding minimizes thermocouple effects.

(3) Sudden motion in the vicinity of the device can also "feed-through" to increase the observed noise.

(4) The test time to measure 0.1Hz-to-10Hz noise should not exceed 10 seconds. As shown in the noise-tester frequency-response curve, the 0.1Hz corner is defined by only one zero. The test time of 10 seconds acts as an additional zero to eliminate noise contributions from the frequency band below 0.1Hz.

(5) A noise-voltage-density test is recommended when measuring noise on a large number of units. A 10Hz noise-voltage-density measurement will correlate well with a 0.1Hz-to-10Hz peak-to-peak noise reading, since both results are determined by the white noise and the location of the 1/f corner frequency.

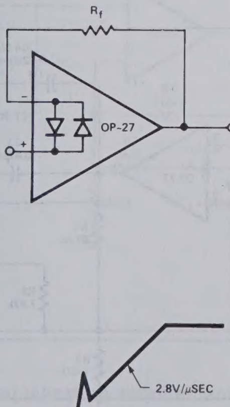
UNITY-GAIN BUFFER APPLICATIONS

When $R_f \leq 100\Omega$ and the input is driven with a fast, large signal pulse (>1V), the output waveform will look as shown in the pulsed operation diagram below.

During the fast feedthrough-like portion of the output, the input protection diodes effectively short the output to the input and a current, limited only by the output short-circuit protection, will be drawn by the signal generator. With $R_f \geq 500\Omega$, the output is capable of handling the current requirements ($I_L \leq 20mA$ at 10V); the amplifier will stay in its active mode and a smooth transition will occur.

When $R_f > 2k\Omega$, a pole will be created with R_f and the amplifier's input capacitance (8pF) that creates additional phase shift and reduces phase margin. A small capacitor (20 to 50pF) in parallel with R_f will eliminate this problem.

PULSED OPERATION



COMMENTS ON NOISE

The OP-27 is a very low-noise monolithic op amp. The outstanding input voltage noise characteristics of the OP-27 are achieved mainly by operating the input stage at a high quiescent current. The input bias and offset currents, which would normally increase, are held to reasonable values by the input-bias-current cancellation circuit. The OP-27A/E has I_B and I_{OS} of only ±40nA and 35nA respectively at 25°C. This is particularly important when the input has a high source-resistance. In addition, many audio amplifier designers prefer to use direct coupling. The high I_B, V_{OS}, TCV_{OS} of previous designs have made direct coupling difficult, if not impossible, to use.

Voltage noise is inversely proportional to the square-root of bias current, but current noise is proportional to the square-root of bias current. The OP-27's noise advantage disappears when high source-resistors are used. Figures 1, 2, and 3 compare OP-27 observed total noise with the noise performance of other devices in different circuit applications.

$$\text{Total noise} = \left[(\text{Voltage noise})^2 + (\text{current noise} \times R_S)^2 + (\text{resistor noise})^2\right]^{1/2}$$

Figure 1 shows noise-versus-source-resistance at 1000Hz. The same plot applies to wideband noise. To use this plot, just multiply the vertical scale by the square-root of the bandwidth.

NOISE vs SOURCE RESISTANCE (INCLUDING RESISTOR NOISE) AT 1000Hz.

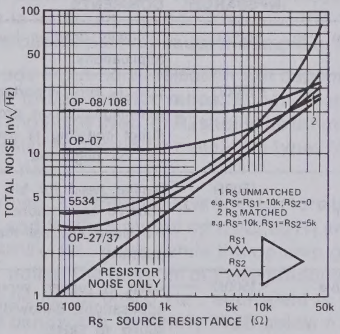


Figure 1

At $R_S < 1k\Omega$, the OP-27's low voltage noise is maintained. With $R_S > 1k\Omega$, total noise increases, but is dominated by the resistor noise rather than current or voltage noise. It is only beyond R_S of $20k\Omega$ that current noise starts to dominate. The argument can be made that current noise is not important for applications with low-to-moderate source resistances. The crossover between the OP-27 and OP-07 and OP-08 noise occurs in the 15-to-40kΩ region.

Figure 2 shows the 0.1Hz-to-10Hz peak-to-peak noise. Here the picture is less favorable; resistor noise is negligible, current noise becomes important because it is inversely proportional to the square-root of frequency. The crossover with the OP-07 occurs in the 3-to-5kΩ range depending on whether balanced or unbalanced source resistors are used (at 3kΩ the I_B, I_{OS} error also can be three times the V_{OS} spec.).

PEAK-TO-PEAK NOISE (0.1 to 10Hz) vs SOURCE RESISTANCE (INCLUDES RESISTOR NOISE).

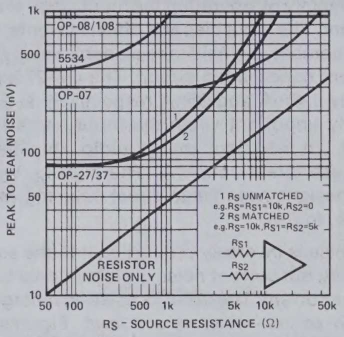


Figure 2

Therefore, for low-frequency applications, the OP-07 is better than the OP-27/37 when $R_S > 3k\Omega$. The only exception is when gain error is important. Figure 3 illustrates the 10Hz noise. As expected, the results are between the previous two figures.

For reference, typical source resistances of some signal sources are listed in Table 1.

Table 1

DEVICE	SOURCE IMPEDANCE	COMMENTS
Strain gauge	<500Ω	Typically used in low-frequency applications.
Magnetic tapehead	<1500Ω	Low I_B very important to reduce self-magnetization problems when direct coupling is used. OP-27 I_B can be neglected.
Magnetic phonograph cartridges	<1500Ω	Similar need for low I_B in direct coupled applications. OP-27 will not introduce any self-magnetization problem.
Linear variable differential transformer	<1500Ω	Used in rugged servo-feedback applications. Bandwidth of interest is 400Hz to 5kHz.

OPEN-LOOP GAIN

FREQUENCY AT:	OP-07	OP-27	OP-37
3Hz	100dB	124dB	125dB
10Hz	100dB	120dB	125dB
30Hz	90dB	110dB	124dB

For further information regarding noise calculations, see "Minimization of Noise in Op-Amp Applications", Application Note AN-15.

10Hz NOISE vs SOURCE RESISTANCE (INCLUDES RESISTOR NOISE).

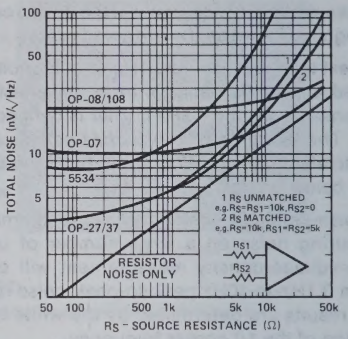


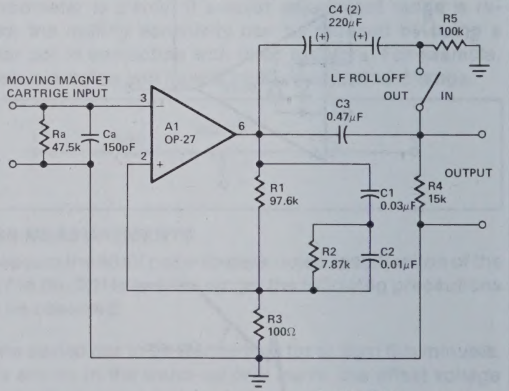
Figure 3

AUDIO APPLICATIONS

The following applications information has been abstracted from a PMI article in the 12/20/80 issue of Electronic Design magazine and updated.

Figure 4 is an example of a phono pre-amplifier circuit using the OP-27 for A_1; R_1-R_2-C_1-C_2 form a very accurate RIAA network with standard component values. The popular method to accomplish RIAA phono equalization is to employ frequency-dependent feedback around a high-quality gain block. Properly chosen, an RC network can provide the three necessary time constants of 3180, 318, and 75μs.[1]

For initial equalization accuracy and stability, precision metal-film resistors and film capacitors of polystyrene or polypropylene are recommended since they have low voltage coefficients, dissipation factors, and dielectric absorption.[4] (High-K ceramic capacitors should be avoided here, though low-K ceramics—such as NPO types, which have excellent dissipation factors, and somewhat lower dielectric absorption—can be considered for small values.)



$$G = \text{1kHz GAIN} = 0.101\ \left(1 + \frac{R1}{R3}\right) = 98.677\ \text{(39.9 dB) AS SHOWN}$$

Figure 4

The OP-27 brings a $3.2\text{nV}/\sqrt{\text{Hz}}$ voltage noise and $0.45\ \text{pA}/\sqrt{\text{Hz}}$ current noise to this circuit. To minimize noise from other sources, R_3 is set to a value of 100Ω, which generates a voltage noise of $1.3\text{nV}/\sqrt{\text{Hz}}$. The noise increases the $3.2\text{nV}/\sqrt{\text{Hz}}$ of the amplifier by only 0.7dB. With a 1kΩ source, the circuit noise measures 63dB below a 1mV reference level, unweighted, in a 20kHz noise bandwidth.

Gain (G) of the circuit at 1kHz can be calculated by the expression:

$$G = 0.101\left(1 + \frac{R_1}{R_3}\right)$$

For the values shown, the gain is just under 100 (or 40dB). Lower gains can be accommodated by increasing R_3, but gains higher than 40dB will show more equalization errors because of the 8MHz gain-bandwidth of the OP-27.

This circuit is capable of very low distortion over its entire range, generally below 0.01% at levels up to 7V rms. At 3V output levels, it will produce less than 0.03% total harmonic distortion at frequencies up to 20kHz.

Capacitor C_3 and resistor R_4 form a simple −6dB-per-octave rumble filter, with a corner at 22Hz. As an option, the switch-selected shunt capacitor C_4, a nonpolarized electrolytic, bypasses the low-frequency rolloff. Placing the rumble filter's high-pass action after the preamp has the desirable result of discriminating against the RIAA-amplified low-frequency noise components and pickup-produced low-frequency disturbances.

A preamplifier for NAB tape playback is similar to an RIAA phono preamp, though more gain is typically demanded, along with equalization requiring a heavy low-frequency boost. The circuit in Fig. 4 can be readily modified for tape use, as shown by Fig. 5.

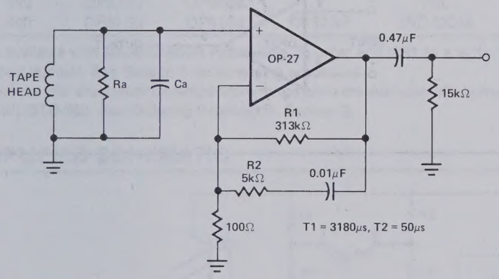


Figure 5

While the tape-equalization requirement has a flat high-frequency gain above 3kHz ($T_2 = 50\mu s$), the amplifier need not be stabilized for unity gain. The decompensated OP-37 provides a greater bandwidth and slew rate. For many applications, the idealized time constants shown may require trimming of R_1 and R_2 to optimize frequency response for nonideal tape-head performance and other factors.[5]

The network values of the configuration yield a 50dB gain at 1kHz, and the dc gain is greater than 70dB. Thus, the worst-case output offset is just over 500mV. A single 0.47μF output capacitor can block this level without affecting the dynamic range.

The tape head can be coupled directly to the amplifier input, since the worst-case bias current of 80nA with a 400mH, 100 μin. head (such as the PRB2H7K) will not be troublesome.

One potential tape-head problem is presented by amplifier bias-current transients which can magnetize a head. The OP-27 and OP-37 are free of bias-current transients upon power up or power down. However, it is always advantageous to control the speed of power supply rise and fall, to eliminate transients.

In addition, the dc resistance of the head should be carefully controlled, and preferably below 1kΩ. For this configuration, the bias-current-induced offset voltage can be greater than the 100μV maximum offset if the head resistance is not sufficiently controlled.

A simple, but effective, fixed-gain transformerless microphone preamp (Fig. 6) amplifies differential signals from low-impedance microphones by 50dB, and has an input impedance of 2kΩ. Because of the high working gain of the circuit, an OP-37 helps to preserve bandwidth, which will be 110kHz. As the OP-37 is a decompensated device (minimum stable gain of 5), a dummy resistor, R_p, may be necessary, if the microphone is to be unplugged. Otherwise the 100% feedback from the open input may cause the amplifier to oscillate.

Common-mode input-noise rejection will depend upon the match of the bridge-resistor ratios. Either close-tolerance (0.1%) types should be used, or R_4 should be trimmed for best CMRR. All resistors should be metal-film types for best stability and low noise.

Noise performance of this circuit is limited more by the input resistors R_1 and R_2 than by the op amp, as R_1 and R_2 each generate a $4\text{nV}/\sqrt{\text{Hz}}$ noise, while the op amp generates a $3.2\text{nV}/\sqrt{\text{Hz}}$ noise. The rms sum of these predominant noise sources will be about $6\text{nV}/\sqrt{\text{Hz}}$, equivalent to 0.9μV in a 20kHz noise bandwidth, or nearly 61dB below a 1mV input signal. Measurements confirm this predicted performance.

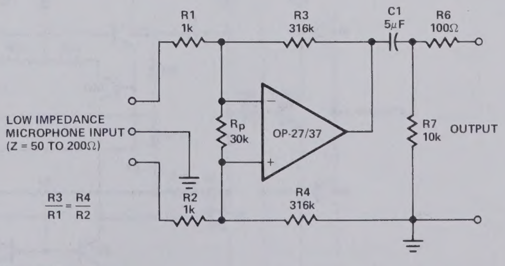


Figure 6

For applications demanding appreciably lower noise, a high-quality microphone-transformer-coupled preamp (Fig. 7) incorporates the internally-compensated OP-27. T_1 is a JE-115K-E 150Ω/15kΩ transformer which provides an optimum source resistance for the OP-27 device. The circuit has an overall gain of 40dB, the product of the transformer's voltage setup and the op amp's voltage gain.

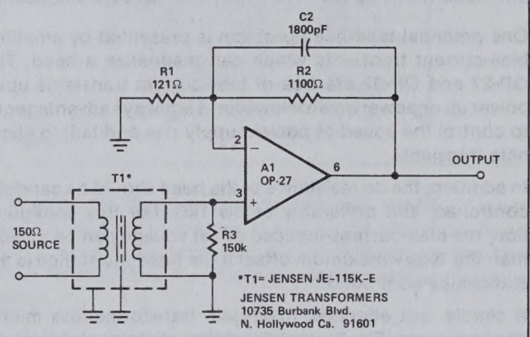


Figure 7

Gain may be trimmed to other levels, if desired, by adjusting R_2 or R_1. Because of the low offset voltage of the OP-27, the output offset of this circuit will be very low, 1.7mV or less, for a 40dB gain. The typical output blocking capacitor can be eliminated in such cases, but is desirable for higher gains to eliminate switching transients.

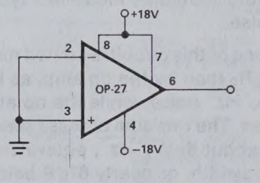
Capacitor C_2 and resistor R_2 form a 2µs time constant in this circuit, as recommended for optimum transient response by the transformer manufacturer. With C_2 in use, A_1 must have unity-gain stability. For situations where the 2µs time constant is not necessary, C_2 can be deleted, allowing the faster OP-37 to be employed.

Some comment on noise is appropriate to understand the capability of this circuit. A 150Ω resistor and R_1 and R_2 gain resistors connected to a noiseless amplifier will generate 220 nV of noise in a 20kHz bandwidth, or 73dB below a 1mV reference level. Any practical amplifier can only approach this noise level; it can never exceed it. With the OP-27 and T_1 specified, the additional noise degradation will be close to 3.6dB (or −69.5 referenced to 1mV).

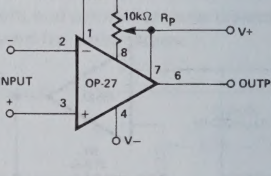
References

1. Lipshitz, S.P., "On RIAA Equalization Networks," *JAES*, Vol. 27, June 1979, p. 458-481.
2. Jung, W.G., *IC Op Amp Cookbook*, 2nd Ed., H.W. Sams and Company, 1980.
3. Jung, W.G., *Audio IC Op Amp Applications*, 2nd Ed., H.W. Sams and Company, 1978.
4. Jung, W.G., and Marsh, R.M., "Picking Capacitors," *Audio*, February & March, 1980.
5. Otala, M., "Feedback-Generated Phase Nonlinearity in Audio Amplifiers," London AES Convention, March 1980, preprint 1976.
6. Stout, D.F., and Kaufman, M., *Handbook of Operational Amplifier Circuit Design*, New York, McGraw Hill, 1976.

BURN-IN CIRCUIT



OFFSET NULLING CIRCUIT



LOW-NOISE PRECISION HIGH-SPEED OPERATIONAL AMPLIFIER ($A_{VCL} \geq 5$)

OP-37

FEATURES

- **Low Noise** .... 80nV p-p (0.1Hz to 10Hz); 3nV/$\sqrt{Hz}$ at 1kHz
- **Low Drift** .... 0.2μV/°C
- **High Speed** .... 17V/μs Slew Rate; 63MHz Gain Bandwidth
- **Low Input Offset Voltage** 10μV
- **Excellent CMRR** ... 126dB (Common-Voltage of ±11V)
- **High Open-Loop Gain** .... 1.8 Million
- **Replaces 725, OP-05, OP-06, OP-07, AD510, AD517, SE5534 in Gains >5**

GENERAL DESCRIPTION

The OP-37 provides the same high performance as the OP-27, but the design is optimized for circuits with gains greater than five. This design change increases slew rate to 17V/μsec and gain-bandwidth product to 63MHz.

The OP-37 provides the low offset and drift of the OP-07 plus higher speed and lower noise. Offsets down to 25μV and drift of 0.6μV/°C maximum make the OP-37 ideal for precision instrumentation applications. Exceptionally low noise (e_n=3.5nV/$\sqrt{Hz}$ at 10Hz), a low 1/f noise corner frequency of 2.7Hz, and the high gain of 1.8 million, allow accurate high-gain amplification of low-level signals.

The low input bias current of ±10nA and offset current of 7nA are achieved by using a bias-current-cancellation circuit. Over the military temperature range this typically holds I_B and I_{OS} to ±20nA and 15nA respectively.

The output stage has good load driving capability. A guaranteed swing of ±10V into 600Ω and low output distortion make the OP-37 an excellent choice for professional audio applications.

PSRR and CMRR exceed 120dB. These characteristics, coupled with long-term drift of 0.2μV/month, allow the circuit designer to achieve performance levels previously attained only by discrete designs.

Low-cost, high-volume production of the OP-37 is achieved by using on-chip zener-zap trimming. This reliable and stable offset trimming scheme has proved its effectiveness over many years of production history.

The OP-37 brings low-noise instrumentation-type performance to such diverse applications as microphone, tapehead, and RIAA phono preamplifiers, high-speed signal conditioning for data acquisition systems, and wide-bandwidth instrumentation.

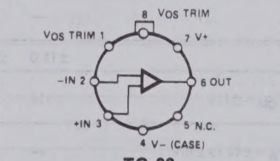
ORDERING INFORMATION†

T_A = 25°C V_{OS} MAX (μV)	PACKAGE HERMETIC TO-99 8-PIN	HERMETIC DIP 8-PIN	PLASTIC DIP 8-PIN	OPERATING TEMPERATURE RANGE
25	OP37AJ*	OP37AZ*		MIL
25	OP37EJ	OP37EZ	OP37EP	IND/COM
60	OP37BJ*	OP37BZ*		MIL
60	OP37FJ	OP37FZ	OP37FP	IND/COM
100	OP37CJ*	OP37CZ*		MIL
100	OP37GJ	OP37GZ	OP37GP	IND/COM

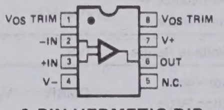
*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

PIN CONNECTIONS


8 VOS TRIM
VOS TRIM 1
7 V+
–IN 2
6 OUT
+IN 3
5 N.C.
4 V– (CASE)

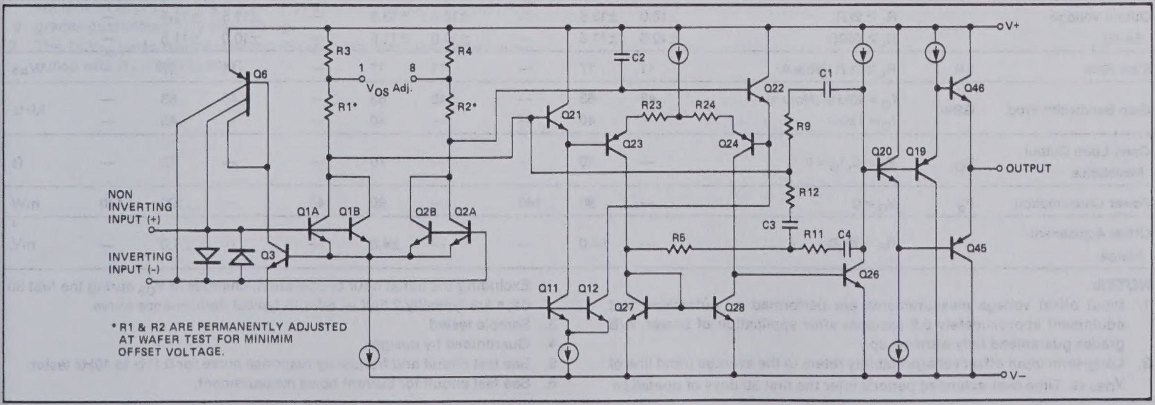
TO-99 (J-Suffix)


VOS TRIM 1
–IN 2
+IN 3
V– 4
8 VOS TRIM
7 V+
6 OUT
5 N.C.

8-PIN HERMETIC DIP (Z-Suffix)

EPOXY MINI-DIP (P-Suffix)

SIMPLIFIED SCHEMATIC


V+
R3
R4
1
8
VOS Adj.
R1*
R2*
Q6
Q21
C2
Q22
C1
Q46
R23
R24
R9
Q23
Q24
Q20
Q19
OUTPUT
R12
NON INVERTING INPUT (+)
INVERTING INPUT (–)
Q1A
Q1B
Q2B
Q2A
Q3
C3
R5
R11
C4
Q45
Q26
Q11
Q12
Q27
Q28
V–
*R1 & R2 ARE PERMANENTLY ADJUSTED AT WAFER TEST FOR MINIMIM OFFSET VOLTAGE.

ABSOLUTE MAXIMUM RATINGS (Note 4)

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	500mW
Input Voltage (Note 3)	±22V
Output Short-Circuit Duration	Indefinite
Differential Input Voltage (Note 2)	±0.7V
Differential Input Current (Note 2)	±25mA
Storage Temperature Range	−65° C to +150° C
Operating Temperature Range	
OP-37A, OP-37B, OP-37C (J, Z)	−55° C to +125° C
OP-37E, OP-37F, OP-37G (J, Z)	−25° C to +85° C
OP-37E, OP-37F, OP-37G (P)	0° C to +70° C
Lead Temperature Range (Soldering, 60 sec)	300° C
DICE Junction Temperature	−65° C to +150° C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80° C	7.1mW/° C
8-Pin Hermetic DIP (Z)	75° C	6.7mW/° C
8-Pin Plastic DIP (P)	62° C	5.6mW/° C

2. The OP-37's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.
3. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
4. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

			OP-37A/E			OP-37B/F			OP-37C/G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	10	25	—	20	60	—	30	100	μV
Long-Term V_{OS} Stability	V_{OS}/Time	(Note 2)	—	0.2	1.0	—	0.3	1.5	—	0.4	2.0	μV/Mo
Input Offset Current	I_{OS}		—	7	35	—	9	50	—	12	75	nA
Input Bias Current	I_B		—	±10	±40	—	±12	±55	—	±15	±80	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Notes 3, 5)	—	0.08	0.18	—	0.08	0.18	—	0.09	0.25	μVp-p
Input Noise Voltage Density	e_n	f_O = 10Hz (Note 3) f_O = 30Hz (Note 3) f_O = 1000Hz (Note 3)	— — —	3.5 3.1 3.0	5.5 4.5 3.8	— — —	3.5 3.1 3.0	5.5 4.5 3.8	— — —	3.8 3.3 3.2	8.0 5.6 4.5	nV/$\sqrt{Hz}$
Input Noise Current Density	i_n	f_O = 10Hz (Notes 3, 6) f_O = 30Hz (Notes 3, 6) f_O = 1000Hz (Notes 3, 6)	— — —	1.7 1.0 0.4	4.0 2.3 0.6	— — —	1.7 1.0 0.4	4.0 2.3 0.6	— — —	1.7 1.0 0.4	— — 0.6	pA/$\sqrt{Hz}$
Input Resistance — Differential-Mode	R_{IN}	(Note 4)	1.5	6	—	1.2	5	—	0.8	4	—	MΩ
Input Resistance — Common-Mode	R_{INCM}		—	3	—	—	2.5	—	—	2	—	GΩ
Input Voltage Range	IVR		±11.0	±12.3	—	±11.0	±12.3	—	±11.0	±12.3	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 11V$	114	126	—	106	123	—	100	120	—	dB
Power Supply Rejection Ratio	PSSR	$V_S = \pm 4V$ to $\pm 18V$	—	1	10	—	1	10	—	2	20	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$ $R_L \geq 1k\Omega$, $V_O = \pm 10V$ $R_L = 600\Omega$, $V_O = \pm 1V$, $V_S = \pm 4V$ (Note 4)	1000 800 250	1800 1500 700	— — —	1000 800 250	1800 1500 700	— — —	700 400 200	1500 1500 500	— — —	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$ $R_L \geq 600\Omega$	±12.0 ±10.0	±13.8 ±11.5	— —	±12.0 ±10.0	±13.8 ±11.5	— —	±11.5 ±10.0	±13.5 ±11.5	— —	V
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 4)	11	17	—	11	17	—	11	17	—	V/μs
Gain Bandwidth Prod.	GBW	f_O = 10kHz (Note 4) f_O = 1MHz	45 —	63 40	— —	45 —	63 40	— —	45 —	63 40	— —	MHz
Open-Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	70	—	—	70	—	—	70	—	Ω
Power Consumption	P_d	$V_O = 0$	—	90	140	—	90	140	—	100	170	mW
Offset Adjustment Range		$R_P = 10k\Omega$	—	±4.0	—	—	±4.0	—	—	±4.0	—	mV,

NOTES:

1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. A/E grades guaranteed fully warmed-up.
2. Long-term input offset voltage stability refers to the average trend line of V_{OSd} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2.5μV — refer to typical performance curve.
3. Sample tested.
4. Guaranteed by design.
5. See test circuit and frequency response curve for 0.1Hz to 10Hz tester.
6. See test circuit for current noise measurement.

ELECTRICAL CHARACTERISTICS for $V_S = \pm15V$, $-55°C \le T_A \le +125°C$, unless otherwise noted.

			OP-37A			OP-37B			OP-37C			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	30	60	—	50	200	—	70	300	μV
Average Input Offset Drift	TCV_{OS} TCV_{OSn}	(Note 2)	—	0.2	0.6	—	0.3	1.3	—	0.4	1.8	μV/°C
Input Offset Current	I_{OS}		—	15	50	—	22	85	—	30	135	nA
Input Bias Current	I_B		—	±20	±60	—	±28	±95	—	±35	±150	nA
Input Voltage Range	IVR		±10.3	±11.5	—	±10.3	±11.5	—	±10.2	±11.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm10V$	108	122	—	100	119	—	94	116	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm4.5V$ to $\pm18V$	—	2	16	—	2	20	—	4	51	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$, $V_O = \pm10V$	600	1200	—	500	1000	—	300	800	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±11.5	±13.5	—	±11.0	±13.2	—	±10.5	±13.0	—	V

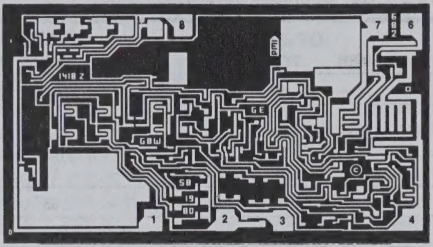
ELECTRICAL CHARACTERISTICS for $V_S = \pm15V$, $-25°C \le T_A \le +85°C$ for OP-37J and OP-37Z, $0°C \le T_A \le +70°C$ for OP-37P, unless otherwise noted.

			OP-37E			OP-37F			OP-37G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		—	20	50	—	40	140	—	55	220	μV
Average Input Offset Drift	TCV_{OS} TCV_{OSn}	(Note 2)	—	0.2	0.6	—	0.3	1.3	—	0.4	1.8	μV/°C
Input Offset Current	I_{OS}		—	10	50	—	14	85	—	20	135	nA
Input Bias Current	I_B		—	±14	±60	—	±18	±95	—	±25	±150	nA
Input Voltage Range	IVR		±10.5	±11.8	—	±10.5	±11.8	—	±10.5	±11.8	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm10V$	110	124	—	102	121	—	96	118	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm4.5V$ to $\pm18V$	—	2	15	—	2	16	—	2	32	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$, $V_O = \pm10V$	750	1500	—	700	1300	—	450	1000	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±11.7	±13.6	—	±11.4	±13.5	—	±11.0	±13.3	—	V

NOTES:

1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. A/E grades guaranteed fully warmed-up.
2. The TCV_{OS} performance is within the specifications unnulled or when nulled with $R_P = 8k\Omega$ to $20k\Omega$.

DICE CHARACTERISTICS



DIE SIZE 0.054 × 0.096 inch, 5184 sq. mils
(1.37 × 2.44mm, 3.35 sq. mm)

1. NULL
2. (−) INPUT
3. (+) INPUT
4. V−
6. OUTPUT
7. V+
8. NULL

For additional DICE information refer to Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

			OP-37N	OP-37G	OP-37GR	
PARAMETER	**SYMBOL**	**CONDITIONS**	**LIMIT**	**LIMIT**	**LIMIT**	**UNITS**
Input Offset Voltage	V_{OS}	(Note 1)	35	60	100	μV MAX
Input Offset Current	I_{OS}		35	50	75	nA MAX
Input Bias Current	I_B		±40	±55	±80	nA MAX
Input Voltage Range	IVR		±11	±11	±11	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 11V$	114	106	100	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4V$ to $\pm 18V$	10	10	20	μV/V MAX
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	1000	1000	700	V/mV MIN
		$R_L \geq 1k\Omega$, $V_O = \pm 10V$	800	800	—	
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12.0	±12.0	±11.5	V MIN
		$R_L \geq 600\Omega$	±10.0	±10.0	±10.0	
Power Consumption	P_d	$V_O = 0$	140	140	170	mW MAX

Note: Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

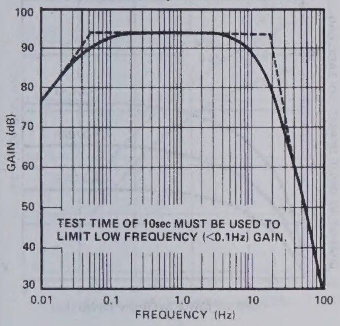
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

			OP-37N	OP-37G	OP-37GR	
PARAMETER	**SYMBOL**	**CONDITIONS**	**TYPICAL**	**TYPICAL**	**TYPICAL**	**UNITS**
Average Input Offset Voltage Drift	TCV_{OS} or TCV_{OSn}	Nulled or Unnulled $R_P = 8k\Omega$ to $20k\Omega$	0.2	0.3	0.4	μV/°C
Average Input Offset Current Drift	TCI_{OS}		80	130	180	pA/°C
Average Input Bias Current Drift	TCI_B		100	160	200	pA/°C
Input Noise Voltage Density	e_n	$f_O = 10Hz$	3.5	3.5	3.8	$nV/\sqrt{Hz}$
		$f_O = 30Hz$	3.1	3.1	3.3	
		$f_O = 1000Hz$	3.0	3.0	3.2	
Input Noise Current Density	i_n	$f_O = 10Hz$	1.7	1.7	1.7	$pA/\sqrt{Hz}$
		$f_O = 30Hz$	1.0	1.0	1.0	
		$f_O = 1000Hz$	0.4	0.4	0.4	
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	0.08	0.08	0.09	μVp-p
Slew Rate	SR	$R_L \geq 2k\Omega$	17	17	17	V/μs
Gain Bandwidth Product	GBW	$f_O = 10kHz$	63	63	63	MHz

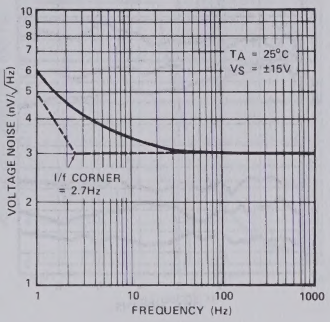
NOTE:
1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

TYPICAL PERFORMANCE CHARACTERISTICS

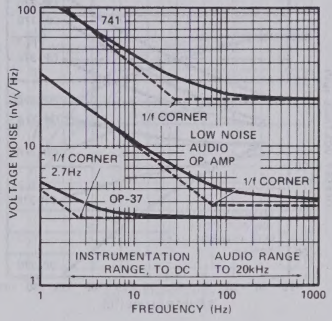
NOISE-TESTER FREQUENCY RESPONSE (0.1Hz TO 10Hz)



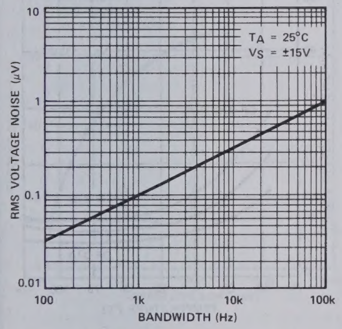
VOLTAGE NOISE DENSITY vs FREQUENCY



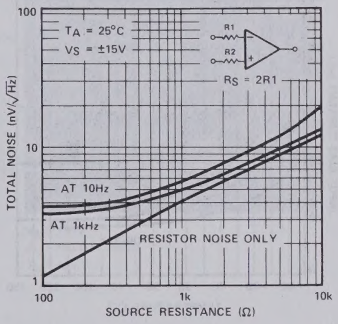
A COMPARISON OF OP AMP VOLTAGE NOISE SPECTRA



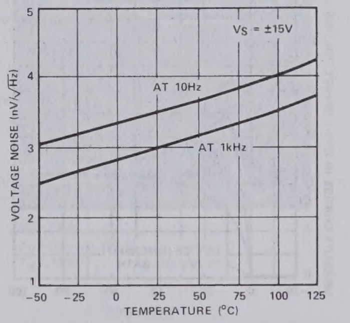
INPUT WIDEBAND VOLTAGE NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



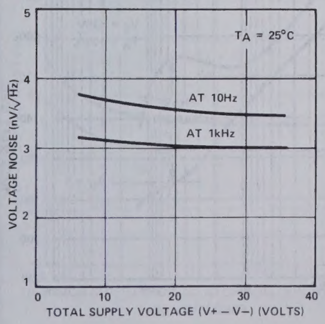
TOTAL NOISE vs SOURCE RESISTANCE



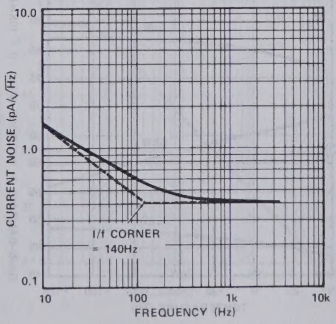
VOLTAGE NOISE DENSITY vs TEMPERATURE



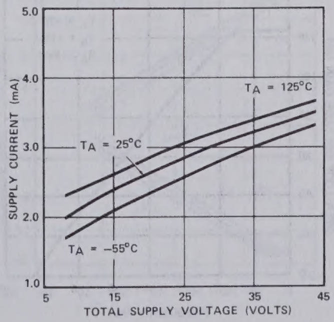
VOLTAGE NOISE DENSITY vs SUPPLY VOLTAGE



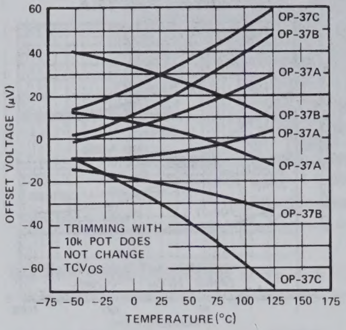
CURRENT NOISE DENSITY vs FREQUENCY

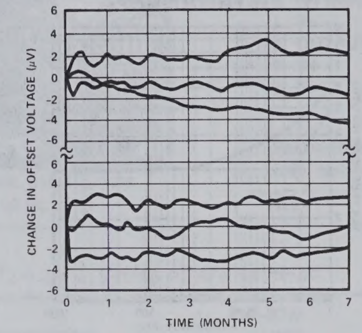


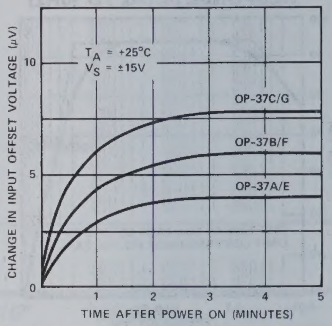
SUPPLY CURRENT vs SUPPLY VOLTAGE

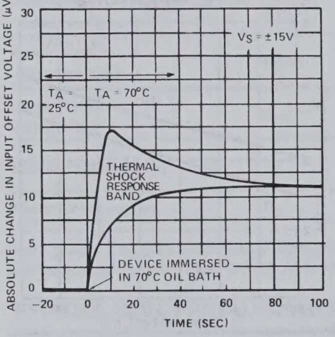


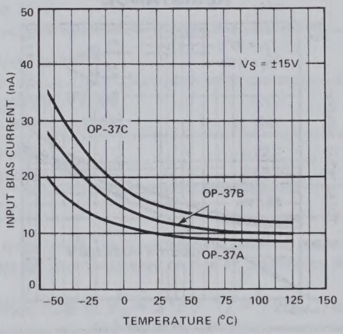
TYPICAL PERFORMANCE CHARACTERISTICS

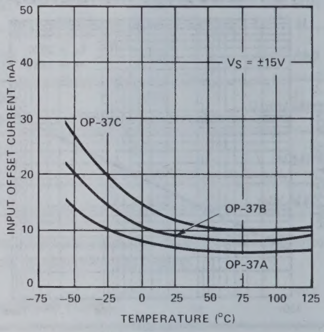

OFFSET VOLTAGE DRIFT OF EIGHT REPRESENTATIVE UNITS vs TEMPERATURE

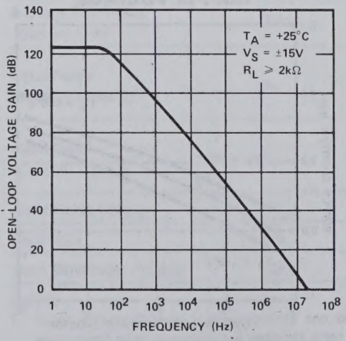

LONG-TERM OFFSET VOLTAGE DRIFT OF SIX REPRESENTATIVE UNITS

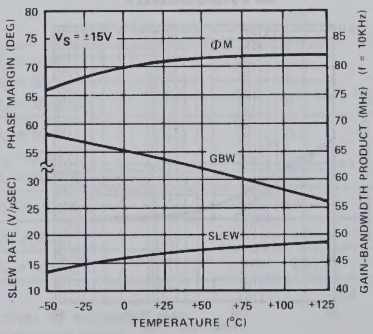

WARM-UP OFFSET VOLTAGE DRIFT

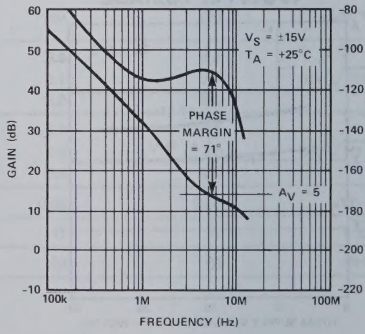

OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK


INPUT BIAS CURRENT vs TEMPERATURE


INPUT OFFSET CURRENT vs TEMPERATURE

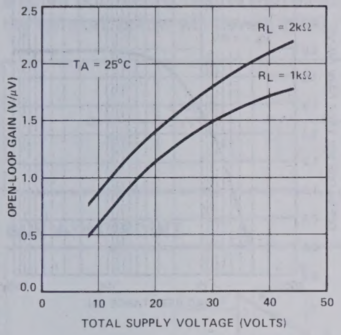

OPEN-LOOP GAIN vs FREQUENCY


SLEW RATE, GAIN BANDWIDTH PRODUCT, PHASE MARGIN vs TEMPERATURE

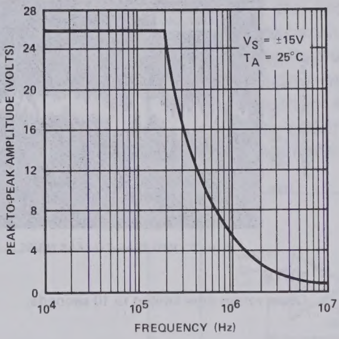

GAIN, PHASE SHIFT vs FREQUENCY

TYPICAL PERFORMANCE CHARACTERISTICS

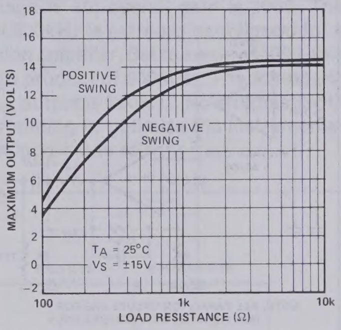
OPEN-LOOP VOLTAGE GAIN vs SUPPLY VOLTAGE



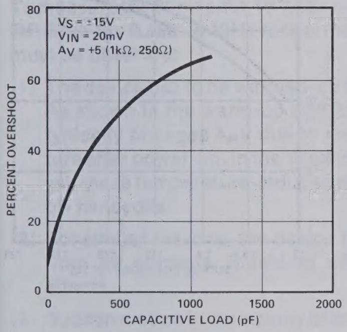
MAXIMUM OUTPUT SWING vs FREQUENCY



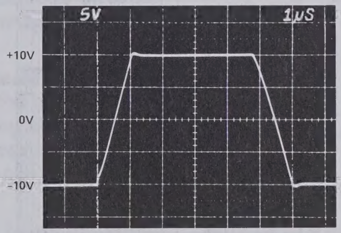
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD

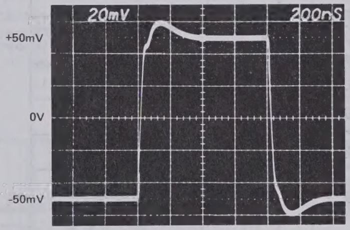


LARGE-SIGNAL TRANSIENT RESPONSE



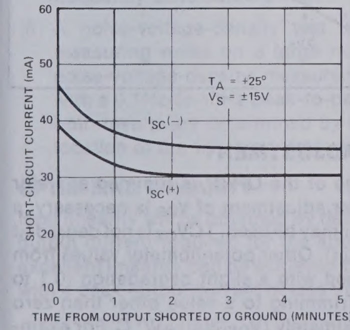
VS = ±15V
AV = +5 (1kΩ, 250Ω)
TA = +25°C

SMALL-SIGNAL TRANSIENT RESPONSE

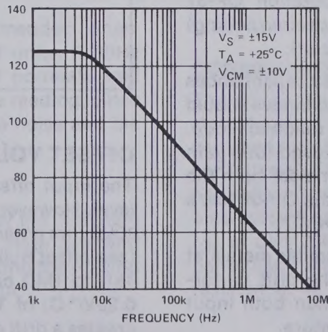


VS = ±15V
AV = +5 (1kΩ, 250Ω)
TA = +25°C

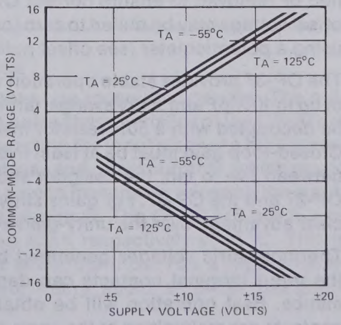
SHORT-CIRCUIT CURRENT vs TIME



CMRR vs FREQUENCY

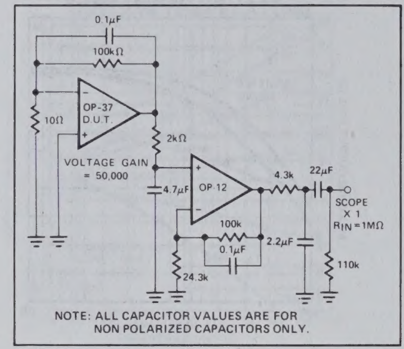


COMMON-MODE INPUT RANGE vs SUPPLY VOLTAGE

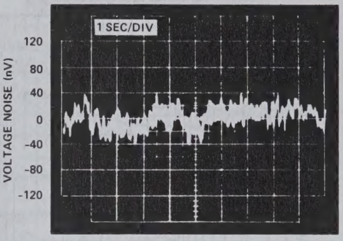


TYPICAL PERFORMANCE CHARACTERISTICS

NOISE TEST CIRCUIT (0.1Hz TO 10Hz)



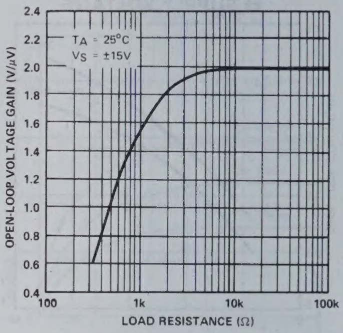
LOW-FREQUENCY NOISE



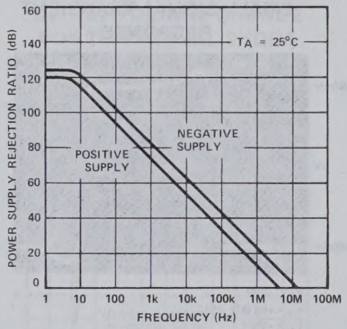
0.1Hz TO 10Hz PEAK-TO-PEAK NOISE

NOTE:
Observation time limited to 10 seconds.

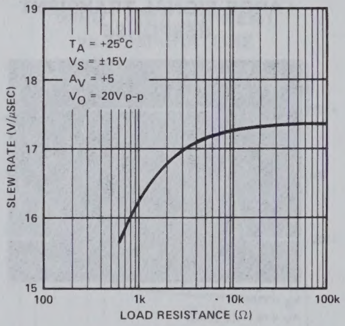
OPEN-LOOP VOLTAGE GAIN vs LOAD RESISTANCE



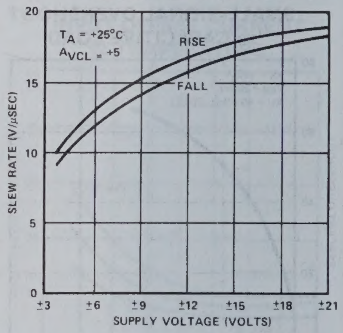
PSRR vs FREQUENCY



SLEW RATE vs LOAD



SLEW RATE vs SUPPLY VOLTAGE



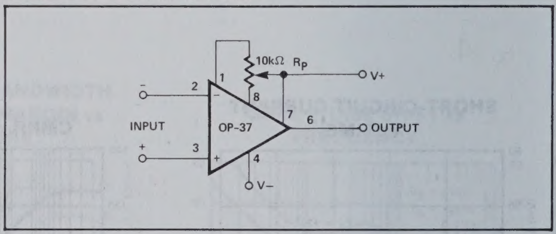
APPLICATIONS INFORMATION

OP-37 Series units may be inserted directly into 725, OP-06, OP-07, and OP-05 sockets with or without removal of external compensation or nulling components. Additionally, the OP-37 may be fitted to unnulled 741-type sockets; however, if conventional 741 nulling circuitry is in use, it should be modified or removed to ensure correct OP-37 operation. OP-37 offset voltage may be nulled to zero (or other desired setting) using a potentiometer (see offset nulling circuit).

The OP-37 provides stable operation with load capacitances of up to 1000pF and ±10V swings; larger capacitances should be decoupled with a 50Ω resistor inside the feedback loop. Closed-loop gain must be at least five. For closed-loop gain between five to ten, the designer should consider both the OP-27 and the OP-37. For gains above ten, the OP-37 has a clear advantage over the unity-gain-stable OP-27.

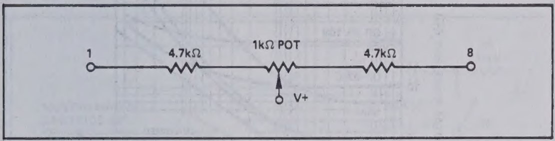
Thermoelectric voltages generated by dissimilar metals at the input terminal contacts can degrade the drift performance. Best operation will be obtained when both input contacts are maintained at the same temperature.

OFFSET NULLING CIRCUIT

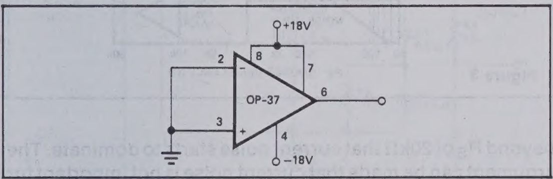


OFFSET VOLTAGE ADJUSTMENT

The input offset voltage of the OP-37 is trimmed at wafer level. However, if further adjustment of V_{OS} is necessary, a 10kΩ trim potentiometer may be used. TCV_{OS} is not degraded (see offset nulling circuit). Other potentiometer values from 1kΩ to 1MΩ can be used with a slight degradation (0.1 to 0.2μV/°C) of TCV_{OS}. Trimming to a value other than zero creates a drift of approximately (V_{OS}/300) μV/°C. For example, the change in TCV_{OS} will be 0.33μV/°C if V_{OS} is adjusted to 100μV. The offset-voltage adjustment range with a 10kΩ potentiometer is ±4mV. If smaller adjustment range is required, the nulling sensitivity can be reduced by using a smaller pot in conjunction with fixed resistors. For example, the network below will have a ±280μV adjustment range.



BURN-IN CIRCUIT



NOISE MEASUREMENTS

To measure the 80nV peak-to-peak noise specification of the OP-37 in the 0.1Hz to 10Hz range, the following precautions must be observed:

(1) The device has to be warmed-up for at least five minutes. As shown in the warm-up drift curve, the offset voltage typically changes 4μV due to increasing chip temperature after power-up. In the 10 second measurement interval, these temperature-induced effects can exceed tens-of- nanovolts.

(2) For similar reasons, the device has to be well-shielded from air currents. Shielding minimizes thermocouple effects.

(3) Sudden motion in the vicinity of the device can also "feed-through" to increase the observed noise.

(4) The test time to measure 0.1Hz-to-10Hz noise should not exceed 10 seconds. As shown in the noise-tester frequency response curve, the 0.1Hz corner is defined by only one zero. The test time of 10 seconds acts as an additional zero to eliminate noise contributions from the frequency band below 0.1Hz.

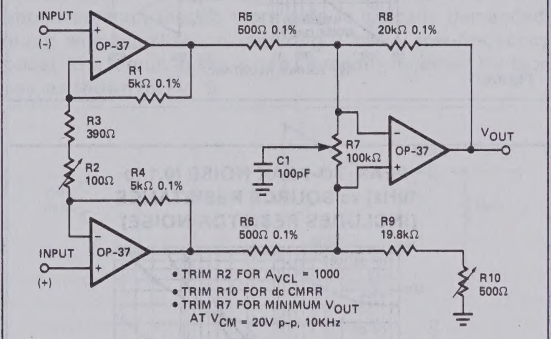
(5) A noise-voltage-density test is recommended when measuring noise on a large number of units. A 10Hz noise-voltage-density measurement will correlate well with a 0.1Hz-to-10Hz peak-to-peak noise reading, since both results are determined by the white noise and the location of the 1/f corner frequency.

OPTIMIZING LINEARITY

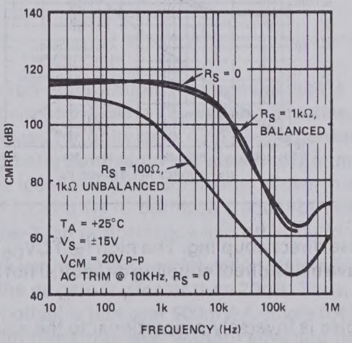
Best linearity will be obtained by designing for the minimum output current required for the application. High gain and excellent linearity can be achieved by operating the op amp with a peak output current of less than ±10mA.

INSTRUMENTATION AMPLIFIER

A three-op-amp instrumentation amplifier provides high gain and wide bandwidth. The input noise of the circuit below is $4.9nV/\sqrt{Hz}$. The gain of the input stage is set at 25 and the gain of the second stage is 40; overall gain is 1000. The amplifier bandwidth of 800kHz is extraordinarily good for a precision instrumentation amplifier. Set to a gain of 1000, this yields a gain-bandwidth product of 800MHz. The full-power bandwidth for a $20V_{p-p}$ output is 250kHz. Potentiometer R7 provides quadrature trimming to optimize the instrumentation amplifier's AC common-mode rejection.



- TRIM R2 FOR A_{VCL} = 1000
- TRIM R10 FOR dc CMRR
- TRIM R7 FOR MINIMUM V_{OUT} AT V_{CM} = 20V p-p, 10KHz



COMMENTS ON NOISE

The OP-37 is a very low-noise monolithic op amp. The outstanding input voltage noise characteristics of the OP-37 are achieved mainly by operating the input stage at a high quiescent current. The input bias and offset currents, which would normally increase, are held to reasonable values by the input-bias-current cancellation circuit. The OP-37A/E has I_B and I_{OS} of only ±40nA and 35nA respectively at 25°C. This is particularly important when the input has a high source-resistance. In addition, many audio amplifier designers

NOISE vs SOURCE RESISTANCE (INCLUDING RESISTOR NOISE) AT 1000Hz

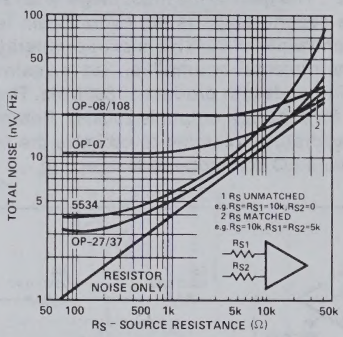


Figure 1

PEAK-TO-PEAK NOISE (0.1 to 10Hz) vs SOURCE RESISTANCE (INCLUDES RESISTOR NOISE)

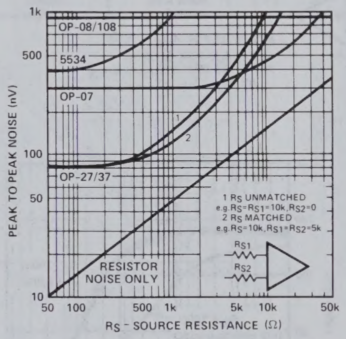


Figure 2

prefer to use direct coupling. The high I_B, TCV_{OS} of previous designs have made direct coupling difficult, if not impossible, to use.

Voltage noise is inversely proportional to the square-root of bias current, but current noise is proportional to the square-root of bias current. The OP-37's noise advantage disappears when high source-resistors are used. Figures 1, 2, and 3 compare OP-37 observed total noise with the noise performance of other devices in different circuit applications.

$$\text{Total noise} = \left[(\text{Voltage noise})^2 + (\text{current noise} \times R_S)^2 + (\text{resistor noise}^2\right]^{1/2}$$

Figure 1 shows noise-versus-source-resistance at 1000Hz. The same plot applies to wideband noise. To use this plot, just multiply the vertical scale by the square-root of the bandwidth.

At R_S<1kΩ, the OP-37's low voltage noise is maintained. With R_S< 1kΩ, total noise increases, but is dominated by the resistor noise rather than current or voltage noise. It is only beyond R_S of 20kΩ that current noise starts to dominate. The argument can be made that current noise is not important for applications with low-to-moderate source resistances. The crossover between the OP-37 and OP-07 and OP-08 noise occurs in the 15-to-40kΩ region.

10Hz NOISE vs SOURCE RESISTANCE (INCLUDES RESISTOR NOISE)

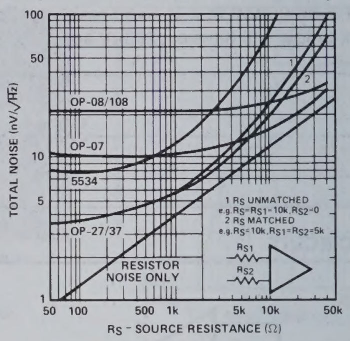


Figure 3

Figure 2 shows the 0.1Hz-to-10Hz peak-to-peak noise. Here the picture is less favorable; resistor noise is negligible, current noise becomes important because it is inversely proportional to the square-root of frequency. The crossover with the OP-07 occurs in the 3-to 5kΩ range depending on whether balanced or unbalanced source resistors are used (at 3kΩ the I_B, I_{OS} error also can be three times the V_{OS} spec.).

Therefore, for low-frequency applications, the OP-07 is better than the OP-27/37 when R_S > 3kΩ. The only exception is when gain error is important. Figure 3 illustrates the 10Hz noise. As expected, the results are between the previous two figures.

For reference, typical source resistances of some signal sources are listed in Table 1.

Table 1

DEVICE	SOURCE IMPEDANCE	COMMENTS
Strain gauge	<500Ω	Typically used in low-frequency applications.
Magnetic tapehead	<1500Ω	Low I_B very important to reduce self-magnetization problems when direct coupling is used. OP-37 I_B can be neglected.
Magnetic phonograph cartridges	<1500Ω	Similar need for low I_B in direct coupled applications. OP-37 will not introduce any self-magnetization problem.
Linear variable differential transformer	<1500Ω	Used in rugged servo-feedback applications. Bandwidth of interest is 400Hz to 5kHz.

AUDIO APPLICATIONS

The following applications information has been abstracted from a PMI article in the 12/20/80 issue of Electronic Design magazine and updated.

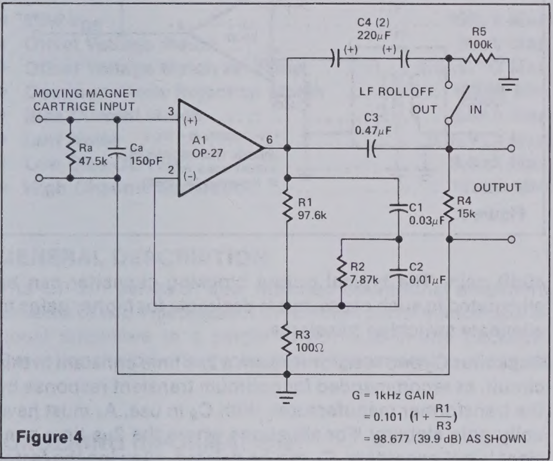


Figure 4

Figure 4 is an example of a phono pre-amplifier circuit using the OP-27 for A_1; R_1-R_2-C_1-C_2 form a very accurate RIAA network with standard component values. The popular method to accomplish RIAA phono equalization is to employ frequency-dependent feedback around a high-quality gain block. Properly chosen, an RC network can provide the three necessary time constants of 3180, 318, and 75μs.[1]

For initial equalization accuracy and stability, precision metal-film resistors and film capacitors of polystyrene or polypropylene are recommended since they have low voltage coefficients, dissipation factors, and dielectric absorption.[4] (High-K ceramic capacitors should be avoided here, though low-K ceramics—such as NPO types, which have excellent dissipation factors, and somewhat lower dielectric absorption — can be considered for small values or where space is at a premium.)

The OP-27 brings a $3.2\text{nV}/\sqrt{\text{Hz}}$ voltage noise and $0.45\ \text{pA}/\sqrt{\text{Hz}}$ current noise to this circuit. To minimize noise from other sources, R_3 is set to a value of 100Ω, which generates a voltage noise of $1.3\text{nV}/\sqrt{\text{Hz}}$. The noise increases the $3.2\text{nV}/\sqrt{\text{Hz}}$ of the amplifier by only 0.7dB. With a 1kΩ source, the circuit noise measures 63dB below a 1mV reference level, unweighted, in a 20kHz noise bandwidth.

Gain (G) of the circuit at 1kHz can be calculated by the expression:

$$G = 0.101\left(1 + \frac{R_1}{R_3}\right)$$

For the values shown, the gain is just under 100 (or 40dB). Lower gains can be accommodated by increasing R_3, but gains higher than 40dB will show more equalization errors because of the 8MHz gain-bandwidth of the OP-27.

This circuit is capable of very low distortion over its entire range, generally below 0.01% at levels up to 7V rms. At 3V output levels, it will produce less than 0.03% total harmonic distortion at frequencies up to 20kHz.

Capacitor C_3 and resistor R_4 form a simple −6dB-per-octave rumble filter, with a corner at 22Hz. As an option, the switch-selected shunt capacitor C_4, a nonpolarized electrolytic, bypasses the low-frequency rolloff. Placing the rumble filter's high-pass action after the preamp has the desirable result of discriminating against the RIAA-amplified low-frequency noise components and pickup-produced low-frequency disturbances.

A preamplifier for NAB tape playback is similar to an RIAA phono preamp, though more gain is typically demanded, along with equalization requiring a heavy low-frequency boost. The circuit in Fig. 4 can be readily modified for tape use, as shown by Fig. 5.

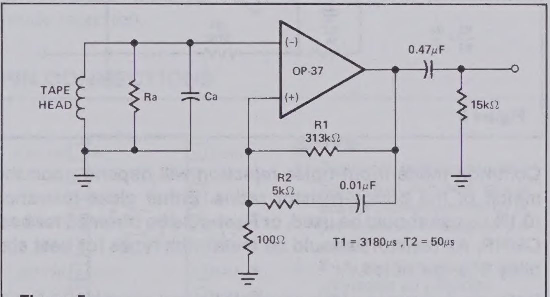


Figure 5

While the tape-equalization requirement has a flat high-frequency gain above 3kHz ($T_2 = 50\mu s$), the amplifier need not be stabilized for unity gain. The decompensated OP-37 provides a greater bandwidth and slew rate. For many applications, the idealized time constants shown may require trimming of R_1 and R_2 to optimize frequency response for nonideal tape-head performance and other factors.[5]

The network values of the configuration yield a 50dB gain at 1kHz, and the dc gain is greater than 70dB. Thus, the worst-case output offset is just over 500mV. A single 0.47μF output capacitor can block this level without affecting the dynamic range.

The tape head can be coupled directly to the amplifier input, since the worst-case bias current of 85nA with a 400mH, 100 μin. head (such as the PRB2H7K) will not be troublesome.

One potential tape-head problem is presented by amplifier bias-current transients which can magnetize a head. The OP-27 and OP-37 are free of bias-current transients upon power up or power down. However, it is always advantageous to control the speed of power supply rise and fall, to eliminate transients.

In addition, the dc resistance of the head should be carefully controlled, and preferably below 1kΩ. For this configuration, the bias-current-induced offset voltage can be greater than the 170μV maximum offset if the head resistance is not sufficiently controlled.

A simple, but effective, fixed-gain transformerless microphone preamp (Fig. 6) amplifies differential signals from low-impedance microphones by 50dB, and has an input impedance of 2kΩ. Because of the high working gain of the circuit, an OP-37 helps to preserve bandwidth, which will be 110kHz. As the OP-37 is a decompensated device (minimum stable gain of 5), a dummy resistor, R_p, may be necessary, if the microphone is to be unplugged. Otherwise the 100% feedback from the open input may cause the amplifier to oscillate.

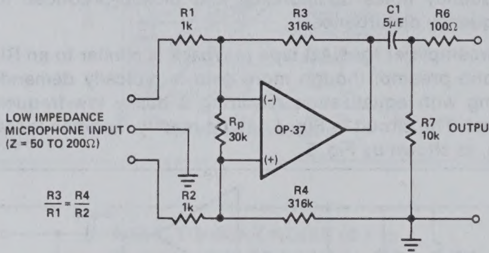


Figure 6

Common-mode input-noise rejection will depend upon the match of the bridge-resistor ratios. Either close-tolerance (0.1%) types should be used, or R_4 should be trimmed for best CMRR. All resistors should be metal-film types for best stability and low noise.

Noise performance of this circuit is limited more by the input resistors R_1 and R_2 than by the op amp, as R_1 and R_2 each generate a $4nV/\sqrt{Hz}$ noise, while the op amp generates a $3.2nV/\sqrt{Hz}$ noise. The rms sum of these predominant noise sources will be about $6nV/\sqrt{Hz}$, equivalent to 0.9µV in a 20kHz noise bandwidth, or nearly 61dB below a 1mV input signal. Measurements confirm this predicted performance.

For applications demanding appreciably lower noise, a high-quality microphone-transformer-coupled preamp (Fig. 7) incorporates the internally compensated OP-27. T_1 is a JE-115K-E 150Ω/15kΩ transformer which provides an optimum source resistance for the OP-27 device. The circuit has an overall gain of 40dB, the product of the transformer's voltage setup and the op amp's voltage gain.

Gain may be trimmed to other levels, if desired, by adjusting R_2 or R_1. Because of the low offset voltage of the OP-27, the output offset of this circuit will be very low, 1.7mV or less, for a 40dB gain. The typical output blocking capacitor can be eliminated in such cases, but is desirable for higher gains to eliminate switching transients.

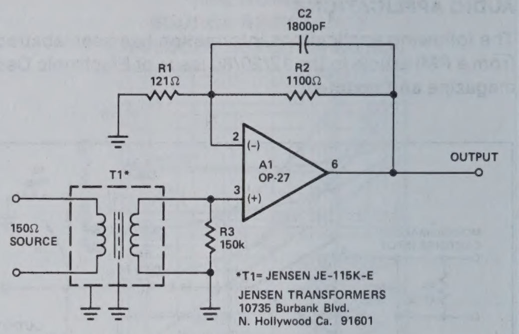


Figure 7

Capacitor C_2 and resistor R_2 form a 2µs time constant in this circuit, as recommended for optimum transient response by the transformer manufacturer. With C_2 in use, A_1 must have unity-gain stability. For situations where the 2µs time constant is not necessary, C_2 can be deleted, allowing the faster OP-37 to be employed.

Some comment on noise is appropriate to understand the capability of this circuit. A 150Ω resistor and R_1 and R_2 gain resistors connected to a noiseless amplifier will generate 220 nV of noise in a 20kHz bandwidth, or 73dB below a 1mV reference level. Any practical amplifier can only approach this noise level; it can never exceed it. With the OP-27 and T_1 specified, the additional noise degradation will be close to 3.6dB (or −69.5 referenced to 1mV).

References

1. Lipshitz, S.P., "On RIAA Equalization Networks," *JAES*, Vol. 27, June 1979, p. 458-481.
2. Jung, W.G., *IC Op Amp Cookbook*, 2nd Ed., H.W. Sams and Company, 1980.
3. Jung, W.G., *Audio IC Op Amp Applications*, 2nd Ed., H.W. Sams and Company, 1978.
4. Jung, W.G., and Marsh, R.M., "Picking Capacitors," *Audio*, February & March, 1980.
5. Otala, M., "Feedback-Generated Phase Nonlinearity in Audio Amplifiers," London AES Convention, March 1980, preprint 1976.
6. Stout, D.F., and Kaufman, M., *Handbook of Operational Amplifier Circuit Design*, New York, McGraw Hill, 1976.

DUAL ULTRA-LOW V_{OS} MATCHED OPERATIONAL AMPLIFIER

OP-207

FEATURES

- **Low V_{OS} .... 100µV Max**
- **Offset Voltage Match .... 90µV Max**
- **Offset Voltage Match vs. Temp. .... 1.0µV/°C Max**
- **Common-Mode Rejection Match .... 103dB Min**
- **Bias Current Match .... 3.5nA Max**
- **Low Noise .... 0.6µV_{p-p} Max**
- **Low Bias Current .... 3.0nA Max**
- **High Channel Separation .... 126dB Min**

GENERAL DESCRIPTION

The OP-207 series of dual matched operational amplifiers consists of two independent OP-07 high performance operational amplifiers in a single 14-pin dual-in-line package. Exceptionally low offset voltage and tight matching of critical parameters is provided between the channels of this dual operational amplifier.

The excellent specifications of the individual amplifiers combined with the tight matching and temperature tracking between channels provide high performance in instrumentation amplifier designs. The individual amplifiers feature very low input offset voltage, low offset voltage drift, low noise voltage, and low bias current. Each amplifier is fully compensated and protected.

Matching between channels is provided on all critical parameters including offset voltage, tracking of offset voltage vs. temperature, noninverting bias currents, and common-mode rejection.

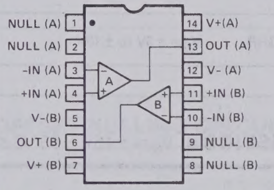
ORDERING INFORMATION†

T_A = 25°C V_{OS} MAX (µV)	HERMETIC DIP 14-PIN	OPERATING TEMPERATURE RANGE
100	OP207AY*	MIL
100	OP207EY	COM
200	OP207BY*	MIL
200	OP207FY	COM

*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

PIN CONNECTIONS

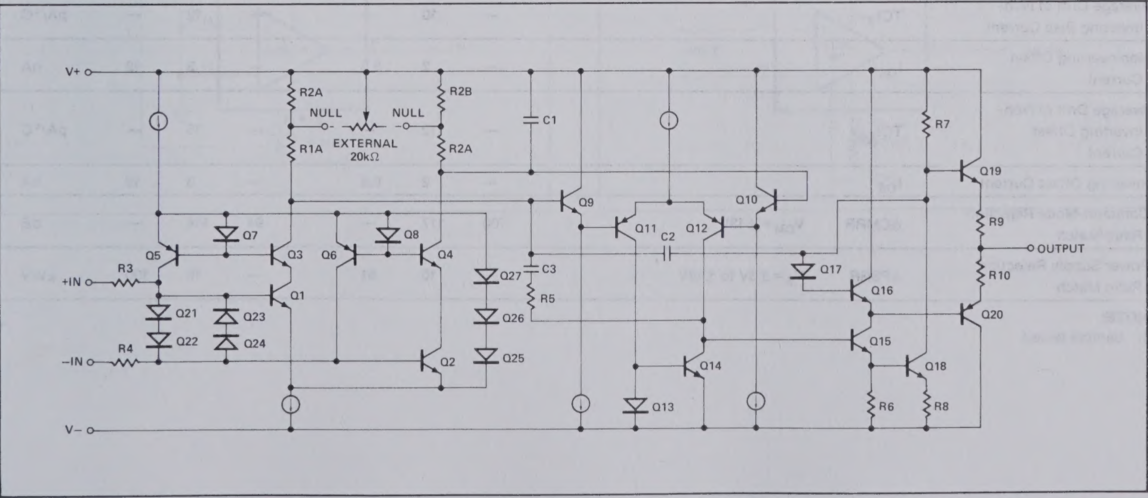

NULL (A) 1
NULL (A) 2
-IN (A) 3
+IN (A) 4
V-(B) 5
OUT (B) 6
V+ (B) 7
14 V+(A)
13 OUT (A)
12 V- (A)
11 +IN (B)
10 -IN (B)
9 NULL (B)
8 NULL (B)
A
B

14-PIN HERMETIC DIP
(Y-Suffix)

NOTES:

1. Device may be operated even if insertion is reversed; this is due to inherent symmmetry of pin locations of amplifiers A and B.
2. V-(A) and V-(B) are internally connected via substrate resistance.

SIMPLIFIED SCHEMATIC (1/2 OP-207)


V+
R2A
R2B
NULL
NULL
EXTERNAL 20kΩ
R1A
R2A
C1
R7
Q19
Q9
Q10
Q11
Q12
C2
R9
OUTPUT
Q7
Q8
Q5
Q3
Q6
Q4
R3
+IN
Q27
C3
Q17
R10
Q1
R5
Q16
Q21
Q23
Q26
Q20
Q22
Q24
Q15
R4
-IN
Q2
Q25
Q14
Q18
Q13
R6
R8
V-

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±22V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
OP-207A, OP-207B	−55°C to +125°C
OP-207E, OP-207F	0°C to +70°C
Lead Temperature (Soldering, 60 sec)	300°C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
14-Pin Hermetic DIP	106°C	11.3mW/°C

2. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

			OP-207A/E			OP-207B/F			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage Match	ΔV_{OS}	$R_S = 100\Omega$	—	30	90	—	50	280	μV
Average Noninverting Bias Current	I_{B^+}		—	±1.5	±3.5	—	±1.5	±6.0	nA
Noninverting Offset Current	I_{OS^+}		—	±0.7	±3.5	—	±1.0	±6.0	nA
Inverting Offset Current	I_{OS^-}		—	±0.7	±3.5	—	±1.0	±6.0	nA
Common-Mode Rejection Ratio Match	ΔCMRR	$V_{CM} = \pm 13V$	103	120	—	96	114	—	dB
Power Supply Rejection Ratio Match	ΔPSRR	$V_S = \pm 3V$ to $\pm 18V$	—	7	32	—	10	51	μV/V
Channel Separation			126	140	—	126	140	—	dB

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \le T_A \le 125°C$, unless otherwise noted.

			OP-207A			OP-207B			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage Match	ΔV_{OS}	$R_S = 100\Omega$	—	70	180	—	180	450	μV
Input Offset Voltage Tracking									
Without External Trim	$TC\Delta V_{OS}$	(Note 1)	—	0.5	1.0	—	0.9	1.5	μV/°C
With External Trim	$TC\Delta V_{OSn}$	$R_P = 20k\Omega$ (Note 1)	—	0.3	1.0	—	0.4	1.3	
Average Noninverting Bias Current	I_{B^+}		—	±2	±6	—	±3	±12	nA
Average Drift of Noninverting Bias Current	TCI_{B^+}		—	10	—	—	12	—	pA/°C
Noninverting Offset Current	I_{OS^+}		—	2	6.5	—	3	12	nA
Average Drift of Noninverting Offset Current	TCI_{OS^+}		—	12	—	—	15	—	pA/°C
Inverting Offset Current	I_{OS^-}		—	2	6.5	—	3	12	nA
Common-Mode Rejection Ratio Match	ΔCMRR	$V_{CM} = \pm 13V$	100	117	—	94	114	—	dB
Power Supply Rejection Ratio Match	ΔPSRR	$V_S = \pm 3V$ to $\pm 18V$	—	10	51	—	16	100	μV/V

NOTE:

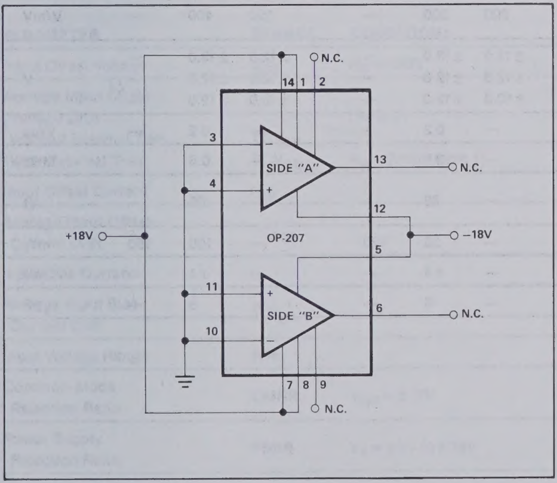
1. Sample tested.

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $0°C \le T_A \le 70°C$, unless otherwise noted.

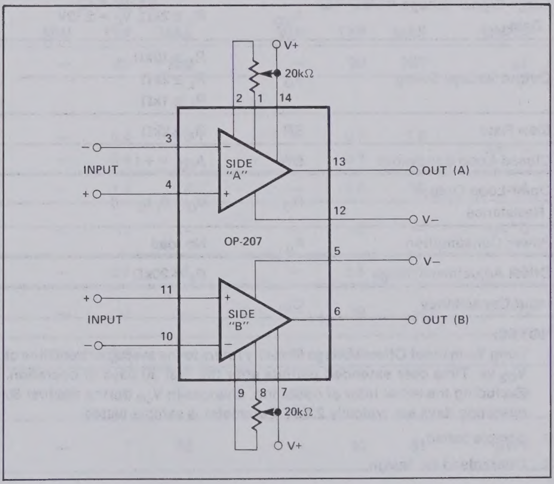
			OP-207E			OP-207F			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage Match	ΔV_{OS}	$R_S = 100\Omega$	—	60	150	—	120	350	µV
Input Offset Voltage Tracking									µV/°C
Without External Trim	$TC\Delta V_{OS}$	(Note 1)	—	0.5	1.0	—	0.9	1.5	
With External Trim	$TC\Delta V_{OSn}$	$R_P = 20k\Omega$ (Note 1)	—	0.3	1.0	—	0.4	1.3	
Average Noninverting Bias Current	$I_B{}^+$		—	±2	±5	—	±3	±10	nA
Average Drift of Noninverting Bias Current	$TCI_B{}^+$		—	10	—	—	12	—	pA/°C
Noninverting Offset Current	$I_{OS}{}^+$		—	2	5	—	3	10	nA
Average Drift of Noninverting Offset Current	$TCI_{OS}{}^+$		—	12	—	—	15	—	pA/°C
Inverting Offset Current	$I_{OS}{}^-$		—	2	5	—	3	10	nA
Common-Mode Rejection Ratio Match	ΔCMRR	$V_{CM} = \pm 13V$	100	117	—	94	114	—	dB
Power Supply Rejection Ratio Match	ΔPSRR	$V_S = \pm 3V$ to $\pm 18V$	—	10	51	—	16	100	µV/V

NOTE:
1. Sample tested.

BURN-IN CIRCUIT


N.C.
14
1
2
3
4
SIDE "A"
13
N.C.
12
+18V
OP-207
−18V
5
11
SIDE "B"
6
N.C.
10
7
8
9
N.C.

OFFSET NULLING CIRCUIT


V+
20kΩ
2
1
14
3
−
INPUT
+
4
SIDE "A"
13
OUT (A)
12
V−
OP-207
5
V−
+
11
INPUT
10
−
SIDE "B"
6
OUT (B)
9
8
7
20kΩ
V+

INDIVIDUAL AMPLIFIER CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

			OP-207A/E			OP-207B/F			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S = 100\Omega$	—	35	100	—	60	200	μV
Input Offset Voltage Stability	ΔV_{OS}/Time	(Note 1)	—	0.3	1.5	—	0.4	2.0	μV/Mo
Input Offset Current	I_{OS}		—	0.9	2.8	—	1.5	6.0	nA
Input Bias Current	I_B		—	±1	±3	—	±2	±7	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 2)	—	0.35	0.6	—	0.35	0.6	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10Hz$ (Note 2)	—	10.3	18.0	—	10.3	18.0	$nV/\sqrt{Hz}$
		$f_O = 100Hz$ (Note 2)	—	10.0	13.0	—	10.0	13.0	
		$f_O = 1000Hz$ (Note 2)	—	9.6	—	—	9.6	—	
Input Noise Current	I_{np-p}	0.1Hz to 10Hz (Note 2)	—	14	30	—	14	30	pA_{p-p}
Input Noise Current Density	i_n	$f_O = 10Hz$ (Note 2)	—	0.32	0.80	—	0.32	0.80	$pA/\sqrt{Hz}$
		$f_O = 100Hz$ (Note 2)	—	0.14	0.23	—	0.14	0.23	
		$f_O = 1000Hz$ (Note 2)	—	0.12	—	—	0.12	—	
Input Resistance — Differential Mode	R_{IN}	(Note 3)	20	60	—	8	30	—	$M\Omega$
Input Resistance — Common-Mode	$R_{IN\,CM}$		—	200	—	—	120	—	$G\Omega$
Input Voltage Range	IVR		±13	±14	—	±13	±14	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	106	123	—	100	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	5	20	—	7	32	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	200	500	—	150	400	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	±12.5	±13.0	—	±12.5	±13.0	—	V
		$R_L \geq 2k\Omega$	±12.0	±12.8	—	±12.0	±12.8	—	
		$R_L \geq 1k\Omega$	±10.0	±12.0	—	±10.0	±12.0	—	
Slew Rate	SR	$R_L \geq 2k\Omega$	—	0.2	—	—	0.2	—	$V/\mu s$
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$	—	0.6	—	—	0.6	—	MHz
Open-Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	60	—	—	60	—	Ω
Power Consumption	P_d	No load	—	90	120	—	100	150	mW
Offset Adjustment Range		$R_P = 20k\Omega$	—	±4	—	—	±4	—	mV
Input Capacitance	C_{IN}		—	8	—	—	8	—	pF

NOTES:

1. Long Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV. Parameter is sample tested.
2. Sample tested.
3. Guaranteed by design.

INDIVIDUAL AMPLIFIER CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \le T_A \le 125°C$, unless otherwise noted.

			OP-207A			OP-207B			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S = 100\Omega$	—	75	230	—	100	400	µV
Average Input Offset Voltage Drift									
Without External Trim	TCV_{OS}	$R_P = 20k\Omega$ (Note 1)	—	0.4	1.3	—	0.7	1.8	µV/°C
With External Trim	TCV_{OSn}		—	0.4	—	—	0.7	—	
Input Offset Current	I_{OS}		—	1.8	5.6	—	3.0	12.0	nA
Average Input Offset Current Drift	TCI_{OS}		—	10	—	—	12	—	pA/°C
Input Bias Current	I_B		—	±3.0	±5.6	—	±4.0	±14.0	nA
Average Input Bias Current Drift	TCI_B		—	12	—	—	18	—	pA/°C
Input Voltage Range	IVR		±13	±13.5	—	±13	±13.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	103	120	—	97	117	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	7	32	—	10	51	µV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$, $V_O = \pm 10V$	150	400	—	120	350	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±12.0	±12.8	—	±12.0	±12.8	—	V

INDIVIDUAL AMPLIFIER CHARACTERISTICS at $V_S = \pm 15V$, $0°C \le T_A \le 70°C$, unless otherwise noted.

			OP-207E			OP-207F			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S = 100\Omega$	—	60	200	—	90	350	µV
Average Input Offset Voltage Drift		(Note 2)							
Without External Trim	TCV_{OS}		—	0.4	1.3	—	0.7	1.8	µV/°C
With External Trim	TCV_{OSn}	$R_P = 20k\Omega$ (Note 1)	—	0.4	—	—	0.7	—	
Input Offset Current	I_{OS}		—	1.4	5	—	2.5	10	nA
Average Input Offset Current Drift	TCI_{OS}		—	10	—	—	12	—	pA/°C
Input Bias Current	I_B		—	±2	±5	—	±3	±11	nA
Average Input Bias Current Drift	TCI_B		—	12	—	—	18	—	pA/°C
Input Voltage Range	IVR		±13	±13.5	—	±13	±13.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	103	120	—	97	117	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	7	32	—	10	51	µV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$, $V_O = \pm 10V$	150	400	—	120	350	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±12.0	±12.8	—	±12.0	±12.8	—	V

NOTES:

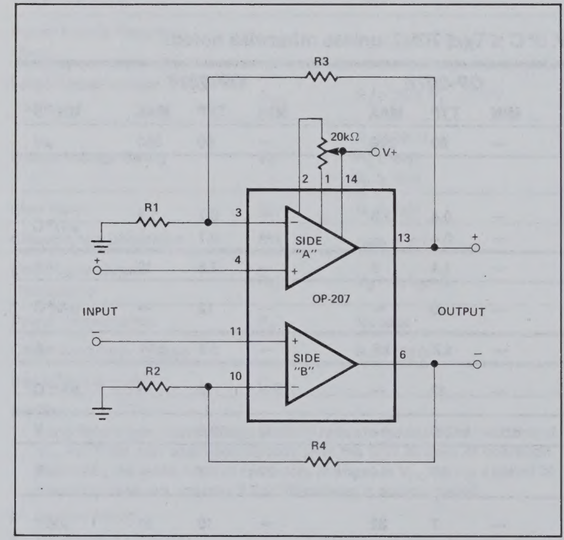
1. Exclude first hour of operation to allow for stabilization of external circuitry.
2. Sample tested.

APPLICATION OF DUAL MATCHED OPERATIONAL AMPLIFIERS

ADVANTAGES OF DUAL MATCHED OPERATIONAL AMPLIFIERS

Dual matched operational amplifiers provide a powerful tool for the solution of some difficult circuit design problems. Circuits include true instrumentation amplifiers, extremely low drift, high common-mode rejection DC amplifiers, low DC drift active filters, dual tracking voltage references, and many other demanding applications. These designs all require good matching between two operational amplifiers.

The circuit below, a differential-in, differential-out amplifier, shows how errors can be reduced. Assuming the resistors used are matched, the gain of each side will be identical; if the offset voltage of each amplifier is matched, then the net differential voltage at the amplifiers output will be zero. Note that the output offset error of this amplifier is not a function of the offset voltage of the individual amplifiers, but only a function of the *difference* between the amplifiers' offset voltages. This error-cancellation principle holds for a number of input-referred error parameters — offset voltage, offset voltage drift, inverting and noninverting bias currents, common-mode and power supply rejection ratios. Note also that the impedances of each input, both common-mode and differential-mode, are extremely high, an important feature not possible with single operational amplifier circuits. Common-mode rejection can be made exceptionally high; this is very important in instrumentation amplifiers where errors due to large common-mode voltages can be far greater than errors due to noise or drift with temperature. For example, consider the case of two op amps, each with 80dB (100µV/V) CMRR. If the CMRR of one device is +100µV/V CMRR and the other is −100µV/V, then the net CMRR will be 200µV/V, a 6dB degradation. The matching of CMRR increases the effective CMRR when used as an instrumentation input stage.



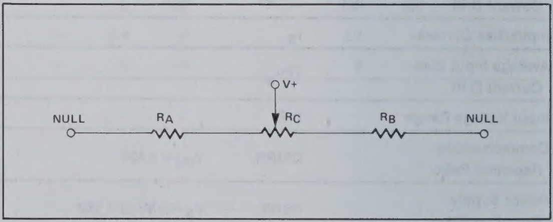
POWER SUPPLIES

The V+ supply terminals are completely independent and may be powered by separate supplies if desired. However, this approach would sacrifice the advantages of the power-supply-rejection-ratio matching. The V− supply terminals are both connected to the common substrate and must be tied to the same voltage.

OFFSET TRIMMING

Offset voltage trimming is provided for each amplifier. Guaranteed performance over temperature is obtained by trimming one side (side A) to match the offset of the other. A net differential offset of zero results. This procedure is used during factory testing of the devices. The same results are obtained by trimming side B to match side A or by nulling each side individually.

The OP-207 is designed to provide best drift performance when trimmed with a 20kΩ potentiometer; this value provides about ±4mV of adjustment range which is adequate for most applications. Trimming resolution can be increased by use of the circuit shown below.



DUAL PRECISION JFET-INPUT OPERATIONAL AMPLIFIER

OP-215

FEATURES

- **High Slew Rate 18V/μs**
- **Fast Settling Time 900ns**
- **Low Input Offset Voltage Drift .... 3.0μV/°C**
- **Wide Bandwidth 6MHz**
- **Temperature-Compensated Input Bias Currents**
- **Guaranteed Input Bias Current ..... 18nA Max (125°C)**
- **Bias Current Specified Warmed-Up Over Temperature**
- **Low Input Noise Current .... 0.01pA/$\sqrt{\text{Hz}}$**
- **High Common-Mode Rejection Ratio 100dB**
- **Pin Compatible With Standard Dual Pinouts**
- **125°C Temperature Tested DICE**
- **Models With MIL-STD-883 Class B Processing Available**

GENERAL DESCRIPTION

The OP-215 offers the proven BIFET performance advantages of high speed and low input bias current with the tracking and convenience advantages of a dual op-amp configuration.

Low input offset voltages, low input currents, and low drift are featured in these high-speed amplifiers.
On-chip zener-zap trimming is used to achieve low V_{OS} while a bias-current compensation scheme gives a low input bias current at elevated temperatures. Thus the OP-215 features an input bias current of 18nA at 125°C ambient (not junction) temperature which greatly extends the application usefulness of this device.

Applications include high-speed amplifiers for current output DACs, active filters, sample-and-hold buffers, and photocell amplifiers. For additional precision JFET op amps, see the OP-15/16/17 data sheet.

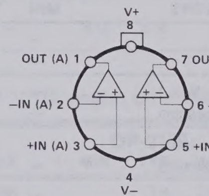
ORDERING INFORMATION†

$T_A = 25°C$ V_{OS} MAX (mV)	PACKAGE			OPERATING TEMPERATURE RANGE
	TO-99 8-PIN	HERMETIC DIP 8-PIN	HERMETIC DIP 14-PIN	
1.0	OP215AJ*	OP215AZ*	OP215AY*	MIL
1.0	OP215EJ	OP215EZ	OP215EY	COM
2.0	OP215BJ*	OP215BZ*	OP215BY*	MIL
2.0	OP215FJ	OP215FZ	OP215FY	COM
4.0	OP215CJ*	OP215CZ*	OP215CY*	MIL
6.0	OP215GJ	OP215GZ	OP215GY	COM

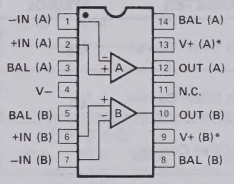
*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

PIN CONNECTIONS

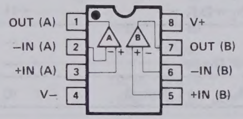

V+
8
OUT (A) 1
7 OUT (B)
−IN (A) 2
6 −IN (B)
+IN (A) 3
5 +IN (B)
4
V−

TO-99 (J-Suffix)


−IN (A) 1
+IN (A) 2
BAL (A) 3
V− 4
BAL (B) 5
+IN (B) 6
−IN (B) 7
8 BAL (B)
9 V+ (B)*
10 OUT (B)
11 N.C.
12 OUT (A)
13 V+ (A)*
14 BAL (A)
A
B

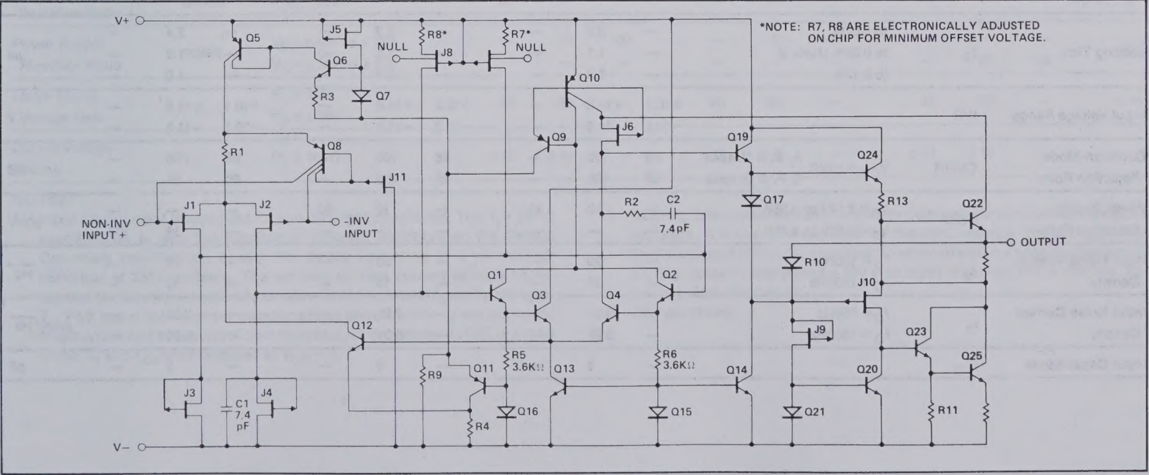
14-PIN HERMETIC DIP (Y-Suffix)

*V+ (A) & V+ (B) INTERNALLY CONNECTED.


OUT (A) 1
−IN (A) 2
+IN (A) 3
V− 4
8 V+
7 OUT (B)
6 −IN (B)
5 +IN (B)
A
B

8-PIN HERMETIC DIP (Z-Suffix)

SIMPLIFIED SCHEMATIC (1/2 OP-215)


V+
Q5
J5
R8*
R7*
NULL
J8
NULL
Q6
R3
Q7
Q10
J6
Q9
Q19
Q24
R1
Q8
J11
R2
C2
7.4pF
Q17
R13
Q22
J1
J2
NON-INV INPUT +
−INV INPUT
OUTPUT
R10
J10
Q1
Q2
Q3
Q4
Q12
J9
Q23
Q25
R5 3.6KΩ
R6 3.6KΩ
R9
Q11
Q13
Q14
Q20
J3
J4
C1 7.4 pF
Q16
Q15
Q21
R4
R11
V−

*NOTE: R7, R8 ARE ELECTRONICALLY ADJUSTED ON CHIP FOR MINIMUM OFFSET VOLTAGE.

ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage
  OP-215A, OP-215B, OP-215E, OP-215F
  (All DICE except GR) .... ±22V
  OP-215C, OP-215G (GR DICE only) .... ±18V
Internal Power Dissipation (Note 1) 500mW
Operating Temperature Range
  OP-215A, OP-215B, OP-215C .... −55°C to +125°C
  OP-215E, OP-215F, OP-215G .... 0°C to +70°C
Maximum Junction Temperature (T_j) .... +150°C
Differential Input Voltage
  OP-215A, OP-215B, OP-215E, OP-215F, (All DICE except GR) ...... ±40V
  OP-215C, OP-215G (GR DICE only) .... ±30V
Input Voltage
  OP-215A, OP-215B, OP-215E, OP-215F, (All DICE except GR) ...... ±20V
  OP-215C, OP-215G (GR DICE only) .... ±16V
  (Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.)
Output Short-Circuit Duration .... Indefinite
Storage Temperature Range .... −65°C to +150°C
Lead Temperature (Soldering, 60 sec) .... 300°C
DICE Junction Temperature (T_j) .... −65°C to +150°C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
14-Pin Hermetic DIP (Y)	100°C	10.0mW/°C
TO-99 (J)	80°C	7.1mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C

2. Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

			OP-215A/E			OP-215B/F			OP-215C/G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$ 'G' Grade	— —	0.2 —	1.0 —	— —	0.8 —	2.0 —	— —	2.0 2.5	4.0 6.0	mV
Input Offset Current	I_{OS}	$T_j = 25°C$ (Note 1) Device Operating	— —	3 5	50 100	— —	3 5	50 100	— —	3 5	100 200	pA
Input Bias Current	I_B	$T_j = 25°C$ (Note 1) Device Operating	— —	±15 ±18	±100 ±300	— —	±15 ±18	±200 ±400	— —	±15 ±18	±300 ±600	pA
Input Resistance	R_{IN}		—	10^{12}	—	—	10^{12}	—	—	10^{12}	—	Ω
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	150	500	—	75	220	—	50	200	—	V/mV
Output Voltage Swing	V_O	$R_L = 10k\Omega$ $R_L = 2k\Omega$	±12 ±11	±13 ±12.7	— —	±12 ±11	±13 ±12.7	— —	±12 ±11	±13 ±12.7	— —	V
Supply Current	I_{SY}	 'G' Grade	— —	6.0 —	8.5 —	— —	6.0 —	8.5 —	— —	7.0 7.0	10.0 12.0	mA
Slew Rate	SR	$A_{VCL} = +1$ (Note 3)	10	18	—	7.5	18	—	5	15	—	V/μs
Gain Bandwidth Product	GBW	(Note 3)	3.5	5.7	—	3.5	5.7	—	3.0	5.4	—	MHz
Closed-Loop Bandwidth	CLBW	$A_{VCL} = +1$	—	13	—	—	13	—	—	12	—	MHz
Settling Time	t_S	to 0.01% to 0.05% (Note 2) to 0.10%	— — —	2.3 1.1 0.9	— — —	— — —	2.3 1.1 0.9	— — —	— — —	2.4 1.2 1.0	— — —	μs
Input Voltage Range	IVR		+10.2 −10.2	+14.8 −11.5	— —	+10.2 −10.2	+14.8 −11.5	— —	+10.1 −10.1	+14.8 −11.5	— —	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm IVR$ A, B, C Grades E, F, G Grades	86 82	100 100	— —	86 82	100 100	— —	82 80	96 96	— —	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 16V$ $V_S = \pm 10V$ to $\pm 15V$	— —	10 —	51 —	— —	10 —	80 —	— —	— 16	— 100	μV/V
Input Noise Voltage Density	e_n	$f_O = 100Hz$ $f_O = 1000Hz$	— —	20 15	— —	— —	20 15	— —	— —	20 15	— —	$nV/\sqrt{Hz}$
Input Noise Current Density	i_n	$f_O = 100Hz$ $f_O = 1000Hz$	— —	0.01 0.01	— —	— —	0.01 0.01	— —	— —	0.01 0.01	— —	$pA/\sqrt{Hz}$
Input Capacitance	C_{IN}		—	3	—	—	3	—	—	3	—	pF

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \le T_A \le +125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-215A			OP-215B			OP-215C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	—	0.5	2.0	—	1.5	3.0	—	3.0	6.0	mV
Average Input Offset Voltage Drift												
Without External Trim	TCV_{OS}	(Note 3)	—	3	10	—	3	10	—	6	—	µV/°C
With External Trim	TCV_{OSn}	$R_P = 100k\Omega$	—	3	—	—	3	—	—	4	—	
Input Offset Current	I_{OS}	$T_j = +125°C$	—	0.8	8	—	0.8	8	—	1.0	12	nA
(Note 1)		$T_A = +125°C$, Device Operating	—	1.2	14	—	1.2	14	—	1.5	22	
Input Bias Current	I_B	$T_j = +125°C$	—	±1.5	±10	—	±1.5	±10	—	±1.8	±15	nA
(Note 1)		$T_A = +125°C$, Device Operating	—	±2.2	±18	—	±2.2	±18	—	±2.7	±28	
Input Voltage Range	IVR		+10.2	+14.6	—	+10.2	+14.6	—	+10.1	+14.6	—	V
			−10.2	−11.3	—	−10.2	−11.3	—	−10.1	−11.3	—	
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm IVR$	82	97	—	82	97	—	80	93	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 16V$	—	10	100	—	15	100	—	—	—	µV/V
		$V_S = \pm 10V$ to $\pm 15V$	—	—	—	—	—	—	—	23	126	
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$ $V_O = \pm 10V$	30	110	—	30	110	—	25	100	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 10k\Omega$	±12	±13	—	±12	±13	—	±12	±13	—	V

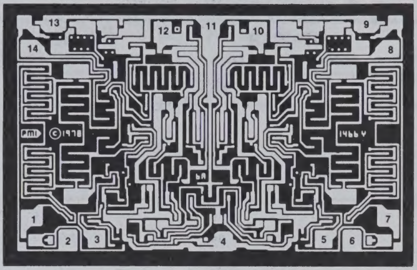
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $0°C \le T_A \le +70°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-215E			OP-215F			OP-215G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	—	0.4	1.65	—	1.4	2.65	—	3.5	8.0	mV
Average Input Offset Voltage Drift												
Without External Trim	TCV_{OS}	(Note 3)	—	3	15	—	3	15	—	6	—	µV/°C
With External Trim	TCV_{OSn}	$R_P = 100k\Omega$	—	3	—	—	3	—	—	4	—	
Input Offset Current	I_{OS}	$T_j = +70°C$	—	0.06	0.45	—	0.06	0.45	—	0.08	0.65	nA
(Note 1)		$T_A = +70°C$, Device Operating	—	0.08	0.80	—	0.08	0.80	—	0.10	1.2	
Input Bias Current	I_B	$T_j = +70°C$	—	±0.12	±0.70	—	±0.12	±0.70	—	±0.14	±0.9	nA
(Note 1)		$T_A = +70°C$, Device Operating	—	±0.16	±1.40	—	±0.16	±1.40	—	±0.19	±1.8	
Input Voltage Range	IVR		+10.2	+14.7	—	+10.2	+14.7	—	+10.1	+14.7	—	V
			−10.2	−11.4	—	−10.2	−11.4	—	−10.1	−11.3	—	
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm IVR$	80	98	—	80	98	—	76	94	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 16V$	—	13	100	—	13	100	—	—	—	µV/V
		$V_S = \pm 10V$ to $\pm 15V$	—	—	—	—	—	—	—	20	159	
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$ $V_O = \pm 10V$	50	180	—	50	180	—	35	130	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 10k\Omega$	±12	±13	—	±12	±13	—	±12	±13	—	V

NOTES:

1. Input bias current is specified for two different conditions. The $T_j = 25°C$ specification is with the junction at ambient temperature; the Device Operating specification is with the device operating in a warmed-up condition at 25°C ambient. The warmed-up bias current value is correlated to the junction temperature value via the curves of I_B vs. T_j and I_B vs. T_A. PMI has a bias current compensation circuit which gives improved bias current and bias current over temperature vs. standard JFET input op amps. I_B and I_{OS} are measured at $V_{CM} = 0$.
2. Settling time is defined here for a unity gain inverter connection using 2kΩ resistors. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within a specified percent of its final value from the time a 10V step input is applied to the inverter. See settling time test circuit.
3. Sample tested.

DICE CHARACTERISTICS (125°C TESTED DICE AVAILABLE)



DIE SIZE 0.059 × 0.093 inch, 5487 sq. mils
(1.50 × 2.36 mm, 3.54 sq. mm)

1. INVERTING INPUT (A)
2. NONINVERTING INPUT (A)
3. NULL (A)
4. V−
5. NULL (B)
6. NONINVERTING INPUT (B)
7. INVERTING INPUT (B)
8. NULL (B)
9. V+
10. V_O (B)
11. V+
12. V_O (A)
13. V+
14. NULL (A)

ALL V+ PADS ARE INTERNALLY CONNECTED.

For additional DICE information refer to Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$ for OP-215N, OP-215G and OP-215GR devices; $T_A = 125°C$ for OP-215NT and OP-215GT devices, unless otherwise noted.

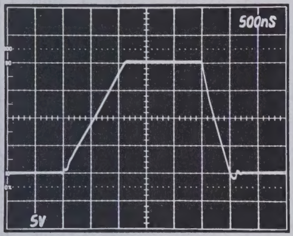
PARAMETER	SYMBOL	CONDITIONS	OP-215NT LIMIT	OP-215N LIMIT	OP-215GT LIMIT	OP-215G LIMIT	OP-215GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	2	1	3	2	6	mV MAX
Input Bias Current	I_B		±18	—	±18	—	—	nA MAX
Input Offset Current	I_{OS}		14	—	14	—	—	nA MAX
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$, $R_L = 2k\Omega$	30	150	30	75	50	V/mV MIN
Input Voltage Range	IVR		±10.2	±10.2	±10.2	±10.2	±10.1	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm IVR$	82	86	82	86	82	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10$ to $\pm 16V$ $V_S = \pm 10$ to $\pm 15V$	100 —	51 —	100 —	80 —	— 100	µV/V MAX
Output Voltage Swing	V_O	$R_L = 10k\Omega$ $R_L = 2k\Omega$	±12 —	±12 ±11	±12 —	±12 ±11	±12 ±11	V MIN
Supply Current	I_{SY}		—	8.5	—	8.5	12.0	mA MAX

NOTE: For 25°C characteristics of NT & GT devices, see N & G characteristics respectively.
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

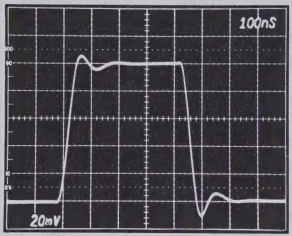
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-215NT TYPICAL	OP-215N TYPICAL	OP-215GT TYPICAL	OP-215G TYPICAL	OP-215GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}	Unnulled $R_p = 100k\Omega$	2	2	3	3	4	µV/°C
Average Input Offset Voltage Drift	TCV_{OSn}	Nulled $R_P = 100k\Omega$	0.5	0.5	1	1	2	µV/°C
Input Offset Current	I_{OS}		3	3	3	3	3	pA
Input Bias Current	I_B		±15	±15	±15	±15	±15	pA
Slew Rate	SR	$A_{VCL} = +1$	17	17	16	16	15	V/µs
Settling Time	t_S	to 0.01% to 0.05% to 0.10%	2.2 1.1 0.9	2.2 1.1 0.9	2.3 1.1 0.9	2.3 1.1 0.9	2.4 1.2 1.0	µs
Gain Bandwidth Product	GBW		6.0	6.0	5.7	5.7	5.4	MHz
Closed-Loop Bandwidth	CLBW	$A_{VCL} = +1$	14	14	13	13	12	MHz
Input Noise Voltage Density	e_n	$f_O = 100Hz$ $f_O = 1000Hz$	20 15	20 15	20 15	20 15	20 15	$nV/\sqrt{Hz}$
Input Noise Current Density	i_n	$f_O = 100Hz$ $f_O = 1000Hz$	0.01	0.01	0.01	0.01	0.01	$pA/\sqrt{Hz}$
Input Capacitance	C_{IN}		3	3	3	3	3	pF

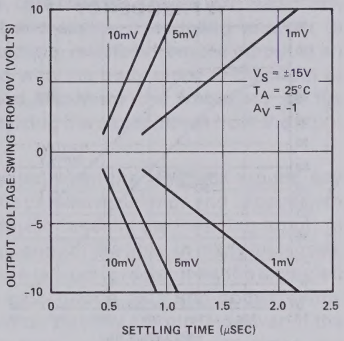
TYPICAL PERFORMANCE CHARACTERISTICS



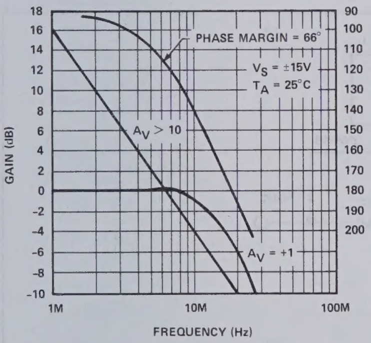
LARGE-SIGNAL TRANSIENT RESPONSE



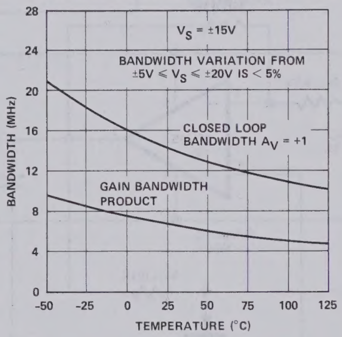
SMALL-SIGNAL TRANSIENT RESPONSE



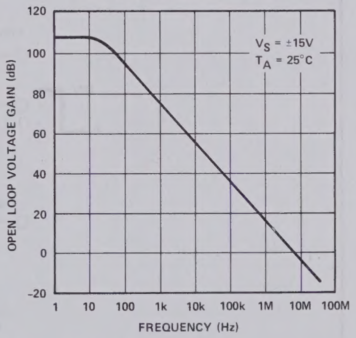
SETTLING TIME



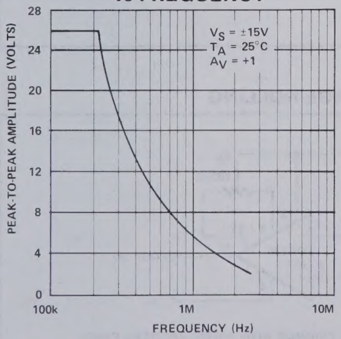
CLOSED-LOOP BANDWIDTH AND PHASE SHIFT vs FREQUENCY



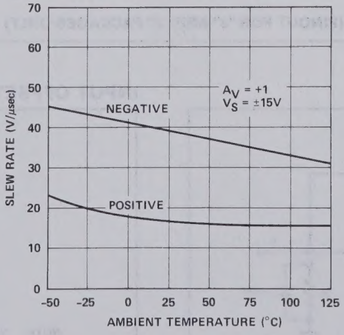
BANDWIDTH vs TEMPERATURE



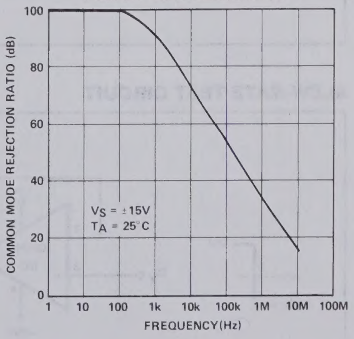
OPEN-LOOP FREQUENCY RESPONSE



MAXIMUM OUTPUT SWING vs FREQUENCY



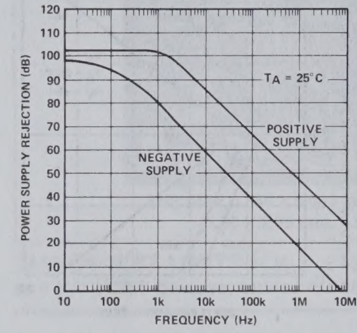
SLEW RATE vs TEMPERATURE



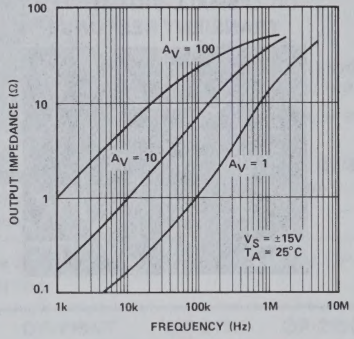
COMMON-MODE REJECTION RATIO vs FREQUENCY

TYPICAL PERFORMANCE CHARACTERISTICS

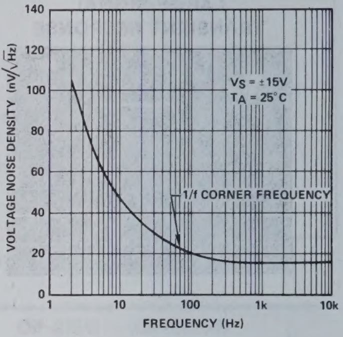
POWER-SUPPLY REJECTION vs FREQUENCY



OUTPUT IMPEDANCE vs FREQUENCY

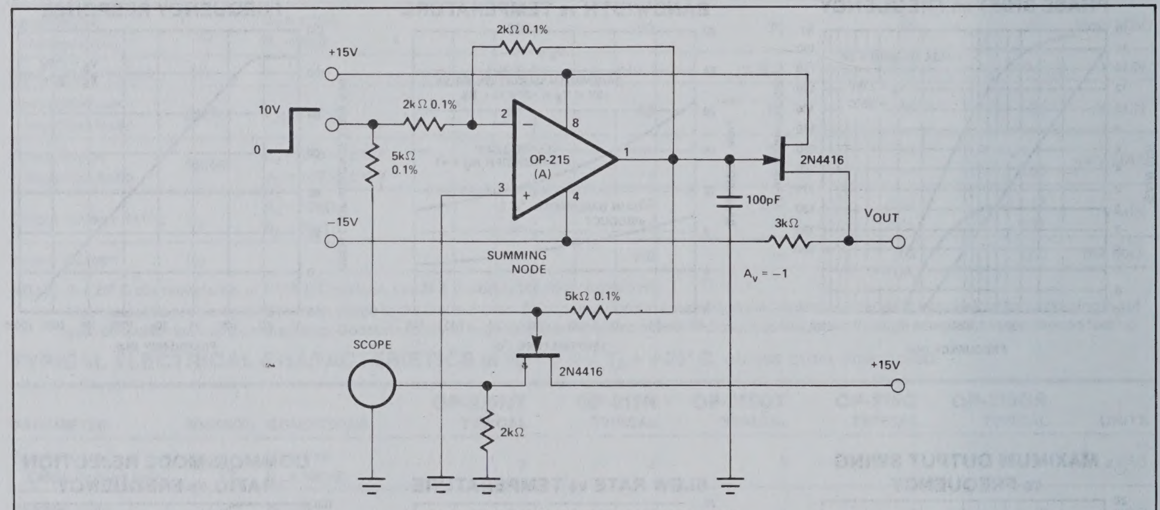


VOLTAGE NOISE DENSITY vs FREQUENCY



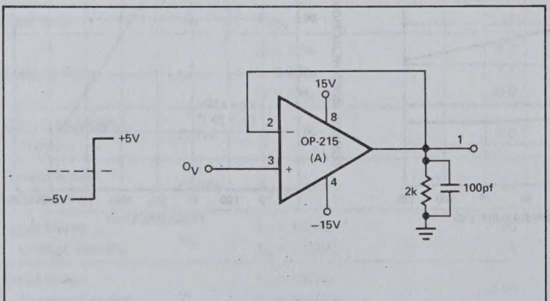
BASIC CONNECTIONS

SETTLING-TIME TEST CIRCUIT


+15V
10V
0
2kΩ 0.1%
2kΩ 0.1%
5kΩ 0.1%
2
8
OP-215 (A)
1
3
4
−15V
SUMMING NODE
5kΩ 0.1%
2N4416
100pF
3kΩ
VOUT
Av = −1
SCOPE
2N4416
+15V
2kΩ

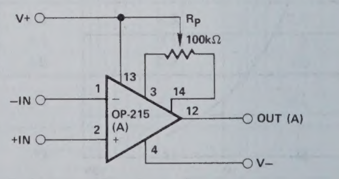
(PINOUT FOR "J" AND "Z" PACKAGES ONLY)

SLEW-RATE TEST CIRCUIT


+5V
−5V
0V
15V
8
2
3
OP-215 (A)
1
4
−15V
2k
100pf

(PINOUT FOR "J" AND "Z" PACKAGES ONLY)

INPUT OFFSET VOLTAGE NULLING

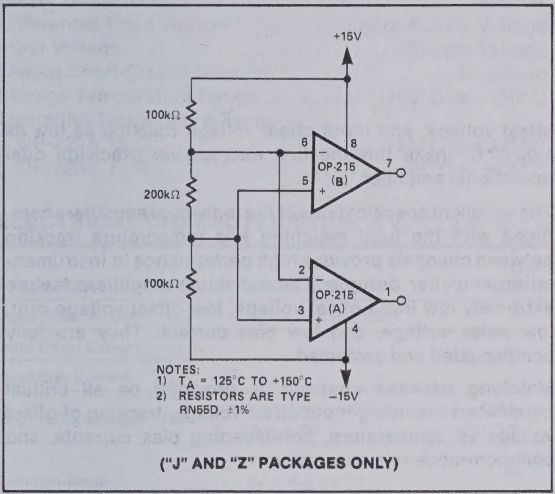

V+
RP
100kΩ
13
3
14
1
−IN
+IN
2
OP-215 (A)
12
OUT (A)
4
V−

NOTE: V_{OS} CAN BE TRIMMED WITH POTENTIOMETERS RANGING FROM 10kΩ TO 1MΩ. FOR MOST UNITS TCV_{OS} WILL BE MINIMUM WHEN V_{OS} IS ADJUSTED WITH A 100kΩ POTENTIOMETER.

("Y" PACKAGE ONLY)

BASIC CONNECTIONS

TYPICAL BURN-IN CIRCUIT



NOTES:
1) T_A = 125°C TO +150°C
2) RESISTORS ARE TYPE RN55D, ±1%

("J" AND "Z" PACKAGES ONLY)

APPLICATIONS INFORMATION

DYNAMIC OPERATING CONSIDERATIONS

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground sets the frequency of the pole. In many instances, the frequency of this pole is much greater than the expected 3dB frequency of the closed-loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3dB frequency, a lead capacitor should be placed from the output to the negative input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than, or equal to, the original feedback-pole time constant.

OP-220

DUAL MICROPOWER OPERATIONAL AMPLIFIER

(SINGLE OR DUAL SUPPLY)

FEATURES

- **Excellent TCV_{OS} Match .... 2μV/°C Max**
- **Low Input Offset Voltage .... 150μV Max**
- **Low Supply Current 100μA**
- **Single-Supply Operation .... +5V to +30V**
- **Low Input Offset Voltage Drift .... 0.75μV/°C**
- **High Open-Loop Gain 2000V/mV**
- **High PSRR 2μV/V**
- **Low Input Bias Current 12nA**
- **Wide Common-Mode Voltage Range .... V− to within 1.5V of V+**
- **Pin Compatible with 1458, LM158, LM2904**

GENERAL DESCRIPTION

The OP-220 is a monolithic dual operational amplifier that can be used either in single or dual supply operation. The low offset voltage, and input offset voltage tracking as low as 1.0μV/°C, make this the first micropower precision dual operational amplifier.

The excellent specifications of the individual amplifiers combined with the tight matching and temperature tracking between channels provides high performance in instrumentation amplifier designs. The individual amplifiers feature extremely low input offset voltage, low offset voltage drift, low noise voltage, and low bias current. They are fully compensated and protected.

Matching between channels is provided on all critical parameters including input offset voltage, tracking of offset voltage vs. temperature, non-inverting bias currents, and common-mode rejection ratios.

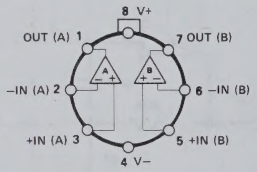
ORDERING INFORMATION†

$T_A = 25°C$ V_{OS} MAX (μV)	PACKAGE HERMETIC TO-99 8-PIN	 HERMETIC DIP 8-PIN	OPERATING TEMPERATURE RANGE
150	OP220AJ*	OP220AZ*	MIL
150	OP220EJ	OP220EZ	IND
300	OP220BJ*	OP220BZ*	MIL
300	OP220FJ	OP220FZ	IND
750	OP220CJ*	OP220CZ*	MIL
750	OP220GJ	OP220GZ	IND

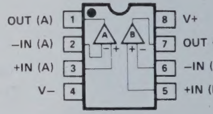
*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

PIN CONNECTIONS

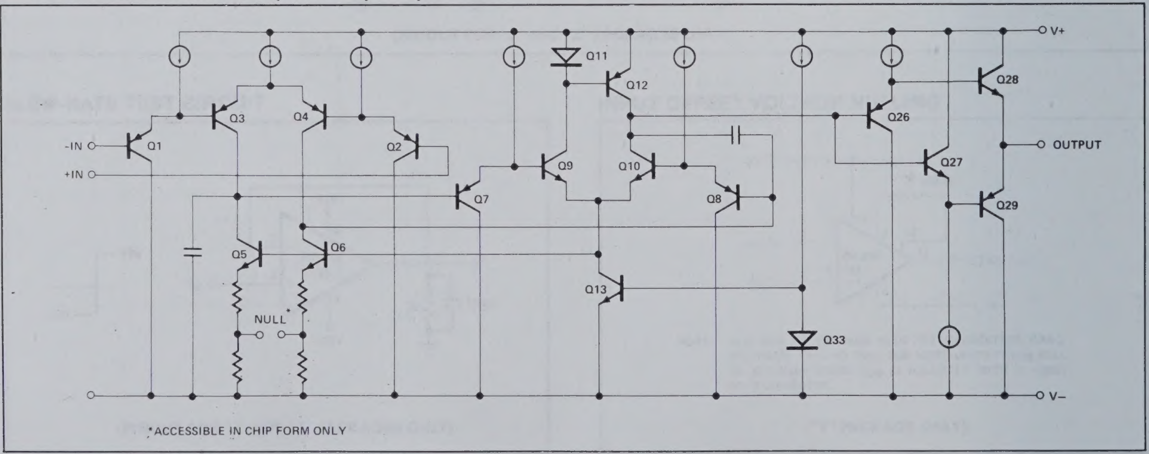


TO-99 (J-Suffix)



8-PIN HERMETIC DIP (Z-Suffix)

SIMPLIFIED SCHEMATIC (Each Amplifier)



ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage	±18V
Power Dissipation (Note 1)	500mW
Differential Input Voltage	30V or Supply Voltage
Input Voltage	Supply Voltage
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
OP-220A, B, C	−55°C to +125°C
OP-220E, F, G	−25°C to +85°C
Lead Temperature (Soldering, 60 sec.)	300°C
DICE Junction Temperature (T_j)	−65°C to +150°C

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.
2. Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 2.5V$ to $\pm 15V$, $T_A = +25°C$, unless otherwise noted.

			OP-220A/E			OP-220B/F			OP-220C/G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	—	120	150	—	250	300	—	500	750	μV
Input Offset Current	I_{OS}		—	0.15	1.5	—	0.2	2	—	0.2	3.5	nA
Input Bias Current	I_B		—	12	20	—	13	25	—	14	30	nA
Input Voltage Range	IVR	V+ = 5V, V− = 0V,	0/3.5	—	—	0/3.5	—	—	0/3.5	—	—	V
		$V_S = \pm 15V$	−15/13.5	—	—	−15/13.5	—	—	−15/13.5	—	—	
Common-Mode Rejection Ratio	CMRR	V+ = 5V, V− = 0V, $0V \leq V_{CM} \leq 3.5V$	90	100	—	85	90	—	75	85	—	dB
		$V_S = \pm 15V$, $-15V \leq V_{CM} \leq 13.5V$	95	100	—	90	95	—	80	90	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$	—	3	10	—	10	32	—	32	100	μV/V
		V− = 0V, V+ = 5V to 30V	—	6	18	—	18	57	—	57	180	
Large-Signal Voltage Gain	A_{VO}	V+ = 5V, V− = 0V, $R_L = 100k\Omega$, $1V \leq V_O \leq 3.5V$	500	1000	—	500	800	—	300	500	—	V/mV
		$V_S = \pm 15V$, $R_L = 25k\Omega$, $V_O = \pm 10V$	1000	2000	—	1000	2000	—	800	1600	—	
Output Voltage Swing	V_O	V+ = 5V, V− = 0V, $R_L = 10k\Omega$	0.7/4	—	—	0.7/4	—	—	0.8/4	—	—	V
		$V_S = \pm 15V$, $R_L = 25k\Omega$	±14	—	—	±14	—	—	±14	—	—	
Slew Rate	SR	$R_L = 25k\Omega$, (Note 1)	—	0.05	—	—	0.05	—	—	0.05	—	V/μs
Bandwidth	BW	$A_{VCL} = +1$, $R_L = 25k\Omega$	—	100	—	—	100	—	—	100	—	kHz
Supply Current (Both Amplifiers)	I_{SY}	$V_S = \pm 2.5V$, No Load	—	100	115	—	115	125	—	125	135	μA
		$V_S = \pm 15V$, No Load	—	140	170	—	150	190	—	205	220	

ELECTRICAL CHARACTERISTICS at $V_S = \pm 2.5V$ to $\pm 15V$, $-55°C \leq T_A \leq +125°C$ for OP-220A, B, and C, $-25°C \leq T_A \leq +85°C$ for OP-220 E, F, and G, unless otherwise noted.

			OP-220A/E			OP-220B/F			OP-220C/G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	$V_S = \pm 15V$	—	0.75	1.5	—	1.2	2	—	2	3	μV/°C
Input Offset Voltage	V_{OS}		—	200	300	—	400	500	—	1000	1300	μV
Input Offset Current	I_{OS}		—	0.5	2	—	0.6	2.5	—	0.8	5	nA
Input Bias Current	I_B		—	12	25	—	13	30	—	14	40	nA
Input Voltage Range	IVR	V+ = 5V, V− = 0V,	0/3.2	—	—	0/3.2	—	—	0/3.2	—	—	V
		$V_S = \pm 15V$	−15/13.2	—	—	−15/13.2	—	—	−15/13.2	—	—	
Common-Mode Rejection Ratio	CMRR	V+ = 5V, V− = 0V, $0V \leq V_{CM} \leq 3.2V$	85	90	—	80	85	—	70	80	—	dB
		$V_S = \pm 15V$, $-15V \leq V_{CM} \leq 13.2V$	90	95	—	85	90	—	75	85	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$	—	6	18	—	18	57	—	57	180	μV/V
		V− = 0V, V+ = 5V to 30V	—	10	32	—	32	100	—	100	320	

ELECTRICAL CHARACTERISTICS at $V_S = \pm2.5V$ to $\pm15V$, $-55°C \le T_A \le +125°C$ for OP-220A, B, and C, $-25°C \le T_A \le +85°C$ for OP-220 E, F, and G, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-220A/E MIN	OP-220A/E TYP	OP-220A/E MAX	OP-220B/F MIN	OP-220B/F TYP	OP-220B/F MAX	OP-220C/G MIN	OP-220C/G TYP	OP-220C/G MAX	UNITS
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm15V$, $R_L = 50k\Omega$ $V_O = \pm10V$	500	1000	—	500	800	—	400	500	—	V/mV
Output Voltage Swing	V_O	$V+ = 5V$, $V- = 0V$, $R_L = 20k\Omega$	0.9/3.8	—	—	0.9/3.8	—	—	1/3.8	—	—	V
		$V_S = \pm15V$, $R_L = 50k\Omega$	±13.8	—	—	±13.8	—	—	±13.8	—	—	
Supply Current (Both Amplifiers)	I_{SY}	$V_S = \pm2.5V$, No Load	—	135	170	—	155	185	—	170	210	μA
		$V_S = \pm15V$, No Load	—	190	250	—	200	280	—	275	330	

NOTE: 1. Sample tested.

MATCHING CHARACTERISTICS at $V_S = \pm15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-220A/E MIN	OP-220A/E TYP	OP-220A/E MAX	OP-220B/F MIN	OP-220B/F TYP	OP-220B/F MAX	OP-220C/G MIN	OP-220C/G TYP	OP-220C/G MAX	UNITS
Input Offset Voltage Match	ΔV_{OS}		—	150	300	—	250	500	—	300	600	μV
Average Noninverting Bias Current	I_B+		—	10	20	—	15	25	—	20	30	nA
Non-Inverting Offset Current	$I_{OS}+$		—	0.7	1.5	—	1	2	—	1.4	2.5	nA
Common-Mode Rejection Ratio Match (Note 1)	ΔCMRR	$V_{CM} = -15V$ to $+13.5V$	92	100	—	87	95	—	72	85	—	dB
Power Supply Rejection Ratio Match (Note 2)	ΔPSRR	$V_S = \pm2.5V$ to $\pm15V$	—	6	14	—	18	44	—	57	140	μV/V

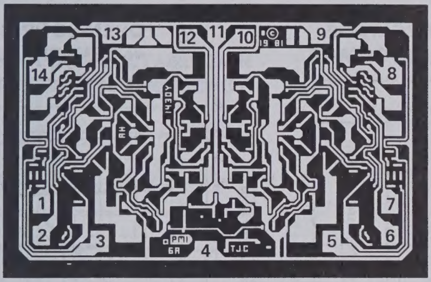
MATCHING CHARACTERISTICS at $V_S = \pm15V$, $-55°C \le T_A \le +125°C$ for OP-220A, B and C; $-25°C \le T_A \le +85°C$ for OP-220 E, F and G, unless otherwise noted. Grades E, F, and G are sample tested.

PARAMETER	SYMBOL	CONDITIONS	OP-220A/E MIN	OP-220A/E TYP	OP-220A/E MAX	OP-220B/F MIN	OP-220B/F TYP	OP-220B/F MAX	OP-220C/G MIN	OP-220C/G TYP	OP-220C/G MAX	UNITS
Input Offset Voltage Match	ΔV_{OS}		—	250	500	—	400	800	—	800	1800	μV
Input Offset Voltage Tracking	$TC\Delta V_{OS}$		—	1	2	—	1.5	3	—	1.5	5	μV/°C
Average Noninverting Bias Current	I_B+		—	10	25	—	15	30	—	22	40	nA
Average Drift of Noninverting Bias Current	TCI_B+		—	15	25	—	15	30	—	30	50	pA/°C
Non-Inverting Offset Current	$I_{OS}+$		—	0.7	2	—	1	2.5	—	2.5	5	nA
Average Drift of Non-Inverting Offset Current	$TCI_{OS}+$		—	7	15	—	12	22.5	—	15	30	pA/°C
Common-Mode Rejection Ratio Match (Note 1)	ΔCMRR	$V_{CM} = -15V$ to $+13V$	87	98	—	82	96	—	72	80	—	dB
Power Supply Rejection Ratio Match (Note 2)	ΔPSRR	$V_S = \pm2.5V$ to $\pm15V$	—	10	26	—	30	78	—	57	250	μV/V

NOTES:

1. ΔCMRR is $20 \log_{10} V_{CM}/\Delta CME$, where V_{CM} is the voltage applied to both non-inverting inputs and ΔCME is the difference in common-mode input-referred error.
2. ΔPSRR is: $\dfrac{\text{Input-referred differential error}}{\Delta V_S}$

DICE CHARACTERISTICS



DIE SIZE 0.096 × 0.061 inch, 5856 sq. mils
(2.438 × 1.549 mm, 3.78 sq. mm)

NOTE: All V+ PADS ARE INTERNALLY CONNECTED.

1. **INVERTING INPUT (A)**
2. **NONINVERTING INPUT (A)**
3. **BALANCE (A)**
4. **V−**
5. **BALANCE (B)**
6. **NONINVERTING INPUT (B)**
7. **INVERTING INPUT (B)**
8. **BALANCE (B)**
9. **V+**
10. **OUT (B)**
11. **V+**
12. **OUT (A)**
13. **V+**
14. **BALANCE (A)**

For additional DICE information refer to Section 2.

WAFER TEST LIMITS at $V_S = \pm 2.5V$ to $\pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-220N LIMIT	OP-220G LIMIT	OP-220GR LIMIT	UNITS
Input Offset Voltage	V_{OS}		200	500	1000	μV MAX
Input Offset Current	I_{OS}		2	3.5	5	nA MAX
Input Bias Current	I_B		25	30	40	nA MAX
Input Voltage Range	IVR	$V_S = \pm 15V$	−15/13.5	−15/13.5	−15/13.5	V MIN
Common-Mode Rejection Ratio	CMRR	$V- = 0V, V+ = 5V, 0V \le V_{CM} \le 3.5V$ $-15V \le V_{CM} \le 13.5V, V_S = \pm 15V$	88 93	83 88	75 80	dB MIN
Power Supply Rejection Ratio	PSRR	 $V- = 0V, V+ = 5V$ to $30V$	12.5 22.5	40 70	100 180	μV/V MAX
Large-Signal Voltage Gain	A_{VO}	$R_L = 25k\Omega, V_S = \pm 15V$ $V_O = \pm 10V$	1000	800	500	V/mV MIN
Output Voltage Swing	V_O	$V+ = 5V, V- = 0V, R_L = 10k\Omega$ $V_S = \pm 15V, R_L = 25k\Omega$	0.7/4 ±14	0.8/4 ±14	0.8/3.8 ±13.8	V MIN
Supply Current (Both Amplifiers)	I_{SY}	$V_S = \pm 2.5V$, No Load $V_S = \pm 15V$, No Load	125 190	135 220	170 300	μA MAX

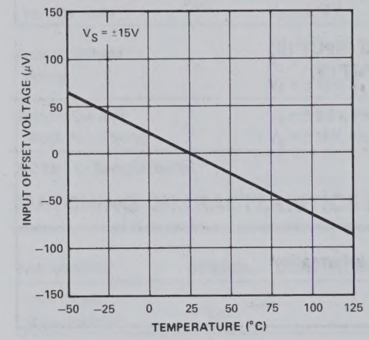
Note: Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

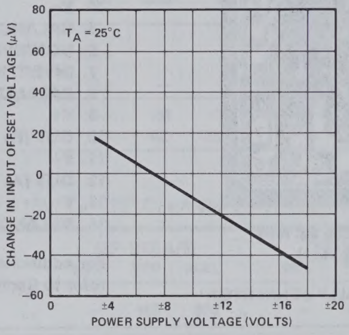
PARAMETER	SYMBOL	CONDITIONS	OP-220N TYPICAL	OP-220G TYPICAL	OP-220GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}		1.5	2	3	μV/°C
Large-Signal Voltage Gain	A_{VO}	$R_L = 25k\Omega$	2000	1600	800	V/mV

TYPICAL PERFORMANCE CHARACTERISTICS

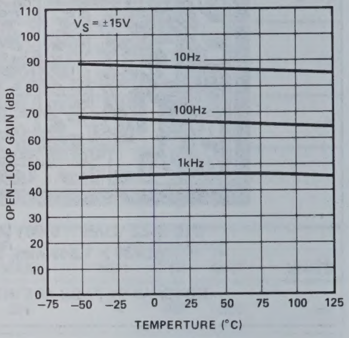
NORMALIZED OFFSET VOLTAGE vs TEMPERATURE



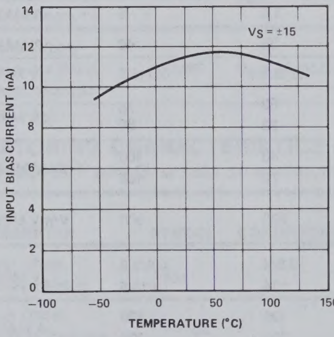
INPUT OFFSET VOLTAGE vs POWER SUPPLY VOLTAGE



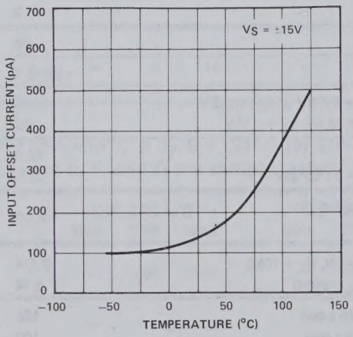
OPEN-LOOP GAIN vs TEMPERATURE



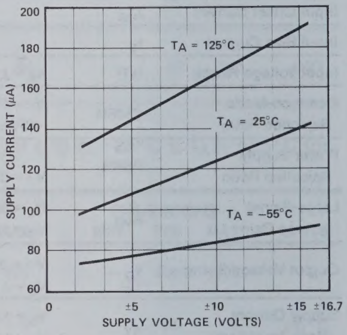
INPUT BIAS CURRENT vs TEMPERATURE



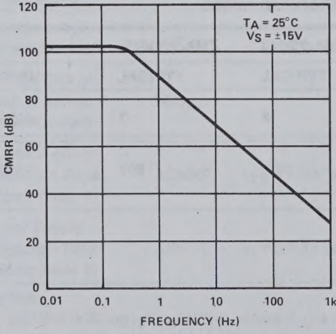
INPUT OFFSET CURRENT vs TEMPERATURE



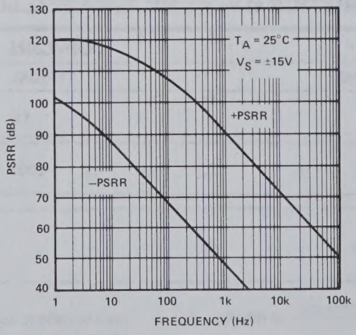
SUPPLY CURRENT vs SUPPLY VOLTAGE



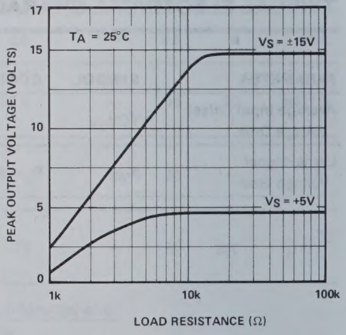
CMMR vs FREQUENCY



PSRR vs FREQUENCY

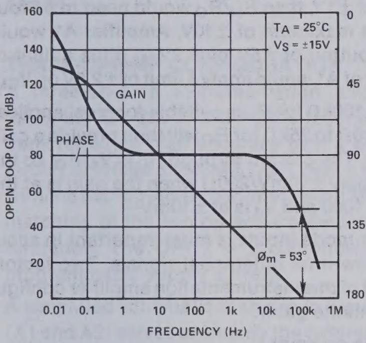


MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE

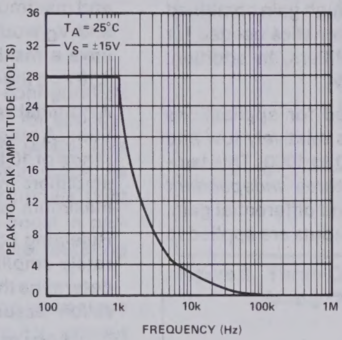


TYPICAL PERFORMANCE CHARACTERISTICS

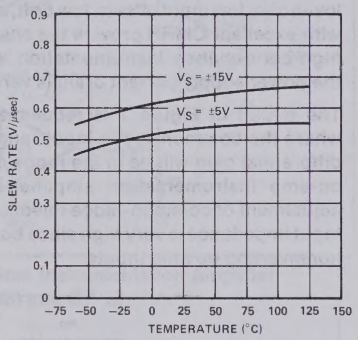
OPEN-LOOP VOLTAGE GAIN AND PHASE vs FREQUENCY



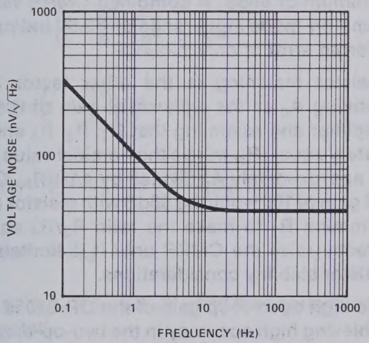
MAXIMUM OUTPUT SWING vs FREQUENCY



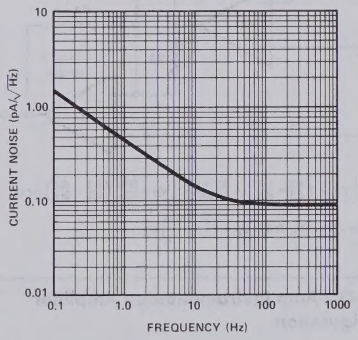
SLEW RATE vs TEMPERATURE



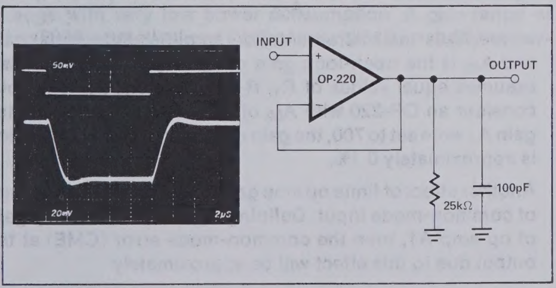
VOLTAGE NOISE DENSITY (e_n) vs FREQUENCY



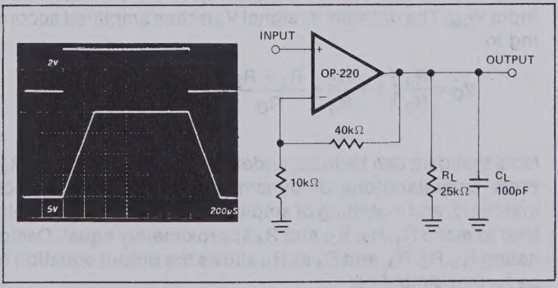
CURRENT NOISE DENSITY (i_n) vs FREQUENCY



SMALL-SIGNAL TRANSIENT RESPONSE


50mV
20mV
2μS
INPUT
OP-220
OUTPUT
100pF
25kΩ

LARGE-SIGNAL TRANSIENT RESPONSE

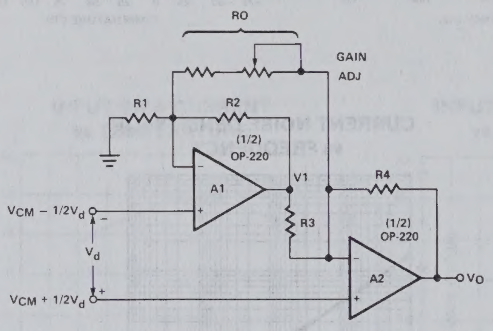

2V
5V
200μS
INPUT
OP-220
OUTPUT
40kΩ
10kΩ
R_L
25kΩ
C_L
100pF

INSTRUMENTATION AMPLIFIER APPLICATIONS OF THE OP-220

TWO-OP-AMP CONFIGURATION

The excellent input characteristics of the OP-220 make it ideal for use in *instrumentation amplifier* configurations where low-level differential signals are to be amplified. The low-noise, low input offsets, low drift, and high gain combined with excellent CMRR provide the characteristics needed for high-performance instrumentation amplifiers. In addition, the power supply current drain is very low.

The circuit of Figure 1 is recommended for applications where the common-mode input range is relatively low and differential gain will be in the range of 10 to 1000. This two-op-amp instrumentation amplifier features *independent* adjustment of common-mode rejection and differential gain. Input impedance is very high since both inputs are applied to noninverting op amp inputs.



$$V_O = \frac{R4}{R3}\left[1 + \frac{1}{2}\left(\frac{R2}{R1} + \frac{R3}{R4}\right) + \frac{R2 + R3}{R0}\right] V_d + \frac{R4}{R3}\left(\frac{R3}{R4} - \frac{R2}{R1}\right) V_{CM}$$

IF $R1 = R2 = R3 = R4$, THEN $V_O = 2\left(1 + \frac{R1}{R0}\right) V_d$

Figure 1. Two-Op-Amp Instrumentation Amplifier Configuration

The input voltages are represented as a common-mode input V_{CM} plus a differential input V_d. The ratio R_3/R_4 is made equal to the ratio R_2/R_1 to reject the common-mode input V_{CM}. The differential signal V_d is then amplified according to:

$$V_O = \frac{R_4}{R_3}\left(1 + \frac{R_3}{R_4} + \frac{R_2 + R_3}{R_O}\right) V_d, \text{ where } \frac{R_3}{R_4} = \frac{R_2}{R_1}$$

Note that gain can be independently varied by adjusting R_O. From considerations of dynamic range, resistor tempco matching, and matching of amplifier response, it is generally best to make R_1, R_2, R_3, and R_4 approximately equal. Designating R_1, R_2, R_3, and R_4 as R_N allows the output equation to be further simplified:

$$V_O = 2\left(1 + \frac{R_N}{R_O}\right) V_d, \text{ where } R_N = R_1 = R_2 = R_3 = R_4$$

Dynamic range is limited by A1 as well as A2; the output of A1 is:

$$V_1 = -\left(1 + \frac{R_N}{R_O}\right) V_d + 2\,V_{CM}$$

If the instrumentation amplifier were designed for a gain of 10 and maximum V_d of ±1V, then R_N/R_O would need to be four and V_O would be a maximum of ±10V. Amplifier A1 would have a maximum output of ±5V plus $2V_{CM}$, thus a limit of ±10V on the output of A1 would imply a limit of ±2.5V on V_{CM}.

A nominal value of 100kΩ for R_N is suitable for most applications. A range of 200Ω to 25kΩ for R_O will then provide a gain range of 10 to 1000. The current through R_O is V_d/R_O, so the amplifiers must supply ±10mV/200Ω when the gain is at the maximum value of 1000 and V_d is at ±10mV.

Rejecting common-mode inputs is most important in accurately amplifying low-level differential signals. Two factors determine the CMR of this instrumentation amplifier configuration (assuming infinite gain):

(1) CMRR of the op amps
(2) Matching of the resistor network ($R_3/R_4 = R_2/R_1$)

In this instrumentation amplifier configuration, error due to CMRR effect is directly proportional to the *differential* CMRR of the op amps. For the OP-220A/E, this combined CMRR is a minimum of 98dB. A combined CMRR value of 100dB and common-mode input range of ±2.5V indicates a peak input-referred error of only ±25μV.

Resistor matching is the other factor affecting CMRR. Defining A_d as the differential gain of the instrumentation amplifier and assuming that R_1, R_2, R_3 and R_4 are approximately equal (R_N will be the nominal value), then CMRR will be approximately A_d divided by $4\Delta R/R_N$. CMRR at differential gain of 100 would be 88dB with resistor matching of 0.1%. Trimming R_1 to make the ratio R_3/R_4 equal to R_2/R_1 will directly raise the CMRR until it is limited by linearity and resistor stability considerations.

The high open-loop gain of the OP-220 is very important in achieving high accuracy in the two-op-amp instrumentation amplifier configuration. Gain error can be approximated by:

$$\text{Gain Error} \sim \frac{1}{1 + \frac{A_d}{A_{02}}}\,, \quad \frac{A_d}{2\,A_{01}\,A_{02}} \ll 1$$

where A_d is the instrumentation amplifier differential gain and A_{02} is the open-loop gain of op amp A2. This analysis assumes equal values of R_1, R_2, R_3, and R_4. For example, consider an OP-220 with A_{02} of 700V/mV. If the differential gain A_d were set to 700, the gain error would be 1/1.001 which is approximately 0.1%.

Another effect of finite op amp gain is undesired feedthrough of common-mode input. Defining A_{01} as the open-loop gain of op amp A1, then the common-mode error (CME) at the output due to this effect will be approximately

$$\text{CME} \sim \frac{2\,A_d}{1 + \frac{A_d}{A_{01}}}\;\frac{1}{A_{01}}\;V_{CM}$$

For $A_d/A_{01}, \ll 1$, this simplifies to $(2\,A_d/A_{01}) \times V_{CM}$. If the op amp gain is 700V/mV, V_{CM} is 2.5V, and A_d is set to 700, then the error at the output due to this effect will be approximately 5mV.

The OP-220 offers a unique combination of excellent dc performance, wide input range, and low supply current drain that is particularly attractive for instrumentation amplifier design.

THREE-OP-AMP CONFIGURATION

A three-op-amp instrumentation amplifier configuration using the OP-220 and OP-22 is recommended for applications requiring high accuracy over a wide gain range. This circuit provides excellent CMR over a wide input range. As with the two-op-amp instrumentation amplifier circuits, tight matching of the two op amps provides a real boost in performance. The OP-22 is a micropower op-amp featuring programmable supply current.

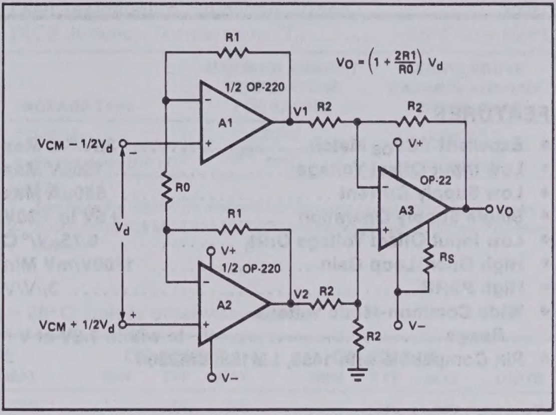


Figure 2. Three-Op-Amp Instrumentation Amplifier Using OP-220 and OP-22

A simplified schematic is shown in Figure 2. The input stage (A1 and A2) serves to amplify the differential input V_d without amplifying the common-mode voltage V_{CM}. The output stage then rejects the common-mode input. With ideal op-amps and no resistor matching errors, the outputs of each amplifier will be:

$$V_1 = -\left(1 + \frac{2R_1}{R_O}\right)\frac{V_d}{2} + V_{CM}$$

$$V_2 = \left(1 + \frac{2R_1}{R_O}\right)\frac{V_d}{2} + V_{CM}$$

$$V_O = V_2 - V_1 = \left(1 + \frac{2R_1}{R_O}\right)V_d$$

$$V_O = A_d\,V_d$$

The differential gain A_d is $1 + 2R_1/R_O$ and the common-mode input V_{CM} is rejected.

This three-op-amp instrumentation amplifier configuration using the OP-220 dual at the input and the OP-22 single at the output can provide excellent performance over a wide gain range with very low power consumption. A gain range of 1 to 2000 is practical and CMR of over 120dB is readily achievable.

OP-221

DUAL LOW-POWER OPERATIONAL AMPLIFIER (SINGLE OR DUAL SUPPLY)

FEATURES

- **Excellent TCV_{OS} Match .... 2µV/°C Max**
- **Low Input Offset Voltage .... 150µV Max**
- **Low Supply Current .... 550µA Max**
- **Single Supply Operation .... +5V to +30V**
- **Low Input Offset Voltage Drift .... 0.75µV/°C**
- **High Open-Loop Gain .... 1500V/mV Min**
- **High PSRR 3µV/V**
- **Wide Common-Mode Voltage Range .... V− to within 1.2V of V+**
- **Pin Compatible with 1458, LM158, LM2904**

GENERAL DESCRIPTION

The OP-221 is a monolithic dual operational amplifier that can be used either in single or dual supply operation. The wide supply voltage range, wide input voltage range, and low supply current drain of the OP-221 make it well-suited for operation from batteries or unregulated power supplies.

ORDERING INFORMATION†

$T_A = 25°C$ V_{OS} MAX (µV)	PACKAGE HERMETIC TO-99 8-PIN	 HERMETIC DIP 8-PIN	OPERATING TEMPERATURE RANGE
150	OP221AJ*	OP221AZ*	MIL
150	OP221EJ	OP221EZ	IND
300	OP221BJ*	OP221BZ*	MIL
300	OP221FJ	OP221FZ	IND
500	OP221CJ*	OP221CZ*	MIL
500	OP221GJ	OP221GZ	IND

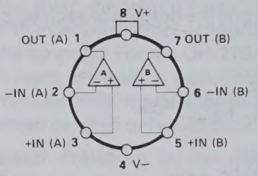
*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

The excellent specifications of the individual amplifiers combined with the tight matching and temperature tracking between channels provide high performance in instrumentation amplifier designs. The individual amplifiers feature very low input offset voltage, low offset voltage drift, low noise voltage, and low bias current. They are fully compensated and protected.

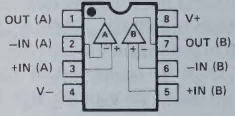
Matching between channels is provided on all critical parameters including input offset voltage, tracking of offset voltage vs. temperature, non-inverting bias currents, and common-mode rejection.

PIN CONNECTIONS

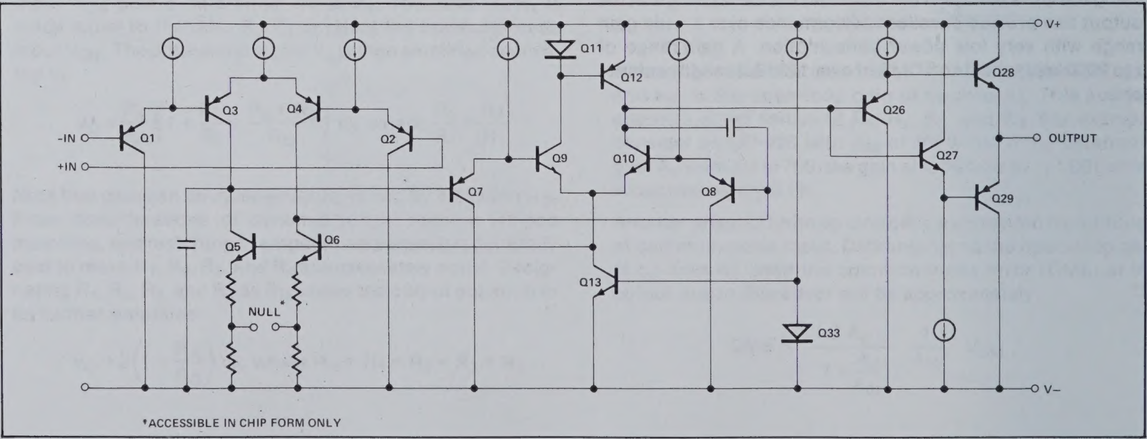


TO-99 (J-Suffix)

8-PIN HERMETIC DIP (Z-Suffix)



SIMPLIFIED SCHEMATIC (Each Amplifier)



*ACCESSIBLE IN CHIP FORM ONLY

ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage	±18V
Power Dissipation (Note 1)	500mW
Differential Input Voltage	30V or Supply Voltage
Input Voltage	Supply Voltage
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	−65° C to +150° C
Operating Temperature Range	
OP-221A, B, C	−55° C to +125° C
OP-221E, F, G	−25° C to +85° C
Lead Temperature (Soldering, 60 sec.)	300° C
DICE Junction Temperature (T_j)	−65° C to +150° C

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80° C	7.1mW/° C
8-Pin Hermetic DIP (Z)	75° C	6.7mW/° C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.
2. Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 2.5V$ to $\pm 15V$, $T_A = 25°C$, unless otherwise noted.

			OP-221A/E			OP-221B/F			OP-221C/G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		—	75	150	—	150	300	—	250	500	μV
Input Offset Current	I_{OS}		—	0.5	3	—	1	5	—	1.5	7	nA
Input Bias Current	I_B		—	50	80	—	60	100	—	70	120	nA
Input Voltage Range	IVR	V+ = 5V, V− = 0V $V_S = \pm 15V$	0/3.5 −15/13.5	— —	— —	0/3.5 −15/13.5	— —	— —	0/3.5 −15/13.5	— —	— —	V
Common-Mode Rejection Ratio	CMRR	V+ = 5V, V− = 0V, $0V \leq V_{CM} \leq 3.5V$ $V_S = \pm 15V$, $-15V \leq V_{CM} \leq 13.5V$	90 95	100 100	— —	85 90	90 95	— —	75 80	85 90	— —	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$ V− = 0V, V+ = 5V to 30V	— —	3 6	10 18	— —	10 18	32 57	— —	32 57	100 180	μV/V
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $R_L = 10k\Omega$, $V_O = \pm 10V$	1500	—	—	1000	—	—	800	—	—	V/mV
Output Voltage Swing	V_O	V+ = 5V, V− = 0V, $R_L = 10k\Omega$ $V_S = \pm 15V$, $R_L = 10k\Omega$	0.7/4.1 ±13.8	— —	— —	0.7/4.1 ±13.8	— —	— —	0.8/4 ±13.5	— —	— —	V
Slew Rate	SR	$R_L = 10k\Omega$, (Note 1)	0.2	0.3	—	0.2	0.3	—	0.2	0.3	—	V/μs
Bandwidth	BW		—	600	—	—	600	—	—	600	—	kHz
Supply Current (Both Amplifiers)	I_{SY}	$V_S = \pm 2.5V$, No Load $V_S = \pm 15V$, No Load	— —	450 600	550 800	— —	500 800	600 850	— —	550 850	650 900	μA

ELECTRICAL CHARACTERISTICS at $V_S = \pm 2.5V$ to $\pm 15V$, $-55°C \leq T_A \leq +125°C$ for OP-221A, B and C; $-25°C \leq T_A \leq +85°C$ for OP-221E, F and G, unless otherwise noted.

			OP-221A/E			OP-221B/F			OP-221C/G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}		—	0.75	1.5	—	1.2	2	—	2	3	μV/° C
Input Offset Voltage	V_{OS}		—	150	300	—	250	450	—	400	700	μV
Input Offset Current	I_{OS}		—	1	5	—	1.5	7	—	2	10	nA
Input Bias Current	I_B		—	55	100	—	65	120	—	80	140	nA
Input Voltage Range	IVR	V+ = 5V, V− = 0V $V_S = \pm 15V$	0/3.2 −15/13.2	— —	— —	0/3.2 −15/13.2	— —	— —	0/3.2 −15/13.2	— —	— —	V
Common-Mode Rejection Ratio	CMRR	V+ = 5V, V− = 0V, $0V \leq V_{CM} \leq 3.2V$ $V_S = \pm 15V$, $-15V \leq V_{CM} \leq 13.2V$	85 90	90 95	— —	80 85	85 90	— —	70 75	80 85	— —	dB

ELECTRICAL CHARACTERISTICS at $V_S = \pm 2.5V$ to $\pm 15V$, $-55°C \leq T_A \leq +125°C$ for OP-221A, B and C; $-25°C \leq T_A \leq +85°C$ for OP-221E, F and G, unless otherwise noted. (Continued)

			OP-221A/E			OP-221B/F			OP-221C/G			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$ $V- = 0V$, $V+ = 5V$ to $30V$	— —	6 10	18 32	— —	18 32	57 100	— —	57 100	180 320	µV/V
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $R_L = 10k\Omega$ $V_O = \pm 10V$	1000	—	—	800	—	—	600	—	—	V/mV
Output Voltage Swing	V_O	$V+ = 5V$, $V- = 0V$, $R_L = 10k\Omega$ $V_S = \pm 15V$, $R_L = 10k\Omega$	0.8/3.8 ±13.5	— ±14	— —	0.8/3.8 ±13.5	— ±14	— —	0.9/3.7 ±13.2	— —	— —	V
Supply Current (Both Amplifiers)	I_{SY}	$V_S = \pm 2.5V$, No Load $V_S = \pm 15V$, No Load	— —	500 700	650 900	— —	550 900	700 950	— —	600 950	750 1000	µA

NOTE:

1. Sample tested.

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

			OP-221A/E			OP-221B/F			OP-221C/G			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage Match	ΔV_{OS}		—	50	200	—	150	400	—	250	600	µV
Average Noninverting Bias Current	I_B+		—	—	80	—	—	100	—	—	120	nA
Noninverting Input Offset Current	$I_{OS}+$		—	2	5	—	2	5	—	4	10	nA
Common-Mode Rejection Ratio Match (Note 1)	ΔCMRR	$V_{CM} = -15V$ to $+13.5V$	92	—	—	87	—	—	72	—	—	dB
Power Supply Rejection Ratio Match (Note 2)	ΔPSRR	$V_S = \pm 2.5V$ to $\pm 15V$	—	—	14	—	—	44	—	—	140	µV/V

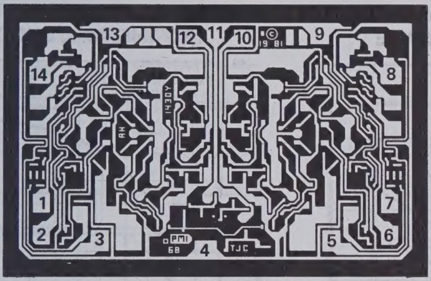
MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$ for OP-221A, B and C; $-25°C \leq T_A \leq +85°C$ for OP-221E, F and G, unless otherwise noted. Grades E, F, and G are sample tested.

			OP-221A/E			OP-221B/F			OP-221C/G			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage Match	ΔV_{OS}		—	100	400	—	250	600	—	400	800	µV
Average Noninverting Bias Current	I_B+		—	—	100	—	—	120	—	—	140	nA
Input Offset Voltage Tracking	$TC\Delta V_{OS}$	(Note 3)	—	1	2	—	1	3	—	3	5	µV/°C
Noninverting Input Offset Current	$I_{OS}+$		—	3	7	—	3	7	—	6	12	nA
Common-Mode Rejection Ratio Match (Note 1)	ΔCMRR	$V_{CM} = -15V$ to $+13.2V$	87	90	—	82	85	—	72	80	—	dB
Power Supply Rejection Ratio Match (Note 2)	ΔPSRR		—	—	26	—	—	78	—	—	250	µV/V

NOTE:

1. ΔCMRR is $20 \log_{10} V_{CM}/\Delta CME$, where V_{CM} is the voltage applied to both noninverting inputs and ΔCME is the difference in common-mode input-referred error.
2. ΔPSRR is: $\dfrac{\text{Input-Referred Differential Error}}{\Delta V_S}$
3. Sample tested.

DICE CHARACTERISTICS



DIE SIZE 0.096 × 0.061 inch, 5856 sq. mils (2.44 × 1.55 mm, 3.78 sq. mm)

NOTE: All V+ PADS ARE INTERNALLY CONNECTED.

1. **INVERTING INPUT (A)**
2. **NONINVERTING INPUT (A)**
3. **BALANCE (A)**
4. **V−**
5. **BALANCE (B)**
6. **NONINVERTING INPUT (B)**
7. **INVERTING INPUT (B)**
8. **BALANCE (B)**
9. **V+**
10. **OUT (B)**
11. **V+**
12. **OUT (A)**
13. **V+**
14. **BALANCE (A)**

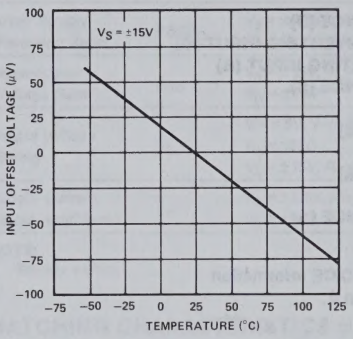
For additional DICE information refer to Section 2.

WAFER TEST LIMITS at $V_S = \pm 2.5V$ to $\pm 15V$, $T_A = 25°C$, unless otherwise noted.

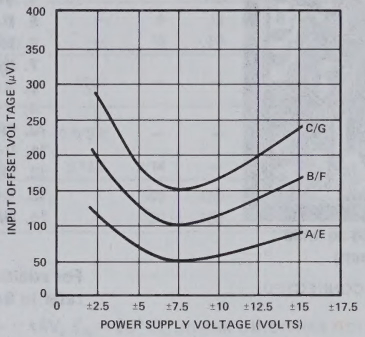
PARAMETER	SYMBOL	CONDITIONS	OP-221N LIMIT	OP-221G LIMIT	OP-221GR LIMIT	UNITS
Input Offset Voltage	V_{OS}		200	350	500	μV MAX
Input Offset Current	I_{OS}		3.5	5.5	7	nA MAX
Input Bias Current	I_B		85	105	120	nA MAX
Input Voltage Range	IVR	V+ = 5V, V− = 0V $V_S = \pm 15V$	0/3.5 −15/13.5	0/3.5 −15/13.5	0/3.5 −15/13.5	V MIN/MAX V MIN
Common-Mode Rejection Ratio	CMRR	V− = 0V, V+ = 5V, $0V \le V_{CM} \le 3.5V$ $V_S = \pm 15V$, $-15V \le V_{CM} \le 13.5V$	88 93	83 88	75 80	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$ V− = 0V, V+ = 5V to 30V	12.5 22.5	40 70	100 180	μV/V MAX
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$ $R_L = 10k\Omega$	1500	1000	800	V/mV MIN
Output Voltage Swing	V_O	V+ = 5V, V− = 0V, $R_L = 10k\Omega$ $V_S = \pm 15V$, $R_L = 10k\Omega$	0.7/4.1 ±13.8	0.7/4.1 ±13.8	0.8/4 ±13.5	V MIN/MAX V MIN
Supply Current (Both Amplifiers)	I_{SY}	$V_S = \pm 2.5V$, No Load $V_S = \pm 15V$, No Load	560 810	610 860	650 900	μA MAX

Note: Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

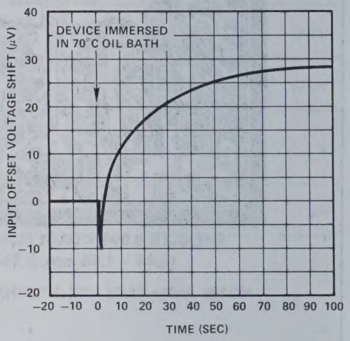
TYPICAL PERFORMANCE CHARACTERISTICS



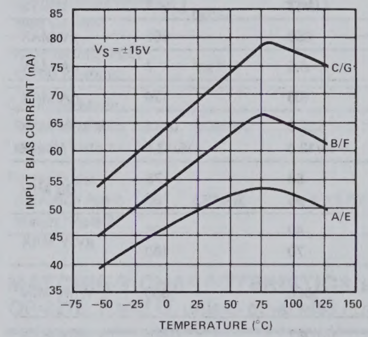
NORMALIZED INPUT OFFSET VOLTAGE vs TEMPERATURE



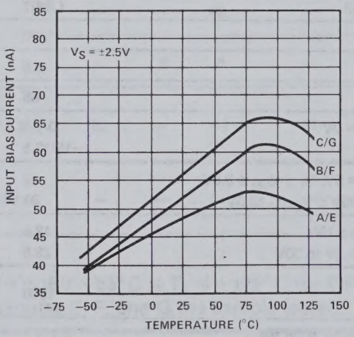
INPUT OFFSET VOLTAGE vs SUPPLY VOLTAGE



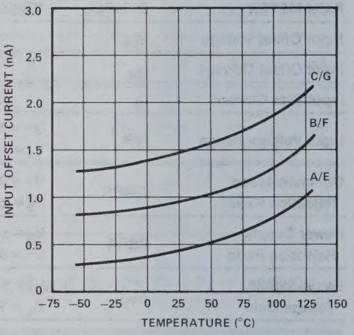
OFFSET VOLTAGE SHIFT DUE TO THERMAL SHOCK



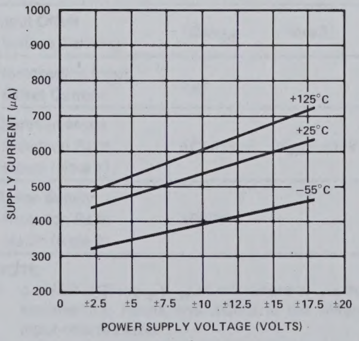
INPUT BIAS CURRENT vs TEMPERATURE



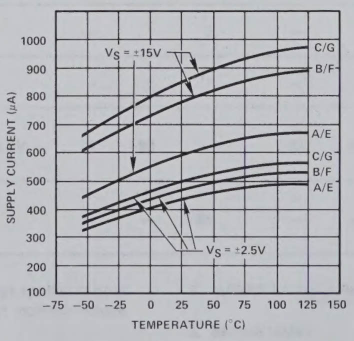
INPUT BIAS CURRENT vs TEMPERATURE



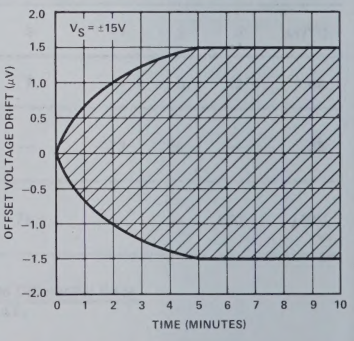
INPUT OFFSET CURRENT vs TEMPERATURE



SUPPLY CURRENT vs SUPPLY VOLTAGE FOR OP-221A/E



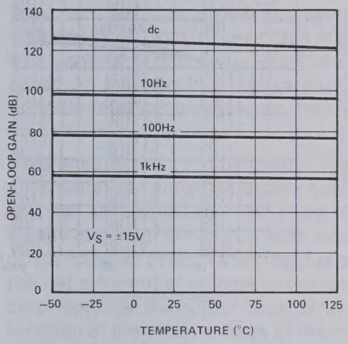
SUPPLY CURRENT vs TEMPERATURE AT $V_S = \pm15V$ AND $\pm2.5V$



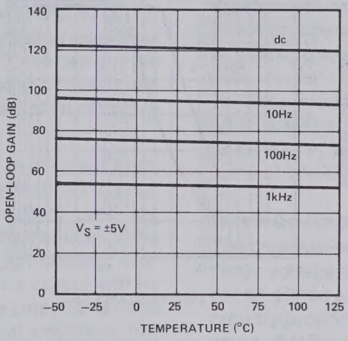
INITIAL OFFSET VOLTAGE DRIFT vs TIME

TYPICAL PERFORMANCE CHARACTERISTICS

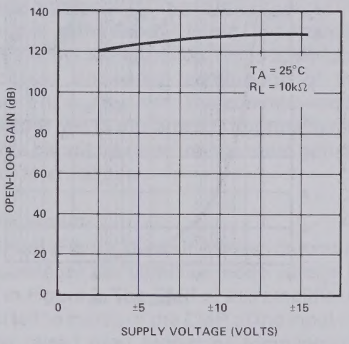
OPEN-LOOP GAIN AT ±15V vs TEMPERATURE



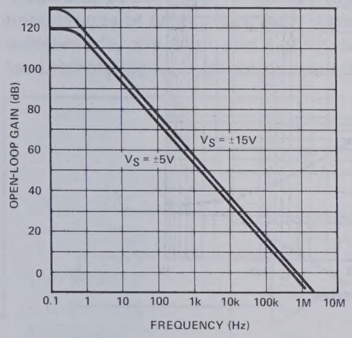
OPEN-LOOP GAIN AT ±5V vs TEMPERATURE



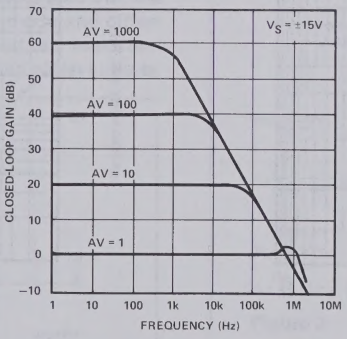
OPEN-LOOP GAIN vs SUPPLY VOLTAGE



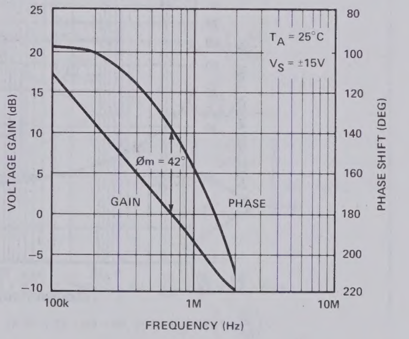
OPEN-LOOP GAIN vs FREQUENCY



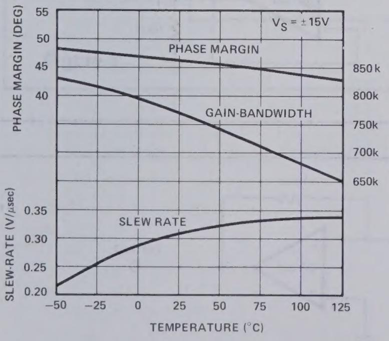
CLOSED-LOOP GAIN vs FREQUENCY



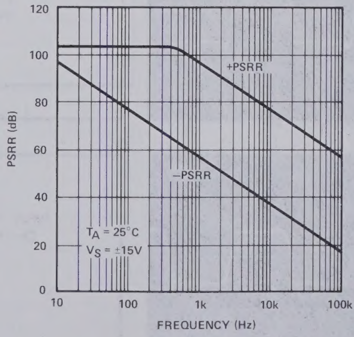
GAIN AND PHASE SHIFT vs FREQUENCY



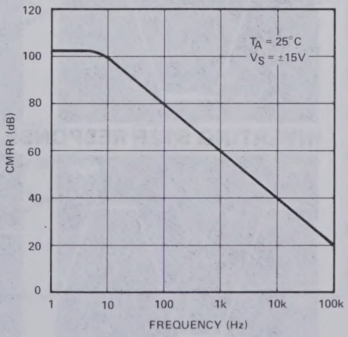
PHASE MARGIN, GAIN-BANDWIDTH, AND SLEW RATE vs TEMPERATURE



PSRR vs FREQUENCY

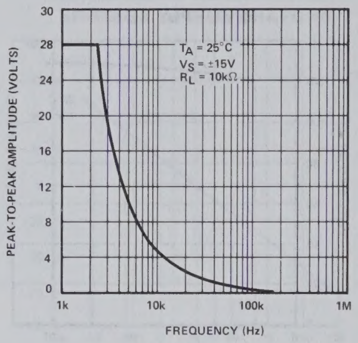


CMRR vs FREQUENCY

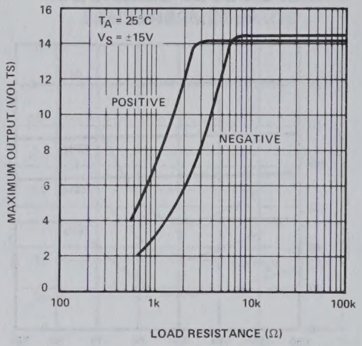


TYPICAL PERFORMANCE CHARACTERISTICS

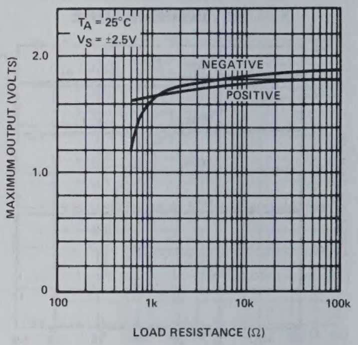
MAXIMUM OUTPUT SWING vs FREQUENCY



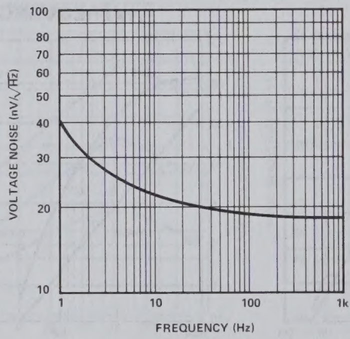
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



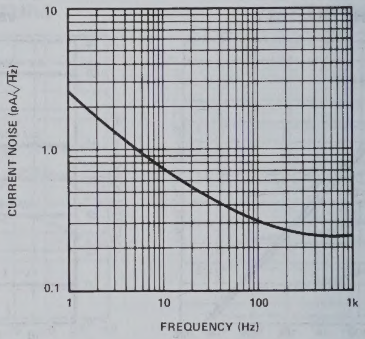
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



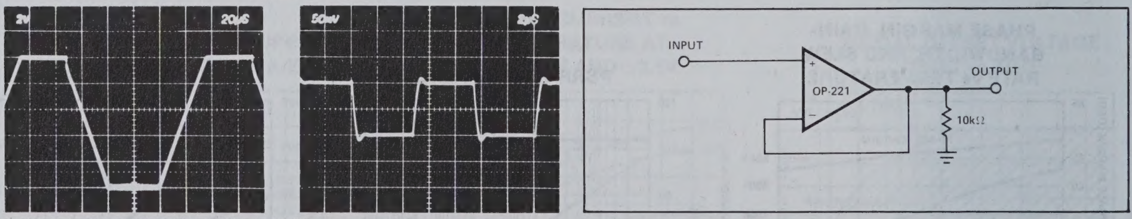
VOLTAGE NOISE DENSITY (e_n) vs FREQUENCY



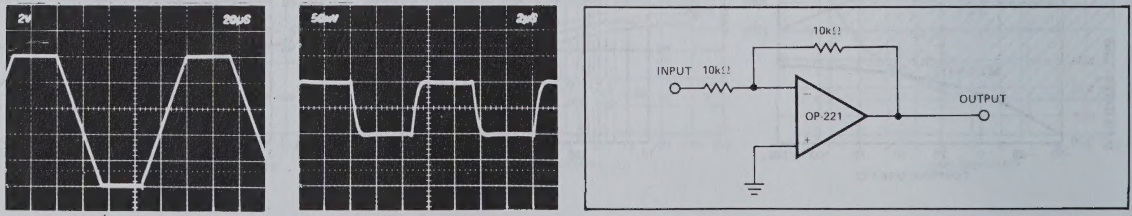
CURRENT NOISE DENSITY (i_n) vs FREQUENCY



NONINVERTING STEP RESPONSE


2V
20μS
50mV
2μS
INPUT
+
−
OP-221
OUTPUT
10kΩ

INVERTING STEP RESPONSE


2V
20μS
50mV
2μS
10kΩ
INPUT
10kΩ
−
+
OP-221
OUTPUT

SPECIAL NOTES ON THE APPLICATION OF DUAL MATCHED OPERATIONAL AMPLIFIERS

ADVANTAGES OF DUAL MONOLITHIC OPERATIONAL AMPLIFIERS

Dual matched operational amplifiers provide the engineer with a powerful tool for designing instrumentation amplifiers and many other differential-input circuits. These designs are based on the principle that careful matching between two operational amplifiers can minimize the effect of DC errors in the individual amplifiers.

Reference to the circuit shown in Figure 1, a differential-in, differential-out amplifier, shows how the reductions in error can be accomplished. Assuming the resistors used are ideally matched, the gain of each side will be identical. If the offset voltages of each amplifier are perfectly matched, then the net differential voltage at the amplifier's output will be zero. Note that the output offset error of this amplifier is not a function of the offset voltage of the individual amplifiers, but only a function of the *difference* (degree of matching) between the amplifiers' offset voltages. This error-cancellation principle holds for a considerable number of input referred error parameters — offset voltage, offset voltage drift, inverting and noninverting bias currents, common-mode and power supply rejection ratios. Note also that the impedances of each input, both common-mode and differential-mode, are high and tightly matched, an important feature not practical with single operational amplifier circuits.

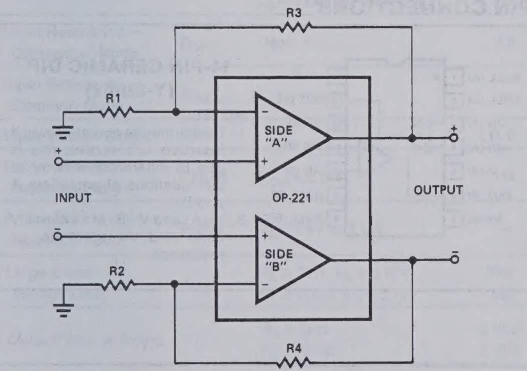


Figure 1

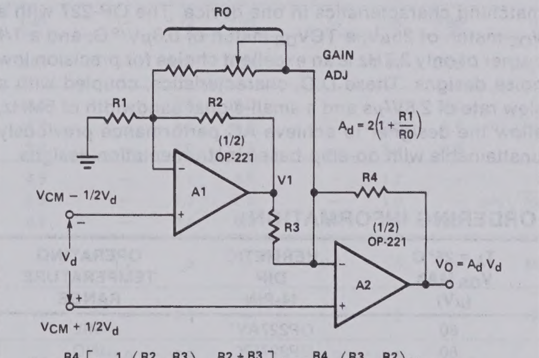
INSTRUMENTATION AMPLIFIER APPLICATIONS

Two-Op-Amp Configuration

The two-op-amp circuit (Figure 2), is recommended where the common-mode input voltage range is relatively limited; the common-mode and differential voltage both appear at V1. The high open-loop gain of the OP-221 is very important in achieving good CMRR in this configuration. Finite open-loop gain of A1 (A_{01}) causes undesired feedthrough of the common-mode input. For $A_d/A_{01} << 1$, the common-mode error (CME) at the output due to this effect is approximately $(2\ A_d/A_{01}) \times V_{CM}$. This circuit features independent adjustment of CMRR and differential gain.

Three-Op-Amp Configuration

The three-op-amp circuit (Figure 3), has increased common-mode voltage range because the common-mode voltage is not amplified as it is in Figure 2. The CMR of this amplifier is directly proportional to the match of the CMR of the input op amps. CMRR can be raised even further by trimming the output stage resistors.

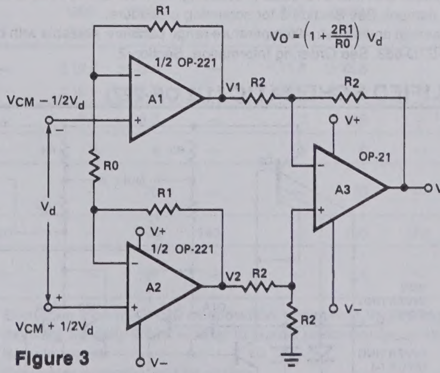


$$A_d = 2\left(1 + \frac{R1}{R0}\right)$$

$$V_O = \frac{R4}{R3}\left[1 + \frac{1}{2}\left(\frac{R2}{R1} + \frac{R3}{R4}\right) + \frac{R2 + R3}{R0}\right] V_d + \frac{R4}{R3}\left(\frac{R3}{R4} - \frac{R2}{R1}\right) V_{CM}$$

Figure 2

IF R1 = R2 = R3 = R4, THEN $V_O = 2\left(1 + \frac{R1}{R0}\right) V_d$



$$V_O = \left(1 + \frac{2R1}{R0}\right) V_d$$

Figure 3

OP-227

DUAL LOW-NOISE LOW-OFFSET INSTRUMENTATION OPERATIONAL AMPLIFIER

FEATURES

- **Excellent Individual Amplifier Parameters**
- **Low V_{OS} 20μV**
- **Offset Voltage Match 25μV**
- **Offset Voltage Match vs. Temperature .... 0.3μV/°C**
- **Stable V_{OS} vs Time 0.2μV/Mo**
- **Low Voltage Noise .... 3nV/$\sqrt{Hz}$**
- **Fast 2.8V/μsec**
- **High Gain .... 1.8 Million**
- **Excellent Gain Match 1.5%**
- **High Channel Separation 154dB**

GENERAL DESCRIPTION

The OP-227 is the first dual amplifier to offer a combination of low offset, low noise, high speed and guaranteed amplifier matching characteristics in one device. The OP-227 with a V_{OS} match of 25μV, a TCV_{OS} match of 0.3μV/°C, and a 1/f corner of only 2.7Hz is an excellent choice for precision low noise designs. These D.C. characteristics, coupled with a slew rate of 2.8V/μs and a small-signal bandwidth of 8MHz, allow the designer to achieve AC performance previously unattainable with op-amp-based instrumentation designs.

When used in a three-op-amp instrumentation amplifier configuration, the OP-227 can achieve a CMRR in excess of 100dB at 10kHz. In addition, this device has an open-loop gain of 1.5M with a 1kΩ load and a gain match of 1.5% between amplifiers. The OP-227 also features an I_B of ±10nA, an I_{OS} of 7nA, and guaranteed matching of input currents between amplifiers. These outstanding input current specifications are realized through the use of a unique input current-cancellation-circuit which typically holds I_B and I_{OS} to ±20nA and 15nA respectively over the full military temperature range.

Other sources of input-referred errors, such as PSRR and CMRR, are reduced by factors in excess of 120dB for the individual amplifiers. D.C. stability is assured by a long-term drift specification of 0.2μV/month.

Matching between channels is provided on all critical parameters including offset voltage, tracking of offset voltage vs. temperature, noninverting bias current, CMRR, and power supply rejection ratio. This unique dual amplifier allows the elimination of external components for offset nulling and frequency compensation.

The OP-227 is pin compatible with the OP-10 and OP-207.

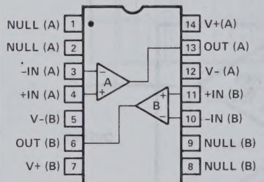
ORDERING INFORMATION†

T_A = 25°C V_{OS} MAX (μV)	HERMETIC DIP 14-PIN	OPERATING TEMPERATURE RANGE
80	OP227AY*	MIL
80	OP227EY	IND
120	OP227BY*	MIL
120	OP227FY	IND
180	OP227CY*	MIL
180	OP227GY	IND

*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

PIN CONNECTIONS

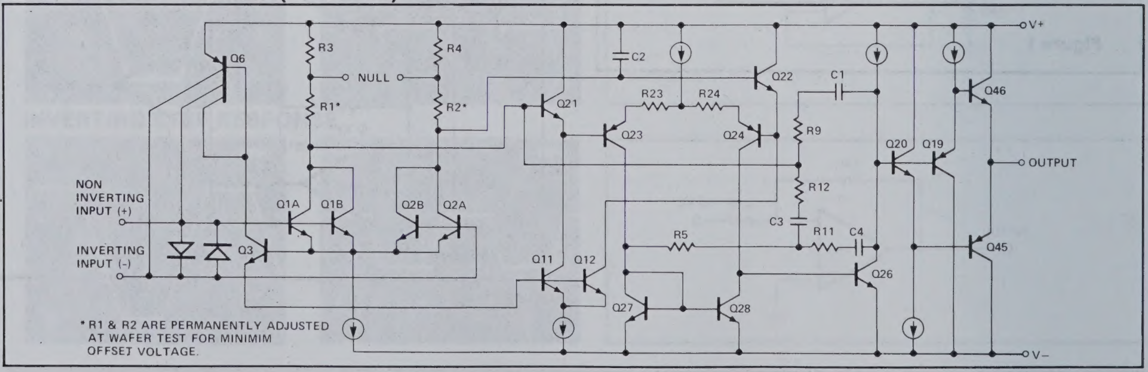


14-PIN CERAMIC DIP (Y-Suffix)

NOTES:

1. Device may be operated even if insertion is reversed; this is due to inherent symmetry of pin locations of amplifiers A and B.
2. V-(A) and V-(B) are internally connected via substrate resistance.

SIMPLIFIED SCHEMATIC (1/2 OP-227)



* R1 & R2 ARE PERMANENTLY ADJUSTED AT WAFER TEST FOR MINIMIM OFFSET VOLTAGE.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	500mW
Input Voltage (Note 3)	±22V
Output Short-Circuit Duration	Indefinite
Differential Input Voltage (Note 2)	±0.7V
Differential Input Current (Note 2)	±25mA
Storage Temperature Range	−65° C to +150° C
Operating Temperature	
OP-227A, OP-227B, OP-227C	−55° C to +125° C
OP-227E, OP-227F, OP-227G	−25° C to +85° C
Lead Temperature Range (Soldering, 60 sec)	300° C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
14-Pin (Y)	106° C	11.3mW/° C

2. The OP-227's inputs are protected by back-to-back diodes, Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.
3. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

INDIVIDUAL AMPLIFIER CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25° C$, unless otherwise noted.

			OP-227A/E			OP-227B/F			OP-227C/G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	20	80	—	40	120	—	60	180	μV
Long Term V_{OS} Stability	V_{OS}/Time	(Notes 2, 4)	—	0.2	1.0	—	0.3	1.5	—	0.4	2.0	μV/Mo
Input Offset Current	I_{OS}		—	7	35	—	9	50	—	12	75	nA
Input Bias Current	I_B		—	±10	±40	—	±12	±55	—	±15	±80	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Notes 3, 5)	—	0.08	0.20	—	0.08	0.20	—	0.09	0.28	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10Hz$ (Note 3) $f_O = 30Hz$ (Note 3) $f_O = 1000Hz$ (Note 3)	— — —	3.5 3.1 3.0	6.0 4.7 3.9	— — —	3.5 3.1 3.0	6.0 4.7 3.9	— — —	3.8 3.3 3.2	9.0 5.9 4.6	$nV/\sqrt{Hz}$
Input Noise Current Density	i_n	$f_O = 10Hz$ (Notes 3, 6) $f_O = 30Hz$ (Notes 3, 6) $f_O = 1000Hz$ (Notes 3, 6)	— — —	1.7 1.0 0.4	4.5 2.5 0.7	— — —	1.7 1.0 0.4	4.5 2.5 0.7	— — —	1.7 1.0 0.4	— — 0.7	$pA/\sqrt{Hz}$
Input Resistance — Differential-Mode	R_{IN}	(Note 4)	1.5	6	—	1.2	5	—	0.8	4	—	MΩ
Input Resistance — Common-Mode	R_{INCM}		—	3	—	—	2.5	—	—	2	—	GΩ
Input Voltage Range	IVR		±11.0	±12.3	—	±11.0	±12.3	—	±11.0	±12.3	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 11V$	114	126	—	106	123	—	100	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4V$ to $\pm 18V$	—	1	10	—	1	10	—	2	20	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$ $R_L \geq 600\Omega$, $V_O = \pm 10V$	1000 800	1800 1500	— —	1000 800	1800 1500	— —	700 600	1500 1500	— —	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$ $R_L \geq 600\Omega$	±12.0 ±10.0	±13.8 ±11.5	— —	±12.0 ±10.0	±13.8 ±11.5	— —	±11.5 ±10.0	±13.5 ±11.5	— —	V
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 4)	1.7	2.8	—	1.7	2.8	—	1.7	2.8	—	V/μs
Gain Bandwidth Prod.	GBW	(Note 4)	5	8	—	5	8	—	5	8	—	MHz
Open-Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	70	—	—	70	—	—	70	—	Ω
Power Consumption	P_d	Each Amplifier	—	90	140	—	90	140	—	100	170	mW
Offset Adjustment Range		$R_P = 10k\Omega$	—	±4	—	—	±4	—	—	±4	—	mV

NOTES:

1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. A/E grade specifications are guaranteed fully warmed up.
2. Long-Term Input Offset Voltage Stability refers to the average trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2.5μV — refer to typical performance curve.
3. Sample tested.
4. Parameter is guaranteed by design.
5. See test circuit and frequency response curve for 0.1Hz to 10Hz tester.
6. See test circuit for current noise measurement.

INDIVIDUAL AMPLIFIER CHARACTERISTICS for $V_S = \pm 15V$, $-55°C \le T_A \le +125°C$, unless otherwise noted.

				OP-227A			OP-227B			OP-227C		
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	60	180	—	80	270	—	110	350	µV
Average Input Offset Drift	TCV_{OS} TCV_{OSn}	(Note 2)	—	0.3	1.0	—	0.4	1.5	—	0.5	1.8	µV/°C
Input Offset Current	I_{OS}		—	15	50	—	22	85	—	30	135	nA
Input Bias Current	I_B		—	±20	±60	—	±28	±95	—	±35	±150	nA
Input Voltage Range	IVR		±10.3	±11.5	—	±10.3	±11.5	—	±10.2	±11.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$	108	122	—	100	119	—	94	116	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	2	16	—	2	20	—	4	51	µV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$, $V_O = \pm 10V$	600	1200	—	500	1000	—	300	800	—	V
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±11.5	±13.5	—	±11.0	±13.2	—	±10.5	±13.0	—	V

INDIVIDUAL AMPLIFIER CHARACTERISTICS for $V_S = \pm 15V$, $-25°C \le T_A \le 85°C$, unless otherwise noted.

				OP-227E			OP-227F			OP-227G		
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	40	140	—	60	200	—	85	280	µV
Average Input Offset Drift	TCV_{OS} TCV_{OSn}	(Note 2)	—	0.5	1.0	—	0.4	1.5	—	0.5	1.8	µV/°C
Input Offset Current	I_{OS}		—	10	50	—	14	85	—	20	135	nA
Input Bias Current	I_B		—	±14	±60	—	±18	±95	—	±25	±150	nA
Input Voltage Range	IVR		±10.5	±11.8	—	±10.5	±11.8	—	±10.5	±11.8	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$	110	124	—	102	121	—	96	118	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	2	15	—	2	16	—	2	32	µV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$, $V_O = \pm 10V$	750	1500	—	700	1300	—	450	1000	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±11.7	±13.6	—	±11.4	±13.5	—	±11.0	±13.3	—	V

NOTES:

1. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. The TCV_{OS} performance is within the specifications unnulled or when nulled with $R_P = 8k\Omega$ to $20k\Omega$, optimum performance is obtained with $R_P = 8k\Omega$.

MATCHING CHARACTERISTICS for $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

				OP-227A/E			OP-227B/F			OP-227C/G		
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage Match	ΔV_{OS}		—	25	80	—	35	150	—	55	300	µV
Average Non-Inverting Bias Current	$I_B{+}$	$I_B{+} = \frac{I_B{+}_A + I_B{+}_B}{2}$	—	±10	±40	—	±12	±55	—	±15	±90	nA
Non-Inverting Offset Current	$I_{OS}{+}$	$I_{OS}{+} = I_B{+}_A - I_B{+}_B$	—	±12	±60	—	±15	±80	—	±20	±130	nA
Inverting Offset Current	$I_{OS}{-}$	$I_{OS}{-} = I_B{-}_A - I_B{-}_B$	—	±12	±60	—	±15	±80	—	±20	±130	nA
Common-Mode Rejection Ratio Match	ΔCMRR	$V_{CM} = \pm 11V$	110	123	—	103	120	—	97	117	—	dB
Power Supply Rejection Ratio Match	ΔPSRR	$V_S = \pm 4V$ to $\pm 18V$	—	2	10	—	2	10	—	2	20	µV/V
Channel Separation	CS	(Note 1)	126	154	—	126	154	—	126	154	—	dB
Gain Match	ΔA_{VO}	$f_O = 100kHz$ (Note 1) $R_L \ge 2k\Omega$, $V_O = \pm 10V$	—	1.5	6.0	—	1.5	6.0	—	2.0	9.0	%

MATCHING CHARACTERISTICS for $V_S = \pm 15V$, $T_A = -55°C$ to $+125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-227A MIN	OP-227A TYP	OP-227A MAX	OP-227B MIN	OP-227B TYP	OP-227B MAX	OP-227C MIN	OP-227C TYP	OP-227C MAX	UNITS
Input Offset Voltage Match	ΔV_{OS}		—	55	180	—	75	300	—	100	480	μV
Input Offset Voltage Tracking	$TC\Delta V_{OS}$	Nulled or Unnulled (Note 2)	—	0.3	1.0	—	0.4	1.5	—	0.5	1.8	μV/°C
Average Non-Inverting Bias Current	I_B^+	$I_B^+ = \frac{I_{B\,A}^{+}+I_{B\,B}^{+}}{2}$	—	±20	±60	—	±28	±95	—	±35	±170	nA
Average Drift of Non-Inverting Bias Current	TCI_B^+		—	100	—	—	160	—	—	200	—	pA/°C
Non-Inverting Offset Current	I_{OS}^+	$I_{OS}^+ = I_{B\,A}^{+}-I_{B\,B}^{+}$	—	±25	±90	—	±35	±140	—	±45	±250	nA
Average Drift of Non-Inverting Offset Current	TCI_{OS}^+		—	130	—	—	200	—	—	250	—	pA/°C
Inverting Offset Current	I_{OS}^-	$I_{OS}^- = I_{B\,A}^{-}-I_{B\,B}^{-}$	—	±25	±90	—	±35	±140	—	±45	±250	nA
Common-Mode Rejection Ratio Match	$\Delta CMRR$	$V_{CM} = \pm 10V$	105	118	—	97	114	—	90	110	—	dB
Power Supply Rejection Ratio Match	$\Delta PSRR$	$V_S = \pm 4.5V$ to $\pm 18V$	—	2	16	—	3	20	—	4	51	μV/V

MATCHING CHARACTERISTICS for $V_S = \pm 15V$, $T_A = -25°C$ to $+85°C$, unless otherwise noted.

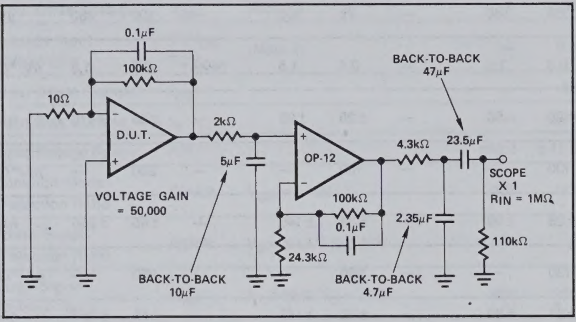
PARAMETER	SYMBOL	CONDITIONS	OP-227E MIN	OP-227E TYP	OP-227E MAX	OP-227F MIN	OP-227F TYP	OP-227F MAX	OP-227G MIN	OP-227G TYP	OP-227G MAX	UNITS
Input Offset Voltage Match	ΔV_{OS}		—	40	140	—	65	210	—	90	400	μV
Input Offset Voltage Tracking	$TC\Delta V_{OS}$	Nulled or Unnulled (Note 1)	—	0.3	1.0	—	0.4	1.5	—	0.5	1.8	μV/°C
Average Non-Inverting Bias Current	I_B^+	$I_B^+ = \frac{I_{B\,A}^{+}+I_{B\,B}^{+}}{2}$	—	±14	±60	—	±18	±95	—	±25	±170	nA
Average Drift of Non-Inverting Bias Current	TCI_B^+		—	80	—	—	140	—	—	180	—	pA/°C
Non-Inverting Offset Current	I_{OS}^+	$I_{OS}^+ = I_{B\,A}^{+}-I_{B\,B}^{+}$	—	±20	±90	—	±25	±140	—	±35	±250	nA
Average Drift of Non-Inverting Offset Current	TCI_{OS}^+		—	130	—	—	200	—	—	250	—	pA/°C
Inverting Offset Current	I_{OS}^-	$I_{OS}^- = I_{B\,A}^{-}-I_{B\,B}^{-}$	—	±20	±90	—	±25	±140	—	±35	±250	nA
Common-Mode Rejection Ratio Match	$\Delta CMRR$	$V_{CM} = \pm 10V$	106	120	—	98	117	—	90	112	—	dB
Power Supply Rejection Ratio Match	$\Delta PSRR$	$V_S = \pm 4.5V$ to $\pm 18V$	—	2	15	—	2	16	—	3	32	μV/V

NOTES:

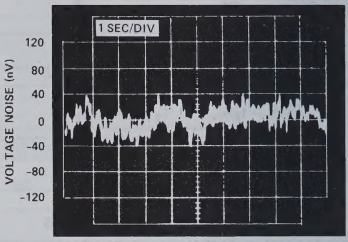
1. Sample tested.
2. Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

VOLTAGE NOISE TEST CIRCUIT (0.1Hz-TO-10Hz$_{p-p}$)


0.1μF
100kΩ
10Ω
D.U.T.
VOLTAGE GAIN = 50,000
2kΩ
5μF
BACK-TO-BACK 10μF
OP-12
100kΩ
0.1μF
24.3kΩ
BACK-TO-BACK 47μF
4.3kΩ
23.5μF
2.35μF
BACK-TO-BACK 4.7μF
SCOPE X 1
RIN = 1MΩ
110kΩ

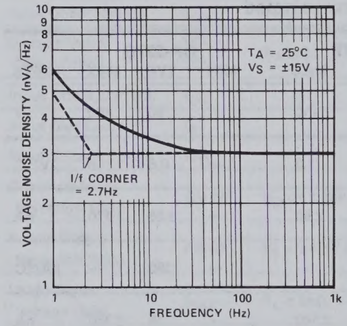
LOW-FREQUENCY NOISE



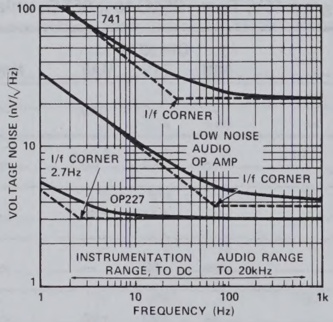
0.1Hz TO 10Hz PEAK-TO-PEAK NOISE

NOTE: OBSERVATION TIME MUST BE LIMITED TO 10 SECONDS TO ENSURE 0.1Hz CUTOFF.

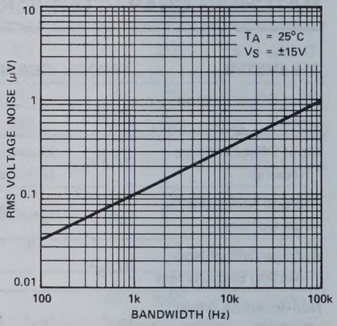
VOLTAGE NOISE DENSITY vs FREQUENCY



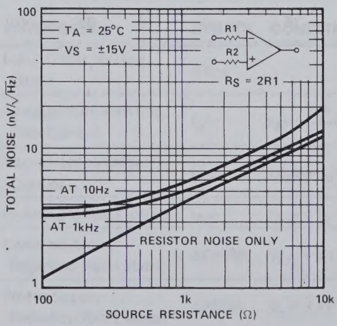
COMPARISON OF OP-AMP VOLTAGE NOISE SPECTRA



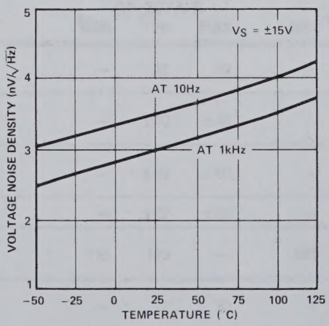
INPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



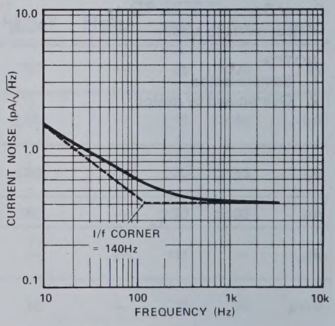
TOTAL NOISE vs SOURCE RESISTANCE



VOLTAGE NOISE DENSITY vs TEMPERATURE

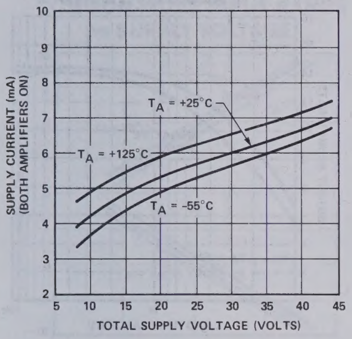


CURRENT NOISE DENSITY vs FREQUENCY

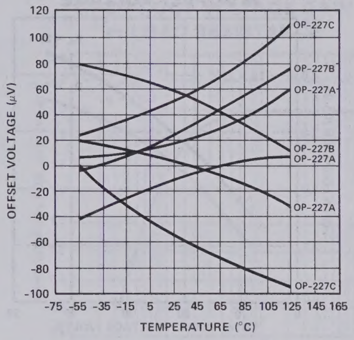


TYPICAL PERFORMANCE CHARACTERISTICS

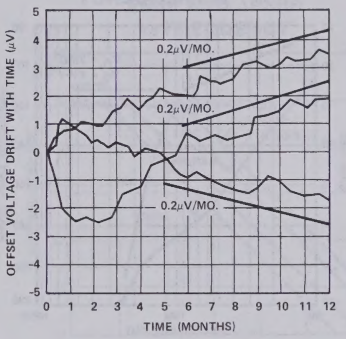
SUPPLY CURRENT vs SUPPLY VOLTAGE



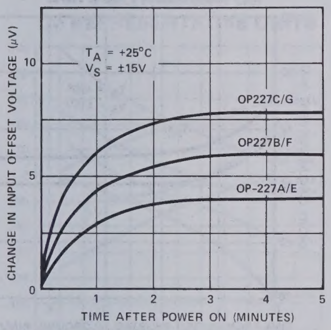
OFFSET VOLTAGE DRIFT OF REPRESENTATIVE UNITS



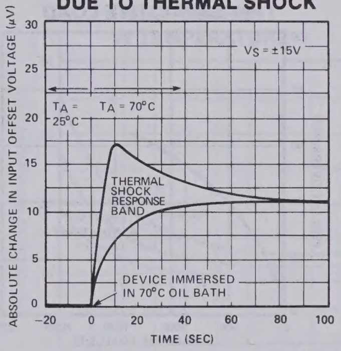
OFFSET VOLTAGE STABILITY WITH TIME



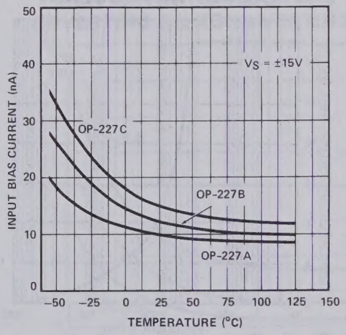
WARM-UP DRIFT



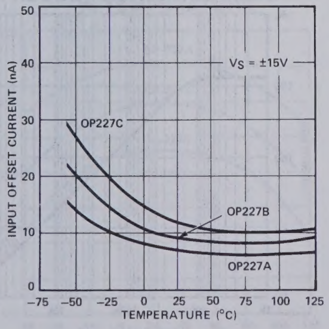
OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



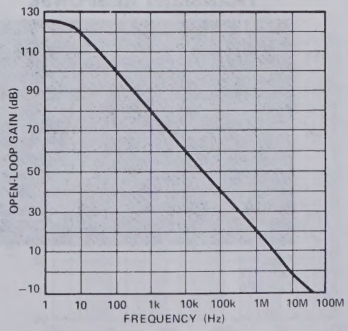
INPUT BIAS CURRENT vs TEMPERATURE



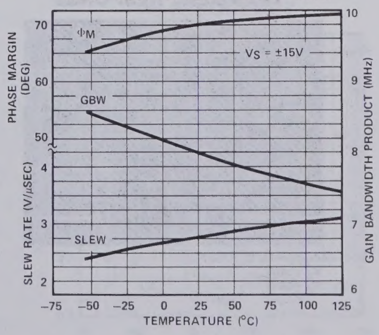
INPUT OFFSET CURRENT vs TEMPERATURE



OPEN-LOOP GAIN vs FREQUENCY

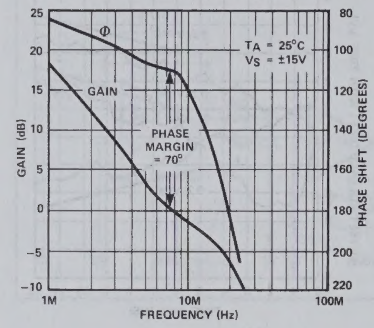


SLEW RATE, GAIN-BANDWIDTH PRODUCT, PHASE MARGIN vs TEMPERATURE

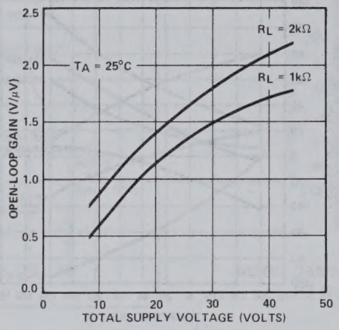


TYPICAL PERFORMANCE CHARACTERISTICS

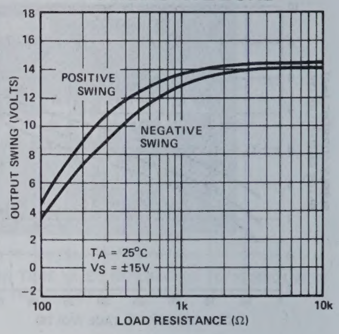
GAIN, PHASE SHIFT vs FREQUENCY



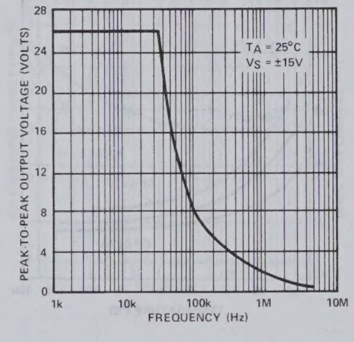
OPEN-LOOP GAIN vs SUPPLY VOLTAGE



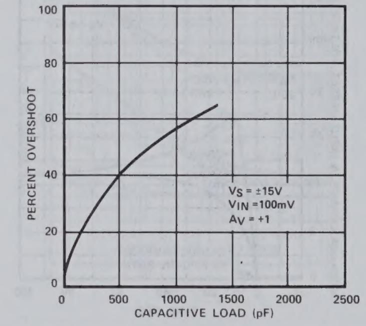
OUTPUT SWING vs RESISTIVE LOAD



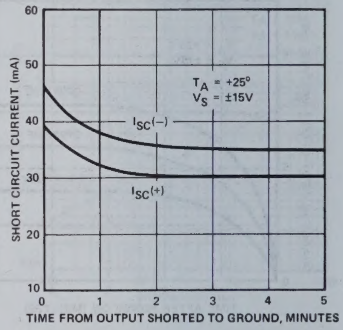
MAXIMUM UNDISTORTED OUTPUT vs FREQUENCY



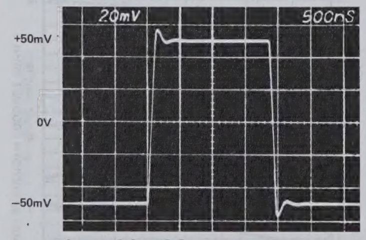
SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD



SHORT-CIRCUIT CURRENT vs TIME

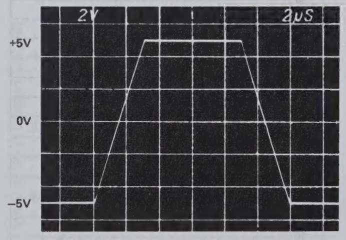


SMALL-SIGNAL TRANSIENT RESPONSE



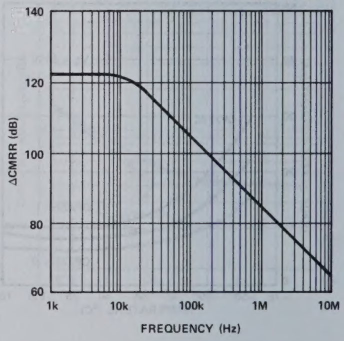
$A_{VCL} = +1$, $C_L = 15pF$
$V_S = \pm 15V$
$T_A = 25°C$

LARGE-SIGNAL TRANSIENT RESPONSE



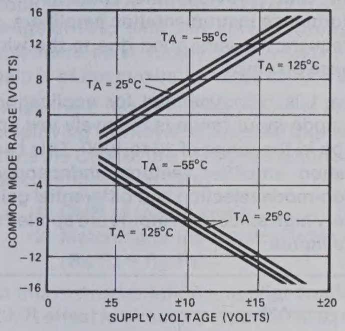
$A_{VCL} = +1$
$V_S = \pm 15V$
$T_A = 25°C$

MATCHING CHARACTERISTIC CMRR MATCH vs FREQUENCY

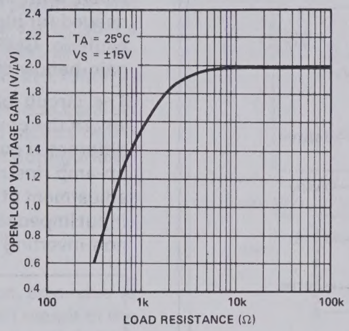


TYPICAL PERFORMANCE CHARACTERISTICS

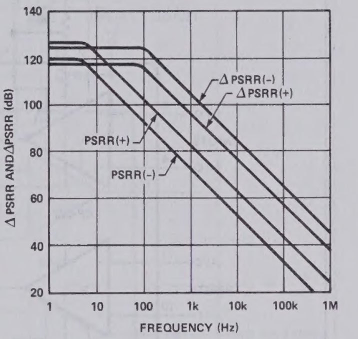
COMMON-MODE INPUT RANGE vs SUPPLY VOLTAGE



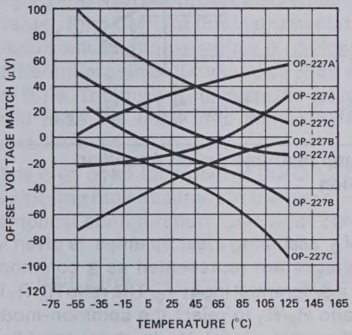
OPEN-LOOP VOLTAGE GAIN vs LOAD RESISTANCE



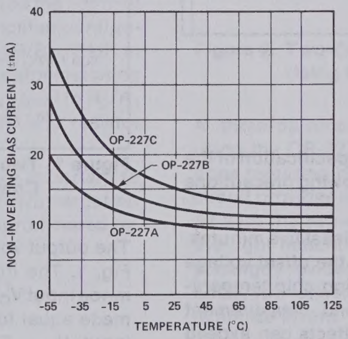
PSRR AND ΔPSRR vs FREQUENCY



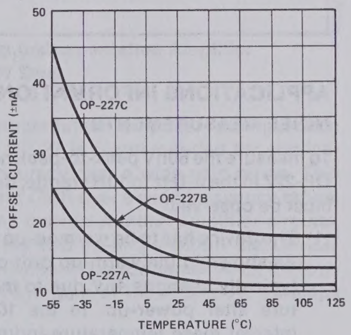
MATCHING CHARACTERISTIC; DRIFT OF OFFSET VOLTAGE MATCH OF REPRESENTATIVE UNITS



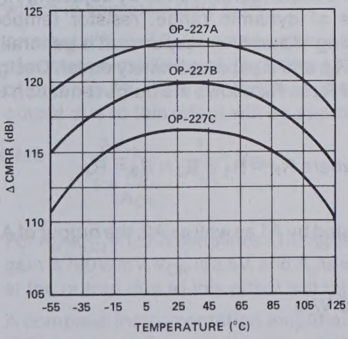
MATCHING CHARACTERISTIC; AVERAGE NONINVERTING BIAS CURRENT vs TEMPERATURE



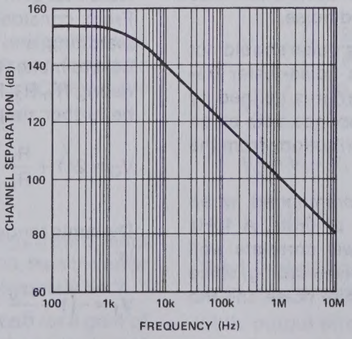
MATCHING CHARACTERISTIC; AVERAGE OFFSET CURRENT vs TEMPERATURE (INVERTING OR NONINVERTING)



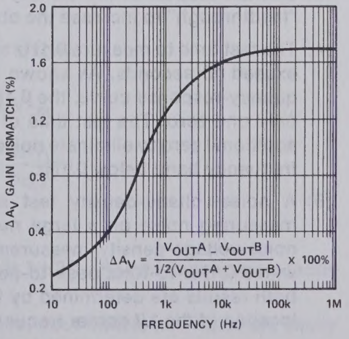
MATCHING CHARACTERISTIC; CMRR MATCH vs TEMPERATURE



CHANNEL SEPARATION vs FREQUENCY

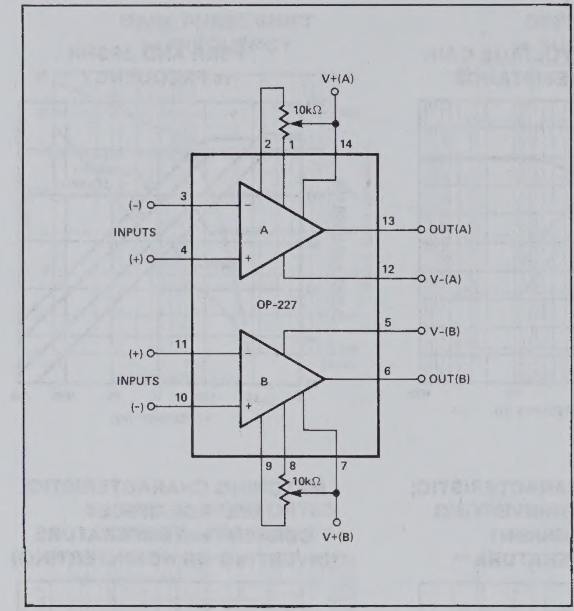


GAIN MISMATCH vs FREQUENCY



BASIC CONNECTIONS

OFFSET NULLING CIRCUIT



APPLICATIONS INFORMATION

NOISE MEASUREMENTS

To measure the 80nV peak-to-peak noise specification of the OP-227 in the 0.1Hz to 10Hz range, the following precautions must be observed:

(1) The device has to be warmed-up for at least five minutes. As shown in the warm-up drift curve, the offset voltage typically changes 4μV due to increasing chip temperature after power-up. In the 10-second measurement interval these temperature-induced effects can exceed tens-of-nanovolts.

(2) For similar reasons, the device has to be well-shielded from air currents. Shielding minimizes thermocouple effects.

(3) Sudden motion in the vicinity of the device can also "feedthrough" to increase the observed noise.

(4) The test time to measure 0.1Hz to 10Hz noise should not exceed 10 seconds. As shown in the noise-tester frequency-response curve, the 0.1Hz corner is defined by only one zero. The test time of 10 seconds acts as an additional zero to eliminate noise contributions from the frequency band below 0.1Hz.

(5) A noise-voltage-density test is recommended when measuring noise on a large number of units. A 10Hz noise-voltage-density measurement will correlate well with a 0.1Hz-to-10Hz peak-to-peak noise reading, since both results are determined by the white noise and the location of the 1/f corner frequency.

INSTRUMENTATION AMPLIFIER APPLICATIONS OF THE OP-227

The excellent input characteristics of the OP-227 make it ideal for use in *instrumentation amplifier* configurations where low-level differential signals are to be amplified. The low-noise, low input offsets, low drift, and high gain combined with excellent CMR provides the characteristics needed for high-performance instrumentation amplifiers. In addition, CMR vs. frequency is very good due to the wide gain-bandwidth of these op amps.

The circuit of Figure 1 is recommended for applications where the common-mode input range is relatively low and differential gain will be in the range of 10 to 1000. This two-op-amp instrumentation amplifier features *independent* adjustment of common-mode rejection and differential gain. Input impedance is very high since both inputs are applied to non-inverting op amp inputs.

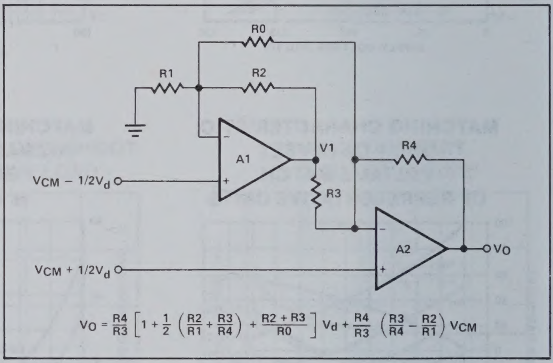

R0
R1
R2
A1
V1
R4
R3
A2
VO
VCM − 1/2Vd
VCM + 1/2Vd
VO = R4/R3 [1 + 1/2 (R2/R1 + R3/R4) + (R2 + R3)/R0] Vd + R4/R3 (R3/R4 − R2/R1) VCM

Figure 1. Two-Op-Amp Instrumentation Amplifier Configuration

The output voltage V_O, assuming ideal op amps, is given in Fig. 1. The input voltages are represented as a common-mode input V_{CM} plus a differential input V_d. The ratio R_3/R_4 is made equal to the ratio R_2/R_1 to reject the common-mode input V_{CM}. The differential signal V_d is then amplified according to:

$$V_O = \frac{R_4}{R_3}\left(1 + \frac{R_3}{R_4} + \frac{R_2 + R_3}{R_O}\right) V_d, \text{ where } \frac{R_3}{R_4} = \frac{R_2}{R_1}$$

Note that gain can be independently varied by adjusting R_O. From considerations of dynamic range, resistor tempco matching, and matching of amplifier response, it is generally best to make R_1, R_2, R_3, and R_4 approximately equal. Designating R_1, R_2, R_3, and R_4 as R_N allows the output equation to be further simplified:

$$V_O = 2\left(1 + \frac{R_N}{R_O}\right) V_d, \text{ where } R_N = R_1 = R_2 = R_3 = R_4$$

Dynamic range is limited by A1 as well as A2; the output of A1 is:

$$V_1 = -\left(1 + \frac{R_N}{R_O}\right) V_d + 2\,V_{CM}$$

If the instrumentation amplifier were designed for a gain of 10 and maximum V_d of ±1V, then R_N/R_O would need to be four and V_O would be a maximum of ±10V. Amplifier A1 would have a maximum output of ±5V plus $2V_{CM}$, thus a limit of ±10V on the output of A1 would imply a limit of ±2.5V on V_{CM}. A nominal value of 10kΩ for R_N is suitable for most applications. A range of 20Ω to 2.5kΩ for R_O will then provide a gain range of 10 to 1000. The current through R_O is V_d/R_O, so the amplifiers must supply ±10mV/20Ω (or ±0.5mA) when the gain is at the maximum value of 1000 and V_d is at ±10mV.

Rejecting common-mode inputs is important in accurately amplifying low-level differential signals. Two factors determine the CMR in this instrumentation amplifier configuration (assuming infinite gain):

(1) CMR of the op amps
(2) Matching of the resistor network ratios
($R_3/R_4 = R_2/R_1$)

In this instrumentation amplifier configuration, error due to CMR effect is directly proportional to the CMR match of the op amps. For the OP-227 this ΔCMR is a minimum of 97dB for the "G" and 110dB for the "E" grade. A ΔCMR value of 100dB and common-mode input range of ±2.5V indicates a peak input-referred error of only ±25μV. Resistor matching is the other factor affecting CMR. Defining A_d as the differential gain of the instrumentation amplifier and assuming that R_1, R_2, R_3 and R_4 are approximately equal (R_N will be the nominal value), then CMR for this instrumentation amplifier configuration will be approximately A_d divided by $4\Delta R/R_N$. CMR at differential gain of 100 would be 88dB with resistor matching of 0.1%. Trimming R_1 to make the ratio R_3/R_4 equal to R_2/R_1 will raise the CMR until limited by linearity and resistor stability considerations.

The high open-loop gain of the OP-227 is very important to achieving high accuracy in the two op-amp instrumentation amplifier configuration. Gain error can be approximated by

$$\text{Gain Error} \sim \frac{1}{1+\dfrac{A_d}{A_{O2}}}\quad , \qquad \frac{A_d}{2\,A_{O1}\,A_{O2}} \ll 1$$

where A_d is the instrumentation amplifier differential gain and A_{O2} is the open-loop gain of op amp A2. This analysis assumes equal values of R_1, R_2, R_3, and R_4. For example, consider an OP-227 with A_{02} of 700V/mV. If the differential gain A_d were set to 700, then the gain error would be 1/1.001 which is approximately 0.1%.

Another effect of finite op amp gain is undesired feedthrough of common-mode input. Defining A_{01} as the open-loop gain of op amp A1, then the common-mode error (CME) at the output due to this effect will be approximately

$$\text{CME} \sim \frac{2\,A_d}{1+\dfrac{A_d}{A_{O1}}}\;\frac{1}{A_{O1}}\;V_{CM}$$

For $A_d/A_{O1} \ll 1$, this simplifies to $(2\,A_d/A_{O1}) \times V_{CM}$. If the op amp gain is 700V/mV, V_{CM} is 2.5V, and A_d is set to 700, then the error at the output due to this effect will be approximately 5mV.

A complete instrumentation amplifier designed for a gain of 100 is shown in Figure 2. It has provision for trimming of input offset voltage, CMR, and gain. Performance is excellent due to the high gain, high CMR, and low noise of the individual amplifiers combined with the tight matching characteristics of the OP-227 dual.

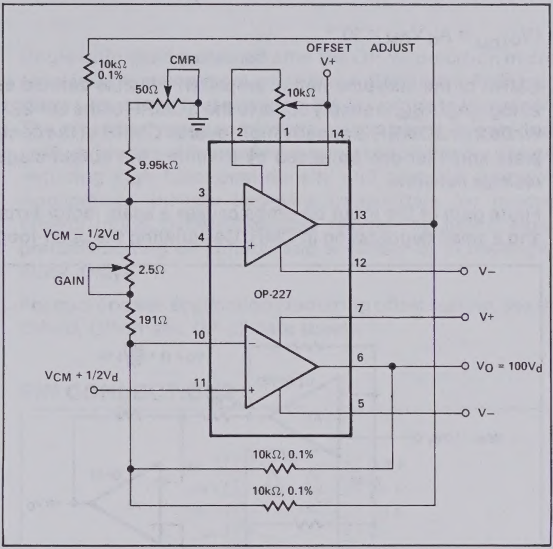


Figure 2. Two-Op-Amp Instrumentation Amplifier Using OP-227 Dual

A three-op-amp instrumentation amplifier configuration using the OP-227 and OP-27 is recommended for applications requiring high accuracy over a wide gain range. This circuit provides excellent CMR over a wide frequency range. As with the two-op-amp instrumentation amplifier circuits, the tight matching of the two op-amps within the OP-227 package provides a real boost in performance. Also, the low-noise, low offset, and high gain of the individual op-amps minimize errors.

A simplified schematic is shown in Figure 3. The input stage (A1 and A2) serves to amplify the differential input V_d without amplifying the common-mode voltage V_{CM}. The output stage then rejects the common-mode input. With ideal op-amps and no resistor matching errors, then the outputs of each amplifier will be:

$$V_1 = -\left(1+\frac{2R_1}{R_O}\right)\frac{V_d}{2} + V_{CM}$$

$$V_2 = \left(1+\frac{2R_1}{R_O}\right)\frac{V_d}{2} + V_{CM}$$

$$V_O = V_2 - V_1 = \left(1+\frac{2R_1}{R_O}\right)V_d$$

$$V_O = A_d\,V_d$$

The differential gain A_d is $1 + 2R_1/R_O$ and the common-mode input V_{CM} is rejected.

While output error due to input offsets and noise are easily determined, the effects of finite gain and common-mode rejection are more subtle. CMR of the complete instrumentation amplifier is directly proportioned to the *match* in CMR of the input op-amps. This match varies from 97dB to 110dB minimum for the OP-227. Using 100dB, then the output response to a common-mode input V_{CM} would be:

$$[V_O]_{CM} = A_d V_{CM} \times 10^{-5}$$

CMRR of the instrumentation amplifier, which is defined as $20 \log_{10} A_d/A_{CM}$, is simply equal to the ΔCMRR of the OP-227. While this ΔCMRR is already high, overall CMRR of the complete amplifier can be raised by trimming the output stage resistor network.

Finite gain of the input op-amps causes a scale factor error and a small degradation in CMR. Designating the open-loop gain of op-amp A_1 as A_{O1}, and op-amp A_2 as A_{O2}, then the following equation approximates the output:

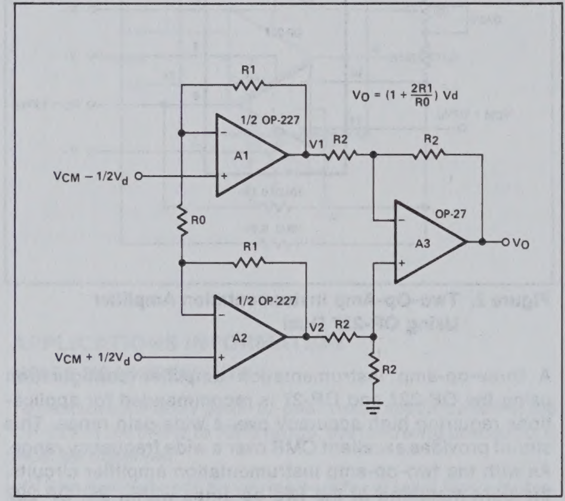


Figure 3. Three-Op-Amp Instrumentation Amplifier Using OP-227 and OP-27

$$V_O \sim \frac{1}{1 + \frac{R_1}{R_O}\left(\frac{1}{A_{O1}} + \frac{1}{A_{O2}}\right)} \left[A_d V_d + \frac{2R_1}{R_O}\left(\frac{1}{A_{O1}} - \frac{1}{A_{O2}}\right) V_{CM} \right]$$

This can be simplified by defining A_O as the nominal open-loop gain and ΔA_O as the differential open-loop gain. Then

$$V_O \sim \frac{1}{1 + \frac{2R_1}{R_O}\frac{1}{A_O}} \left[A_d V_d + \frac{2R_1 \Delta A_O}{R_O A_O^2} V_{CM} \right]$$

The high open-loop gain of each amplifier within the OP-227 (700,000 minimum at 25° C into $R_L \geq 2k$) assures good gain accuracy even at high values of A_d. The effect of finite open-loop gain on CMR can be approximated by:

$$\mathrm{CMRR} \sim \frac{A_O^2}{\Delta A_O}$$

If $\Delta A_O/A_O$ were 6% and A_O were 600,000, then the CMRR due to finite gain of the input op-amps would be approximately 140dB.

The unity-gain output stage contributes negligible error to the overall amplifier. However, matching of the four-resistor R_2–network is critical to achieving high CMR. Consider a worst-case situation where each R_2 resistor has an error of $\pm\Delta R_2$. If the resistor ratio is high on one side and low on the other, then the common-mode gain will be $2\Delta R_2/R_2$. Since the output stage gain is unity, CMRR will then be $R_2/2\Delta R_2$. It is common practice to trim the R_2 resistor connected to ground to maximize overall CMRR for the total instrumentation amplifier circuit.

This three-op-amp instrumentation amplifier configuration provides excellent performance over a wide gain range. A gain range of 1 to 2000 is practical and CMR of over 120dB is achievable.

QUAD MICROPOWER OPERATIONAL AMPLIFIER

OP-420

FEATURES

- **Low Supply Current** .... **200μA Max @ $V_S = +5V$**
- **Single-Supply Operation** .... **+5V to +30V**
- **Dual-Supply Operation** .... **±2.5V to ±15V**
- **Low Input Offset Voltage** .... **500μV Typ**
- **Low Input Offset Voltage Drift** .... **5μV/°C Typ**
- **High Common-Mode Input Range** ... **V− to (V+ − 1.5V)**
- **High CMRR** .... **100dB Typ**
- **High Open-Loop Gain** .... **1100V/mV Typ**
- **LM 148 Pinout**

GENERAL DESCRIPTION

The OP-420 quad micropower operational amplifier is a single-chip quad patterned after the OP-20 precision micropower single operational amplifier. A Darlington PNP input stage allows the input common-mode voltage to include V−. The wide input range combined with low power-supply drain (~40μA/section at 5V), provides a unique solution for designs requiring high functional density and portable operation. Applications include two-wire transmitters for process control loops, battery-operated remote-line filters, signal preconditioning amplifiers, and a variety of multiple-gain block arrays.

For micropower applications requiring offset nulling, see the OP-20, OP-21 and OP-22 data sheets.

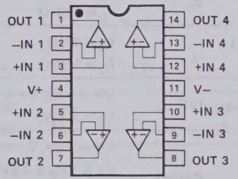
ORDERING INFORMATION†

$T_A = 25°C$ V_{OS} MAX (mV)	HERMETIC DIP 14-PIN	OPERATING TEMPERATURE RANGE
2.5	OP420BY*	MIL
2.5	OP420FY	IND
4.0	OP420CY*	MIL
4.0	OP420GY	IND
6.0	OP420HY	COM

*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

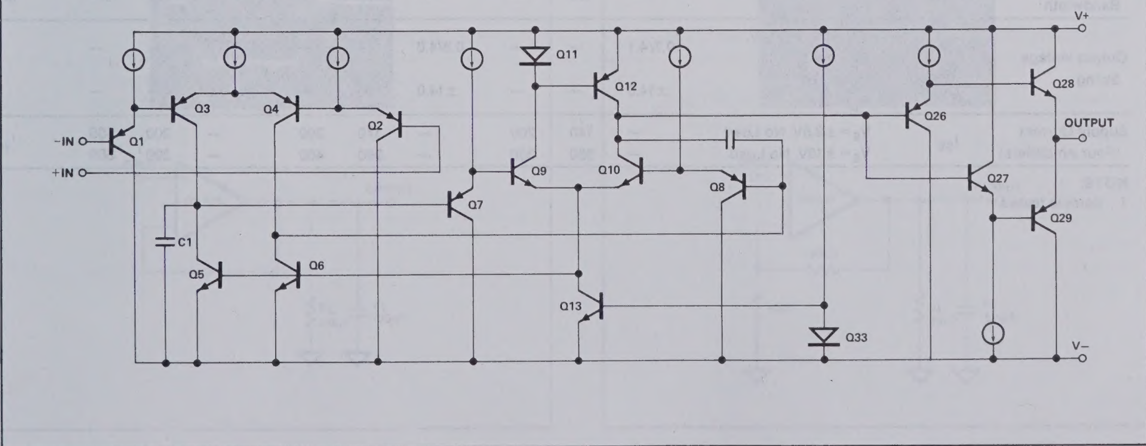
†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

PIN CONNECTIONS



14-PIN HERMETIC DIP
(Y-Suffix)

SIMPLIFIED SCHEMATIC (1/4 Shown)



ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage .... ±18V
Internal Power Dissipation (Note 1) 500mW
Differential Input Voltage .... ±30V
Input Voltage .... Supply Voltage
Output Short-Circuit Duration .... Continuous
(One Amplifier Only)
Storage Temperature Range .... −65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) ...... 300°C
Operating Temperature Range
OP-420BY, OP-420CY .... −55°C to +125°C
OP-420FY, OP-420GY .... −25°C to +85°C
OP-420HY .... 0°C to +70°C
DICE Junction Temperature (T_j) .... −65°C to +150°C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
14-Pin Hermetic DIP (Y)	100°C	10.0mW/°C

2. Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $T_A = +25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-420B OP-420F MIN	TYP	MAX	OP-420C OP-420G MIN	TYP	MAX	OP-420H MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$V_S = \pm2.5V$ to $\pm15V$	—	0.5	2.5	—	1	4	—	2	6	mV
Input Offset Current	I_{OS}	$V_S = \pm2.5V$ to $\pm15V$	—	0.5	1.5	—	0.8	2.5	—	1.2	6	nA
Input Bias Current	I_B	$V_S = \pm2.5V$ to $\pm15V$	—	9	20	—	12	30	—	18	40	nA
Input Noise Voltage Density	e_n	$f_O = 10Hz$ $f_O = 100Hz$	—	50	—	—	50	—	—	50	—	$nV/\sqrt{Hz}$
Input Noise Current Density	i_n	$f_O = 10Hz$ $f_O = 100Hz$	—	0.12	—	—	0.12	—	—	0.12	—	$pA/\sqrt{Hz}$
Input Voltage Range	IVR	$V+ = +5V$, $V- = 0V$ $V_S = \pm15V$	0/3.5 −15/13.5	— —	— —	0/3.5 −15/13.5	— —	— —	0/3.5 −15/13.5	— —	— —	V
Common-Mode Rejection Ratio	CMRR	$V+ = +5V$, $V- = 0V$ $0V \leq V_{CM} \leq 3.5V$ $V_S = \pm15V$ $-15V \leq V_{CM} \leq 13.5V$	83 83	100 100	— —	80 80	96 96	— —	76 76	90 90	— —	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm2.5V$ to $\pm15V$; & $V- = 0V$, $V+ = 5V$ to $30V$	—	10	30	—	20	50	—	30	80	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L = 25k\Omega$, $V_O = 10V$	600	1100	—	400	900	—	200	800	—	V/mV
Slew Rate	SR		—	0.05	—	—	0.05	—	—	0.05	—	$V/\mu s$
Closed-Loop Bandwidth	BW	$A_{VCL} = +1.0$ $R_L = 10k\Omega$	—	150	—	—	150	—	—	150	—	kHz
Output Voltage Swing	V_O	$V+ = 5V$, $V- = 0V$, $R_L = 10k\Omega$ $V_S = \pm15V$, $R_L = 25k\Omega$	0.7/4.1 ±14.0	— —	— —	0.8/4.0 ±14.0	— —	— —	0.9/3.8 ±13.8	— —	— —	V
Supply Current (Four Amplifiers)	I_{SY}	$V_S = \pm2.5V$, No Load $V_S = \pm15V$, No Load	— —	140 330	200 360	— —	170 360	300 460	— —	200 390	400 600	μA

NOTE:

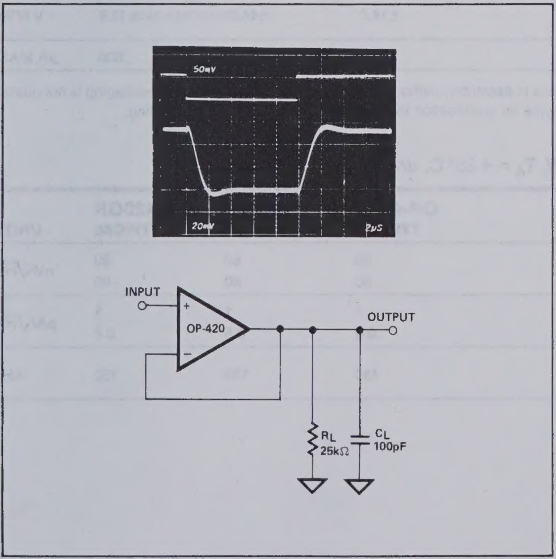
1. Sample tested.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \le T_A \le +125°C$ for OP-420B and OP-420C, $-25°C \le T_A \le +85°C$ for OP-420F and OP-420G, and $0°C \le T_A \le +70°C$ for OP-420H, unless otherwise noted.

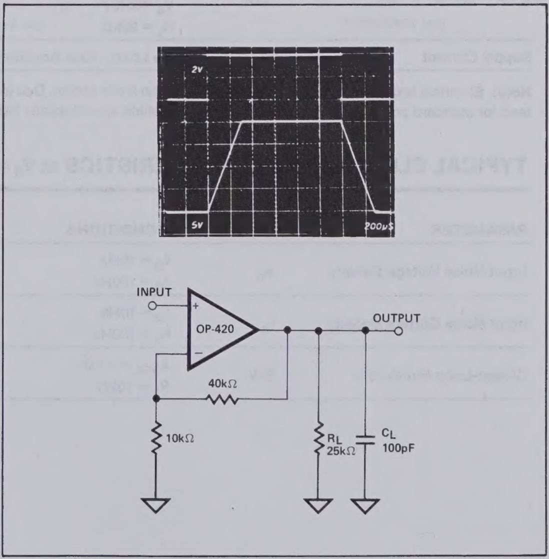
			OP-420B OP-420F			OP-420C OP-420G			OP-420H			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	Unnulled	—	5	10	—	8	15	—	15	25	µV/°C
Input Offset Voltage	V_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	—	—	3.5	—	—	5.5	—	—	7.5	mV
Input Offset Current	I_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	—	—	3	—	—	4	—	—	8	nA
Input Bias Current	I_B	$V_S = \pm 2.5V$ to $\pm 15V$	—	—	30	—	—	40	—	—	60	nA
Input Voltage Range	IVR	$V+ = +5V$, $V- = 0V$	0/3.2	—	—	0/3.2	—	—	0/3.2	—	—	V
		$V_S = \pm 15V$	−15/13.2	—	—	−15/13.2	—	—	−15/13.2	—	—	
Common-Mode Rejection Ratio	CMRR	$V+ = +5V$, $V- = 0V$, $0V \le V_{CM} \le 3.2V$	76	96	—	73	92	—	73	86	—	dB
		$V_S = \pm 15V$, $-15V \le V_{CM} \le 13.2V$	76	96	—	73	92	—	73	86	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$ and $V- = 0V$, $V+ = 5V$ to 30V	—	15	50	—	25	80	—	40	100	µV/V
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $R_L = 50k\Omega$, $V_O = 10V$	300	800	—	200	650	—	100	400	—	V/mV
Output Voltage Swing	V_O	$V+ = 5V$, $V- = 0V$, $R_L = 20k\Omega$	0.9/3.9	—	—	1.0/3.8	—	—	1.1/3.6	—	—	V
		$V_S = \pm 15V$, $R_L = 50k\Omega$	±13.8	—	—	±13.8	—	—	±13.6	—	—	
Supply Current (Four Amplifiers)	I_{SY}	$V_S = \pm 2.5V$, No Load	—	170	300	—	210	400	—	250	600	µA
		$V_S = \pm 15V$, No Load	—	390	500	—	420	640	—	500	800	

NOTE:
1. Sample tested.

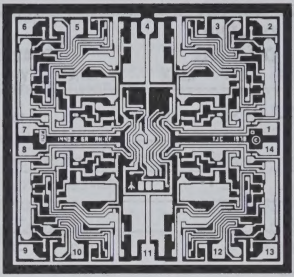
SMALL-SIGNAL TRANSIENT RESPONSE



LARGE-SIGNAL TRANSIENT RESPONSE



DICE CHARACTERISTICS



1. OUTPUT 1
2. INVERTING INPUT 1
3. NONINVERTING INPUT 1
4. V+
5. NONINVERTING INPUT 2
6. INVERTING INPUT 2
7. OUTPUT 2
8. OUTPUT 3
9. INVERTING INPUT 3
10. NONINVERTING INPUT 3
11. V−
12. NONINVERTING INPUT 4
13. INVERTING INPUT 4
14. OUTPUT 4

DIE SIZE 0.092 × 0.086 inch, 7912 sq. mils (2.34 × 2.18 mm, 5.10 sq. mm)

For additional DICE information refer to Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-420N LIMIT	OP-420G LIMIT	OP-420GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	2.5	4	6	mV MAX
Input Offset Current	I_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	1.5	2.5	6	nA MAX
Input Bias Current	I_B	$V_S = \pm 2.5V$ to $\pm 15V$	20	30	40	nA MAX
Input Voltage Range	IVR		−15/13.5	−15/13.5	−15/13.5	V MIN
Common-Mode Rejection Ratio	CMRR	$V+ = +5V$, $V- = 0V$ $0V \leq V_{CM} \leq 3.5V$	83	80	76	dB MIN
		$V_S = \pm 15V$, $-15V \leq V_{CM} \leq 13.5V$	83	80	76	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$ $V- = 0V$, $V+ = +5V$ to $+30V$	30	50	80	μV/V MAX
Large-Signal Voltage Gain	A_{VO}	$R_L = 25k\Omega$, $V_O = \pm 10V$	600	400	200	V/mV MIN
Output Voltage Swing	V_O	$V+ = +5V$, $V- = 0V$ $R_L = 10k\Omega$	0.7/4.1	0.8/4.0	0.9/3.8	VMAX
		$V_S = \pm 15V$ $R_L = 25k\Omega$	±14.0	±14.0	±13.8	V MIN
Supply Current	I_{SY}	No Load, (Four Amplifiers)	360	460	600	μA MAX

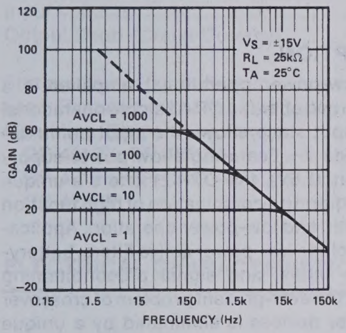
Note: Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

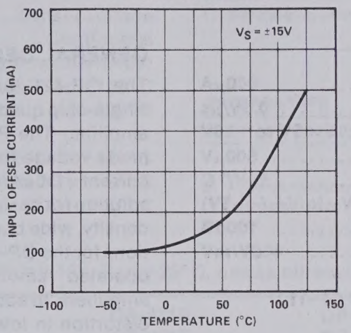
PARAMETER	SYMBOL	CONDITIONS	OP-420N TYPICAL	OP-420G TYPICAL	OP-420GR TYPICAL	UNITS
Input Noise Voltage Density	e_n	$f_O = 10Hz$	80	80	80	$nV/\sqrt{Hz}$
		$f_O = 100Hz$	60	60	60	
Input Noise Current Density	i_n	$f_O = 10Hz$	1	1	1	$pA/\sqrt{Hz}$
		$f_O = 100Hz$	0.8	0.8	0.8	
Closed-Loop Bandwidth	BW	$A_{VCL} = +1.0$ $R_L = 10k\Omega$	150	150	150	kHz

TYPICAL PERFORMANCE CHARACTERISTICS

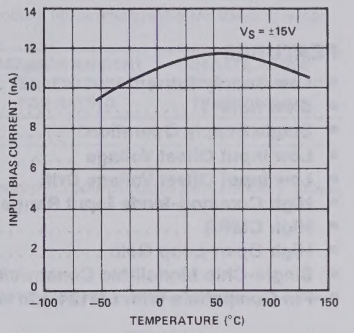
CLOSED-LOOP GAIN vs FREQUENCY



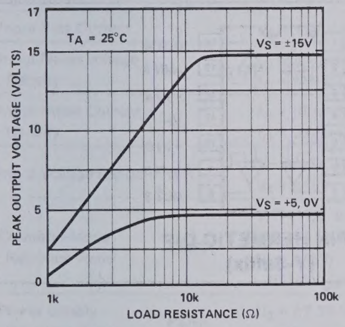
INPUT OFFSET CURRENT vs TEMPERATURE



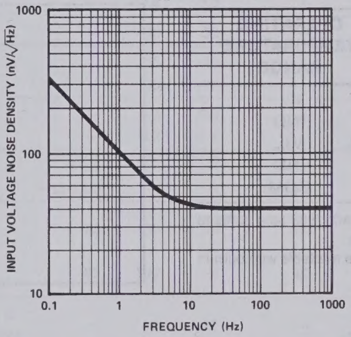
INPUT BIAS CURRENT vs TEMPERATURE



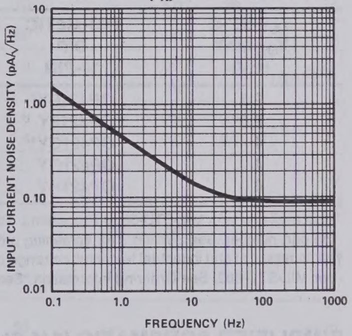
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



INPUT VOLTAGE NOISE DENSITY (e_n) vs FREQUENCY



INPUT CURRENT NOISE DENSITY (i_n) vs FREQUENCY



OP-421

QUAD LOW-POWER OPERATIONAL AMPLIFIER

FEATURES

- **Low Supply Current 600μA**
- **Slew Rate 0.5V/μs**
- **Single Supply Operation .... +5V to +30V**
- **Low Input Offset Voltage 500μV**
- **Low Input Offset Voltage Drift .... 5μV/°C**
- **High Common-Mode Input Range ... V− to V+ (−1.5V)**
- **High CMRR 100dB**
- **High Open-Loop Gain 400V/mV**
- **Single-Chip Monolithic Construction**
- **Pin Compatible With LM124, LM148, and OP-11**

GENERAL DESCRIPTION

The OP-421 quad low-power operational amplifier is a single-chip quad patterned after the OP-21 single operational amplifier. The PNP input stage allows the input common-mode voltage to include V−. Featuring a low power-supply current (150μA/section at 5V), the OP-421 offers a unique solution for designs requiring a combination of high function density, wide bandwidth, and low-power operation. Applications for the OP-421 include low-power active filters, battery-operated remote line filters, and signal preconditioning amplifiers. In addition, the ever-present problem of crossover distortion in low-power devices is eliminated by a unique double-buffered output section.

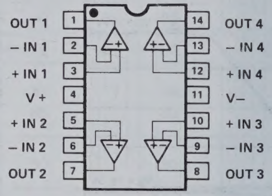
ORDERING INFORMATION†

T_A = 25°C V_{OS} MAX (mV)	HERMETIC DIP 14-PIN	OPERATING TEMPERATURE RANGE
2.5	OP421BY*	MIL
2.5	OP421FY	IND
4	OP421CY*	MIL
4	OP421GY	IND
6	OP421HY	COM

*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

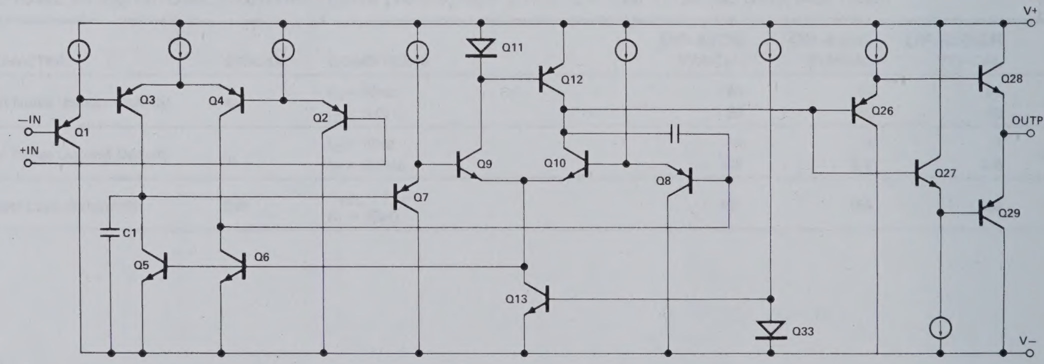
†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

PIN CONNECTIONS



14-PIN HERMETIC DIP
(Y-Suffix)

SIMPLIFIED SCHEMATIC (1/4 Shown)



ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage .... ±18V
Internal Power Dissipation (Note 1) 500mW
Differential Input Voltage .... ±30V
Input Voltage .... Supply Voltage
Output Short-Circuit Duration .... Continuous
(One Amplifier Only)
Storage Temperature Range .... −65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
Operating Temperature Range
OP-421BY, OP-421CY .... −55°C to +125°C
OP-421FY, OP-421GY .... −25°C to +85°C
OP-421HY .... 0°C to +70°C
DICE Junction Temperature (T_j) .... −65°C to +150°C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
14-Pin Hermetic DIP (Y)	100°C	10.0mW/°C

2. Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

			OP-421B OP-421F			OP-421C OP-421G			OP-421H			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	—	0.5	2.5	—	1	4	—	2	6	mV
Input Offset Current	I_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	—	0.6	5.0	—	2.0	10	—	5.0	20	nA
Input Bias Current	I_B	$V_S = \pm 2.5V$ to $\pm 15V$	—	20	50	—	50	80	—	100	150	nA
Input Noise Voltage Density	e_n	f_O = 10Hz (Note 1)	—	20	40	—	20	40	—	20	40	$nV/\sqrt{Hz}$
		f_O = 100Hz (Note 1)	—	15	30	—	15	30	—	15	30	
Input Noise Current Density	i_n	f_O = 10Hz (Note 1)	—	0.3	0.6	—	0.3	0.6	—	0.3	0.6	$pA/\sqrt{Hz}$
		f_O = 100Hz (Note 1)	—	0.2	0.4	—	0.2	0.4	—	0.2	0.4	
Input Voltage Range	IVR	V+ = +5V, V− = 0V	0/3.5	—	—	0/3.5	—	—	0/3.5	—	—	V
		$V_S = \pm 15V$	−15/13.5	—	—	−15/13.5	—	—	−15/13.5	—	—	
Common-Mode Rejection Ratio	CMRR	V+ = +5V, V− = 0V, $0V \le V_{CM} \le +3.5V$	83	100	—	80	96	—	76	90	—	dB
		$V_S = \pm 15V$, $-15V \le V_{CM} \le +13.5V$	83	100	—	80	96	—	76	90	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$; & V− = 0V, V+ = 5V to 30V	—	10	30	—	20	50	—	30	80	µV/V
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$ $R_L = 10k\Omega$	200	400	—	100	200	—	100	200	—	V/mV
Output Voltage Swing	V_O	V+ = 5V, V− = 0V $R_L = 5k\Omega$	0.7/4.0	—	—	0.8/3.9	—	—	0.9/3.8	—	—	V
		$V_S = \pm 15V$, $R_L = 10k\Omega$	±14	—	—	±13.9	—	—	±13.8	—	—	
Closed-Loop Bandwidth (Note 2)	BW	$A_{VCL} = +1.0$, $R_L = 10k\Omega$	1.0	1.9	—	1.0	1.9	—	1.0	1.9	—	MHz
Supply Current (Four Amplifiers)	I_{SY}	$V_S = \pm 2.5V$, No Load	—	0.6	1.0	—	0.7	1.5	—	0.9	2.0	mA
		$V_S = \pm 15V$, No Load	—	1.2	1.8	—	1.4	2.3	—	1.8	3.0	
Slew Rate	SR	(Note 1)	0.25	0.5	—	0.25	0.5	—	0.25	0.5	—	V/µs
Channel Separation	CS	(Note 1)	100	120	—	100	120	—	100	120	—	dB

NOTES:

1. Sample tested.
2. Guaranteed by design.

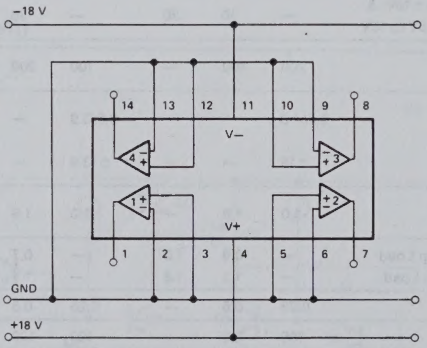
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \le T_A \le +125°C$ for OP-421B and OP-421C, $-25°C \le T_A \le +85°C$ for OP-421F and OP-421G, and $0°C \le T_A \le +70°C$ for OP-421H, unless otherwise noted.

			OP-421B OP-421F			OP-421C OP-421G			OP-421H			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}		—	5	10	—	8	15	—	10	15	µV/°C
Input Offset Voltage	V_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	—	1	3.5	—	1.8	5.5	—	3	7.5	mV
Input Offset Current	I_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	—	1.6	8	—	3.0	15	—	6.0	30	nA
Input Bias Current	I_B	$V_S = \pm 2.5V$ to $\pm 15V$	—	25	70	—	60	125	—	140	230	nA
Input Voltage Range	IVR	$V+ = +5V$, $V- = 0V$	0/3.2	—	—	0/3.2	—	—	0/3.2	—	—	V
		$V_S = \pm 15V$	−15/13.2	—	—	−15/13.2	—	—	−15/13.2	—	—	
Common-Mode Rejection Ratio	CMRR	$V+ = +5V$, $V- = 0V$, $0V \le V_{CM} \le +3.2V$	78	96	—	74	94	—	73	86	—	dB
		$V_S = \pm 15V$, $-15V \le V_{CM} \le +13.2V$	78	96	—	74	94	—	73	86	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$; &	—	15	50	—	25	80	—	40	100	µV/V
		$V- = 0V$, $V+ = 5V$ to $30V$	—	15	50	—	25	80	—	40	100	
Large-Signal Voltage Gain	A_{VO}	$V_O = 10V$ $R_L = 20k\Omega$	100	200	—	50	100	—	50	100	—	V/mV
Output Voltage Swing	V_O	$V+ = 5V$, $V- = 0V$ $R_L = 10k\Omega$	0.8/3.9	—	—	0.9/3.8	—	—	1.0/3.7	—	—	V
		$V_S = \pm 15V$, $R_L = 20k\Omega$	±13.8	—	—	±13.7	—	—	±13.7	—	—	
Supply Current (Four Amplifiers)	I_{SY}	$V_S = \pm 2.5V$, No Load	—	1.2	1.5	—	1.5	2.0	—	2.0	3.0	mA
		$V_S = \pm 15V$, No Load	0.68	2.0	2.5	0.68	2.5	3.2	0.68	3.2	4.0	

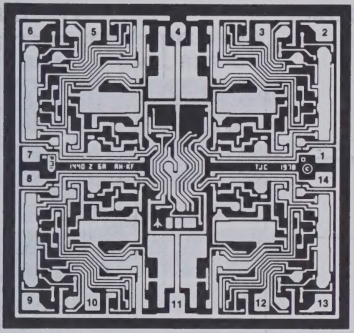
NOTE:

1. Sample tested.

BURN-IN CIRCUIT



DICE CHARACTERISTICS



DIE SIZE 0.086 × 0.092 inch, 7912 sq. mils (2.34 × 2.18 mm, 5.10 sq. mm)

1. **OUTPUT 1**
2. **INVERTING INPUT 1**
3. **NONINVERTING INPUT 1**
4. **V+**
5. **NONINVERTING INPUT 2**
6. **INVERTING INPUT 2**
7. **OUTPUT 2**
8. **OUTPUT 3**
9. **INVERTING INPUT 3**
10. **NONINVERTING INPUT 3**
11. **V−**
12. **NONINVERTING INPUT 4**
13. **INVERTING INPUT 4**
14. **OUTPUT 4**

For additional DICE information refer to Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-421N LIMIT	OP-421G LIMIT	OP-421GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	2.5	4	6	mV MAX
Input Offset Current	I_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	5	10	20	nA MAX
Input Bias Current	I_B	$V_S = \pm 2.5V$ to $\pm 15V$	50	80	150	nA MAX
Input Voltage Range	IVR		−15/13.5	−15/13.5	−15/13.5	V MIN
Common-Mode Rejection Ratio	CMRR	$V+ = +5V$, $V- = 0V$ $0V \le V_{CM} \le +3.5V$ $V_S = \pm 15V$, $-15V \le V_{CM} \le +13.5V$	83	80	76	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$; and $V- = 0V$, $V+ = +5V$ to $30V$	30	50	80	μV/V MAX
Large Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$ $R_L = 20k\Omega$	200	200	100	V/mV MIN
Output Voltage Swing	V_O	$V+ = +5V$, $V- = 0V$, $R_L = 5k\Omega$ $V_S = \pm 15V$, $R_L = 10k\Omega$	0.7/4.0 ±14	0.8/3.9 ±13.9	0.9/3.8 ±13.8	V MIN
Supply Current (Four Amplifiers)	I_{SY}	$V_S = \pm 2.5V$, No Load $V_S = \pm 15V$, No Load	1.0 1.8	1.5 2.3	2.0 3.0	mA MAX

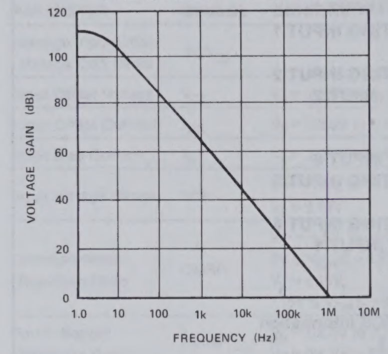
Note: Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

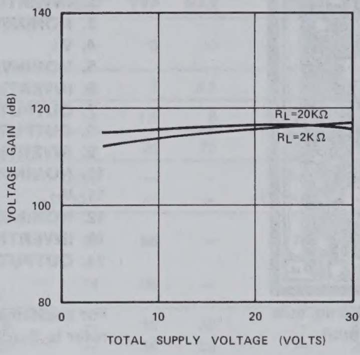
PARAMETER	SYMBOL	CONDITIONS	OP-421N TYPICAL	OP-421G TYPICAL	OP-421GR TYPICAL	UNITS
Input Noise Voltage Density	e_n	$f_O = 10Hz$ $f_O = 100Hz$	20 15	20 15	20 15	$nV/\sqrt{Hz}$
Closed-Loop Bandwidth	BW	$A_{VCL} = +1.0$ $R_L = 10k\Omega$	1.9	1.9	1.9	MHz
Slew Rate	SR		0.5	0.5	0.5	V/μs
Channel Separation	CS		120	120	120	dB

TYPICAL PERFORMANCE CHARACTERISTICS

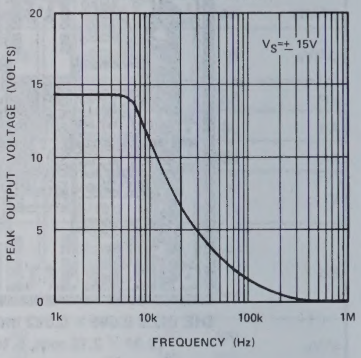
OPEN-LOOP FREQUENCY RESPONSE



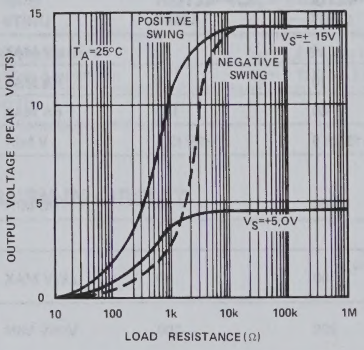
OPEN-LOOP GAIN vs POWER SUPPLY VOLTAGE



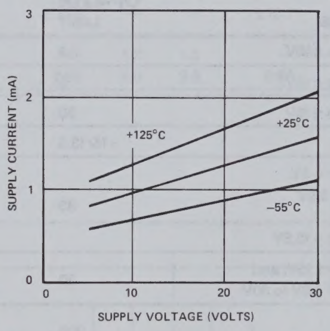
OUTPUT SWING vs FREQUENCY



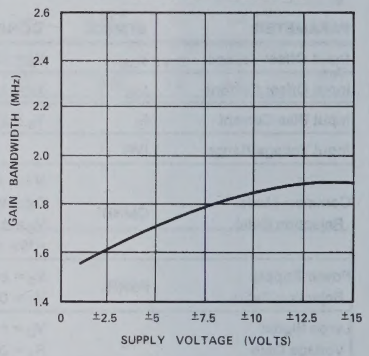
OUTPUT SWING vs OUTPUT LOAD



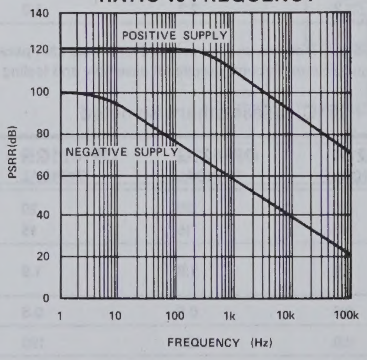
SUPPLY CURRENT vs SUPPLY VOLTAGE



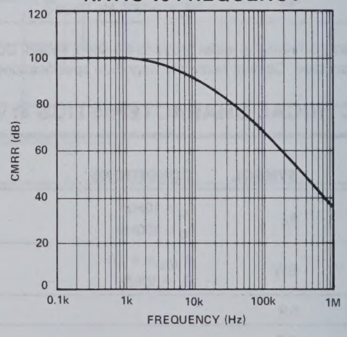
GAIN BANDWIDTH vs SUPPLY VOLTAGE



POWER SUPPLY REJECTION RATIO vs FREQUENCY

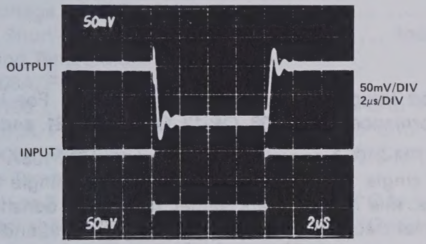


COMMON-MODE REJECTION RATIO vs FREQUENCY



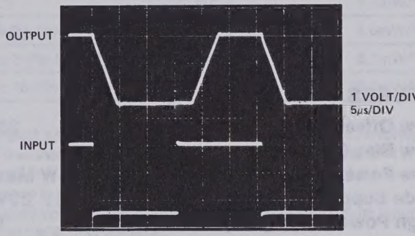
TYPICAL PERFORMANCE CHARACTERISTICS

VOLTAGE FOLLOWER SMALL-SIGNAL RESPONSE



V_S = 0V, +15V
R_L = 10kΩ
T_A = 25°C
C_L = 50pf

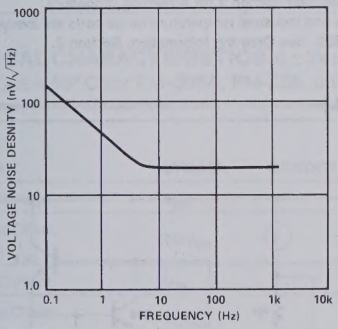
VOLTAGE FOLLOWER LARGE-SIGNAL RESPONSE



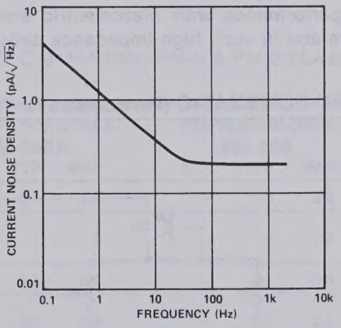
V_S = 0V, +15V
R_L = 10kΩ
T_A = 25°C
C_L = 50pf

NOISE CHARACTERISTICS

INPUT NOISE VOLTAGE DENSITY vs FREQUENCY



INPUT NOISE CURRENT DENSITY vs FREQUENCY



PM-108A/PM-2108A LOW-INPUT-CURRENT OPERATIONAL AMPLIFIERS

PM-108A/PM-208A/PM-308A/PM-108/PM-208/PM-308/PM-2108A/PM-2108

FEATURES

- **Low Offset Current .... 200pA Max**
- **Low Bias Current .... 2nA Max**
- **Low Power Consumption .... 18mW Max @ ±15V**
- **Wide Supply Range .... ±3V to ±20V**
- **High Power-Supply Rejection Ratio .... 96dB Min**
- **Low Offset Voltage Drift .... 5μV/°C Max**
- **High Common-Mode Input Range .... ±13.5V Min**
- **High Common-Mode Rejection Ratio .... 96dB Min**
- **MIL-STD-883 Class B Processing Models Available**
- **Silicon-Nitride Passivation**

GENERAL DESCRIPTION

The PM-108A series of precision operational amplifiers feature very low input offset and bias currents. Although directly interchangeable with industry-standard types, Precision Monolithics' advanced processing provides the PM-108A series with a significant improvement in input noise voltage. Low supply current drain over a wide power-supply range makes the PM-108A attractive in battery operated and other low-power applications. The low bias current provides excellent performance with piezoelectric and capacitive transducers and in such high-impedance circuits as long-period integrators and sample-and-holds. For improved performance see OP-08, OP-12, OP-20, OP-21, and OP-22.

The PM-2108A contains two superbeta, PM-108A op amps in a single 16-pin DIP. Compared to the single PM-108A types, this model offers higher packaging density, closer thermal tracking between the two amplifiers, and reduced insertion cost.

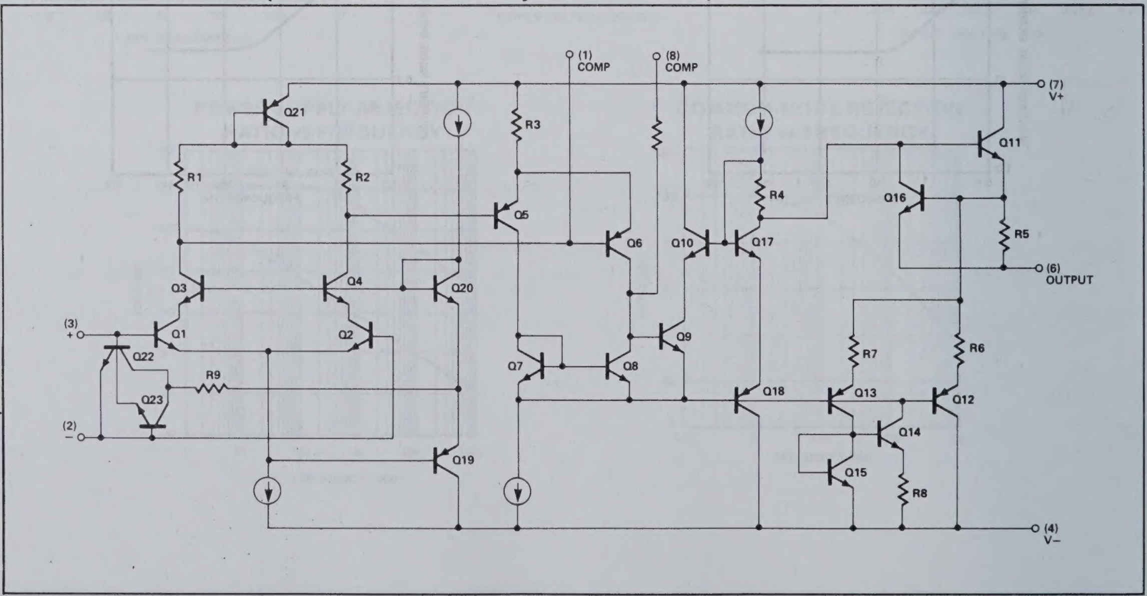
ORDERING INFORMATION†

$T_A = 25°C$ V_{OS} MAX (mV)	PACKAGE HERMETIC TO-99 8-PIN	PACKAGE HERMETIC DIP 8-PIN	PACKAGE HERMETIC DIP 16-PIN	PACKAGE PLASTIC DIP 8-PIN	OPERATING TEMPERATURE RANGE
0.5	PM108AJ*	PM108AZ*	PM2108AQ*		MIL
0.5	PM208AJ	PM208AZ			IND
0.5	PM308AJ	PM308AZ		PM308AP	COM
2.0	PM108J*	PM108Z*	PM2108Q*		MIL
2.0	PM208J	PM208Z			IND
7.5	PM308J	PM308Z		PM308P	COM

*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

SIMPLIFIED SCHEMATIC (Pin numbers for PM-108 only. Circuit is 1/2 2108.)



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
PM-108A, PM-108, PM-208A, PM-208, PM-2108A, PM-2108	±20V
PM-308A, PM-308	±18V
Internal Power Dissipation (Note 1)	500mW
Differential Input Current (Note 2)	±10mA
Input Voltage (Note 3)	±15V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	
PM-108A, PM-108, PM-2108A, PM-2108	−55°C to +125°C
PM-208A, PM-208	−25°C to +85°C
PM-308A, PM-308	0°C to +70°C
Storage Temperature Range	
(Q-, J- or Z-Package)	−65°C to +150°C
(P-Package)	−65°C to +125°C
Lead Temperature Range (Soldering, 60 sec)	300°C

NOTES:

1. Maximum package power dissipation vs. ambient temperature.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
Plastic 8-Pin DIP (P)	36°C	5.6mW/°C
Hermetic 8-Pin DIP (Z)	75°C	6.7mW/°C
Hermetic 16-Pin DIP (Q)	100°C	10.0mW/°C

2. The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, if a differential input voltage in excess of 1V is applied between the inputs, excessive current will flow, unless some limiting resistance is provided.
3. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

ELECTRICAL CHARACTERISTICS at $\pm5V \le V_S \le \pm20V$ and $T_A = 25°C$, unless otherwise noted.

			PM-108A/PM-2108A PM-208A			PM-108/PM-2108 PM-208			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.3	0.5	—	0.7	2.0	mV
Input Offset Current	I_{OS}		—	0.05	0.2	—	0.05	0.2	nA
Input Bias Current	I_B		—	0.8	2.0	—	0.8	2.0	nA
Input Resistance	R_{IN}	(Note 1)	30	70	—	30	70	—	MΩ
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm15V$, $V_{OUT} = \pm10V$, $R_L \ge 10k\Omega$	80	300	—	50	300	—	V/mV
Supply Current	I_{SY}	$I_{OUT} = 0$, $V_{OUT} = 0$, Each Amplifier	—	0.3	0.6	—	0.3	0.6	mA

ELECTRICAL CHARACTERISTICS at $\pm5V \le V_S \le \pm20V$, $-55°C \le T_A \le +125°C$ for PM-108A, PM-108, PM-2108A and PM-2108, $-25°C \le T_A \le +85°C$ for PM-208A, PM-208, unless otherwise noted.

			PM-108A/PM-2108A PM-208A			PM-108/PM-2108 PM-208			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.4	1.0	—	1.0	3.0	mV
Average Input Offset Voltage Drift	TCV_{OS}		—	1	5	—	3	15	µV/°C
Input Offset Current	I_{OS}		—	0.1	0.4	—	0.1	0.4	nA
Average Input Offset Current Drift	TCI_{OS}		—	0.5	2.5	—	0.5	2.5	pA/°C
Input Bias Current	I_B		—	1	3	—	1	3	nA
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm15V$, $V_{OUT} = \pm10V$, $R_L \ge 10k\Omega$	40	200	—	25	200	—	V/mV
Output Voltage Swing	V_O	$V_S = \pm15V$, $R_L = 10k\Omega$	±13	±14	—	±13	±14	—	V
Input Voltage Range	IVR	$V_S = \pm15V$	±13.5	—	—	±13.5	—	—	V
Common-Mode Rejection Ratio	CMRR	$V_S = \pm15V$, $V_{CM} = \pm13.5V$	96	110	—	85	100	—	dB
Power-Supply Rejection Ratio	PSRR	$V_S = \pm5V$ to $\pm20V$	—	3	15	—	15	100	µV/V
Supply Current	I_{SY}	$V_{OUT} = 0$, $T_A = MAX$, Each Amplifier	—	0.15	0.4	—	0.15	0.4	mA

NOTE:

1. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at $\pm5V \le V_S \le \pm20V$ and $T_A = 25°C$, unless otherwise noted.

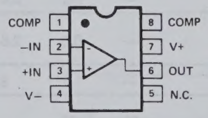
PARAMETER	SYMBOL	CONDITIONS	PM-308A MIN	PM-308A TYP	PM-308A MAX	PM-308 MIN	PM-308 TYP	PM-308 MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.3	0.5	—	2.0	7.5	mV
Input Offset Current	I_{OS}		—	0.2	1.0	—	0.2	1.0	nA
Input Bias Current	I_B		—	1.5	7.0	—	1.5	7.0	nA
Input Resistance	R_{IN}	(Note 1)	10	40	—	10	40	—	MΩ
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm15V$, $V_{OUT} = \pm10V$, $R_L \ge 10k\Omega$	80	300	—	25	300	—	V/mV
Supply Current	I_{SY}	$I_{OUT} = 0$, $V_{OUT} = 0$, Each Amplifier	—	0.3	0.8	—	0.3	0.8	mA

ELECTRICAL CHARACTERISTICS at $\pm5V \le V_S \le \pm15V$ and $0°C \le T_A \le +70°C$, unless otherwise noted.

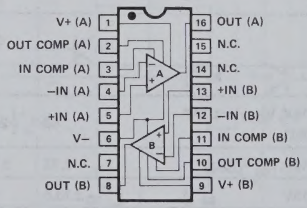
PARAMETER	SYMBOL	CONDITIONS	PM-308A MIN	PM-308A TYP	PM-308A MAX	PM-308 MIN	PM-308 TYP	PM-308 MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.4	0.73	—	3.0	10.0	mV
Average Input Offset Voltage Drift	TCV_{OS}		—	1	5	—	6	30	μV/°C
Input Offset Current	I_{OS}		—	0.3	1.5	—	0.3	1.5	nA
Average Input Offset Current Drift	TCI_{OS}		—	2	10	—	2	10	pA/°C
Input Bias Current	I_B		—	2	10	—	2	10	nA
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm15V$, $V_{OUT} = \pm10V$, $R_L \ge 10k\Omega$	60	200	—	15	100	—	V/mV
Output Voltage Swing	V_O	$V_S = \pm15V$, $R_L = 10k\Omega$	±13	±14	—	±13	±14	—	V
Input Voltage Range	IVR	$V_S = \pm15V$	±14	—	—	±13	—	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm13.5V$	96	110	—	80	100	—	dB
Power-Supply Rejection Ratio	PSRR	$V_S = \pm5V$ to $\pm15V$	—	3	15	—	15	100	μV/V
Supply Current	I_{SY}	$V_{OUT} = 0$, $T_A = MAX$, Each Amplifier	—	0.23	—	—	0.23	—	mA

NOTE:
1. Guaranteed by design.

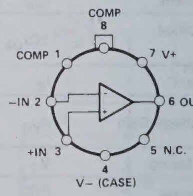
PIN CONNECTIONS


COMP 1
−IN 2
+IN 3
V− 4
8 COMP
7 V+
6 OUT
5 N.C.

EPOXY MINI-DIP
(P-Suffix)
AND
8-PIN HERMETIC DIP
(Z-Suffix)


V+ (A) 1
OUT COMP (A) 2
IN COMP (A) 3
−IN (A) 4
+IN (A) 5
V− 6
N.C. 7
OUT (B) 8
16 OUT (A)
15 N.C.
14 N.C.
13 +IN (B)
12 −IN (B)
11 IN COMP (B)
10 OUT COMP (B)
9 V+ (B)
A
B

16-PIN HERMETIC DIP
(Q-Suffix)


COMP 8
COMP 1
7 V+
−IN 2
6 OUT
+IN 3
5 N.C.
4 V− (CASE)

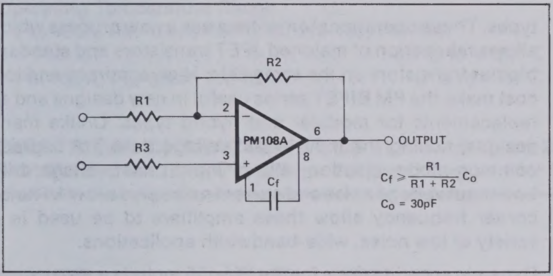
TO-99 (J-Suffix)

APPLICATIONS INFORMATION

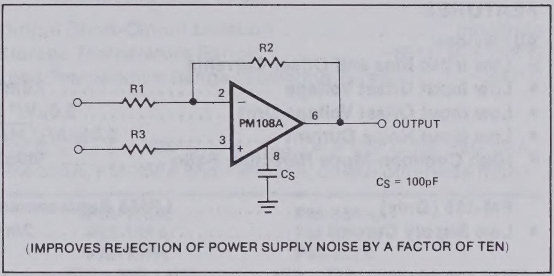
The PM-108A series has very low input offset and bias currents; the user is cautioned that printed circuit board leakages can produce significant errors, especially at high board temperatures. Careful attention to board layout and cleaning procedure is required to achieve the PM-108A's rated performance. It is suggested that board leakage be minimized by encircling the input pins with a guard ring maintained at a potential close to that of the inputs. The guard ring should be driven by a low impedance source such as an amplifier's output or ground.

COMPENSATION CIRCUITS

STANDARD


R2
R1
R3
2
3
PM108A
6
8
1
Cf
OUTPUT
$C_f \geq \frac{R1}{R1 + R2} C_o$
C_o = 30pF

ALTERNATE


R2
R1
R3
2
3
PM108A
6
8
OUTPUT
C_S
C_S = 100pF

(IMPROVES REJECTION OF POWER SUPPLY NOISE BY A FACTOR OF TEN)

PM-155A/PM-156A/PM-157A MONOLITHIC JFET-INPUT OPERATIONAL AMPLIFIERS

LOW SUPPLY CURRENT — PM-155A/PM-355A/PM-155
GENERAL PURPOSE — PM-156A/PM-356A/PM-156
WIDE-BANDWIDTH — PM-157A/PM-357A/PM-157

FEATURES

All Devices

- **Low Input Bias and Offset Currents**
- **Low Input Offset Voltage 1.0mV**
- **Low Input Offset Voltage Drift .... 3.0μV/° C**
- **Low Input Noise Current .... 0.01pA/√Hz**
- **High Common-Mode Rejection Ratio 100dB**

PM-155 (Only) .... LF155 Replacement

- **Low Supply Current 2mA**

PM-156 (Only) .... LF156 Replacement

- **High Slew Rate 12V/μsec**
- **Fast Settling to ±0.01% 4.0μsec**

PM-157 (Only) .... LF157 Replacement

- **Wide-Bandwidth Decompensated (A_{VCL} = 5 Min)...20MHz**
- **High Slew Rate 45V/μsec**
- **Fast Settling to ±0.01% 4.0μsec**

GENERAL DESCRIPTION

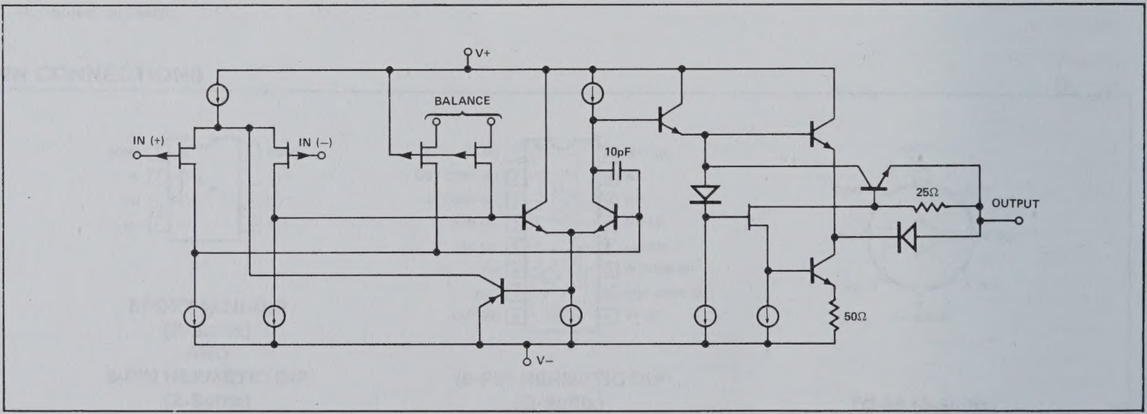
The PM BIFET series provides low input current, high slew rate, and direct interchangeability with LF155, 156, and 157 types. These operational amplifiers use a new process which allows fabrication of matched JFET transistors and standard bipolar transistors on the same chip. High accuracy and low cost make the PM BIFET series useful in new designs and as replacements for modular and hybrid types. Unlike many designs, nulling the input offset voltage does not degrade common-mode rejection ratio or input offset voltage drift. Low input voltage noise and current noise plus a low 1/f noise corner frequency allow these amplifiers to be used in a variety of low noise, wide-bandwidth applications.

Dynamic specifications for the PM-155 include a slew rate of 5V/μs, a 2.5MHz gain bandwidth product, and settling time to within ±0.01% of final value in 5.0μs. The PM-156 has a slew rate of 12V/μs and a settling time of 4.0μs to ±0.01% of final value.

The PM-157 is a very fast decompensated device. This results in a 45V/μs slew rate, a 20MHz gain bandwidth product, and a settling time of 4.0μs. Decompensation requires a minimum closed-loop gain of five because of stability considerations.

For improved performance, see the OP-15/OP-16/OP-17 data sheet. For duals, see the OP-215 data sheet.

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Supply Voltage
PM-155A, PM-156A, PM-157A, PM-155, PM-156, PM-157,
PM-355A, PM-356A, PM-357A .... ±22V
Internal Power Dissipation
PM-155A, PM-156A, PM-157, PM-155, PM-156,
PM-157 .... 670mW
PM-355A, PM-356A, PM-357A 500mW
(Derate based on a thermal resistance of 150° C/W junction to ambient or 45° C/W junction to case.)
Operating Temperature Range
PM-155A, PM-156A, PM-157A, PM-155, PM-156,
PM-157 .... −55° C to +125° C
PM-355A, PM-356A, PM-357A .... 0° C to +70° C
Maximum Junction Temperature (T_j)
PM-155A, PM-156A, PM-157A, PM-155, PM-156,
PM-157 .... +150° C
PM-355A, PM-356A, PM-357A .... +100° C
Differential Input Voltage
PM-155A, PM-156A, PM-157A, PM-155, PM-156, PM-157,
PM-355A, PM-356A, PM-357A .... ±40V
Input Voltage
PM-155A, PM-156A, PM-157A, PM-155, PM-156, PM-157,
PM-355A, PM-356A, PM-357A .... ±20V

NOTE: The absolute maximum negative input voltage is equal to the negative power supply voltage.

Output Short-Circuit Duration .... Indefinite
Storage Temperature Range .... −65° C to +150° C
Lead Temperature Range (Soldering, 60 sec) .... +300° C

ELECTRICAL CHARACTERISTICS at $\pm15V \le V_S \le \pm20V$, $-55°C \le T_A \le +125°C$ and $T_{HIGH} = +125°C$ for PM-155A, PM-156A and PM-157A, $0°C \le T_A \le +70°C$ and $T_{HIGH} = +70°C$ for PM-355A, PM-356A and PM-357A, unless otherwise noted.

			PM-155A/ PM-156A/ PM-157A			PM-355A/ PM-356A/ PM-357A			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	—	1.4	2.5	—	1.2	2.3	mV
Input Offset Voltage Drift	TCV_{OS}	$R_S = 50\Omega$	—	3	5	—	3	5	μV/° C
Change in Input Offset Drift with V_{OS} Adjust	$\left(\frac{\Delta TCV_{OS}}{\Delta V_{OS}}\right)$	$R_S = 50\Omega$	—	0.5	—	—	0.5	—	μV/° C per mV
Input Offset Current	I_{OS}	$T_j \le T_{HIGH}$ (Note 1)	—	4.0	10	—	0.4	1.0	nA
Input Bias Current	I_B	$T_j \le T_{HIGH}$ (Note 1)	—	±10	±25	—	±2	±5	nA
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm15V$, $V_O = \pm10V$, $R_L = 2k\Omega$	25	75	—	25	75	—	V/mV
Output Voltage Swing	V_O	$V_S = \pm15V$, $R_L = 10k\Omega$ $V_S = \pm15V$, $R_L = 2k\Omega$	±12 ±10	±13 ±12	— —	±12 ±10	±13 ±12	— —	V
Input Voltage Range	IVR	$V_S = \pm15V$	±10.4	+15.1 −12.0	—	±10.4	+15.1 −12.0	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm IVR$	85	100	—	85	100	—	dB
Power Supply Rejection Ratio	PSRR	(Note 2)	—	10	57	—	10	57	μV/V

NOTES:

1. PMI has a bias current compensation circuit which gives improved bias current over the standard JFET input op amps. I_B and I_{OS} are measured at $V_{CM} = 0$.
2. Power supply rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

ELECTRICAL CHARACTERISTICS at ±15V ≤ V_S ≤ ±20V, T_A = 25° C, unless otherwise noted.

				PM-155A/ PM-156A/ PM-157A			PM-355A/ PM-356A/ PM-357A			
PARAMETER	**SYMBOL**	**CONDITIONS**		**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$		—	1	2	—	1	2	mV
Input Offset Current	I_{OS}	T_j = 25° C (Note 1)		—	3	10	—	3	10	pA
Input Bias Current	I_B	T_j = 25° C (Note 1)		—	±30	±50	—	±30	±50	pA
Input Resistance	R_{IN}			—	10^{12}	—	—	10^{12}	—	Ω
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $V_O = \pm 10V$, $R_L = 2k\Omega$		50	200	—	50	200	—	V/mV
Supply Current	I_{SY}	$V_S = \pm 15V$	PM-155	—	2	4	—	2	4	mA
			PM-156/PM-157	—	5	7	—	5	7	
Slew Rate	SR	$A_{VCL} = +1$, $V_S = \pm 15V$	PM-155	3	5	—	3	5	—	V/μs
			PM-156	10	12	—	10	12	—	
		$A_{VCL} = +5$, $V_S = \pm 15V$	PM-157	40	45	—	40	45	—	
Gain Bandwidth Product	GBW	$A_{VCL} = +1$, $V_S = \pm 15V$	PM-155	—	2.5	—	—	2.5	—	MHz
			PM-156	4.0	4.5	—	4.0	4.5	—	
		$A_{VCL} = +5$, $V_S = \pm 15V$	PM-157	15	20	—	15	20	—	
Settling Time (to ±0.01%)	t_S	$V_S = \pm 15V$ (Note 2)	PM-155	—	5.0	—	—	4.0	—	μs
			PM-156	—	4.0	—	—	1.5	—	
		$V_S = \pm 15V$ (Note 3)	PM-157	—	4.0	—	—	1.5	—	
Input Noise Voltage	e_n	$R_S = 100\Omega$, f = 100Hz	PM-155	—	25	—	—	25	—	nV/$\sqrt{Hz}$
		$R_S = 100\Omega$, f = 1000Hz		—	20	—	—	20	—	
		$R_S = 100\Omega$, f = 100Hz	PM-156/PM-157	—	15	—	—	15	—	
		$R_S = 100\Omega$, f = 1000Hz		—	12	—	—	12	—	
Input Noise Current	i_n	f = 100Hz, $V_S = \pm 15V$		—	0.01	—	—	0.01	—	pA/$\sqrt{Hz}$
		f = 1000Hz, $V_S = \pm 15V$		—	0.01	—	—	0.01	—	
Input Capacitance	C_{IN}			—	3	—	—	3	—	pF

NOTES:

1. PMI has a bias current compensation circuit which gives improved bias current over the standard JFET input op amps. I_B and I_{OS} are measured at $V_{CM} = 0$.
2. Settling time is defined here for a unity gain inverter connection using 2kΩ resistors. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter. See settling time test circuit.
3. Settling time is defined here for a $A_V = -5$ connection with $R_F = 2k\Omega$. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 2V step input is applied to the inverter. See settling time test circuit.

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $\pm15V \leq V_S \leq \pm20V$ for PM-155, PM-156 and PM-157, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS		PM-155 PM-156 PM-157 MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$		—	3	5	mV
Input Offset Current	I_{OS}	$T_j = 25°C$ (Note 1)		—	3	20	pA
Input Bias Current	I_B	$T_j = 25°C$ (Note 1)		—	±30	±100	pA
Input Resistance	R_{IN}			—	10^{12}	—	Ω
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm15V$, $V_O = \pm10V$, $R_L = 2k\Omega$		50	200	—	V/mV
Supply Current	I_{SY}	$V_S = \pm15V$	PM-155	—	2	4	mA
			PM-156/PM-157	—	5	7	
Slew Rate	SR	$A_{VCL} = +1$, $V_S = \pm15V$	PM-155	—	5	—	V/μs
			PM-156	7.5	12	—	
		$A_{VCL} = +5$, $V_S = \pm15V$	PM-157	30	40	—	
Gain Bandwidth Product	GBW	$A_{VCL} = +1$, $V_S = \pm15V$	PM-155	—	2.5	—	MHz
			PM-156	—	5	—	
		$A_{VCL} = +5$, $V_S = \pm15V$	PM-157	—	20	—	
Settling Time (to ±0.01%)	t_S	$V_S = \pm15V$ (Note 2)	PM-155	—	5	—	μs
			PM-156	—	4	—	
		$V_S = \pm15V$ (Note 3)	PM-157	—	4	—	
Input Noise Voltage	e_n	$R_S = 100\Omega$, f = 100Hz	PM-155	—	25	—	$nV/\sqrt{Hz}$
		$R_S = 100\Omega$, f = 1000Hz		—	20	—	
		$R_S = 100\Omega$, f = 100Hz	PM-156/PM-157	—	15	—	
		$R_S = 100\Omega$, f = 1000Hz		—	12	—	
Input Noise Current	i_n	f = 100Hz, $V_S = \pm15V$ f = 1000Hz, $V_S = \pm15V$		—	0.01	—	$pA/\sqrt{Hz}$
Input Capacitance	C_{IN}			—	3	—	pF

NOTES:

1. PMI has a bias current compensation circuit which gives improved bias current over the standard JFET input op amps. I_B and I_{OS} are measured at $V_{CM} = 0$.
2. Settling time is defined here for a unity gain inverter connection using 2kΩ resistors. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter. See settling time test circuit.
3. Settling time is defined here for a $A_V = -5$ connection with $R_F = 2k\Omega$. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 2V step input is applied to the inverter. See settling time test circuit.

ELECTRICAL CHARACTERISTICS at $\pm 15V \leq V_S \leq \pm 20V$ and $-55°C \leq T_A \leq +125°C$ and $T_{HIGH} = +125°C$ for PM-155, PM-156 and PM-157, unless otherwise noted.

			PM-155 PM-156 PM-157			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	—	4	7	mV
Input Offset Voltage Drift	TCV_{OS}	$R_S = 50\Omega$	—	5	—	μV/°C
Change In Input Offset Drift With V_{OS} Adjust.	$\left(\frac{\Delta TCV_{OS}}{\Delta V_{OS}}\right)$	$R_S = 50\Omega$	—	0.5	—	μV/°C per mV
Input Offset Current	I_{OS}	$T_j \leq T_{HIGH}$ (Note 1)	—	8	20	nA
Input Bias Current	I_B	$T_j \leq T_{HIGH}$ (Note 1)	—	±2	±50	nA
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $V_O = \pm 10V$ $R_L = 2k\Omega$	25	75	—	V/mV
Output Voltage Swing	V_O	$V_S = \pm 15V$, $R_L = 10k\Omega$ $V_S = \pm 15V$, $R_L = 2k\Omega$	±12 ±10	±13 ±12	— —	V
Input Voltage Range	IVR	$V_S = \pm 15V$	±10.4	+15.1 −12.0	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm IVR$	85	100	—	dB
Power Supply Rejection Ratio	PSRR	(Note 2)	—	10	57	μV/V

NOTES:

1. PMI has a bias current compensation circuit which gives improved bias current over the standard JFET input op amps. I_B and I_{OS} are measured at $V_{CM} = 0$, $T_j = +125°C$.
2. Power supply rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

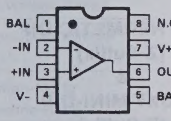
ORDERING INFORMATION†

$T_A = 25°C$ V_{OS} MAX (mV)	PACKAGE TO-99 8-PIN	 8-PIN HERMETIC DIP	OPERATING TEMPERATURE RANGE
2.0	PM155AJ* PM156AJ* PM157AJ*	PM155AZ* PM156AZ* PM157AZ*	MIL
2.0	PM355AJ PM356AJ PM357AJ	PM355AZ PM356AZ PM357AZ	COM
5.0	PM155J* PM156J* PM157J*	PM155Z PM156Z PM157Z	MIL

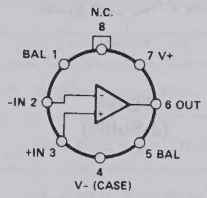
*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

PIN CONNECTIONS



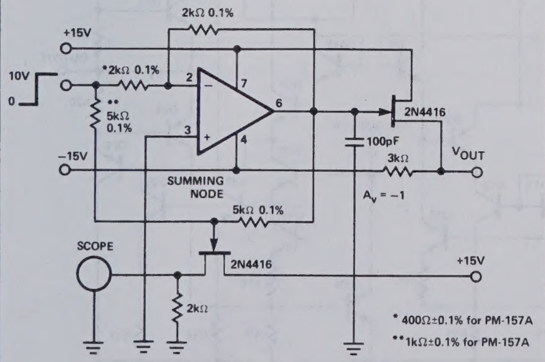
8-PIN HERMETIC DIP (Z-Suffix)



TO-99 (J-Suffix)

BASIC CONNECTIONS

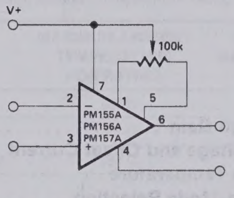
SETTLING-TIME TEST CIRCUIT



* 400Ω±0.1% for PM-157A

** 1kΩ±0.1% for PM-157A

INPUT OFFSET VOLTAGE NULLING



NOTE: FOR POTENTIOMETERS WITH A TEMPERATURE COEFFICIENT ≤ 100ppm/°C, THE ADDED TCV_{os} WITH NULLING IS ≈ 0.5μV/°C/mV OF ADJUSTMENT.

APPLICATIONS INFORMATION

INPUT VOLTAGE CONSIDERATIONS

The PM series JFET input stages can accommodate large input differential voltages without external clamping as long as neither input exceeds the negative power supply. An input voltage which is more negative than V− can result in a destroyed unit.

If both inputs exceed the negative common-mode voltage limit, the amplifier will be forced to a high positive output. If only one input exceeds the negative common-mode voltage limit, a phase reversal takes place forcing the output to the corresponding high or low state. In either of the above conditions, normal operation will return when both inputs are returned to within the specified common-mode voltage range. Exceeding the positive common-mode limit on a single input will not change the phase of the output. However, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

POWER SUPPLY CONSIDERATIONS

Power supply polarity reversal can result in a destroyed unit.

DYNAMIC OPERATING CONSIDERATIONS

As with most amplifiers, care should be taken with lead dress, component placement, and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input. This minimizes "pick-up" and increases the frequency of the feedback pole by minimizing the capacitance from input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device to AC ground sets the frequency of the pole. In many instances, the frequency of this pole is much greater than the expected 3dB frequency of the closed-loop gain. Consequently, the pole has negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3dB frequency, a lead capacitor should be placed from the output to the inverting input of the op amp. The capacitor value should be such that the RC time constant of the capacitor and feedback resistor is greater than, or equal to, the original feedback-pole time constant.

PM-725

INSTRUMENTATION OPERATIONAL AMPLIFIER

FEATURES

- **Extremely High Gain .... 3M Typ**
- **Low Offset Voltage and Offset Current**
- **Low Drift with Temperature**
- **High Common-Mode Rejection .... 110dB Min**
- **High Power Supply Rejection .... 10μV/V Max**
- **Silicon-Nitride Passivation**
- **Differential-Input Overvoltage Protection**

GENERAL DESCRIPTION

The PM-725 series of monolithic instrumentation operational amplifiers provide industry-standard 725 specifications. In addition, Precision Monolithics' exclusive Silicon-Nitride "Triple Passivation" process minimizes "popcorn noise" and provides maximum reliability and long-term stability. For improved specifications, refer to the OP-06 series data sheet. For devices with internal frequency compensation, refer to the OP-05 instrumentation amplifier and OP-07 ultra-low offset voltage operational amplifier data sheets.

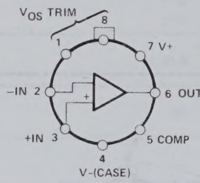
ORDERING INFORMATION†

$T_A = 25°C$ V_{OS} MAX (mV)	HERMETIC TO-99 8-PIN	HERMETIC DIP 8-PIN	PLASTIC DIP 8-PIN	OPERATING TEMPERATURE RANGE
1.0	PM725J*	PM725Z*		MIL
2.5	PM725CJ	PM725CZ	PM725CP	COM

*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

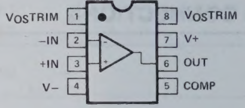
†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

PIN CONNECTIONS



V_{OS} TRIM
8
1
7 V+
−IN 2
6 OUT
+IN 3
5 COMP
4
V-(CASE)

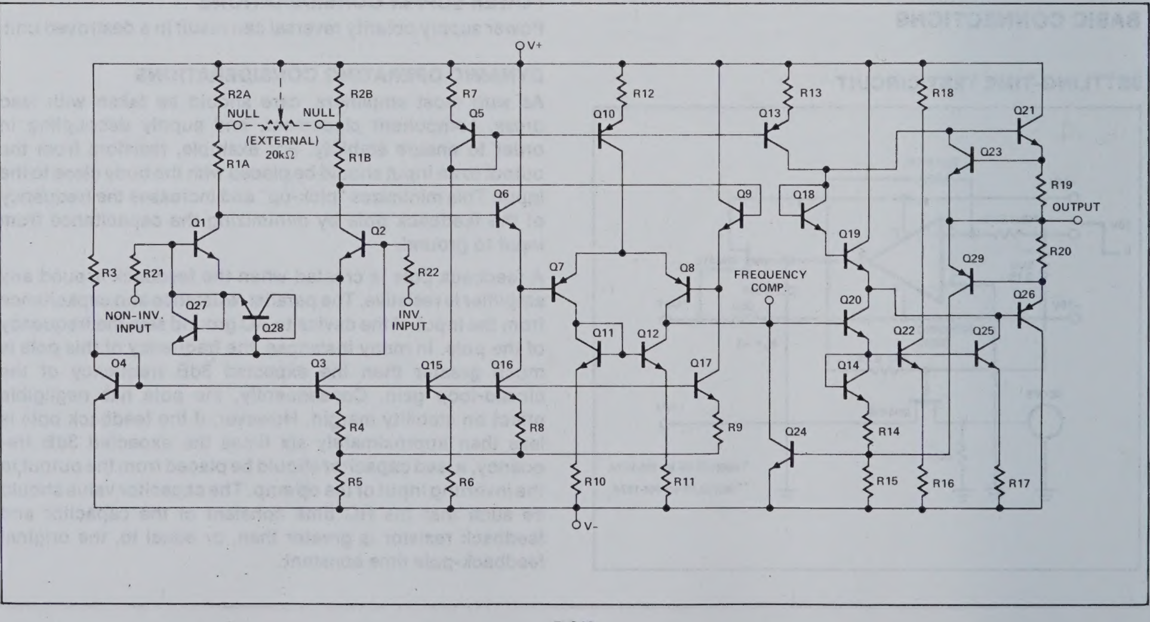
TO-99 (J-Suffix)



V_{OS}TRIM 1
−IN 2
+IN 3
V− 4
8 V_{OS}TRIM
7 V+
6 OUT
5 COMP

8-PIN HERMETIC DIP (Z-Suffix) & EPOXY MINI-DIP (P-Suffix)

SIMPLIFIED SCHEMATIC



V+
R2A
R2B
NULL
NULL
(EXTERNAL) 20kΩ
R1A
R1B
R7
Q5
R12
Q10
R13
Q13
R18
Q21
Q23
R19
OUTPUT
R20
Q29
Q26
Q25
Q22
Q14
Q20
Q19
Q18
Q9
Q6
Q1
Q2
R3
R21
Q27
Q28
NON-INV. INPUT
INV. INPUT
R22
Q7
Q8
FREQUENCY COMP.
Q11
Q12
Q17
Q4
Q3
Q15
Q16
R4
R8
R9
Q24
R14
R5
R6
R10
R11
R15
R16
R17
V−

ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... ±22V
Internal Power Dissipation (see note) 500mW
Differential Input Voltage .... ±30V
Input Voltage .... Supply Voltage
Output Short-Circuit Duration .... Indefinite
Storage Temperature Range
  J and Z Packages .... −65°C to +150°C
  P Package .... −65°C to +125°C
Operating Temperature Range
  PM-725 .... −55°C to +125°C
  PM-725C .... 0°C to +70°C
Lead Temperature Range (Soldering, 60 sec) ...... 300°C

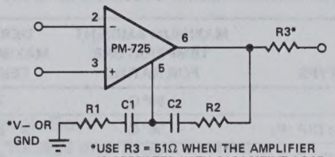
NOTE:
1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
8-Pin Plastic DIP (P)	36°C	5.6mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

			PM-725			PM-725C			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$	—	0.5	1.0	—	0.5	2.5	mV
Input Offset Current	I_{OS}		—	2	20	—	2	35	nA
Input Bias Current	I_B		—	42	100	—	42	125	nA
Input Noise Voltage	e_n	$f_O = 10Hz$ $f_O = 100Hz$ $f_O = 1000Hz$	— — —	15 9 8	— — —	— — —	15 9 8	— — —	$nV/\sqrt{Hz}$
Input Resistance	R_{IN}		—	1.5	—	—	1.5	—	MΩ
Input Voltage Range	IVR		±13.5	±14	—	±13.5	±14	—	V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	1,000	3,000	—	250	3,000	—	V/mV
Common-Mode Rejection Ratio	CMRR	$R_S \leq 10k\Omega$, $V_{CM} = \pm 13.5V$	110	120	—	94	120	—	dB
Power Supply Rejection Ratio	PSRR	$R_S \leq 10k\Omega$, $V_S = \pm 5V$ to $\pm 15V$	—	2	10	—	2	35	μV/V
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$	±12.0 ±10.0	±13.5 ±13.5	— —	±12.0 ±10.0	±13.5 ±13.5	— —	V
Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	150	—	—	150	—	Ω
Power Consumption	P_d	No Load	—	80	105	—	80	150	mW

COMPENSATION CIRCUIT



*USE R3 = 51Ω WHEN THE AMPLIFIER IS OPERATED WITH CAPACITIVE LOAD.

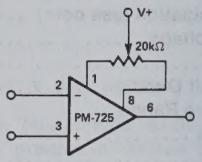
COMPENSATION COMPONENT VALUES

Av	R_1 (Ω)	C_1 (µF)	R_2 (Ω)	C_2 (µF)
10,000	10k	50pF		
1,000	470	0.001		
100	47	0.01		
10	27	0.05	270	0.0015
1	10	0.05	39	0.02

*FOR MAXIMUM PSRR VS FREQUENCY COMPENSATION NETWORK SHOULD BE RETURNED TO V−

PINOUTS FOR J, Z, AND P PACKAGES.

OFFSET VOLTAGE NULL CIRCUIT



PINOUTS FOR J, Z, AND P PACKAGES.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \le T_A \le +125°C$ for PM-725, $0°C \le T_A \le +70°C$ for PM-725C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-725 MIN	PM-725 TYP	PM-725 MAX	PM-725C MIN	PM-725C TYP	PM-725C MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \le 10k\Omega$	—	—	1.5	—	—	3.5	mV
Average Input Offset Voltage Drift	TCV_{OS}	$R_S = 50\Omega$, Unnulled (Note 1)	—	2	5	—	2	—	µV/°C
Average Input Offset Voltage Drift	TCV_{OSn}	$R_S = 50\Omega$, Nulled	—	0.6	—	—	0.6	—	µV/°C
Input Offset Current	I_{OS}	$T_A = MAX$ $T_A = MIN$	— —	1.2 7.5	20 40	— —	1.2 4.0	35 50	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 1)	—	35	150	—	10	—	pA/°C
Input Bias Current	I_B	$T_A = MAX$ $T_A = MIN$	— —	20 80	100 200	— —	30 100	125 250	nA
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$, $T_A = MAX$ $R_L \ge 2k\Omega$, $T_A = MIN$	1,000 250	— —	— —	125 125	— —	— —	V/mV
Common-Mode Rejection Ratio	CMRR	$R_S \le 10k\Omega$, $V_{CM} = \pm 13.5V$	100	—	—	—	115	—	dB
Power Supply Rejection Ratio	PSRR	$R_S \le 10k\Omega$, $V_S = \pm 5V$ to $\pm 15V$	—	—	20	—	20	—	µV/V
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±10	—	—	±10	—	—	V

NOTE: 1. Sample tested.

COMPENSATED OPERATIONAL AMPLIFIER

PM-741

FEATURES

- **Industry Standard 741 Specifications**
- **Internal Frequency Compensation**
- **Continuous Short-Circuit Protection**
- **Silicon-Nitride Passivation**
- **Low Noise**

GENERAL DESCRIPTION

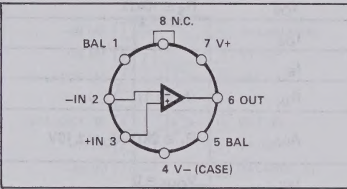
The PM-741 series of internally-compensated operational amplifiers provide industry-standard 741 specifications. In addition, Precision Monolithics' exclusive Silicon-Nitride "Triple Passivation" process provides high reliability and long-term stability of parameters. For higher performance general purpose op amps, refer to the OP-02 data sheet. See the OP-04/OP-14 data sheet for duals.

ORDERING INFORMATION†

$T_A = 25°C$ V_{OS} MAX (mV)	PACKAGE TO-99 8-PIN	OPERATING TEMPERATURE RANGE
5.0	PM741J	MIL
6.0	PM741CJ	COM

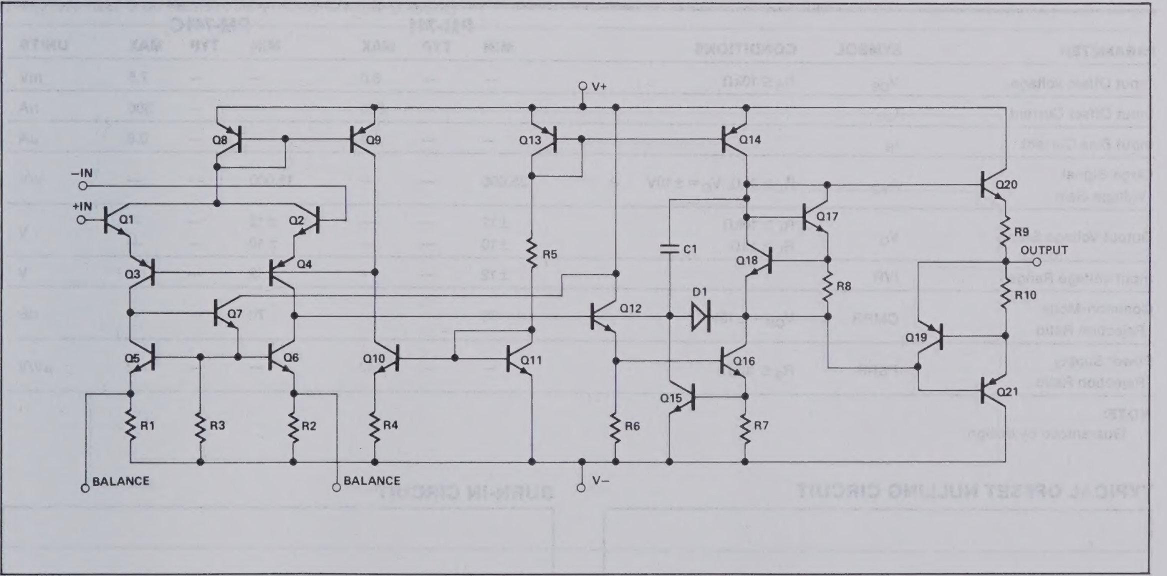
†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

PIN CONNECTIONS


8 N.C.
BAL 1
7 V+
–IN 2
6 OUT
+IN 3
5 BAL
4 V– (CASE)

TO-99 (J-Suffix)

SIMPLIFIED SCHEMATIC


V+
Q8
Q9
Q13
Q14
Q20
–IN
+IN
Q1
Q2
Q17
R9
OUTPUT
R5
C1
Q18
Q3
Q4
R8
D1
R10
Q7
Q12
Q19
Q5
Q6
Q10
Q11
Q16
Q21
Q15
R1
R3
R2
R4
R6
R7
BALANCE
BALANCE
V–

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
PM-741	±22V
PM-741C	±18V
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage	Supply Voltage
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range (Soldering, 60 sec)	300°C
Operating Temperature Range	
PM-741	−55°C to +125°C
PM-741C	0°C to +70°C

NOTE:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, $V_S = \pm15V$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-741 MIN	PM-741 TYP	PM-741 MAX	PM-741C MIN	PM-741C TYP	PM-741C MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$	—	—	5.0	—	—	6.0	mV
Input Offset Current	I_{OS}		—	—	200	—	—	200	nA
Input Bias Current	I_B		—	—	500	—	—	500	nA
Input Resistance	R_{IN}	(Note 1)	0.3	—	—	0.3	—	—	MΩ
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm10V$	50,000	—	—	25,000	—	—	V/V
Supply Current	I_{SY}	$V_{OUT} = 0$	—	—	2.8	—	—	2.8	mA

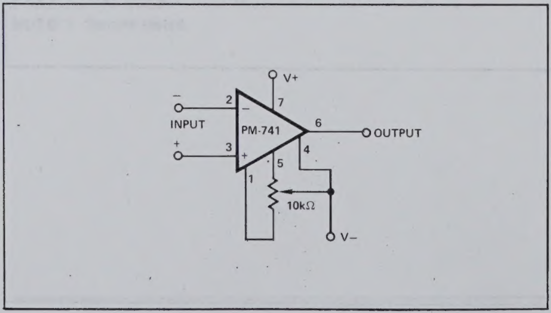
ELECTRICAL CHARACTERISTICS at $-55°C \leq T_A \leq +125°C$ for PM741, $0°C \leq T_A \leq +70°C$ for PM741C, $V_S = \pm15V$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-741 MIN	PM-741 TYP	PM-741 MAX	PM-741C MIN	PM-741C TYP	PM-741C MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$	—	—	6.0	—	—	7.5	mV
Input Offset Current	I_{OS}		—	—	500	—	—	300	nA
Input Bias Current	I_B		—	—	1.5	—	—	0.8	μA
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm10V$	25,000	—	—	15,000	—	—	V/V
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$ $R_L \geq 1k\Omega$	±12 ±10	— —	— —	±12 ±10	— —	— —	V
Input Voltage Range	IVR		±12	—	—	±12	—	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm10V$	70	—	—	70	—	—	dB
Power Supply Rejection Ratio	PSRR	$R_S \leq 10k\Omega$	—	—	142	—	—	142	μV/V

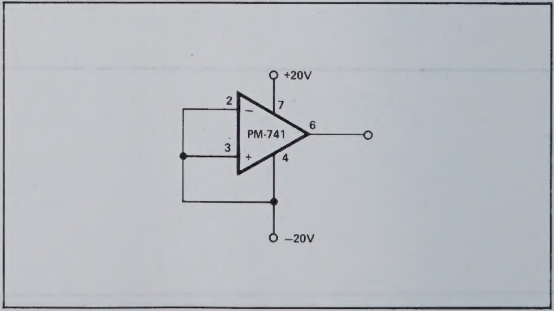
NOTE:

1. Guaranteed by design.

TYPICAL OFFSET NULLING CIRCUIT



BURN-IN CIRCUIT



DUAL COMPENSATED OPERATIONAL AMPLIFIER

PM-747

FEATURES

- **Dual PM-741 Internally-Compensated Operational Amplifier**
- **Internal Frequency Compensation**
- **Low Power Consumption**
- **Continuous Short-Circuit Protection**
- **Silicon-Nitride Passivation**

ORDERING INFORMATION†

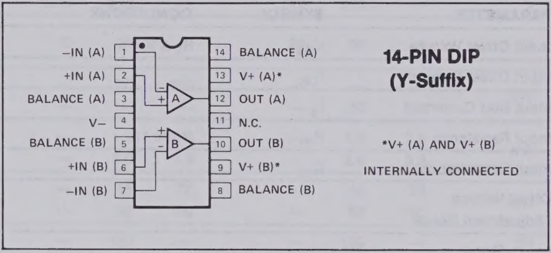
$T_A = 25°C$ V_{OS} MAX (mV)	PACKAGE HERMETIC DIP 14-Pin	OPERATING TEMPERATURE Range
5.0	PM747Y	MIL
6.0	PM747CY	COM

†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

GENERAL DESCRIPTION

The PMI series of internally-compensated operational amplifiers provides industry-standard 747 specifications. In addition, Precision Monolithics' exclusive Silicon-Nitride "Triple Passivation" process provides maximum reliability and long-term stability of parameters for lowest overall system operating cost.

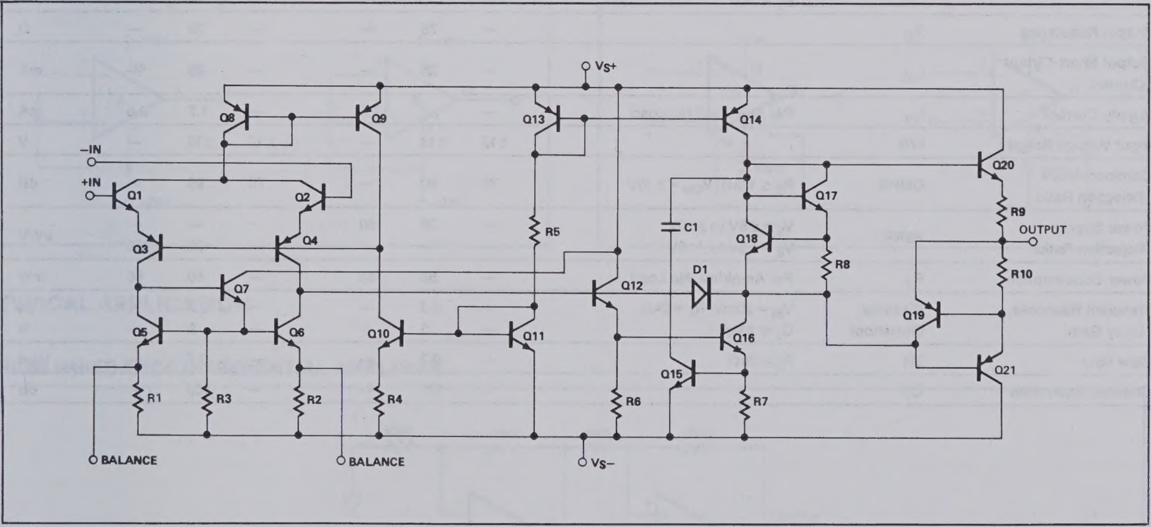
PIN CONNECTIONS


–IN (A) 1
+IN (A) 2
BALANCE (A) 3
V– 4
BALANCE (B) 5
+IN (B) 6
–IN (B) 7
14 BALANCE (A)
13 V+ (A)*
12 OUT (A)
11 N.C.
10 OUT (B)
9 V+ (B)*
8 BALANCE (B)
A
B
+
–

14-PIN DIP (Y-Suffix)

*V+ (A) AND V+ (B) INTERNALLY CONNECTED

SIMPLIFIED SCHEMATIC (1/2 of Circuit Shown)


Vs+
–IN
+IN
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q19
Q20
Q21
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
C1
D1
OUTPUT
BALANCE
BALANCE
Vs–

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
PM-747	±22V
PM-747C	±18V
Internal Power Dissipation (Note 1)	
Y Package	670mW
Differential Input Voltage	±30V
Input Voltage	Supply Voltage
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range (Soldering, 60 sec)	300°C
Operating Temperature Range	
PM-747	−55°C to +125°C
PM-747C	0°C to +70°C

NOTE:
1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
14-Pin Hermetic DIP (Y)	83°C	10.0mW/°C

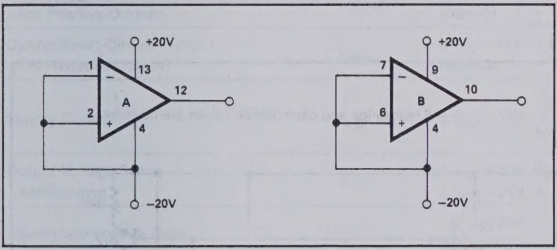
ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, $V_S = \pm 15V$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-747 MIN	PM-747 TYP	PM-747 MAX	PM-747C MIN	PM-747C TYP	PM-747C MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$	—	1.0	5.0	—	1.0	6.0	mV
Input Offset Current	I_{OS}		—	20	200	—	20	200	nA
Input Bias Current	I_B		—	80	500	—	80	500	nA
Input Resistance	R_{IN}	(Note 1)	0.3	2.0	—	0.3	2.0	—	MΩ
Input Capacitance	C_{IN}		—	1.4	—	—	1.4	—	pF
Offset Voltage Adjustment Range			—	±15	—	—	±15	—	mV
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	50	200	—	25	200	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$	±12 ±10	±14 ±13	— —	±12 ±10	±14 ±13	— —	V
Output Resistance	R_O		—	75	—	—	75	—	Ω
Output Short-Circuit Current	I_{SC}		—	25	—	—	25	—	mA
Supply Current	I_{SY}	Per Amplifier, No Load	—	1.7	2.8	—	1.7	2.8	mA
Input Voltage Range	IVR		±12	±13	—	±12	±13	—	V
Common-Mode Rejection Ratio	CMRR	$R_S \leq 10k\Omega$, $V_{CM} = \pm 10V$	70	90	—	70	90	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$ $V_S = \pm 5V$ to $\pm 18V$	— —	30 —	150 —	— —	— 30	— 150	μV/V
Power Consumption	P_d	Per Amplifier, No Load	—	50	85	—	50	85	mW
Transient Response, Unity Gain	Risetime Overshoot	$V_{IN} = 20mV$, $R_L = 2k\Omega$ $C_L \leq 100pF$	— —	0.3 5	— —	— —	0.3 5	— —	μs %
Slew Rate	SR	$R_L \geq 2k\Omega$	—	0.7	—	—	0.7	—	V/μs
Channel Separation	CS		—	120	—	—	120	—	dB

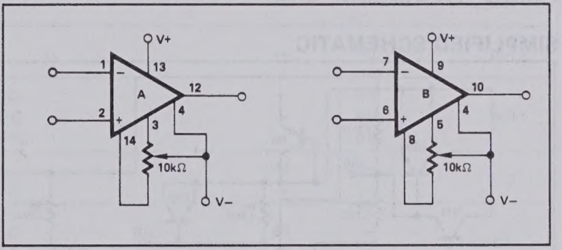
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$ for PM-747, $0°C \leq T_A \leq +70°C$ for PM-747C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-747 MIN	PM-747 TYP	PM-747 MAX	PM-747C MIN	PM-747C TYP	PM-747C MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$	—	1.0	6.0	—	1.0	7.5	mV
Input Offset Current	I_{OS}	$T_A = MAX$ $T_A = MIN$	— —	7 85	200 500	— —	7 30	200 300	nA
Input Bias Current	I_B	$T_A = MAX$ $T_A = MIN$	— —	0.03 0.3	0.5 1.5	— —	0.03 0.10	0.5 0.8	μA
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$	±12 ±10	±14 ±13	— —	±12 ±10	±14 ±13	— —	V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	25	50	—	15	25	—	V/mV
Input Voltage Range	IVR		±12	±13	—	±12	±13	—	V
Common-Mode Rejection Ratio	CMRR	$R_S \leq 10k\Omega$, $V_{CM} = \pm 10V$	70	90	—	70	90	—	dB
Power Supply Rejection Ratio	PSRR	$R_S \leq 10k\Omega$ $V_S = \pm 5V$ to $\pm 20V$ $V_S = \pm 5V$ to $\pm 18V$	— —	30 —	150 —	— —	— 30	— 150	μV/V
Supply Current	I_{SY}	$T_A = MAX$ Per Amplifier, $T_A = MIN$ No Load	— —	1.5 2.0	2.5 3.3	— —	1.5 2.0	2.5 3.3	mA
Power Consumption	P_d	$T_A = MAX$ Per Amplifier, $T_A = MIN$ No Load	— —	45 60	75 100	— —	45 60	75 100	mW
Channel Separation	CS		—	120	—	—	120	—	dB

BURN-IN CIRCUIT

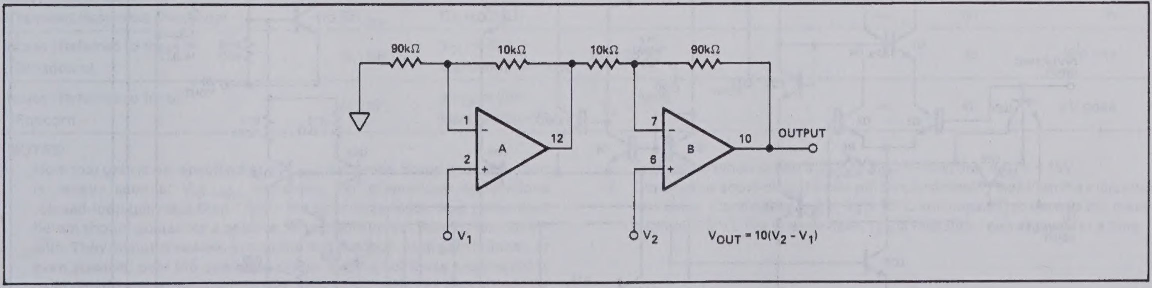

+20V
1
13
A
12
2
4
−20V
+20V
7
9
B
10
6
4
−20V

TYPICAL OFFSET NULLING CIRCUIT


V+
1
13
A
12
2
4
3
14
10kΩ
V−
V+
7
9
B
10
6
4
5
8
10kΩ
V−

TYPICAL APPLICATION

HIGH IMPEDANCE DIFFERENTIAL AMPLIFIER


90kΩ
10kΩ
10kΩ
90kΩ
1
2
A
12
7
6
B
10
OUTPUT
V1
V2
VOUT = 10(V2 - V1)

JM38510/10104 JAN SINGLE LOW-INPUT-CURRENT OPERATIONAL AMPLIFIER (EXTERNALLY COMPENSATED)

GENERAL DESCRIPTION

This data sheet covers the electrical requirements for a monolithic, low input-current, externally-compensated operational amplifier as specified in MIL-M-38510/101 for device type 04. Devices supplied to this data sheet are manufactured and tested at PMI's MIL-M-38510 certified facility and are listed in QPL-38510.

Complete device requirements will be found in MIL-M-38510 and MIL-M-38510/101 for Class B processed devices.

GENERIC CROSS-REFERENCE INFORMATION

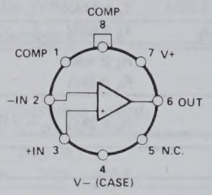
This cross-reference information is presented for the convenience of the user. The generic-industry types listed may not have identical operational performance characteristics across the military temperature range or reliability factors equivalent to the MIL-M-38510 device.

Military Device Type	Generic-Industry Type
04	LM108A

CASE OUTLINE

Per MIL-M-38510, Appendix C, Case Outline A-1 (8 Lead Can). Package Type Designator "G".

PIN CONNECTIONS AND ORDERING INFORMATION


COMP
8
COMP 1
7 V+
−IN 2
6 OUT
+IN 3
5 N.C.
4
V− (CASE)

TO-99 (J-Suffix)

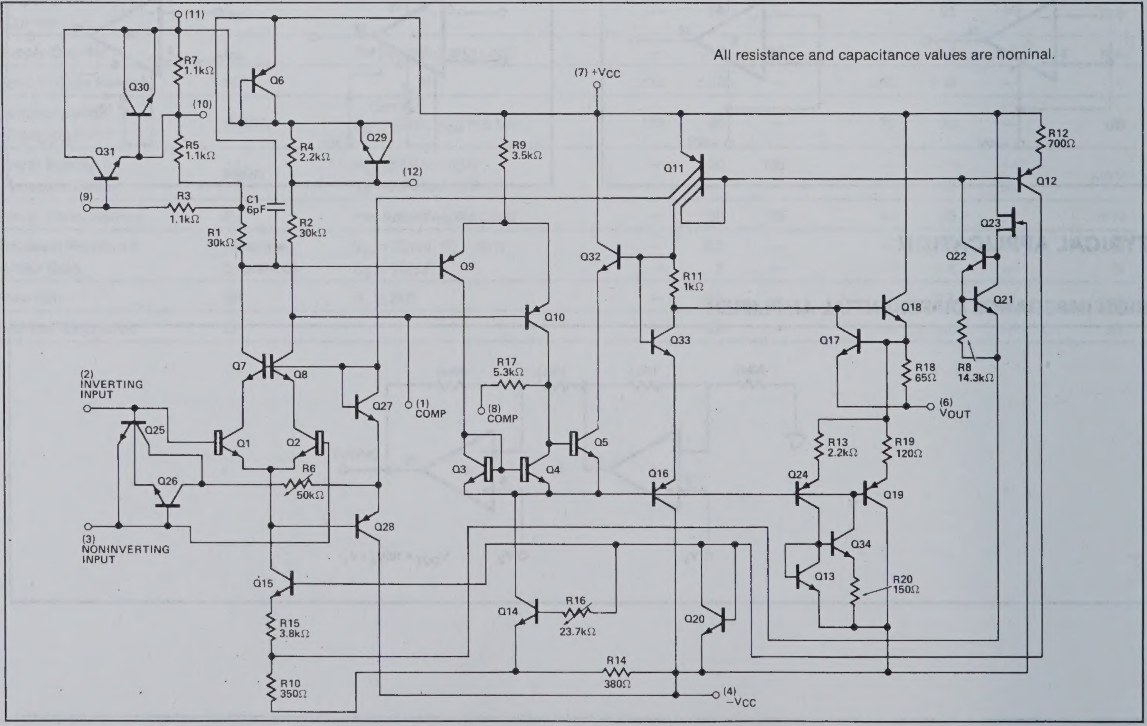
Jan Device	PMI Device Type
JM38510/10104BGC	PM108AJ1/38510

NOTE: Lead Finish: Gold Plate.
Check with factory for other qualified lead finishes.

POWER AND THERMAL CHARACTERISTICS

Package	Case outline	Maximum allowable power dissipation	Maximum $\theta J\text{—}C$	Maximum $\theta J\text{—}A$
8 Lead Can (TO-99)	G	330mW at $T_A = 125°C$	40° C/W	150° C/W

SIMPLIFIED SCHEMATIC


(11)
R7 1.1kΩ
Q30
(10)
Q31
R5 1.1kΩ
(9)
R3 1.1kΩ
C1 6pF
R1 30kΩ
Q6
R4 2.2kΩ
R2 30kΩ
Q29
(12)
R9 3.5kΩ
Q9
Q10
Q7
Q8
(2) INVERTING INPUT
Q25
Q26
Q1
Q2
R6 50kΩ
(3) NONINVERTING INPUT
Q27
(1) COMP
R17 5.3kΩ
(8) COMP
Q28
Q3
Q4
Q5
Q15
R15 3.8kΩ
R10 350Ω
Q14
R16 23.7kΩ
R14 380Ω
(4) −VCC
(7) +VCC
Q11
Q32
R11 1kΩ
Q33
Q16
Q20
R12 700Ω
Q12
Q23
Q22
Q21
Q18
Q17
R18 65Ω
R8 14.3kΩ
(6) VOUT
R13 2.2kΩ
R19 120Ω
Q24
Q19
Q34
Q13
R20 150Ω

All resistance and capacitance values are nominal.

ELECTRICAL CHARACTERISTICS at $5V \le \pm V_{CC} \le 20V$ and $-55°C \le T_A \le +125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Input Offset Voltage	V_{IO}	(Note 2) $T_A = 25°C$	−0.5	+0.5	mV
		$R_S = 50\Omega$ $-55°C \le T_A \le 125°C$	−1.0	+1.0	
Input Offset Voltage Temperature Sensitivity	$\frac{\Delta V_{IO}}{\Delta T}$	ΔT_A from −55°C to +25°C	−5.0	+5.0	µV/°C
		ΔT_A from +25°C to +125°C	−5.0	+5.0	
Input Offset Current	I_{IO}	(Note 2) $T_A = 25°C$	−0.2	+0.2	nA
		$-55°C \le T_A \le 125°C$	−0.4	+0.4	
Input Offset Current Temperature Sensitivity	$\frac{\Delta I_{IO}}{\Delta T}$	ΔT_A from −55°C to +25°C	−2.5	+2.5	pA/°C
		ΔT_A from +25°C to +125°C	−2.5	+2.5	
Input Bias Current	$+I_{IB}$	(Note 2) $25°C \le T_A \le 125°C$	−0.1	+2.0	nA
		$-55°C \le T_A \le +25°C$	−0.1	+3.0	
	$-I_{IB}$	(Note 2) $25°C \le T_A \le 125°C$	−0.1	+2.0	nA
		$-55°C \le T_A \le +25°C$	−0.1	+3.0	
Power Supply Rejection Ratio	+PSRR	$+V_{CC} = 10V$ $-V_{CC} = 20V$ $R_S = 50\Omega$ $T_A = 25°C$	−16	+16	µV/V
		$-55°C \le T_A$ 125°C	−16	+16	
Power Supply Rejection Ratio	−PSRR	$+V_{CC} = 20V$ $-V_{CC} = -10V$ $R_S = 50\Omega$ $T_A = 25°C$	−16	+16	µV/V
		$-55°C \le T_A \le 125°C$	−16	+16	
Input Voltage Common-Mode Rejection	CMR	$\pm V_{CC} = 20V$ $V_{IN} = \pm 15V$ $R_S = 50\Omega$	96	—	dB
Adjustment For Input Offset Voltage	V_{IO} ADJ (+)	$\pm V_{CC} = 20V$	No External Adjustment		mV
Adjustment For Input Offset Voltage	V_{IO} ADJ (−)	$\pm V_{CC} = 20V$	No External Adjustment		mV
Output Short-Circuit Current (For Positive Output)	$I_{OS(+)}$	$\pm V_{CC} = 15V$ $t \le 25ms$ (Note 3)	15	—	mA
Output Short-Circuit Current (For Negative Output)	$I_{OS(-)}$	$\pm V_{CC} = 15V$ $t \le 25ms$ (Note 3)	—	15	mA
Supply Current	I_{CC}	$\pm V_{CC} = 15V$ $T_A = -55°C$	—	0.8	mA
		$T_A = +25°C$	—	0.6	
		$T_A = +125°C$	—	0.6	
Output Voltage Swing (Maximum)	V_{OP}	$\pm V_{CC} = 20V$, $R_L = 10k\Omega$	±16	—	V
		$\pm V_{CC} = 20V$, $R_L = 2k\Omega$	—	—	
Open-Loop Voltage Gain (Single Ended) (Note 1)	$A_{VS(\pm)}$	$\pm V_{CC} = 20V$ $R_L = 10k\Omega$ $V_{OUT} = \pm 15V$ $T_A = 25°C$	80	—	V/mV
		$-55°C \le T_A \le 125°C$	40	—	
Open-Loop Voltage Gain (Single Ended) (Note 1)	A_{VS}	$\pm V_{CC} = 5V$ $R_L = 10k\Omega$ $V_{OUT} = \pm 2V$	20	—	V/mV
Transient Response Rise Time	$TR_{(tr)}$	$C_F = 10pF$	—	1000	nsec
Transient Response Overshoot	$TR_{(OS)}$	$C_F = 10pF$	—	50	%
Noise (Referred to Input) Broadband	N_I (BB)	$V_{CC} = 20V$ Bandwidth = 5kHz $T_A = 25°C$	—	15	µV rms
Noise (Referred to Input) Popcorn	N_I (PC)	$\pm V_{CC} = 20V$ Bandwidth = 5kHz $T_A = 25°C$	—	40	µV peak

NOTES:

1. Note that gain is not specified at $V_{IO(ADJ)}$ extremes. Some gain reduction is usually seen at $V_{IO(ADJ)}$ extremes. For closed-loop applications (closed-loop gain less than 1,000), the open-loop tests (A_{VS}) prescribed herein should guarantee a positive, reasonably linear, transfer characteristic. They do not, however, guarantee that the open-loop gain is linear, or even positive, over the operating range. If either of these requirements exist (positive open-loop gain or open-loop gain linearity), they should be specified in the individual procurement document as additional requirements.
2. Tests at common-mode $V_{CM} = 0$, $V_{CM} = -15V$, and $V_{CM} = +15V$.
3. Continuous short-circuit limits will be considerably less than the indicated test limits. Continuous I_{OS} at $T_A \le 75°C$ will cause T_j to exceed the maximum of 175°C. For dual devices, I_{OS} is measured one channel at a time.

ELECTRICAL CHARACTERISTICS at $5V \leq \pm V_{CC} \leq 20V$ and $-55°C \leq T_A \leq +125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
Slew Rate	SR (+)	$A_V = 1$	$-55°C \leq T_A \leq 25°C$	0.05	—	V/μsec
		$V_{IN} = +5V$	$T_A = 125°C$	0.05	—	
Slew Rate	SR (−)	$A_V = 1$	$-55°C \leq T_A \leq 25°C$	0.05	—	V/μsec
		$V_{IN} = \pm 5V$	$T_A = 125°C$	0.05	—	
Settling Time	t_S (+)	$T_A = 25°C$		—	—	ns
		$-55°C \leq T_A \leq 125°C$		—	—	
	t_S (−)	$T_A = 25°C$		—	—	ns
		$-55°C \leq T_A \leq 125°C$		—	—	

NOTES:

1. Note that gain is not specified at $V_{IO\,(ADJ)}$ extremes. Some gain reduction is usually seen at $V_{IO\,(ADJ)}$ extremes. For closed-loop applications (closed-loop gain less than 1,000), the open-loop tests (A_{VS}) prescribed herein should guarantee a positive, reasonably linear, transfer characteristic. They do not, however, guarantee that the open-loop gain is linear, or even positive, over the operating range. If either of these requirements exist (positive open-loop gain or open-loop gain linearity). they should be specified in the individual procurement document as additional requirements.
2. Tests at common-mode $V_{CM} = 0$, $V_{CM} = -15V$, and $V_{CM} = +15V$.
3. Continuous short-circuit limits will be considerably less than the indicated test limits. Continuous I_{OS} at $T_A \leq 75°C$ will cause T_j to exceed the maximum of 175°C. For dual devices, I_{OS} is measured one channel at a time.

For Test Circuit Diagrams, See MIL-M-38510/101

JAN JFET-INPUT OPERATIONAL AMPLIFIERS

JM38510/11401/11402/11403 11404/11405/11406

GENERAL DESCRIPTION

This data sheet covers the electrical requirements for a monolithic, low-power, internally compensated BIFET operational amplifier as specified in MIL-M-38510/114 for device types 01 to 06. Devices supplied to this data sheet are manufactured and tested at PMI's MIL-M-38510 certified facility and are listed in QPL-38510.

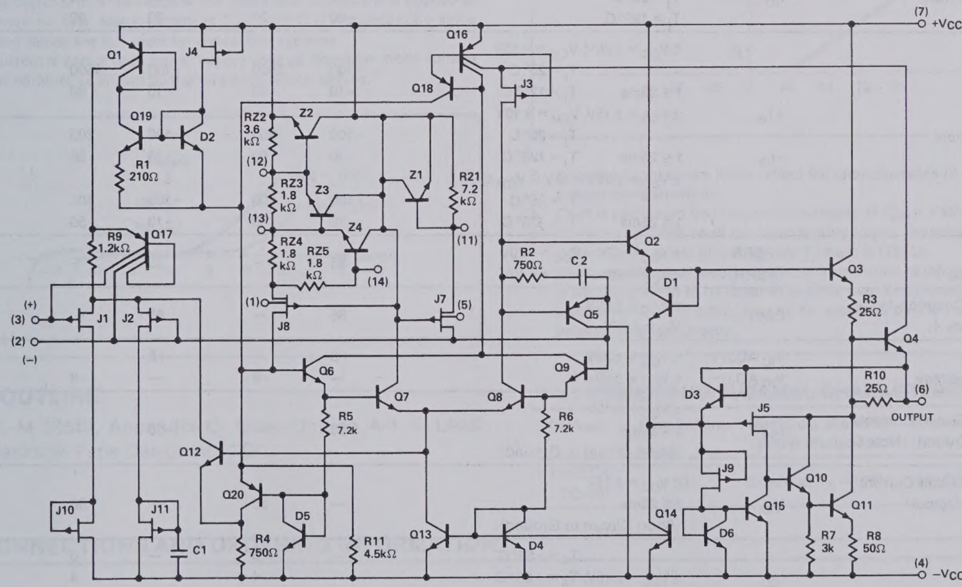
Complete device requirements will be found in MIL-M-38510 and MIL-M-38510/114 for Class B processed devices.

GENERIC CROSS-REFERENCE INFORMATION

This cross-reference information is presented for the convenience of the user. The generic-industry types listed may not have identical operational performance characteristics across the military temperature range or reliability factors equivalent to the MIL-M-38510 device.

Military Device Type	Generic-Industry Type
01	LF-155
04	LF-155A
02	LF-156
05	LF-156A
03	LF-157
06	LF-157A

SIMPLIFIED SCHEMATIC


(7)
+VCC
Q16
Q1
J4
Q18
J3
Q19
D2
RZ2 3.6 kΩ
Z2
R1 210Ω
(12)
Z1
R21 7.2 kΩ
RZ3 1.8 kΩ
Z3
(13)
(11)
Z4
R9 1.2kΩ
Q17
RZ4 1.8 kΩ
RZ5 1.8 kΩ
(14)
Q2
R2 750Ω
C2
Q3
D1
(+)
(3)
J1
J2
(1)
J8
J7
(5)
Q5
R3 25Ω
(2)
(–)
Q4
Q6
Q9
Q7
Q8
D3
R10 25Ω
(6)
OUTPUT
R5 7.2k
R6 7.2k
J5
Q12
J9
Q10
Q20
J10
J11
D5
Q15
Q11
Q14
C1
R4 750Ω
R11 4.5kΩ
Q13
D4
D6
R7 3k
R8 50Ω
(4)
–VCC

NOTE: For values of C1, C2, R5, R6 see the following table:

	01 04 02 05	03 06
C1	7pF	1.7pF
C2	7pF	1.7pF
R5	7.2kΩ	3.6kΩ
R6	7.2kΩ	3.6kΩ

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range	±22V
Input Voltage Range (Note 1)	±20V
Differential Input Voltage Range	±40V
Lead Temperature (Soldering, 60 sec)	300°C
Junction Temperature	T_j = 175°C (Note 3)
Storage Temperature Range	−65°C to +150°C
Output Short-Circuit Duration	Unlimited (Note 2)

NOTES:

1. The absolute maximum negative input voltage is equal to the negative power supply voltage.
2. Short circuit may be to ground to either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.
3. For short-term test (in the specific burn-in and life test configuration when required and up to 168 hours maximum), T_j = 275°C.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range	±5 to ±20 VDC
Ambient Temperature Range	−55°C to +125°C

ELECTRICAL CHARACTERISTICS at V_{CC} from ±5V to ±20V; source resistance = 50 ohm; ambient temperature range = −55°C to +125°C and figure 1, unless otherwise noted.

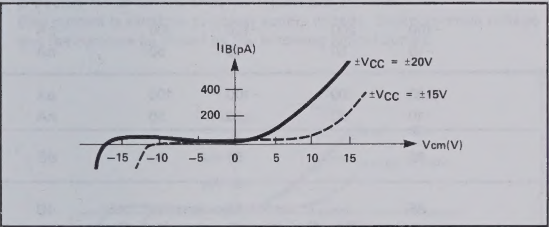
			01 LIMITS		04 LIMITS		
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**
Input Offset Voltage	V_{IO}	$\pm V_{CC} = \pm 5V$, $V_{CM} = 0V$ $T_A = 25°C$	−5	5	−2	2	mV
		$\pm V_{CC} = \pm 20V$ $V_{CM} = \pm 15V$, 0V $-55°C \le T_A \le +125°C$	−7	7	−2.5	2.5	
Input Offset Voltage Temperature Sensitivity	$\frac{\Delta V_{IO}}{\Delta T}$	$\pm V_{CC} = \pm 20V$ $V_{CM} = 0V$	−30	30	−10	10	µV/°C
Input Offset Current	I_{IO}	$\pm V_{CC} = \pm 20V$, $V_{CM} = 0V$, $T_j = 25°C$	−20	20	−20	20	pA
		$T_j = 125°C$	−20	20	−20	20	nA
Input Bias Current (Note 1) (Note 2) (Note 3)	$+I_{IB}$ $-I_{IB}$	$\pm V_{CC} = \pm 20V$, $V_{CM} = +15V$ $T_j = 25°C$	−100	3500	−100	3500	pA
		$t \le 25ms$ $T_j = 125°C$	−10	60	−10	60	nA
		$\pm V_{CC} = \pm 15V$, $V_{CM} = +10V$ $T_j = 25°C$	−100	300	−100	300	pA
		$t \le 25ms$ $T_j = 125°C$	−10	50	−10	50	nA
		$\pm V_{CC} = \pm 20V$, $-15V \le V_{CM} \le 0V$ $T_j = 25°C$	−100	100	−100	100	pA
		$t \le 25ms$ $T_j = 125°C$	−10	50	−10	50	nA
Power Supply Rejection Ratio	+PSRR −PSRR	$+V_{CC} = 10V$, $-V_{CC} = -20V$ $+V_{CC} = 20V$, $-V_{CC} = -10V$	85	—	85	—	dB
Input Voltage Common-Mode Rejection (Note 4)	CMR	$\pm V_{CC} = \pm 20V$ $V_{IN} = \pm 15V$	85	—	85	—	dB
Adjustment for Input Offset Voltage	V_{IO} ADJ(+)	$\pm V_{CC} = \pm 20V$	+8	—	+8	—	mV
	V_{IO} ADJ(−)	$\pm V_{CC} = \pm 20V$	—	−8	—	−8	
Output Short Circuit Current (for Positive Output) (Note 5)	$I_{OS(+)}$	$\pm V_{CC} = \pm 15V$ $t \le 25ms$ (Short Circuit to Ground)	−50	—	−50	—	mA
Output Short Circuit Current (for Negative Output) (Note 5)	$I_{OS(-)}$	$\pm V_{CC} = \pm 15V$ $t \le 25ms$ (Short Circuit to Ground)	—	50	—	50	mA
Supply Current	I_{CC}	$T_A = -55°C$	—	6	—	6	mA
		$\pm V_{CC} = \pm 15V$, $T_A = +25°C$	—	4	—	4	
		$T_A = +125°C$	—	4	—	4	
Output Voltage Swing (Maximum)	V_{OP}	$\pm V_{CC} = \pm 20V$, $R_L = 10k\Omega$	±16	—	±16	—	V
		$\pm V_{CC} = \pm 20V$, $R_L = 2k\Omega$	±15	—	±15	—	
Open-Loop Voltage Gain (Single Ended) (Note 6)	$A_{VS(+)}$ $A_{VS(-)}$	$\pm V_{CC} = \pm 20V$, $V_{OUT} = \pm 15V$ $R_L = 2k\Omega$, $T_A = 25°C$	50	—	50	—	V/mV
		$-55°C \le T_A \le +125°C$	25	—	25	—	
Open-Loop Voltage Gain (Single Ended) (Note 6)	A_{VS}	$\pm V_{CC} = \pm 5V$ $R_L = 2k\Omega$ $V_{OUT} = \pm 2V$	10	—	10	—	V/mV

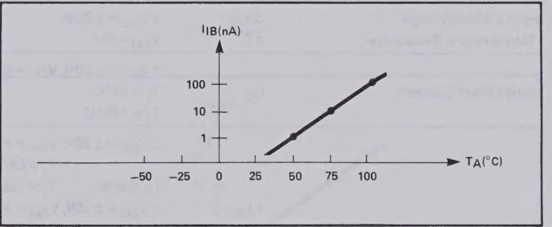
ELECTRICAL CHARACTERISTICS at V_{CC} from ±5V to ±20V; source resistance = 50 ohm; ambient temperature range = −55° C to +125° C and figure 1, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	01 LIMITS MIN	01 LIMITS MAX	04 LIMITS MIN	04 LIMITS MAX	UNITS
Transient Response Rise Time	$TR_{(tr)}$	$\pm V_{CC} = \pm 15V$, $R_L = 2k\Omega$, $A_V = 1$ $C_L = 100pF$, See Figure 2 $V_{IN} = 50mV$	—	150	—	150	ns
Transient Response Overshoot	$TR_{(os)}$	$\pm V_{CC} = \pm 15V$, $R_L = 2k\Omega$, $A_V = 1$ $C_L = 100pF$, See Figure 2 $V_{IN} = 50mV$	—	40	—	40	%
Slew Rate	SR(+) and SR(−)	$V_{IN} = \pm 5V$, $\pm V_{CC} = \pm 15V$ $A_V = 1$, See Figure 2 $T_A = 25° C$	2	—	3	—	V/μs
		$T_A = -55° C, +125° C$	1	—	1.5	—	
Settling Time	ts(+) and ts(−)	$\pm V_{CC} = \pm 15V$ (0.1% error) $T_A = 25° C$, $A_V = -1$ See Figure 3	—	1500	—	1500	ns
Noise (Referred to Input) Broadband	$N_I(BB)$	$\pm V_{CC} = \pm 20V$, $T_A = 25° C$ Bandwidth = 5kHz	—	10	—	10	μV_{rms}
Noise (Referred to Input) Popcorn	$N_I(PC)$	$\pm V_{CC} = \pm 20V$, $T_A = 25° C$ Bandwidth = 5kHz	—	80	—	80	μV_{pk}

NOTES:

1. Bias currents are actually junction leakage currents which double (approximately) for each 10° C increase in junction temperature T_j. Measurement of bias current is specified at T_j rather than T_A, since normal warm-up thermal transients will affect the bias currents. The measurements for bias currents must be made within 25ms after power is first applied to the device for test. Measurement at $T_A = -55° C$ is not necessary since expected values are too small for typical test systems.
2. Bias current is sensitive to power supply voltage, common-mode voltage and temperature as shown by the following typical curves:





3. Negative I_{IB} minimum limits reflect the characteristics of device with bias current compensation.
4. CMR is calculated from V_{IO} measurements at $V_{CM} = +15V$ and −15V.
5. Continuous limits shall be considerably lower. Protection for shorts to either supply exists providing that $T_j(max) \leq 175° C$.
6. Because of thermal feedback effects from output to input, open-loop gain is not guaranteed to be linear or positive over the operating range. These requirements, if needed, should be specified by the user in additional procurement documents.

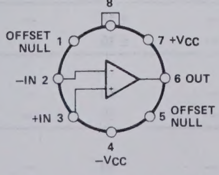
CASE OUTLINE

Per MIL-M-38510, Appendix C, Case Outline A-1 (8 Lead Can). Package Type Designator "G".

POWER AND THERMAL CHARACTERISTICS

Package	Case outline	Maximum allowable power dissipation	Maximum θJ—C	Maximum θJ—A
8 Lead Can (TO-99)	G	330mW at $T_A = 125° C$	40° C/W	150° C/W

PIN CONNECTIONS AND ORDERING INFORMATION



(PIN 4 CONNECTED TO CASE)

Jan Device	PMI Device Type
JM38510/11401BGC	PM155J1/38510
JM38510/11404BGC	PM155AJ1/38510
JM38510/11402BGC	PM156J1/38510
JM38510/11405BGC	PM156AJ1/38510
JM38510/11403BGC	PM157J1/38510
JM38510/11406BGC	PM157AJ1/38510

NOTE: Lead Finish-Gold Plate.
Check with factory for other qualified lead finishes.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range	±22V
Input Voltage Range (Note 1)	±20V
Differential Input Voltage Range	±40V
Lead Temperature (Soldering, 60 sec)	300°C
Junction Temperature	$T_j = 175°C$ (Note 3)
Storage Temperature Range	−65°C to +150°C
Output Short-Circuit Duration	Unlimited (Note 2)

NOTES:

1. The absolute maximum negative input voltage is equal to the negative power supply voltage.
2. Short circuit may be to ground to either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.
3. For short-term test (in the specific burn-in and life test configuration when required and up to 168 hours maximum), $T_j = 275°C$.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range	±5 to ±20 VDC
Ambient Temperature Range	−55°C to +125°C

ELECTRICAL CHARACTERISTICS at V_{CC} from ±5V to ±20V; source resistance = 50 ohm; ambient temperature range = −55°C to +125°C and figure 1, unless otherwise noted.

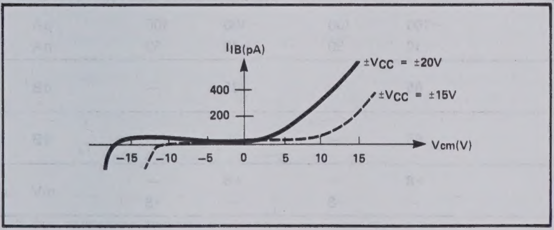
PARAMETER	SYMBOL	CONDITIONS	02 LIMITS MIN	02 LIMITS MAX	05 LIMITS MIN	05 LIMITS MAX	UNITS
Input Offset Voltage	V_{IO}	$\pm V_{CC} = \pm 5V$, $V_{CM} = 0V$ $T_A = 25°C$	−5	5	−2	2	mV
		$\pm V_{CC} = \pm 20V$ $V_{CM} = \pm 15V$, 0V $-55°C \le T_A \le +125°C$	−7	7	−2.5	2.5	
Input Offset Voltage Temperature Sensitivity	$\frac{\Delta V_{IO}}{\Delta T}$	$\pm V_{CC} = \pm 20V$ $V_{CM} = 0V$	−30	30	−10	10	µV/°C
Input Offset Current	I_{IO}	$\pm V_{CC} = \pm 20V$, $V_{CM} = 0V$, $T_j = 25°C$	−20	20	−20	20	pA
		$T_j = 125°C$	−20	20	−20	20	nA
Input Bias Current (Note 1) (Note 2) (Note 3)		$\pm V_{CC} = \pm 20V$, $V_{CM} = +15V$ $T_j = 25°C$	−100	3500	−100	3500	pA
		$t \le 25ms$ $T_j = 125°C$	−10	60	−10	60	nA
	$+I_{IB}$	$\pm V_{CC} = \pm 15V$, $V_{CM} = +10V$ $T_j = 25°C$	−100	300	−100	300	pA
	$-I_{IB}$	$t \le 25ms$ $T_j = 125°C$	−10	50	−10	50	nA
		$\pm V_{CC} = \pm 20V$, $-15V \le V_{CM} \le 0V$ $T_j = 25°C$	−100	100	−100	100	pA
		$t \le 25ms$ $T_j = 125°C$	−10	50	−10	50	nA
Power Supply Rejection Ratio	$+PSRR$ $-PSRR$	$+V_{CC} = 10V$, $-V_{CC} = -20V$ $+V_{CC} = 20V$, $-V_{CC} = -10V$	85	—	85	—	dB
Input Voltage Common-Mode Rejection (Note 4)	CMR	$\pm V_{CC} = \pm 20V$ $V_{IN} = \pm 15V$	85	—	85	—	dB
Adjustment for Input Offset Voltage	V_{IO} ADJ (+)	$\pm V_{CC} = \pm 20V$	+8	—	+8	—	mV
	V_{IO} ADJ (−)	$\pm V_{CC} = \pm 20V$	—	−8	—	−8	
Output Short Circuit Current (for Positive Output) (Note 5)	$I_{OS(+)}$	$\pm V_{CC} = \pm 15V$ $t \le 25ms$ (Short Circuit to Ground)	−50	—	−50	—	mA
Output Short Circuit Current (for Negative Output) (Note 5)	$I_{OS(-)}$	$\pm V_{CC} = \pm 15V$ $t \le 25ms$ (Short Circuit to Ground)	—	50	—	50	mA
Supply Current	I_{CC}	$T_A = -55°C$	—	11	—	11	mA
		$\pm V_{CC} = \pm 15V$, $T_A = +25°C$	—	7	—	7	
		$T_A = +125°C$	—	7	—	7	
Output Voltage Swing (Maximum)	V_{OP}	$\pm V_{CC} = \pm 20V$, $R_L = 10k\Omega$	±16	—	±16	—	V
		$\pm V_{CC} = \pm 20V$, $R_L = 2k\Omega$	±15	—	±15	—	
Open-Loop Voltage Gain (Single Ended) (Note 6)	$A_{VS(+)}$ $A_{VS(-)}$	$\pm V_{CC} = \pm 20V$, $V_{OUT} = \pm 15V$ $R_L = 2k\Omega$, $T_A = 25°C$	50	—	50	—	V/mV
		$-55°C \le T_A \le +125°C$	25	—	25	—	
Open-Loop Voltage Gain (Single Ended) (Note 6)	A_{VS}	$\pm V_{CC} = \pm 5V$ $R_L = 2k\Omega$ $V_{OUT} = \pm 2V$	10	—	10	—	V/mV

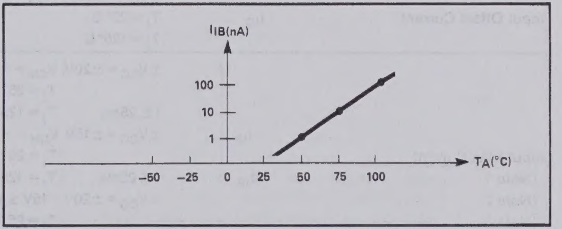
ELECTRICAL CHARACTERISTICS at V_{CC} from ±5V to ±20V; source resistance = 50 ohm; ambient temperature range = −55° C to +125° C and figure 1, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	02 LIMITS MIN	02 LIMITS MAX	05 LIMITS MIN	05 LIMITS MAX	UNITS
Transient Response Rise Time	$TR_{(tr)}$	$\pm V_{CC} = \pm 15V$, $R_L = 2k\Omega$, $A_V = 1$ $C_L = 100pF$, See Figure 2 $V_{IN} = 50mV$	—	100	—	100	ns
Transient Response Overshoot	$TR_{(os)}$	$\pm V_{CC} = \pm 15V$, $R_L = 2k\Omega$, $A_V = 1$ $C_L = 100pF$, See Figure 2 $V_{IN} = 50mV$	—	40	—	40	%
Slew Rate	SR(+) and SR(−)	$V_{IN} = \pm 5V$, $\pm V_{CC} = \pm 15V$ $A_V = 1$, See Figure 2 $T_A = 25° C$ $T_A = -55° C, +125° C$	7.5 5	— —	10 7	— —	V/μs
Settling Time	ts(+) and ts(−)	$\pm V_{CC} = \pm 15V$ (0.1% error) $T_A = 25° C$, $A_V = -1$ See Figure 3	—	1500	—	1500	ns
Noise (Referred to Input) Broadband	$N_I(BB)$	$\pm V_{CC} = \pm 20V$, $T_A = 25° C$ Bandwidth = 5kHz	—	10	—	10	μV_{rms}
Noise (Referred to Input) Popcorn	$N_I(PC)$	$\pm V_{CC} = \pm 20V$, $T_A = 25° C$ Bandwidth = 5kHz	—	80	—	80	μV_{pk}

NOTES:

1. Bias currents are actually junction leakage currents which double (approximately) for each 10°C increase in junction temperature T_j. Measurement of bias current is specified at T_j rather than T_A, since normal warm-up thermal transients will affect the bias currents. The measurements for bias currents must be made within 25ms after power is first applied to the device for test. Measurement at $T_A = -55° C$ is not necessary since expected values are too small for typical test systems.
2. Bias current is sensitive to power supply voltage, common-mode voltage and temperature as shown by the following typical curves:





3. Negative I_{IB} minimum limits reflect the characteristics of device with bias current compensation.
4. CMR is calculated from V_{IO} measurements at $V_{CM} = +15V$ and $-15V$.
5. Continuous limits shall be considerably lower. Protection for shorts to either supply exists providing that $T_j(max) \leq 175° C$.
6. Because of thermal feedback effects from output to input, open-loop gain is not guaranteed to be linear or positive over the operating range. These requirements, if needed, should be specified by the user in additional procurement documents.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range	±22V
Input Voltage Range (Note 1)	±20V
Differential Input Voltage Range	±40V
Lead Temperature (Soldering, 60 sec)	300°C
Junction Temperature	T_j = 175°C (Note 3)
Storage Temperature Range	−65°C to +150°C
Output Short-Circuit Duration	Unlimited (Note 2)

NOTES:

1. The absolute maximum negative input voltage is equal to the negative power supply voltage.
2. Short circuit may be to ground to either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.
3. For short-term test (in the specific burn-in and life test configuration when required and up to 168 hours maximum), T_j = 275°C.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range	±5 to ±20 VDC
Ambient Temperature Range	−55°C to +125°C

ELECTRICAL CHARACTERISTICS at V_{CC} from ±5V to ±20V; source resistance = 50 ohm; ambient temperature range = −55°C to +125°C and figure 1, unless otherwise noted.

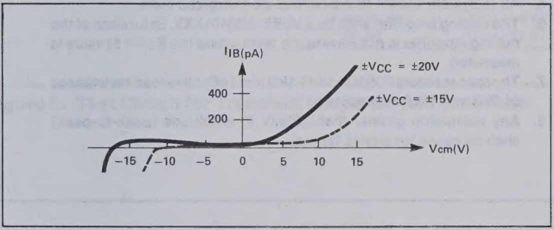
PARAMETER	SYMBOL	CONDITIONS	03 LIMITS MIN	03 LIMITS MAX	06 LIMITS MIN	06 LIMITS MAX	UNITS
Input Offset Voltage	V_{IO}	$\pm V_{CC} = \pm 5V$, $V_{CM} = 0V$ $T_A = 25°C$	−5	5	−2	2	mV
		$\pm V_{CC} = \pm 20V$ $V_{CM} = \pm 15V, 0V$ $-55°C \le T_A \le +125°C$	−7	7	−2.5	2.5	mV
Input Offset Voltage Temperature Sensitivity	$\frac{\Delta V_{IO}}{\Delta T}$	$\pm V_{CC} = \pm 20V$ $V_{CM} = 0V$	−30	30	−10	10	μV/°C
Input Offset Current	I_{IO}	$\pm V_{CC} = \pm 20V$, $V_{CM} = 0V$, $T_j = 25°C$	−20	20	−20	20	pA
		$T_j = 125°C$	−20	20	−20	20	nA
Input Bias Current (Note 1) (Note 2) (Note 3)	$+I_{IB}$ $-I_{IB}$	$\pm V_{CC} = \pm 20V$, $V_{CM} = +15V$ $T_j = 25°C$	−100	3500	−100	3500	pA
		$t \le 25ms$ $T_j = 125°C$	−10	60	−10	60	nA
		$\pm V_{CC} = \pm 15V$, $V_{CM} = +10V$ $T_j = 25°C$	−100	300	−100	300	pA
		$t \le 25ms$ $T_j = 125°C$	−10	50	−10	50	nA
		$\pm V_{CC} = \pm 20V$, $-15V \le V_{CM} \le 0V$ $T_j = 25°C$	−100	100	−100	100	pA
		$t \le 25ms$ $T_j = 125°C$	−10	50	−10	50	nA
Power Supply Rejection Ratio	+PSRR −PSRR	$+V_{CC} = 10V$, $-V_{CC} = -20V$ $+V_{CC} = 20V$, $-V_{CC} = -10V$	85	—	85	—	dB
Input Voltage Common-Mode Rejection (Note 4)	CMR	$\pm V_{CC} = \pm 20V$ $V_{IN} = \pm 15V$	85	—	85	—	dB
Adjustment for Input Offset Voltage	V_{IO} ADJ (+)	$\pm V_{CC} = \pm 20V$	+8	—	+8	—	mV
	V_{IO} ADJ (−)	$\pm V_{CC} = \pm 20V$	—	−8	—	−8	mV
Output Short Circuit Current (for Positive Output) (Note 5)	$I_{OS(+)}$	$\pm V_{CC} = \pm 15V$ $t \le 25ms$ (Short Circuit to Ground)	−50	—	−50	—	mA
Output Short Circuit Current (for Negative Output) (Note 5)	$I_{OS(-)}$	$\pm V_{CC} = \pm 15V$ $t \le 25ms$ (Short Circuit to Ground)	—	50	—	50	mA
Supply Current	I_{CC}	$\pm V_{CC} = \pm 15V$, $T_A = -55°C$	—	11	—	11	mA
		$T_A = +25°C$	—	7	—	7	mA
		$T_A = +125°C$	—	7	—	7	mA
Output Voltage Swing (Maximum)	V_{OP}	$\pm V_{CC} = \pm 20V$, $R_L = 10k\Omega$	±16	—	±16	—	V
		$\pm V_{CC} = \pm 20V$, $R_L = 2k\Omega$	±15	—	±15	—	V
Open-Loop Voltage Gain (Single Ended) (Note 6)	$A_{VS(+)}$ $A_{VS(-)}$	$\pm V_{CC} = \pm 20V$, $V_{OUT} = \pm 15V$ $R_L = 2k\Omega$, $T_A = 25°C$	50	—	50	—	V/mV
		$-55°C \le T_A \le +125°C$	25	—	25	—	V/mV
Open-Loop Voltage Gain (Single Ended) (Note 6)	A_{VS}	$\pm V_{CC} = \pm 5V$ $R_L = 2k\Omega$ $V_{OUT} = \pm 2V$	10	—	10	—	V/mV

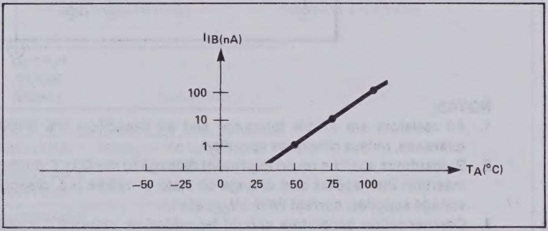
ELECTRICAL CHARACTERISTICS at V_{CC} from ±5V to ±20V; source resistance = 50 ohm; ambient temperature range = −55° C to +125° C and figure 1, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	03 LIMITS MIN	03 LIMITS MAX	06 LIMITS MIN	06 LIMITS MAX	UNITS
Transient Response Rise Time	$TR_{(tr)}$	$\pm V_{CC} = \pm 15V$, $R_L = 2k\Omega$, $A_V = 5$ $C_L = 100pF$, See Figure 2 $V_{IN} = 50mV$	—	450	—	450	ns
Transient Response Overshoot	$TR_{(os)}$	$\pm V_{CC} = \pm 15V$, $R_L = 2k\Omega$, $A_V = 5$ $C_L = 100pF$, See Figure 2 $V_{IN} = 50mV$	—	25	—	25	%
Slew Rate	SR(+) and SR(−)	$V_{IN} = \pm 1V$, $\pm V_{CC} = \pm 15V$ $A_V = 5$, See Figure 2 $T_A = 25°C$	30	—	40	—	V/μs
		$T_A = -55°C, +125°C$	20	—	25	—	
Settling Time	ts(+) and ts(−)	$\pm V_{CC} = \pm 15V$ (0.1% error) $T_A = 25°C$, $A_V = -5$ See Figure 3	—	800	—	800	ns
Noise (Referred to Input) Broadband	$N_I(BB)$	$\pm V_{CC} = \pm 20V$, $T_A = 25°C$ Bandwidth = 5kHz	—	10	—	10	μV_{rms}
Noise (Referred to Input) Popcorn	$N_I(PC)$	$\pm V_{CC} = \pm 20V$, $T_A = 25°C$ Bandwidth = 5kHz	—	80	—	80	μV_{pk}

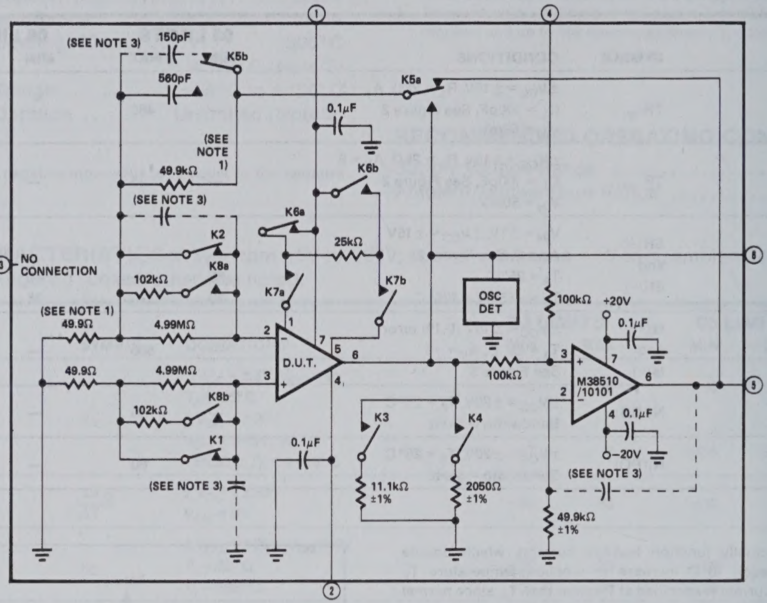
NOTES:

1. Bias currents are actually junction leakage currents which double (approximately) for each 10°C increase in junction temperature T_j. Measurement of bias current is specified at T_j rather than T_A, since normal warm-up thermal transients will affect the bias currents. The measurements for bias currents must be made within 25ms after power is first applied to the device for test. Measurement at $T_A = -55°C$ is not necessary since expected values are too small for typical test systems.
2. Bias current is sensitive to power supply voltage, common-mode voltage and temperature as shown by the following typical curves:





3. Negative I_{IB} minimum limits reflect the characteristics of device with bias current compensation.
4. CMR is calculated from V_{IO} measurements at $V_{CM} = +15V$ and −15V.
5. Continuous limits shall be considerably lower. Protection for shorts to either supply exists providing that $T_j(max) \leq 175°C$.
6. Because of thermal feedback effects from output to input, open-loop gain is not guaranteed to be linear or positive over the operating range. These requirements, if needed, should be specified by the user in additional procurement documents.

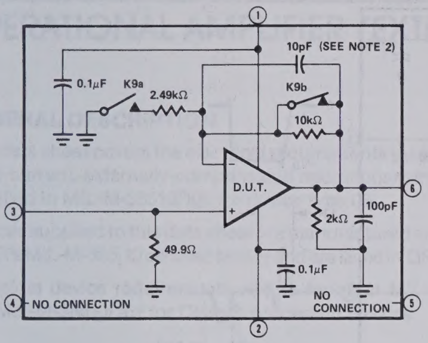


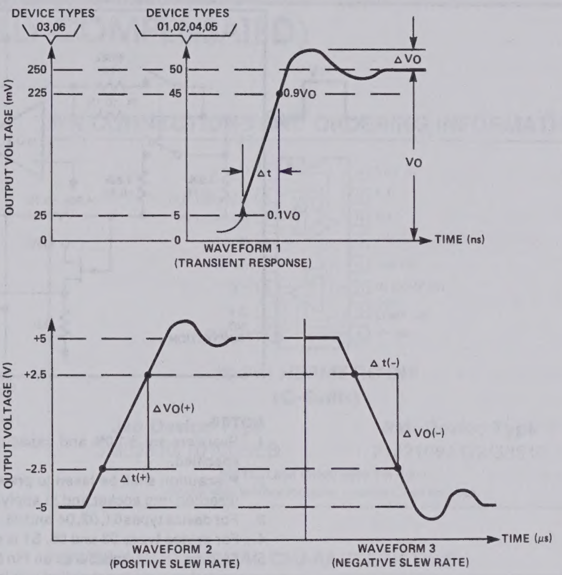
(SEE NOTE 3)
150pF
K5b
560pF
K5a
0.1μF
(SEE NOTE 1)
49.9kΩ
K6b
(SEE NOTE 3)
K6a
K2
25kΩ
NO CONNECTION
K8a
102kΩ
K7a
K7b
(SEE NOTE 1)
49.9Ω
4.99MΩ
D.U.T.
OSC DET
100kΩ
+20V
0.1μF
100kΩ
M38510 /10101
49.9Ω
4.99MΩ
K8b
102kΩ
K3
K4
0.1μF
K1
0.1μF
-20V
(SEE NOTE 3)
(SEE NOTE 3)
11.1kΩ ±1%
2050Ω ±1%
49.9kΩ ±1%
1
2
3
4
5
6
7
8

NOTES:

1. All resistors are ±0.1% tolerance and all capacitors are ±10% tolerance, unless otherwise specified.
2. Precautions shall be taken to prevent damage to the D.U.T. during insertion into socket and change of state of relays (i.e. disable voltage supplies, current limit $\pm V_{CC}$, etc.).
3. Compensation capacitors should be added as required for test circuit stability. Two general methods for stability compensation exist. One method is with a capacitor for nulling amp feedback. The other method is with a capacitor in parallel with the 49.9kΩ closed-loop feedback resistor. Both methods should not be used simultaneously. Proper wiring procedures shall be followed to prevent unwanted coupling and oscillations, etc. Loop response and settling time shall be consistent with the test rate such that any value has settled for at least five loop time constants before the value is measured.
4. Adequate settling time should be allowed such that each parameter has settled to within 5% of its final value.
5. All relays are shown in the normal de-energized state.
6. The nulling amplifier shall be a M38510/10101XXX. Saturation of the nulling amplifier is not allowed on tests where the E (Pin 5) value is measured.
7. The load resistors 2050Ω and 11.1kΩ yield effective load resistances of 2kΩ and 10kΩ respectively.
8. Any oscillation greater than 300mV in amplitude (peak-to-peak) shall be cause for device failure.

Figure 1. Test Circuit for Static Tests


①
10pF (SEE NOTE 2)
0.1μF
K9a
2.49kΩ
K9b
10kΩ
D.U.T.
⑥
③
2kΩ
100pF
49.9Ω
0.1μF
④ NO CONNECTION
NO CONNECTION
⑤
②

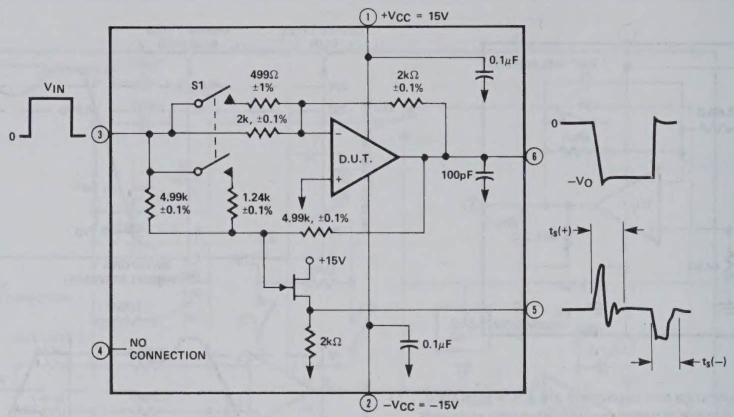

DEVICE TYPES 03,06
DEVICE TYPES 01,02,04,05
OUTPUT VOLTAGE (mV)
250
225
25
0
50
45
5
0
ΔVO
0.9VO
Δt
VO
0.1VO
TIME (ns)
WAVEFORM 1 (TRANSIENT RESPONSE)
OUTPUT VOLTAGE (V)
+5
+2.5
-2.5
-5
ΔVO(+)
Δ t(+)
Δ t(-)
Δ VO(-)
TIME (μs)
WAVEFORM 2 (POSITIVE SLEW RATE)
WAVEFORM 3 (NEGATIVE SLEW RATE)

NOTES:

1. Resistors are ±1.0% tolerance and capacitors are ±10% tolerance.
2. This capacitance includes the actual measured value with stray and wire capacitance.
3. Precautions shall be taken to prevent damage to the D.U.T. during insertion into socket and in applying power.

PARAMETER SYMBOL	DEVICE TYPE	INPUT PULSE SIGNAL AT $t_r \leq 50ns$	OUTPUT PULSE SIGNAL	EQUATION
TR (t_r)	ALL	+50mV	WAVEFORM 1	TR (t_r) = Δt
TR (O_S)	ALL	+50mV	WAVEFORM 1	TR (O_S) = 100 ($\Delta V_O/V_O$) %
SR (+)	01, 02, 04, 05 03, 06	-5V to +5V STEP -1V to +1V STEP	WAVEFORM 2 WAVEFORM 2	SR (+) = $\Delta V_O(+)/\Delta t(+)$
SR (−)	01, 02, 04, 05 03, 06	+5V to −5V STEP −1V to +1V STEP	WAVEFORM 3 WAVEFORM3	SR (−) = $\Delta V_O(-)/\Delta t(-)$

Figure 2. Test Circuit for Transient Response and Slew Rate.



① +VCC = 15V
0.1μF
VIN
S1
499Ω
±1%
2kΩ
±0.1%
2k, ±0.1%
0
③
D.U.T.
⑥
100pF
0
−VO
4.99k
±0.1%
1.24k
±0.1%
4.99k, ±0.1%
ts(+)
+15V
⑤
2kΩ
0.1μF
④ NO CONNECTION
ts(−)
② −VCC = −15V

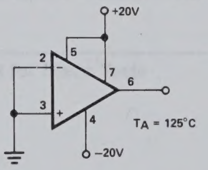
NOTES:

1. Resistors are ±1.0% and capacitors are ±10%, unless otherwise specified.
2. Precaution shall be taken to prevent damage to the D.U.T. during insertion into socket and in applying power.
3. For device types 01, 02, 04 and 05, S1 is open, $A_V = -1$ and $V_{IN} = 10V$.
4. For device types 03 and 06, S1 is closed, $A_V = -5$ and $V_{IN} = 2V$.
5. Settling time, t_s measured on Pin 5, is the interval during which the summing node is not nulled within the specified accuracy referred to the output.

Figure 3. Test Circuit for Settling Time

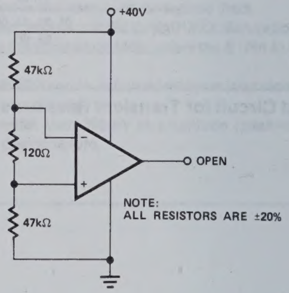
BURN-IN

Devices supplied by PMI have been subjected to burn-in per Method 1015 of MIL-STD-883 using test condition C with circuit shown on Figure 4 or test condition F using circuit shown on Figure 5.



+20V
2
5
7
6
3
4
TA = 125°C
−20V

Figure 4. Test Circuit, Burn-In (Steady-State Power and Reverse Bias) and Operating Life Test



+40V
47kΩ
120Ω
OPEN
47kΩ
NOTE:
ALL RESISTORS ARE ±20%

Figure 5. Accelerated Burn-In and Life Test Circuit

JAN DUAL
LOW-INPUT-CURRENT JM38510/10106
OPERATIONAL AMPLIFIER (EXTERNALLY COMPENSATED)

GENERAL DESCRIPTION

This data sheet covers the electrical requirements for a dual low input-current, externally-compensated operational amplifier as specified in MIL-M-38510/101 for device type 06.

Devices supplied to this data sheet are manufactured and tested at PMI's MIL-M-385]10 certified facility and are listed in QPL-38510.

Complete device requirements will be found in MIL-M-38510 and MIL-M-38510/101 for Class B processed devices.

GENERIC CROSS-REFERENCE INFORMATION

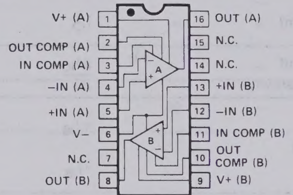
This cross-reference information is presented for the convenience of the user. The generic-industry types listed may not have identical operational performance characteristics across the military temperature range or reliability factors equivalent to the MIL-M-38510 device.

Military Device Type	Generic-Industry Type
06	LM2108A

CASE OUTLINE

Per MIL-M-38510, Appendix C, Case Outline D-2 (16-pin DIP). Package Type Designator "E".

PIN CONNECTIONS AND ORDERING INFORMATION


V+ (A)
OUT COMP (A)
IN COMP (A)
–IN (A)
+IN (A)
V–
N.C.
OUT (B)
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
OUT (A)
N.C.
N.C.
+IN (B)
–IN (B)
IN COMP (B)
OUT COMP (B)
V+ (B)
A
B

16-PIN HERMETIC DIP
(Q-Suffix)

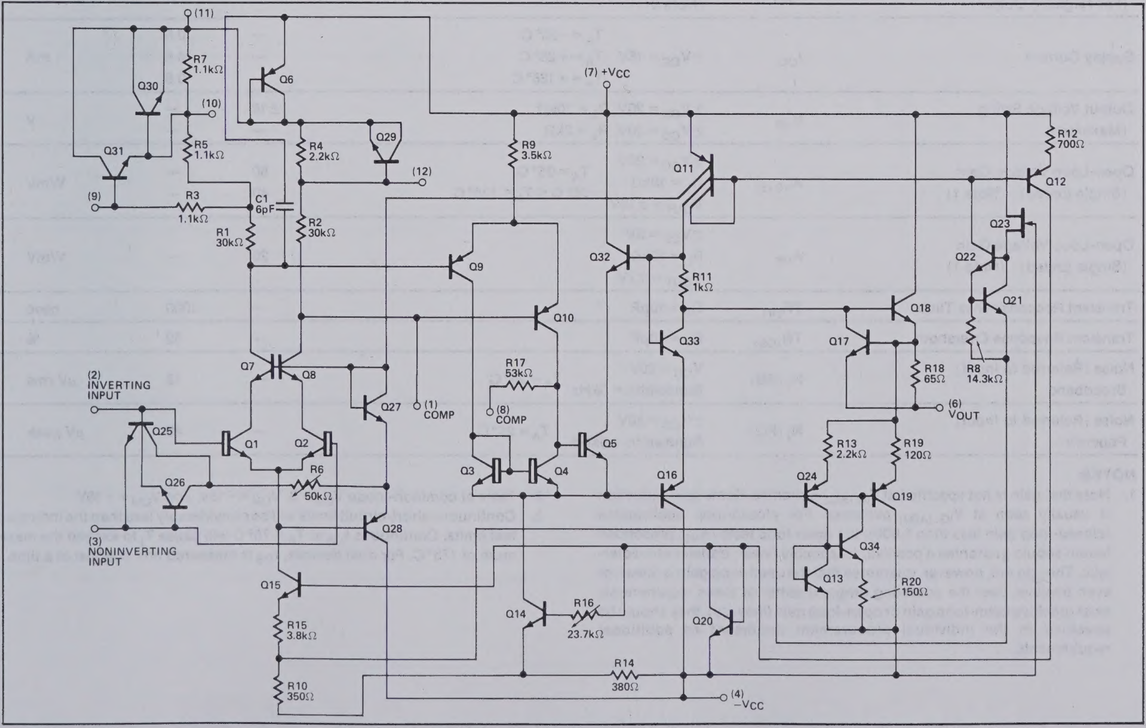
Jan Device Type	PMI Device Type
JM38510/10106BEB	PM2108AQ2/38510

NOTE: Lead finish: Acid Tin Plate
Check with factory for other qualified lead finishes.

POWER AND THERMAL CHARACTERISTICS

Package	Case outline	Maximum allowable power dissipation	Maximum θJ—C	Maximum θJ—A
Dual-in-line	E	400mW at $T_A = 125°C$	35°C/W	120°C/W

SIMPLIFIED SCHEMATIC (Each Amplifier)


(11)
R7
1.1kΩ
Q30
Q6
(10)
(7) +VCC
R5
1.1kΩ
R4
2.2kΩ
Q29
R9
3.5kΩ
R12
700Ω
Q31
(12)
Q11
Q12
(9)
R3
1.1kΩ
C1
6pF
R2
30kΩ
Q23
R1
30kΩ
Q9
Q32
R11
1kΩ
Q22
Q21
Q10
Q18
Q33
Q17
Q7
Q8
R17
53kΩ
R18
65Ω
R8
14.3kΩ
(2)
INVERTING
INPUT
Q27
(1)
COMP
(8)
COMP
(6)
VOUT
Q25
Q1
Q2
Q5
R13
2.2kΩ
R19
120Ω
Q3
Q4
Q26
R6
50kΩ
Q16
Q24
Q19
Q28
(3)
NONINVERTING
INPUT
Q34
Q15
Q13
R20
150Ω
Q14
R16
23.7kΩ
Q20
R15
3.8kΩ
R14
380Ω
R10
350Ω
(4)
–VCC

ELECTRICAL CHARACTERISTICS at $5V \leq \pm V_{CC} \leq 20V$ and $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Input Offset Voltage	V_{IO}	(Note 2) $T_A = 25^\circ C$ $R_S = 50\Omega$ $-55^\circ C \leq T_A \leq 125^\circ C$	-0.5 -1.0	+0.5 +1.0	mV
Input Offset Voltage Temperature Sensitivity	$\frac{\Delta V_{IO}}{\Delta T}$	ΔT_A from $-55^\circ C$ to $+25^\circ C$ ΔT_A from $+25^\circ C$ to $+125^\circ C$	-5.0 -5.0	+5.0 +5.0	µV/°C
Input Offset Current	I_{IO}	(Note 2) $T_A = 25^\circ C$ $-55^\circ C \leq T_A \leq 125^\circ C$	-0.2 -0.4	+0.2 +0.4	nA
Input Offset Current Temperature Sensitivity	$\frac{\Delta I_{IO}}{\Delta T}$	ΔT_A from $-55^\circ C$ to $+25^\circ C$ ΔT_A from $+25^\circ C$ to $+125^\circ C$	-2.5 -2.5	+2.5 +2.5	pA/°C
Input Bias Current	$+I_{IB}$	(Note 2) $25^\circ C \leq T_A \leq 125^\circ C$ $-55^\circ C \leq T_A \leq +25^\circ C$	-0.1 -0.1	+2.0 +3.0	nA
	$-I_{IB}$	(Note 2) $25^\circ C \leq T_A \leq 125^\circ C$ $-55^\circ C \leq T_A \leq +25^\circ C$	-0.1 -0.1	+2.0 +3.0	nA
Power Supply Rejection Ratio	$+PSRR$	$+V_{CC} = 10V$ $R_S = 50\Omega$ $T_A = 25^\circ C$ $-V_{CC} = 20V$ $-55^\circ C \leq T_A \leq 125^\circ C$	-16 -16	+16 +16	µV/V
Power Supply Rejection Ratio	$-PSRR$	$+V_{CC} = 20V$ $R_S = 50\Omega$ $T_A = 25^\circ C$ $-V_{CC} = -10V$ $-55^\circ C \leq T_A \leq 125^\circ C$	-16 -16	+16 +16	µV/V
Input Voltage Common-Mode Rejection	CMR	$\pm V_{CC} = 20V$ $V_{IN} = \pm 15V$ $R_S = 50\Omega$	96	—	dB
Adjustment For Input Offset Voltage	V_{IO} ADJ (+)	$\pm V_{CC} = 20V$	No External Adjustment		mV
Adjustment For Input Offset Voltage	V_{IO} ADJ (−)	$\pm V_{CC} = 20V$	No External Adjustment		mV
Output Short-Circuit Current (For Positive Output)	$I_{OS\,(+)}$	$\pm V_{CC} = 15V$ $t \leq 25ms$ (Note 3)	15	—	mA
Output Short-Circuit Current (For Negative Output)	$I_{OS\,(-)}$	$\pm V_{CC} = 15V$ $t \leq 25ms$ (Note 3)	—	15	mA
Supply Current	I_{CC}	$\pm V_{CC} = 15V$ $T_A = -55^\circ C$ $T_A = +25^\circ C$ $T_A = +125^\circ C$	— — —	0.8 0.6 0.6	mA
Output Voltage Swing (Maximum)	V_{OP}	$\pm V_{CC} = 20V$, $R_L = 10k\Omega$ $\pm V_{CC} = 20V$, $R_L = 2k\Omega$	±16 —	— —	V
Open-Loop Voltage Gain (Single Ended) (Note 1)	$A_{VS\,(\pm)}$	$\pm V_{CC} = 20V$ $R_L = 10k\Omega$ $T_A = 25^\circ C$ $V_{OUT} = \pm 15V$ $-55^\circ C \leq T_A \leq 125^\circ C$	80 40	— —	V/mV
Open-Loop Voltage Gain (Single Ended) (Note 1)	A_{VS}	$\pm V_{CC} = 5V$ $R_L = 10k\Omega$ $V_{OUT} = \pm 2V$	20	—	V/mV
Transient Response Rise Time	$TR_{(tr)}$	$C_F = 10pF$	—	1000	nsec
Transient Response Overshoot	$TR_{(OS)}$	$C_F = 10pF$	—	50	%
Noise (Referred to Input) Broadband	N_I (BB)	$V_{CC} = 20V$ Bandwidth = 5kHz $T_A = 25^\circ C$	—	15	µV rms
Noise (Referred to Input) Popcorn	N_I (PC)	$\pm V_{CC} = 20V$ Bandwidth = 5kHz $T_A = 25^\circ C$	—	40	µV peak

NOTES:

1. Note that gain is not specified at $V_{IO\,(ADJ)}$ extremes. Some gain reduction is usually seen at $V_{IO\,(ADJ)}$ extremes. For closed-loop applications (closed-loop gain less than 1,000), the open-loop tests (A_{VS}) prescribed herein should guarantee a positive, reasonably linear, transfer characteristic. They do not, however, guarantee that the open-loop gain is linear, or even positive, over the operating range. If either of these requirements exist (positive open-loop gain or open-loop gain linearity), they should be specified in the individual procurement document as additional requirements.
2. Tests at common-mode $V_{CM} = 0$, $V_{CM} = -15V$, and $V_{CM} = +15V$.
3. Continuous short-circuit limits will be considerably less than the indicated test limits. Continuous I_{OS} at $T_A \leq 75^\circ C$ will cause T_j to exceed the maximum of 175° C. For dual devices, I_{OS} is measured one channel at a time.

ELECTRICAL CHARACTERISTICS at $5V \leq \pm V_{CC} \leq 20V$ and $-55°C \leq T_A \leq +125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
Slew Rate	SR (+)	$A_V = 1$	$-55°C \leq T_A \leq 25°C$	0.05	—	V/μsec
		$V_{IN} = +5V$	$T_A = 125°C$	0.05	—	
Slew Rate	SR (−)	$A_V = 1$	$-55°C \leq T_A \leq 25°C$	0.05	—	V/μsec
		$V_{IN} = \pm 5V$	$T_A = 125°C$	0.05	—	
Settling Time	t_S (+)	$T_A = 25°C$		—	—	ns
		$-55°C \leq T_A \leq 125°C$		—	—	
	t_S (−)	$T_A = 25°C$		—	—	ns
		$-55°C \leq T_A \leq 125°C$		—	—	
Channel Separation	CS	$\pm V_{CC} = 20V$ $T_A = 25°C$		80	—	dB

NOTES:

1. Note that gain is not specified at $V_{IO\,(ADJ)}$ extremes. Some gain reduction is usually seen at $V_{IO\,(ADJ)}$ extremes. For closed-loop applications (closed-loop gain is less than 1,000), the open-loop tests (A_{VS}) prescribed herein should guarantee a positive, reasonably linear, transfer characteristic. They do not, however, guarantee that the open-loop gain is linear, or even positive, over the operating range. If either of these requirements exist (positive open-loop gain or open-loop gain linearity), they should be specified in the individual procurement document as additional requirements.
2. Tests at common-mode $V_{CM} = 0$, $V_{CM} = -15V$, and $V_{CM} = +15V$.
3. Continuous short-circuit limits will be considerably less than the indicated test limits. Continuous I_{OS} at $T_A \leq 75°C$ will cause T_j to exceed the maximum of 175° C. For dual devices, I_{OS} is measured one channel at a time.

For Test Circuit Diagrams, See MIL-M-38510/101

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INSTRUMENTATION AMPLIFIER

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AMP-01 6-5
Low-Noise Precision Instrumentation Amplifier

INSTRUMENTATION AMPLIFIER

INTRODUCTION

An instrumentation amplifier is a committed gain block that amplifies a differential input voltage by a precisely set gain. Voltages common to both inputs are rejected. Differential gain is set by one or two external resistors, usually over a range of 1 to 1000. Instrumentation amplifiers are designed to have very high input impedance; this assures that the gain will not be affected by signal-source impedances (R_S). Input bias current must be low to minimize input offset voltages due to $I_B \times R_S$. In the output stage, low output impedance keeps the output voltage from being affected by the load impedance. Instrumentation amplifiers employ heavy negative feedback which provides excellent gain linearity even at high gains.

Most instrumentation amplifiers have an output sense pin (SENSE) and a reference input pin (REFERENCE). As shown in Figure 1, the load is usually connected between SENSE and REFERENCE points. The amplifier will make $V_{OUT} = GV_{IN}$ despite voltage drops between OUTPUT and LOAD, or from REFERENCE to GROUND. The SENSE and REFERENCE inputs are particularly useful for driving remote loads with high currents. The essential characteristics of instrumentation amplifiers—high input impedance, low output impedance, low offset, high linearity, stable gain, and ability to reject common-mode inputs—make them very useful for amplifying low-level transducer outputs. Transducers such as thermocouples, strain-gage bridges, biological probes, and current shunts produce small differential signals superimposed on common-mode bias voltages. In addition, common-mode ground noise is usually prevelant. Instrumentation amplifiers are gain blocks that have been optimized for preamplifying low-level transducer signals in the presence of common-mode noise.

The PMI AMP-01 instrumentation amplifier has all the features needed for use in high-accuracy data-acquisition systems and high-performance instruments:

- Wide Gain Range ($0.1 \leq G \leq 10{,}000$)
- High Input Impedance
- Low Input Bias Current
- Low Offsets
- Excellent Linearity

Unlike conventional instrumentation amplifiers, the AMP-01 has high output drive capability; it can supply ±10V at ±50mA. This enhanced output drive capability enables the AMP-01 to drive unusually large capacitive loads without encountering stability problems.

Gain of the AMP-01 is set by the ratio of two external resistors according to:

$$V_{OUT} = \left(\frac{20 \times R_{SCALE}}{R_{GAIN}}\right) V_{IN}$$

Output sense and reference points are provided. The AMP-01 is unusually versatile, and can be connected as a precision current source or high-performance op amp as well as a conventional instrumentation amplifier.

DEFINITIONS

Voltage Offsets — Offset at the output of an instrumentation amplifier consists of two terms, a gain-dependent input-offset-voltage and a gain-independent output-offset-voltage. Total offset is the sum of the unity-gain-output-offset (V_{OOS}) plus input-offset (V_{IOS}) multiplied by the gain (Output Offset $= V_{OOS} + GV_{IOS}$). At high gain, the input offset term dominates. For the AMP-01, both input and output offsets can be trimmed externally if desired.

Power Supply Rejection — Offset changes with variations in the power supply voltages. The ability of the instrumentation amplifier to reject fluctuations in power supply voltage is referred to as "power supply rejection". It varies with gain and is different for the positive and negative supplies. The offset change referred-to-input (RTI) is usually specified in dB form. For example, a PSR of 100dB at a gain of 1000 would imply an input-offset-voltage change of $10\mu V$-per-volt of power supply change. The output offset change-per-volt of power-supply change would be 10mV. PSR in the specification tables is measured at DC.

INSTRUMENTATION AMPLIFIER

Input Bias Current — The input bias currents are currents flowing into (or out of) the two inputs of the amplifier. The value given in the specification table is the maximum current into either input. Input offset current is the difference between the two input bias currents.

Input Voltage Range — The linear operating range of the amplifier is referred to as the "input voltage range". When operating at high gains with small differential inputs, this input range is the common-mode input voltage range.

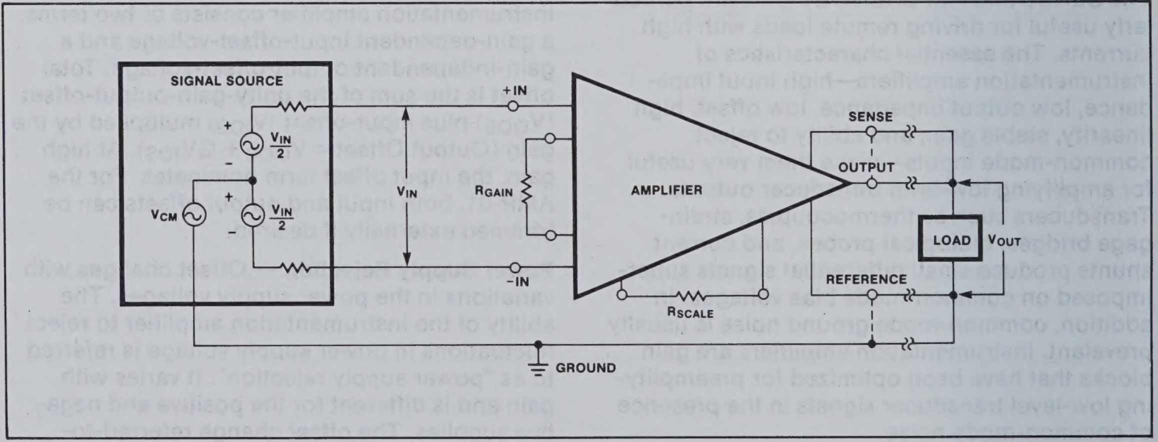
Common-Mode Rejection — Common-mode rejection (CMR) specifies the amplifiers ability to reject common-mode inputs. The ratio of change in output voltage to a change in common-mode input voltage is the common-mode gain ($\Delta V_O/\Delta V_{CM}$). The ratio of differential gain (G) to common-mode gain (A_{CM}) is defined as common-mode rejection ratio (CMRR). The CMR is conventionally specified in log form; $CMR = 20 \log_{10} CMRR$.

Since instrumentation amplifiers are designed to amplify differential signals while rejecting common-mode inputs, common-mode gain stays essentially independent of gain setting. Therefore, CMRR increases almost directly with the gain setting.

As an example, consider a CMR of 120dB at a gain of 1000 with a common-mode input range of ±10V. The 120dB of CMR implies a CMRR of $1000/A_{CM} = 1,000,000$, or a common-mode gain of 1/1000. A ±10V common-mode input will cause an output change of ±10mV for this example (CMR = 120dB, G = 1000).

Gain Equation Accuracy — Differential gain is given as a function of the two external resistors. For the AMP-01, the relationship is ideally $20 \times R_S/R_G$. The specified accuracy limits indicate the accuracy of the amplifier given an exact ratio of R_S/R_G.

INSTRUMENTATION AMPLIFIER FUNCTIONAL DIAGRAM



LOW-NOISE PRECISION INSTRUMENTATION AMPLIFIER

AMP-01

PRELIMINARY

FEATURES

Low Offset Voltage	**$15\mu V$**
Very Low Offset Voltage Drift	**$0.1\mu V/°C$**
Low Noise	**$0.2\mu V_{p-p}$ (0.1Hz to 10Hz)**
Excellent Output Drive	**±10V at ±50mA**
Capacitive Load Stability	**to $1\mu F$**
Gain Range	**0.1 to 10,000**
Excellent Linearity	**16-Bit at G = 1000**
High CMR	**140dB (G = 1000)**
Low Bias Current	**1nA**
May be Configured as a Precision Op-Amp	
Output-Stage Thermal Shutdown	

GENERAL DESCRIPTION

The AMP-01 is a monolithic instrumentation amplifier designed for high-precision data acquisition and general instrumentation applications. The design combines the conventional features of an instrumentation amplifier with a high-current output stage. The output remains stable with high capacitance loads ($1\mu F$), a unique ability for an instrumentation amplifier. Consequently, the AMP-01 can amplify low-level signals for transmission through long cables without requiring an output buffer. The output stage may be configured as a voltage or current generator.

Input offset voltage is very low ($15\mu V$) which generally eliminates the need for an external null potentiometer. Temperature changes have minimal effect on offset; TCV_{IOS} is typically $0.1\mu V/°C$. Excellent low-frequency noise performance is achieved with a minimal compromise on input protection. Bias current is very low, less than 10nA over the industrial temperature range. High common-mode rejection

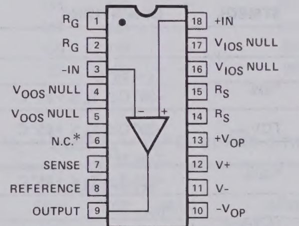
ORDERING INFORMATION†

PACKAGE CERDIP 18-PIN	OPERATING TEMPERATURE RANGE
AMP01AX*	MIL
AMP01BX*	MIL
AMP01EX	IND
AMP01FX	IND

*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

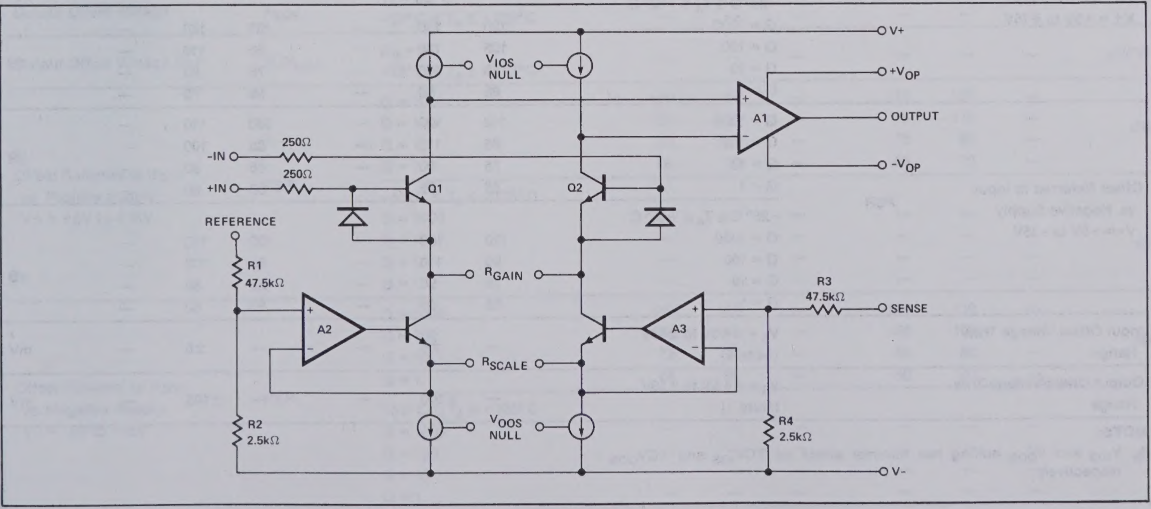
PIN CONNECTIONS


R_G 1
R_G 2
-IN 3
V_{OOS} NULL 4
V_{OOS} NULL 5
N.C.* 6
SENSE 7
REFERENCE 8
OUTPUT 9
18 +IN
17 V_{IOS} NULL
16 V_{IOS} NULL
15 R_S
14 R_S
13 $+V_{OP}$
12 V+
11 V-
10 $-V_{OP}$

18-PIN HERMETIC DIP (X-Suffix)

*MAKE NO ELECTRICAL CONNECTION TO PIN 6.

SIMPLIFIED SCHEMATIC


V+
V_{IOS} NULL
$+V_{OP}$
A1
OUTPUT
$-V_{OP}$
-IN
+IN
250Ω
250Ω
Q1
Q2
REFERENCE
R1 47.5kΩ
R_{GAIN}
R3 47.5kΩ
SENSE
A2
A3
R_{SCALE}
V_{OOS} NULL
R2 2.5kΩ
R4 2.5kΩ
V-

of 140dB, 16-bit linearity at a gain of 1000, and 50mA peak output current are achievable simultaneously. This combination takes the instrumentation amplifier one step further towards the ideal amplifier.

AC performance complements the superb DC specifications. The AMP-01 slews at 4.5V/µs into capacitive loads of up to 15nF, settles in 70µs to 0.01% at a gain of 1000, and boasts a healthy 26MHz gain-bandwidth product. These features make the AMP-01 ideal for high-speed data-acquisition systems.

Gain is set by the ratio of two external resistors over a range of 0.1 to 10,000. A very low gain-temperature-coefficient of 10ppm/°C is achievable over the whole gain range. Output voltage swing is guaranteed with three load resistances; 50Ω, 500Ω, and 2kΩ. Loaded with 500Ω, the output delivers ±12.0V minimum. A thermal shutdown circuit prevents destruction of the output transistors during overload conditions.

The AMP-01 can also be configured as a high-performance operational amplifier. In many applications, the AMP-01 can be used in place of op-amp/power-buffer combinations.

ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage .... ±18V
Internal Power Dissipation (Note 1) 500mW
Common-Mode Input Voltage .... Supply Voltage
Differential Input Voltage, $R_G \geq 2k\Omega$ .... ±20V
$R_G < 2k\Omega$ .... ±10V
Output Short-Circuit Duration .... Indefinite
Storage Temperature Range .... −65°C to +150°C
Operating Temperature Range
AMP-01A, B .... −55°C to +125°C
AMP-01E, F .... −25°C to +85°C
Lead Temperature (Soldering, 60 sec) .... 300°C
DICE Junction Temperature (T_j) .... −65°C to +150°C

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
18-Pin Hermetic DIP (X)	100°C	10mW/°C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.
2. Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $R_S = 10k\Omega$, $R_L = 2k\Omega$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	AMP-01E MIN	AMP-01E TYP	AMP-01E MAX	AMP-01F MIN	AMP-01F TYP	AMP-01F MAX	UNITS
OFFSET VOLTAGE									
Input Offset Voltage	V_{IOS}	$T_A = 25°C$	—	15	50	—	25	100	µV
		$-25°C \leq T_A \leq +85°C$	—	—	70	—	—	150	
Input Offset Voltage Drift	TCV_{IOS}	$-25°C \leq T_A \leq +85°C$	—	0.1	0.3	—	0.2	1.0	µV/°C
Output Offset Voltage	V_{OOS}	$T_A = 25°C$	—	1	3	—	4	10	mV
		$-25°C \leq T_A \leq +85°C$	—	—	9	—	—	15	
Output Offset Voltage Drift	TCV_{OOS}	$R_G = \infty$ $-25°C \leq T_A \leq +85°C$	—	50	100	—	60	120	µV/°C
Offset Referred to Input vs. Positive Supply V+ = +5V to +15V	PSR	G = 1000	120	130	—	110	120	—	dB
		G = 100	105	120	—	95	110	—	
		G = 10	85	100	—	75	90	—	
		G = 1	65	80	—	55	70	—	
		$-25°C \leq T_A \leq +85°C$							
		G = 1000	120	130	—	105	120	—	dB
		G = 100	105	120	—	95	110	—	
		G = 10	85	100	—	75	90	—	
		G = 1	65	80	—	55	70	—	
Offset Referred to Input vs. Negative Supply V− = −5V to −15V	PSR	G = 1000	110	120	—	100	110	—	dB
		G = 100	95	110	—	85	100	—	
		G = 10	75	90	—	65	80	—	
		G = 1	55	65	—	50	60	—	
		$-25°C \leq T_A \leq +85°C$							
		G = 1000	110	120	—	100	110	—	dB
		G = 100	95	110	—	85	100	—	
		G = 10	75	90	—	65	80	—	
		G = 1	55	65	—	50	60	—	
Input Offset Voltage Trim Range		$V_S = \pm 4.5V$ to $\pm 18V$ (Note 1)	—	±6	—	—	±6	—	mV
Output Offset Voltage Trim Range		$V_S = \pm 4.5V$ to $\pm 18V$ (Note 1)	—	±100	—	—	±100	—	mV

NOTE:

1. V_{IOS} and V_{OOS} nulling has minimal affect on TCV_{IOS} and TCV_{OOS}, respectively.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $R_S = 10k\Omega$, $R_L = 2k\Omega$, $T_A = 25°C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	AMP-01E MIN	AMP-01E TYP	AMP-01E MAX	AMP-01F MIN	AMP-01F TYP	AMP-01F MAX	UNITS
INPUT CURRENT									
Input Bias Current	I_B	$T_A = 25°C$	—	1	5	—	3	15	nA
		$-25°C \le T_A \le +85°C$	—	—	10	—	—	20	
Input Bias Current Drift	TCI_B	$-25°C \le T_A \le +85°C$	—	40	85	—	50	100	pA/°C
Input Offset Current	I_{OS}	$T_A = 25°C$	—	0.1	0.5	—	0.5	3	nA
		$-25°C \le T_A \le +85°C$	—	—	1.5	—	—	5	
Input Offset Current Drift	TCI_{OS}	$-25°C \le T_A \le +85°C$	—	3	20	—	5	50	pA/°C
INPUT									
Input Impedance	Z_{IN}	Differential	—	—	—	—	—	—	MΩ
		Common-Mode	—	—	—	—	—	—	
Input Voltage Range	IVR	$T_A = 25°C$	±10.5	—	—	±10.5	—	—	V
		$-25°C \le T_A \le +85°C$	±10.0	—	—	±10.0	—	—	
Common-Mode Rejection	CMR	$V_{CM} = \pm 10V$ Measured with 1kΩ source imbalance							
		G = 1000	125	140	—	110	130	—	dB
		G = 100	120	130	—	100	120	—	
		G = 10	100	110	—	90	110	—	
		G = 1	85	100	—	80	90	—	
		$-25°C \le T_A \le +85°C$							
		G = 1000	115	130	—	105	125	—	dB
		G = 100	110	125	—	100	120	—	
		G = 10	100	110	—	90	110	—	
		G = 1	85	100	—	80	90	—	

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $R_S = 10k\Omega$, $R_L = 2k\Omega$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	AMP-01A MIN	AMP-01A TYP	AMP-01A MAX	AMP-01B MIN	AMP-01B TYP	AMP-01B MAX	UNITS
OFFSET VOLTAGE									
Input Offset Voltage	V_{IOS}	$T_A = 25°C$	—	15	50	—	25	100	μV
		$-55°C \le T_A \le +125°C$	—	—	—	—	—	—	
Input Offset Voltage Drift	TCV_{IOS}	$-55°C \le T_A \le +125°C$	—	0.1	0.3	—	0.2	1.0	μV/°C
Output Offset Voltage	V_{OOS}	$T_A = 25°C$	—	1	3	—	4	10	mV
		$-55°C \le T_A \le +125°C$	—	—	—	—	—	—	
Output Offset Voltage Drift	TCV_{OOS}	$R_G = \infty$ $-55°C \le T_A \le +125°C$	—	—	—	—	—	—	μV/°C
Offset Referred to Input vs. Positive Supply V+ = +5V to +15V	PSR	G = 1000	120	130	—	110	120	—	dB
		G = 100	105	120	—	95	110	—	
		G = 10	85	100	—	75	90	—	
		G = 1	65	80	—	55	70	—	
		$-55°C \le T_A \le +125°C$							
		G = 1000	—	—	—	—	—	—	dB
		G = 100	—	—	—	—	—	—	
		G = 10	—	—	—	—	—	—	
		G = 1	—	—	—	—	—	—	
Offset Referred to Input vs. Negative Supply V− = −5V to −15V	PSR	G = 1000	110	120	—	100	110	—	dB
		G = 100	95	110	—	85	100	—	
		G = 10	75	90	—	65	80	—	
		G = 1	55	65	—	50	60	—	
		$-55°C \le T_A \le +125°C$							
		G = 1000	—	—	—	—	—	—	dB
		G = 100	—	—	—	—	—	—	
		G = 10	—	—	—	—	—	—	
		G = 1	—	—	—	—	—	—	

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $R_S = 10k\Omega$, $R_L = 2k\Omega$, $T_A = 25°C$, unless otherwise noted. (Continued)

			AMP-01A			AMP-01B			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage Trim Range		$V_S = \pm 4.5V$ to $\pm 18V$ (Note 1)	—	±6	—	—	±6	—	mV
Output Offset Voltage Trim Range		$V_S = \pm 4.5V$ to $\pm 18V$ (Note 1)	—	±100	—	—	±100	—	mV
INPUT CURRENT									
Input Bias Current	I_B	$T_A = 25°C$	—	1	5	—	3	15	nA
		$-55°C \le T_A \le +125°C$	—	—	—	—	—	—	
Input Bias Current Drift	TCI_B	$-55°C \le T_A \le +125°C$	—	—	—	—	—	—	pA/°C
Input Offset Current	I_{OS}	$T_A = 25°C$	—	0.1	0.5	—	0.5	3	nA
		$-55°C \le T_A \le +125°C$	—	—	—	—	—	—	
Input Offset Current Drift	TCI_{OS}	$-55°C \le T_A \le +125°C$	—	—	—	—	—	—	pA/°C
INPUT									
Input Impedance	Z_{IN}	Differential Common-Mode	—	—	—	—	—	—	MΩ
Input Voltage Range	IVR	$T_A = 25°C$	±10.5	—	—	±10.5	—	—	V
		$-55°C \le T_A \le +125°C$	±10.0	—	—	±10.0	—	—	
Common-Mode Rejection	CMR	$V_{CM} = \pm 10V$ Measured with 1kΩ source imbalance							
		G = 1000	125	140	—	110	130	—	dB
		G = 100	120	130	—	100	120	—	
		G = 10	100	110	—	90	110	—	
		G = 1	85	100	—	80	90	—	
		$-55°C \le T_A \le +125°C$							
		G = 1000	—	—	—	—	—	—	dB
		G = 100	—	—	—	—	—	—	
		G = 10	—	—	—	—	—	—	
		G = 1	—	—	—	—	—	—	

NOTE:

1. V_{IOS} and V_{OOS} nulling has minimal affect on TCV_{IOS} and TCV_{OOS}, respectively.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $R_S = 10k\Omega$, $R_L = 2k\Omega$, $T_A = 25°C$, unless otherwise noted.

			AMP-01A/E			AMP-01B/F			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
GAIN									
Gain Equation Accuracy		$G = \frac{20 \times R_S}{R_G}$ Accuracy Measured from G = 1 to 1000	—	0.3	0.6	—	0.6	0.8	%
Gain Range	G		0.1	—	10k	0.1	—	10k	V/V
Nonlinearity		G = 1000 (Note 1)	—	0.0007	0.005	—	0.0007	0.005	%
		G = 100	—	—	0.005	—	—	0.005	
		G = 10	—	—	0.005	—	—	0.007	
		G = 1	—	—	0.010	—	—	0.015	
Temperature Coefficient	G_{TC}	$1 \le G \le 1000$ (Notes 1, 2)	—	5	10	—	5	15	ppm/°C
OUTPUT RATING									
Output Voltage Swing	V_{OUT}	$R_L = 2k\Omega$	±12.0	±13.5	—	±12.0	±13.5	—	V
		$R_L = 500\Omega$	±12.0	±13.0	—	±12.0	±13.0	—	
		$R_L = 50\Omega$	±2.5	±4.0	—	±2.5	±4.0	—	
		$R_L = 2k\Omega$ Over Temp.	±10.0	±13.5	—	±10.0	±13.5	—	V
		$R_L = 500\Omega$	±10.0	±13.0	—	±10.0	±13.0	—	

NOTES:

1. Guaranteed by design.
2. Gain tempco does not include the effects of gain and scale resistor tempco match.

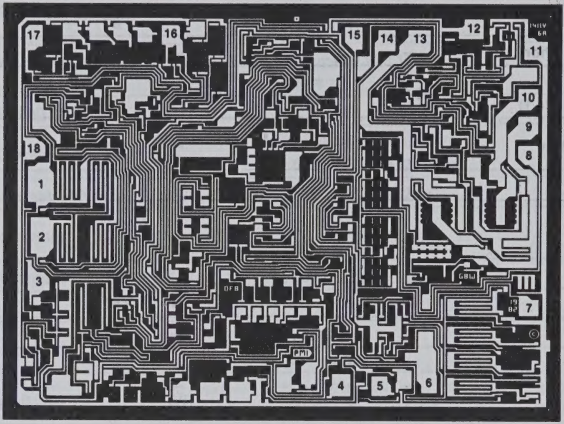
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $R_S = 10k\Omega$, $R_L = 2k\Omega$, $T_A = 25°C$, unless otherwise noted.

			AMP-01A/E			AMP-01B/F			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Positive Current Limit		Output-to-Ground Short	—	80	—	—	80	—	mA
Negative Current Limit		Output-to-Ground Short	—	80	—	—	80	—	mA
Capacitive Load Stability		$1 \le G \le 1000$ No Oscillations, (Note 1)	0.1	1	—	0.1	1	—	μF
Thermal Shutdown Temperature		Junction Temperature	—	165	—	—	165	—	°C
NOISE									
Voltage Density, RTI	e_n	f_O = 1kHz							nV/$\sqrt{Hz}$
		G = 1000	—	5	—	—	5	—	
		G = 100	—	—	—	—	—	—	
		G = 10	—	—	—	—	—	—	
		G = 1	—	450	—	—	450	—	
Noise Current Density, RTI	i_n	f_O = 1kHz	—	—	—	—	—	—	pA/$\sqrt{Hz}$
Input Noise Voltage	$e_{np\text{-}p}$	0.1Hz to 10Hz	—	—	—	—	—	—	$\mu V_{p\text{-}p}$
		G = 1000	—	—	—	—	—	—	
		G = 100	—	—	—	—	—	—	
		G = 10	—	—	—	—	—	—	
		G = 1	—	—	—	—	—	—	
Input Noise Current	$i_{np\text{-}p}$	0.1Hz to 10Hz, G = 1000	—	—	—	—	—	—	$pA_{p\text{-}p}$
DYNAMIC RESPONSE									
Small-Signal Bandwidth (−3dB)	BW	G = 1	—	570	—	—	570	—	kHz
		G = 10	—	100	—	—	100	—	
		G = 100	—	82	—	—	82	—	
		G = 1000	—	26	—	—	26	—	
Slew Rate	SR	G = 10	3.5	4.5	—	3.0	4.5	—	V/μs
Settling Time	t_S	To 0.01%, 20V step							μs
		G = 1	—	11	—	—	11	—	
		G = 10	—	16	—	—	16	—	
		G = 100	—	20	—	—	20	—	
		G = 1000	—	70	—	—	70	—	
SENSE INPUT									
Input Resistance	R_{IN}		35	50	65	35	50	65	kΩ
Input Current	I_{IN}	Referenced to $-V_S$	—	280	—	—	280	—	μA
Voltage Range		(Note 1)	−10.5	—	+15	−10.5	—	+15	V
REFERENCE INPUT									
Input Resistance	R_{IN}		35	50	65	35	50	65	kΩ
Input Current	I_{IN}	Referenced to $-V_S$	—	280	—	—	280	—	μA
Voltage Range		(Note 1)	−10.5	—	+15	−10.5	—	+15	V
Gain to Output			—	1	—	—	1	—	V/V
POWER SUPPLY $-25°C \le T_A \le +85°C$ for E/F Grades, $-55°C \le T_A \le +125°C$ for A/B Grades									
Supply Voltage Range	V_S	+V linked to $+V_{OP}$ −V linked to $-V_{OP}$	±4.5	—	±18	±4.5	—	±18	V
Quiescent Current	I_Q	+V linked to $+V_{OP}$ −V linked to $-V_{OP}$	—	2.9	4.8	—	2.9	4.8	mA

NOTES:

1. Guaranteed by design.
2. Gain tempco does not include the effects of gain and scale resistor tempco match.

DICE CHARACTERISTICS



DIE SIZE 0.110 × 0.148 inch, 16,280 sq. mils
(2.79 × 3.76 mm, 10.50 sq. mm)

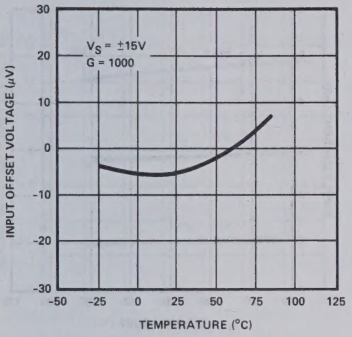
1. R_G
2. R_G
3. −INPUT
4. V_{OOS} NULL
5. V_{OOS} NULL
6. N.C.*
7. SENSE
8. REFERENCE
9. OUTPUT
10. V− (OUTPUT)
11. V−
12. V+
13. V+ (OUTPUT)
14. R_S
15. R_S
16. V_{IOS} NULL
17. V_{IOS} NULL
18. +INPUT

* Make no electrical connection

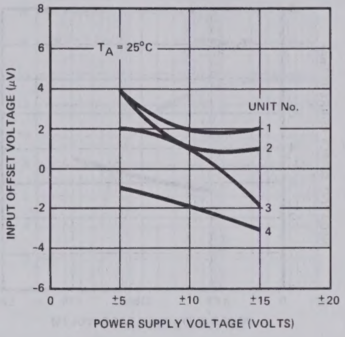
For additional DICE information refer to Section 2.

TYPICAL PERFORMANCE CHARACTERISTICS

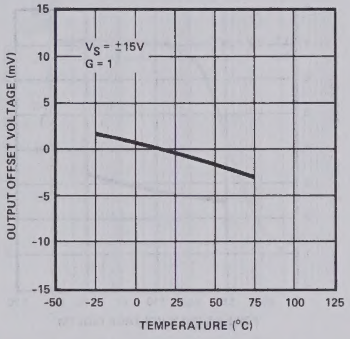
INPUT OFFSET VOLTAGE vs TEMPERATURE



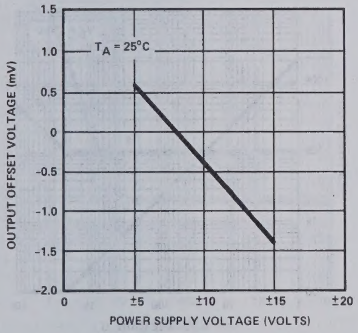
INPUT OFFSET VOLTAGE vs SUPPLY VOLTAGE



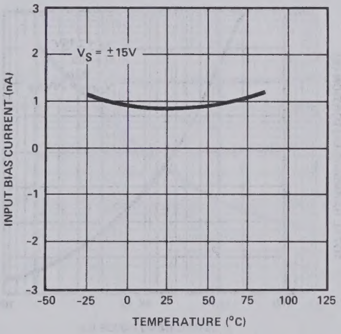
OUTPUT OFFSET VOLTAGE vs TEMPERATURE



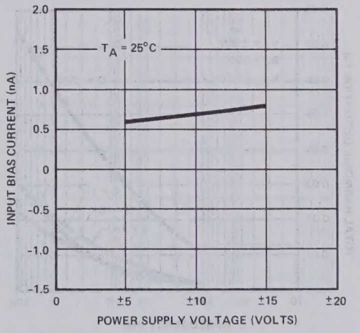
OUTPUT OFFSET VOLTAGE vs SUPPLY VOLTAGE



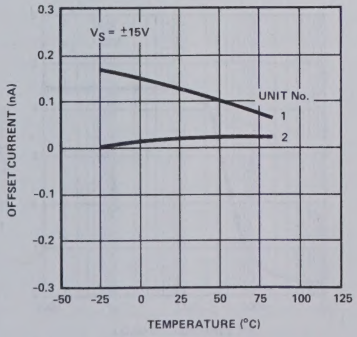
INPUT BIAS CURRENT vs TEMPERATURE



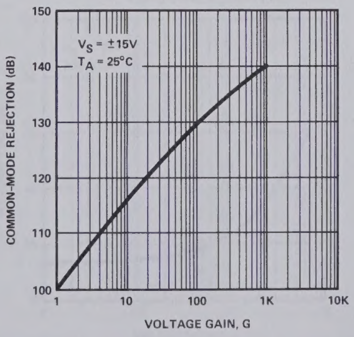
INPUT BIAS CURRENT vs SUPPLY VOLTAGE



INPUT OFFSET CURRENT vs TEMPERATURE



COMMON-MODE REJECTION vs VOLTAGE GAIN

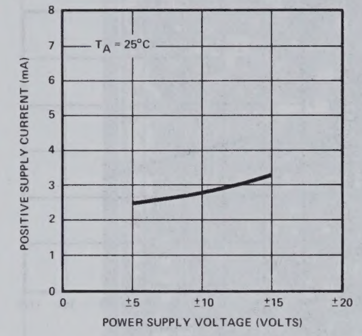


COMMON-MODE REJECTION vs FREQUENCY

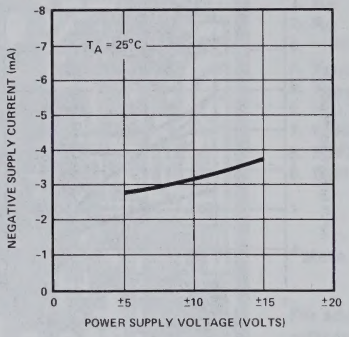
DATA NOT
AVAILABLE
AT TIME OF PRINTING

TYPICAL PERFORMANCE CHARACTERISTICS

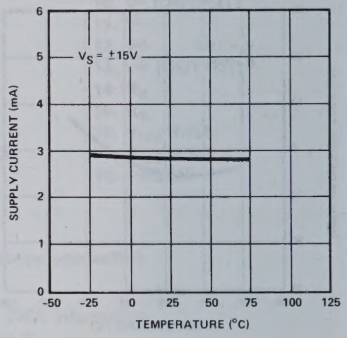
POSITIVE SUPPLY CURRENT vs SUPPLY VOLTAGE



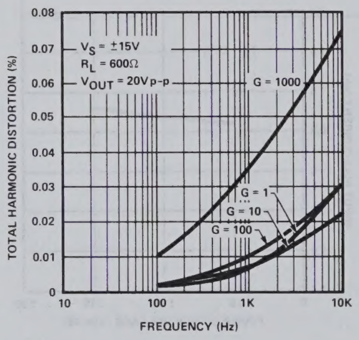
NEGATIVE SUPPLY CURRENT vs SUPPLY VOLTAGE



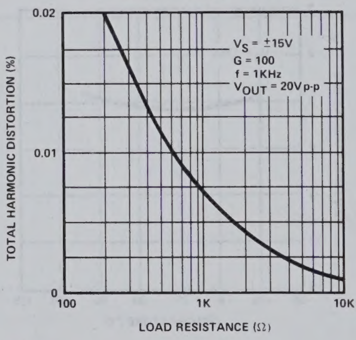
SUPPLY CURRENT vs TEMPERATURE



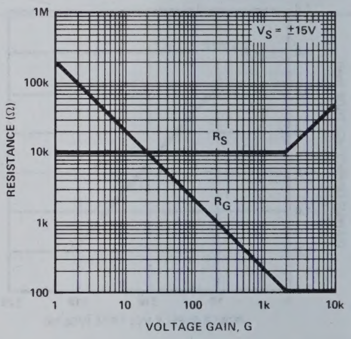
TOTAL HARMONIC DISTORTION vs FREQUENCY



TOTAL HARMONIC DISTORTION vs LOAD RESISTANCE

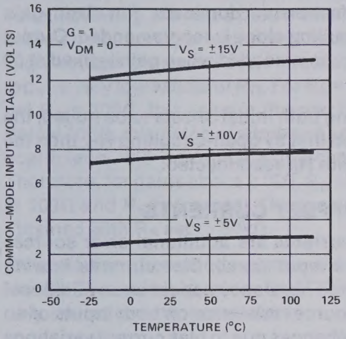


R_G AND R_S SELECTION

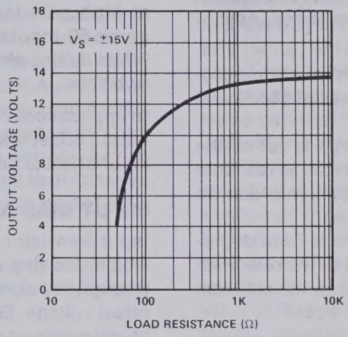


TYPICAL PERFORMANCE CHARACTERISTICS

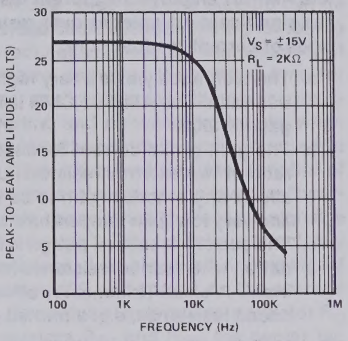
COMMON-MODE VOLTAGE RANGE vs TEMPERATURE



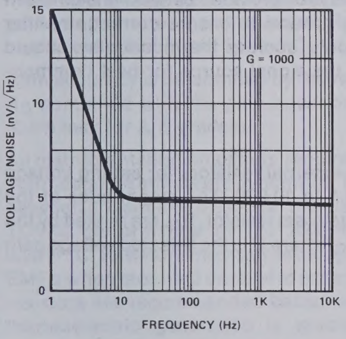
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



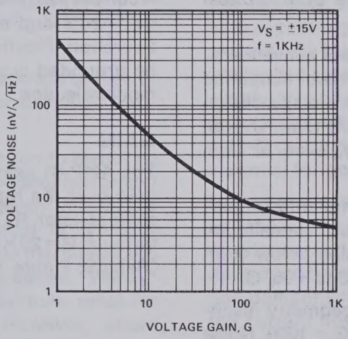
MAXIMUM OUTPUT SWING vs FREQUENCY



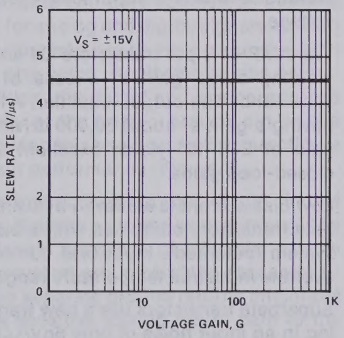
VOLTAGE NOISE DENSITY vs FREQUENCY



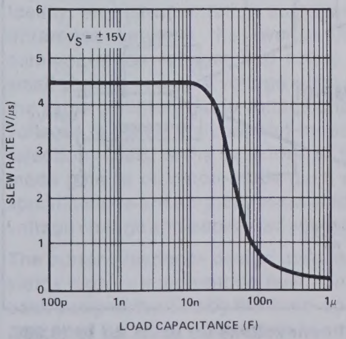
RTI VOLTAGE NOISE DENSITY vs GAIN



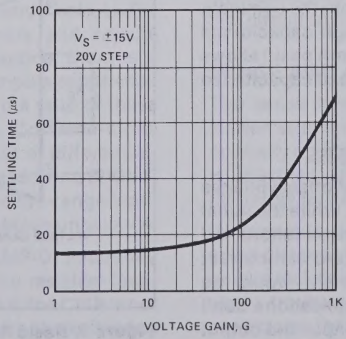
SLEW RATE vs VOLTAGE GAIN



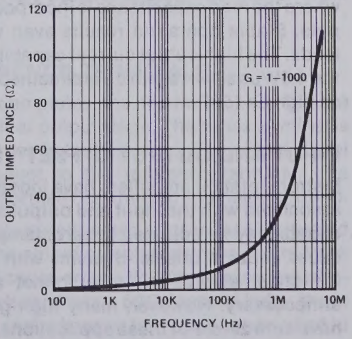
SLEW RATE vs LOAD CAPACITANCE



SETTLING TIME TO 0.01% vs VOLTAGE GAIN



CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY



THEORY OF OPERATION

An instrumentation amplifier, unlike an op amp, requires precise internal feedback. The two techniques presently in use are resistive and current feedback.

The AMP-01 employs the current feedback approach which has significant advantages over resistive feedback. Advantages of current-feedback are:

a. The technique yields a very high common-mode rejection ratio. The AMP-01 CMR is in excess of 140dB at a gain of 1000.
b. The gain of the current feedback design is set by the ratio of two external resistors. Using external resistors allows any practical gain to be set with high precision and very low gain temperature coefficient.
c. The current-feedback design is immune to CMR degradation when series resistance is added to the reference input. A small (trimmable) offset change results from added resistance, e.g. a printed circuit track.

The AMP-01 utilizes low-drift thin-film resistors to minimize output offset temperature drift. A feedback voltage-to-current converter is employed having high linearity and low noise, particularly at low frequencies. Parameter shifts during packaging are eliminated by a post-assembly trimming technique which electronically adjusts the output offset voltage.

The AMP-01 input transistors Q1 and Q2 feed active loads, yielding stage gain in excess of 4000 (see simplified schematic) The output amplifier, A1, is a two-stage design having a gain of about 50,000 driving a 100Ω load. Overall gain of 2×10^8 yields excellent linearity, even at high closed-loop gains.

Low bias current is achieved by using Ion-implanted superbeta transistors combined with a bias-current cancellation system (patented). Input bias current remains below 10nA over the industrial temperature range, −25° C to +85° C.

Superbeta transistors use a new transistor geometry resulting in an input noise of only $5\text{nV}/\sqrt{\text{Hz}}$ at G = 1000. Noise includes contributions from the gain-setting resistor and internal overload-protection resistor. The input stage achieves an offset voltage drift of less than 0.3μV/°C (E Grade).

The AMP-01 uses a unique two-pole compensation scheme where the load capacitance is incorporated into the dominate pole. Stable operation results even with high capacitance loads. The high output current capability (80mA peak) allows the 4.5V/μs slew-rate to be maintained with load capacitance as high as 15nF.

INPUT AND OUTPUT OFFSET VOLTAGES

Instrumentation amplifiers have independent offset voltages associated with the input and output stages. While the initial offsets may be adjusted to zero, temperature variations will cause shifts in offsets. Systems with auto-zero can correct for offset errors, so initial offset adjustment would be unnecessary. However, many high-gain applications don't have auto zero. For these applications, both input and output offsets can be trimmed. Adjustment of these offsets has minimal effect on TCV_{IOS} or TCV_{OOS}.

The input offset component is directly multiplied by the amplifier gain, whereas output offset is independent of gain. Therefore, at low gain output-offset-errors dominate, while at high gain input-offset-errors dominate. For fixed gain above 50, input offset nulling alone is recommended. Output offset nulling alone is recommended when gain is fixed at 50 or below.

In applications requiring both initial offsets to be nulled, the output offset is adjusted first by open-circuiting R_G, then the input offset is nulled with R_G reconnected.

INPUT BIAS AND OFFSET CURRENTS

Input transistor bias currents are additional error sources which can degrade the input signal. Bias currents flowing through the signal source resistance appear as an additional offset voltage. Equal source resistance on both inputs of an IA will minimize offset changes due to bias current variations with signal voltage and temperature. However, the difference between the two bias currents, the input offset current, produces a non-trimmable error. The magnitude of the error is the offset current times the source resistance.

A current path must always be provided between the differential inputs and analog ground to ensure correct amplifier operation. Floating inputs, such as thermocouples, should be grounded close to the signal source for best common-mode rejection.

GAIN

The AMP-01 uses two external resistors for setting voltage gain over the range 0.1 to 10,000. The magnitudes of the scale resistor, R_S, and gain-set resistor, R_G, are related by the formula: $G = 20 \times R_S/R_G$, where G is the selected voltage gain (Refer to Figure 1).

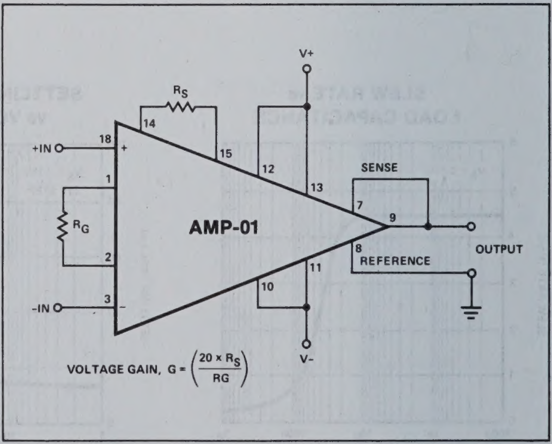


Figure 1. Basic AMP-01 connections for gains 0.1 to 10,000.

The magnitude of R_S affects linearity and output referred errors. Circuit performance is optimized by making $R_S = 10k\Omega$ when operating on ±15 volt supplies and driving a ±10 volt output. R_S may be reduced to $5k\Omega$ when operating on ±5 volt supplies or if the output voltage swing is limited to ±5 volts. Lowering the value below $5k\Omega$ can cause instability in some circuit configurations and usually has no advantage. High voltage gains between two and ten thousand would require very low values of R_G. For $R_S = 10k\Omega$ and $A_V = 2000$ we get $R_G = 100\Omega$; this value is the practical lower limit for R_G. Below 100Ω, mismatch of wirebond and resistor temperature coefficients will introduce significant gain tempco errors. Therefore, for gains above 2,000, R_G should be kept constant at 100Ω and R_S increased. The maximum gain of 10,000 is obtained with R_S set to $50k\Omega$.

Metal-film or wirewound resistors are recommended for best results. The absolute values and TC's are not too important, only the ratiometric parameters.

AC amplifiers require good gain stability with temperature and time, but DC performance is unimportant. Therefore, low cost metal-film types with TC's of 50ppm/°C are usually adequate for R_S and R_G. Realizing the full potential of the AMP-01's offset voltage and gain stability requires precision metal-film or wirewound resistors. Achieving a 15ppm/°C gain tempco at all gains requires R_S and R_G temperature coefficient matching to 5ppm/°C or better.

Gain accuracy is determined by the ratio accuracy of R_S and R_G combined with the gain equation error of the AMP-01 (0.5% max for A/E grades).

All instrumentation amplifiers require attention to layout so thermocouple effects are minimized. Thermocouples formed between copper and dissimilar metals can easily destroy the TCV_{OS} performance of the AMP-01 which is typically $0.2\mu V/°C$. Resistors themselves can generate thermoelectric EMF's when mounted parallel to a thermal gradient. "Vishay" resistors are recommended because a maximum value for thermoelectric generation is specified. However, where thermal gradients are low and gain TC's of 20-50ppm are sufficient, general-purpose metal-film resistors can be used for R_G and R_S.

COMMON-MODE REJECTION

Ideally, an instrumentation amplifier responds only to the difference between the two input signals and rejects common-mode voltages and noise. In practice, there is a small change in output voltage when both inputs experience the same common-mode voltage change; the ratio of these voltages is called the common-mode gain. Common-mode rejection (CMR) is the logarithm of the ratio of differential-mode gain to common-mode gain, expressed in dB. CMR specifications are normally measured with a full-range input voltage change and a specified source resistance unbalance.

The current-feedback design used in the AMP-01 inherently yields high common-mode rejection. Unlike resistive feedback designs, typified by the three-op-amp IA, the CMR is not degraded by small resistances in series with the reference input. A slight, but trimmable, output offset voltage change results from resistance in series with the reference input.

ACTIVE GUARD DRIVE

Rejection of common-mode noise and line pick-up can be improved by using shielded cable between the signal source and the IA. Shielding reduces pick-up, but increases input capacitance, which in turn degrades the settling-time for signal changes. Further, any imbalance in the source resistance between the inverting and noninverting inputs, when capacitively loaded, converts the common-mode voltage into a differential voltage. This effect reduces the benefits of shielding. AC common-mode rejection is improved by "bootstrapping" the input cable capacitance to the input signal, a technique called "guard driving". This technique effectively reduces the input capacitance. A single guard-driving signal is adequate at gains above 100 and should be the average value of the two inputs. The value of external gain resistor R_G is split between two resistors R_{G1} and R_{G2}; the center tap provides the required signal to drive the buffer amplifier (Figure 2).

GROUNDING

The majority of instruments and data acquisition systems have separate grounds for analog and digital signals. Analog ground may also be divided into two or more grounds which will be tied together at one point, usually the analog power-supply ground. In addition, the digital and analog grounds may be joined, normally at the analog ground pin on the A-to-D converter. Following this basic grounding practice is essential for good circuit performance (Figure 3).

Mixing grounds causes interactions between digital circuits and the analog signals. Since the ground returns have finite resistance and inductance, hundreds of millivolts can be developed between the system ground and the data acquisition components. Using separate ground returns minimizes the current flow in the sensitive analog return path to the system ground point. Consequently, noisy ground currents from logic gates do not interact with the analog signals.

Inevitably, two or more circuits will be joined together with their grounds at differential potentials. In these situations, the differential input of an instrumentation amplifier, with its high CMR, can accurately transfer analog information from one circuit to another.

SENSE AND REFERENCE TERMINALS

The sense terminal completes the feedback path for the instrumentation amplifier output stage. The sense terminal is normally connected directly to the output. The output signal is specified with respect to the reference terminal. The reference terminal is normally connected to analog ground.

If heavy output currents are expected and the load is situated some distance from the amplifier, voltage drops due to track or wire resistance will cause errors. Voltage drops are particularly troublesome when driving 50Ω loads. Under these conditions, the sense and reference terminals can be used to

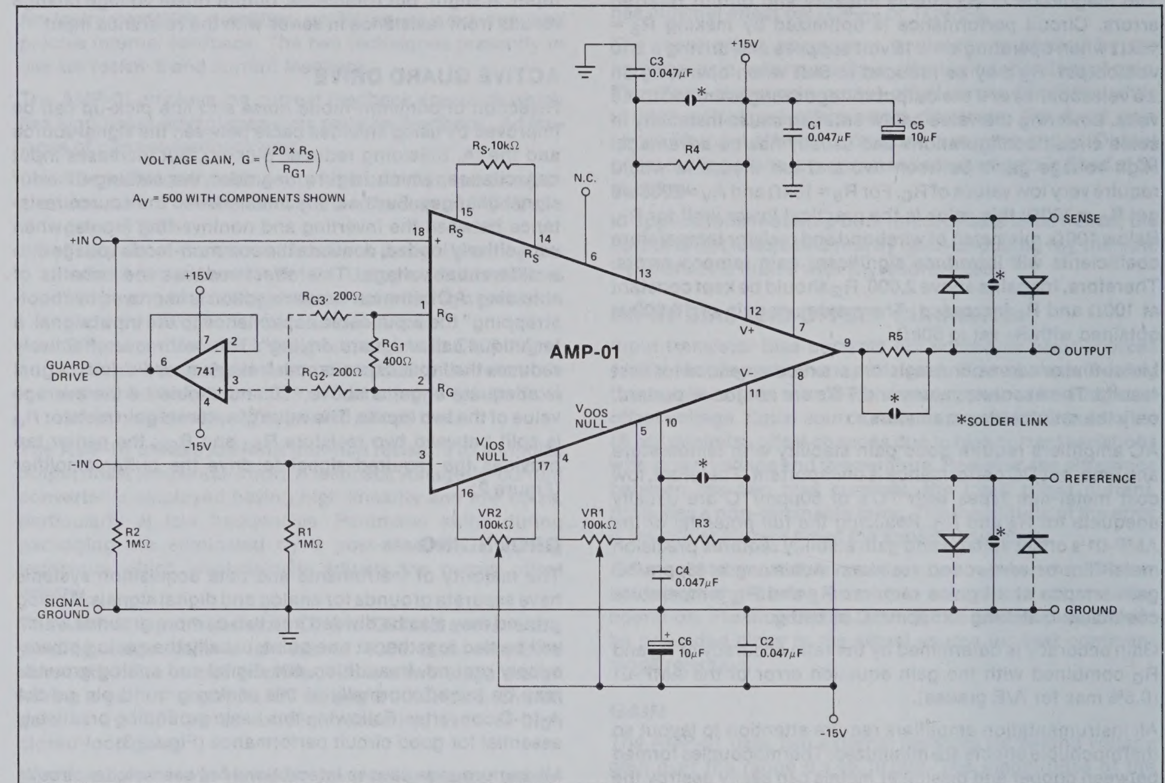

VOLTAGE GAIN, G = $\left(\frac{20 \times R_S}{R_{G1}}\right)$
A_V = 500 WITH COMPONENTS SHOWN
+IN
-IN
GUARD DRIVE
SIGNAL GROUND
+15V
-15V
741
R_{G3}, 200Ω
R_{G1} 400Ω
R_{G2}, 200Ω
R2 1MΩ
R1 1MΩ
R_S, 10kΩ
N.C.
AMP-01
R_S
R_G
V+
V-
V_{OOS} NULL
V_{IOS} NULL
VR2 100kΩ
VR1 100kΩ
C3 0.047μF
C1 0.047μF
C5 10μF
R4
R5
R3
C4 0.047μF
C6 10μF
C2 0.047μF
*SOLDER LINK
SENSE
OUTPUT
REFERENCE
GROUND
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18

Figure 2. AMP-01 evaluation circuit showing guard-drive connection.

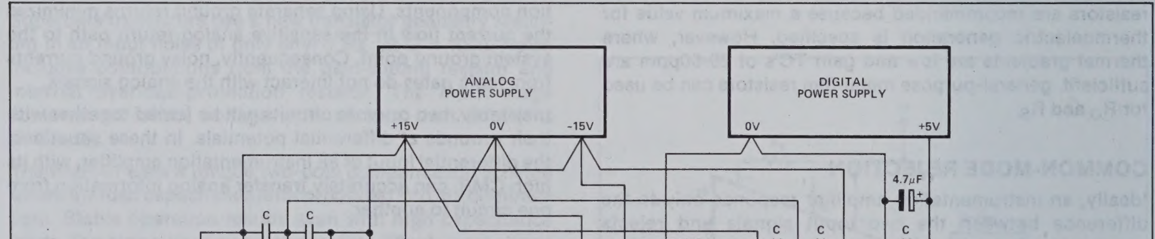
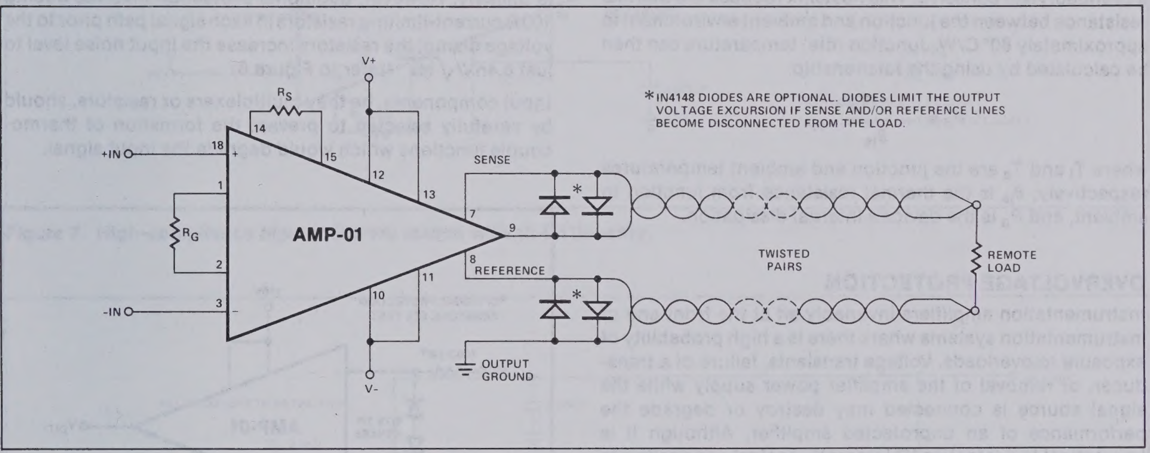

ANALOG POWER SUPPLY
+15V
0V
-15V
DIGITAL POWER SUPPLY
0V
+5V
4.7μF
C
DIGITAL GROUND
AMP-01
7
9
8
OUTPUT REFERENCE
SMP-11 SAMPLE AND HOLD
HOLD CAPACITOR
ANALOG GROUND
DIGITAL GROUND
ADC
DIGITAL DATA OUTPUT
C - 0.047μF CERAMIC CAPACITORS

Figure 3. Basic grounding practice.

"remote sense" the load as shown in Figure 4. This method of connection puts the I×R drops inside the feedback loop and virtually eliminates the error. An unbalance in the lead resistances from the sense and reference pins does not degrade CMR, but will change the output offset voltage. For example, a large unbalance of 3Ω will change the output offset by only 1mV.

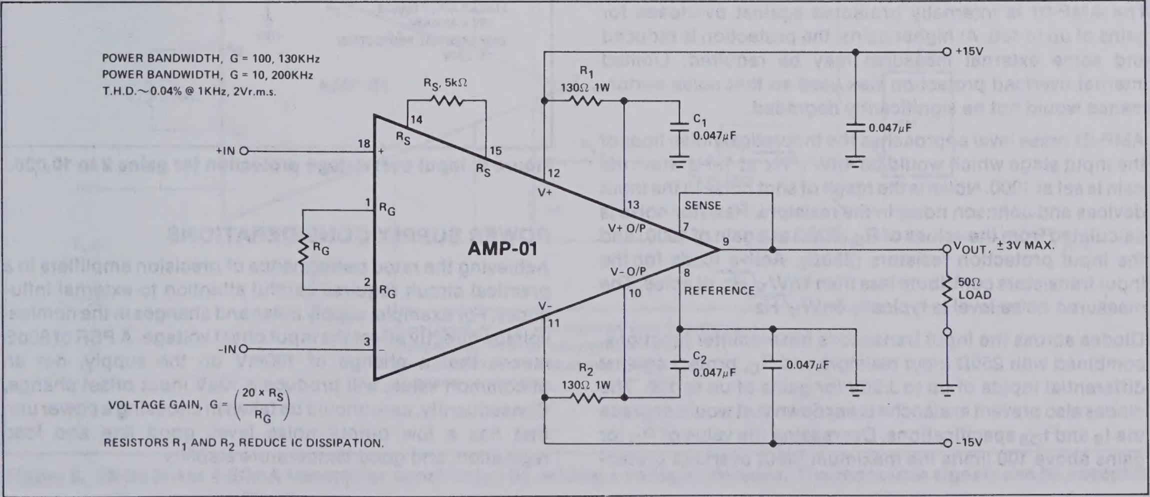
DRIVING 50Ω LOADS

Output currents of 50mA are guaranteed into loads of up to 50Ω and 24mA into 500Ω. In addition, the output is stable and free from oscillation even with a high load capacitance. The combination of these unique features in an instrumentation amplifier allows low-level transducer signals to be conditioned and directly transmitted through long cables in voltage or current form. Increased output current brings increased internal dissipation, especially with 50Ω loads. For this reason, the power-supply connections are split into two pairs; pins 10 and 13 connect to the output stage only and pins 11 and 12 provide power to the input and following stages. Dual supply pins allow dropper resistors to be connected in series with the output stage so excess power is dissipated outside the package. Additional decoupling is necessary between pins 10 and 13 to ground to maintain stability when dropper resistors are used. Figure 5 shows a complete circuit for driving 50Ω loads.


V+
R_S
14
18
+IN
+
15
12
SENSE
1
R_G
AMP-01
13
7
9
2
8
REFERENCE
11
3
-IN
–
10
V-
OUTPUT GROUND
TWISTED PAIRS
REMOTE LOAD
*

*IN4148 DIODES ARE OPTIONAL. DIODES LIMIT THE OUTPUT VOLTAGE EXCURSION IF SENSE AND/OR REFERENCE LINES BECOME DISCONNECTED FROM THE LOAD.

Figure 4. Remote load sensing.


R_S, 5kΩ
14
R_S
+IN
18
+
15
R_S
12
V+
1
R_G
R_G
2
R_G
AMP-01
13
V+ O/P
SENSE
7
9
V- O/P
8
10
REFERENCE
V-
11
3
-IN
R_1
130Ω 1W
C_1
0.047μF
0.047μF
+15V
V_{OUT}, ±3V MAX.
50Ω LOAD
C_2
0.047μF
0.047μF
R_2
130Ω 1W
-15V

POWER BANDWIDTH, G = 100, 130KHz
POWER BANDWIDTH, G = 10, 200KHz
T.H.D.~0.04% @ 1KHz, 2Vr.m.s.

VOLTAGE GAIN, $G = \left(\frac{20 \times R_S}{R_G}\right)$

RESISTORS R_1 AND R_2 REDUCE IC DISSIPATION.

Figure 5. Driving 50Ω loads.

HEATSINKING

To maintain high reliability, the die temperature of any IC should be kept as low as practicable, preferably below 100°C. Although most AMP-01 application circuits will produce very little internal heat — little more than the quiescent dissipation of 90mW — some circuits will raise that to several hundred milliwatts (for example, the 4-20mA current transmitter application, Figure 8). Excessive dissipation will cause thermal shutdown of the output stage thus protecting the device from damage. A heatsink is recommended, however, to reduce the die temperature.

Several appropriate heatsinks are available; the Thermalloy 6010B is especially easy to use and is inexpensive. Intended for dual-in-line packages, the heatsink may be attached with a cyanoacrylate adhesive. This heatsink reduces the thermal resistance between the junction and ambient environment to approximately 80°C/W. Junction (die) temperature can then be calculated by using the relationship:

$$P_d = \frac{T_j - T_a}{\theta_{ja}}$$

where T_j and T_a are the junction and ambient temperatures respectively, θ_{ja} is the thermal resistance from junction to ambient, and P_d is the device's internal dissipation.

OVERVOLTAGE PROTECTION

Instrumentation amplifiers invariably sit at the front end of instrumentation systems where there is a high probability of exposure to overloads. Voltage transients, failure of a transducer, or removal of the amplifier power supply while the signal source is connected may destroy or degrade the performance of an unprotected amplifier. Although it is impractical to protect an IC internally against connection to power lines, it is relatively easy to provide protection against typical system overloads.

The AMP-01 is internally protected against overloads for gains of up to 100. At higher gains, the protection is reduced and some external measures may be required. Limited internal overload protection was used so that noise performance would not be significantly degraded.

AMP-01 noise level approaches the theoretical noise floor of the input stage which would be $4\text{nV}/\sqrt{\text{Hz}}$ at 1kHz when the gain is set at 1000. Noise is the result of shot noise in the input devices and Johnson noise in the resistors. Resistor noise is calculated from the values of R_G (200Ω at a gain of 1000) and the input protection resistors (250Ω). Active loads for the input transistors contribute less than $1\text{nV}/\sqrt{\text{Hz}}$ of noise. The measured noise level is typically $5\text{nV}/\sqrt{\text{Hz}}$.

Diodes across the input transistor's base-emitter junctions, combined with 250Ω input resistors and R_G, protect against differential inputs of up to ±20V for gains of up to 100. The diodes also prevent avalanche breakdown that would degrade the I_B and I_{OS} specifications. Decreasing the value of R_G for gains above 100 limits the maximum input overload protection to ±10V. External series resistors could be added to guard against higher voltage levels at the input, but resistors alone increase the input noise and degrade the signal-to-noise ratio, especially at high gains.

Protection can also be achieved by connecting back-to-back 9.1V zener diodes across the differential inputs. This technique does not affect the input noise level and can be used down to a gain of 2 with minimal increase in input current. Although voltage-clamping elements look like short circuits at the limiting voltage, the majority of signal sources provide less than 50mA, producing power levels that are easily handled by low-power zeners.

Simultaneous connection of the differential inputs to a low-impedance signal above 10V during normal circuit operation is unlikely. However, additional protection involves adding 100Ω current-limiting resistors in each signal path prior to the voltage clamp; the resistors increase the input noise level to just $5.4\text{nV}/\sqrt{\text{Hz}}$ (refer to Figure 6).

Input components, be they multiplexers or resistors, should be carefully selected to prevent the formation of thermocouple junctions which would degrade the input signal.

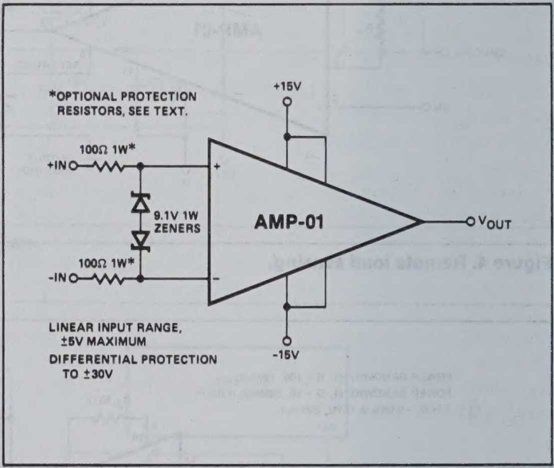
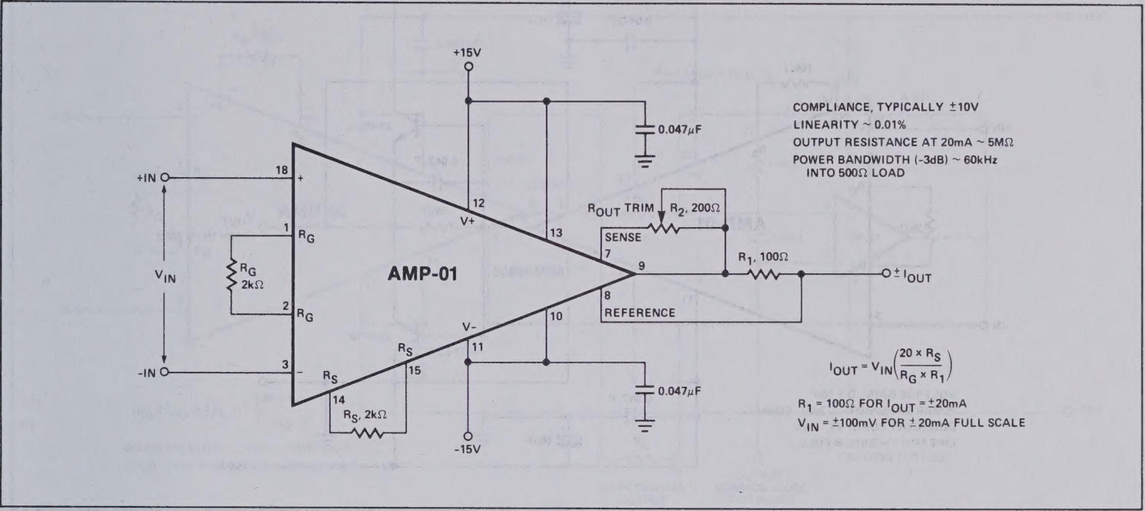


Figure 6. Input overvoltage protection for gains 2 to 10,000.

POWER SUPPLY CONSIDERATIONS

Achieving the rated performance of precision amplifiers in a practical circuit requires careful attention to external influences. For example, supply noise and changes in the nominal voltage directly affect the input offset voltage. A PSR of 80dB means that a change of 100mV on the supply, not an uncommon value, will produce a 10μV input offset change. Consequently, care should be taken in choosing a power unit that has a low output noise level, good line and load regulation, and good temperature stability.

APPLICATIONS INFORMATION

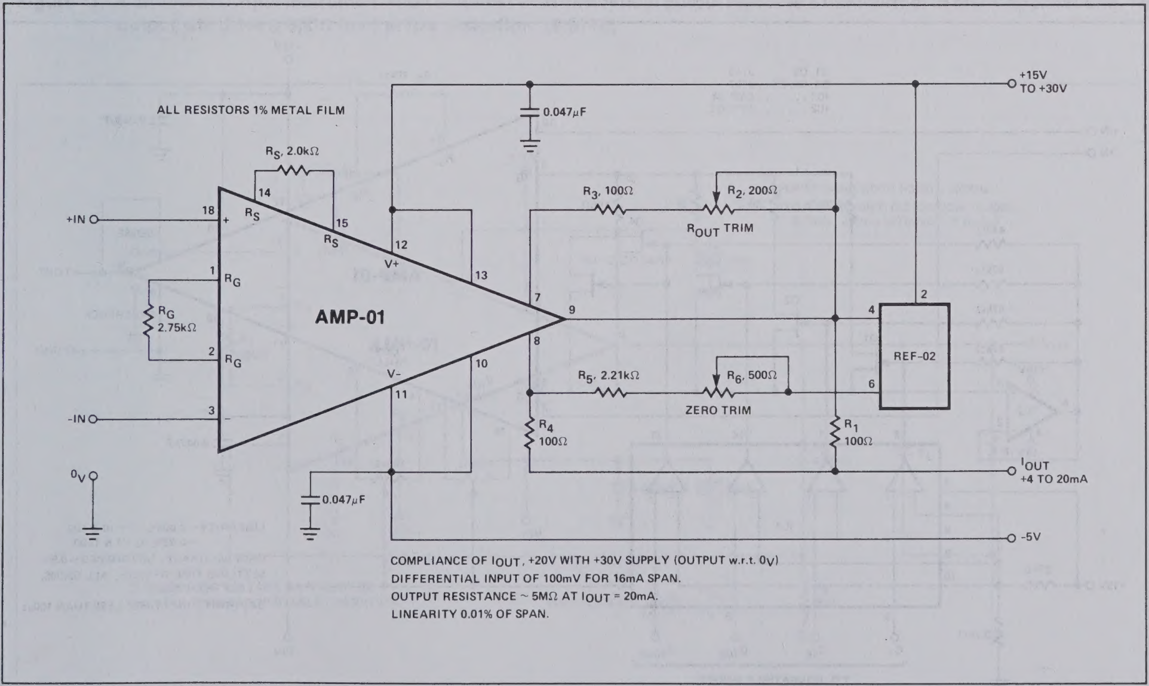

+15V
0.047µF
+IN
18
+
1
R_G
R_G
2kΩ
V_{IN}
2
R_G
3
-IN
−
R_S
14
R_S, 2kΩ
R_S
15
12
V+
13
AMP-01
10
V-
11
-15V
0.047µF
R_{OUT} TRIM
R_2, 200Ω
SENSE
7
9
8
REFERENCE
R_1, 100Ω
$\pm I_{OUT}$

COMPLIANCE, TYPICALLY ±10V
LINEARITY ~ 0.01%
OUTPUT RESISTANCE AT 20mA ~ 5MΩ
POWER BANDWIDTH (-3dB) ~ 60kHz
INTO 500Ω LOAD

$$I_{OUT} = V_{IN}\left(\frac{20 \times R_S}{R_G \times R_1}\right)$$

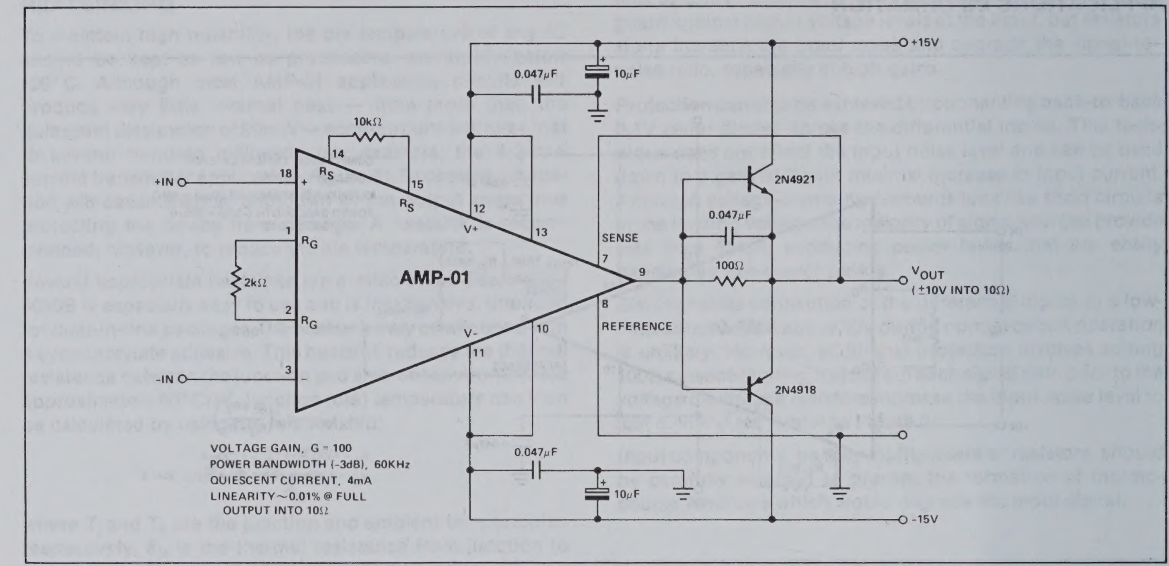
$R_1 = 100\Omega$ FOR $I_{OUT} = \pm 20mA$
$V_{IN} = \pm 100mV$ FOR ±20mA FULL SCALE

Figure 7. High-compliance bipolar current source with 13-bit linearity.


ALL RESISTORS 1% METAL FILM
R_S, 2.0kΩ
14
R_S
15
R_S
18
+
+IN
1
R_G
R_G
2.75kΩ
2
R_G
3
−
-IN
AMP-01
12
V+
13
7
9
8
10
V-
11
0.047µF
0.047µF
0_V
R_3, 100Ω
R_2, 200Ω
R_{OUT} TRIM
R_5, 2.21kΩ
R_6, 500Ω
ZERO TRIM
R_4
100Ω
R_1
100Ω
REF-02
2
4
6
+15V
TO +30V
I_{OUT}
+4 TO 20mA
-5V

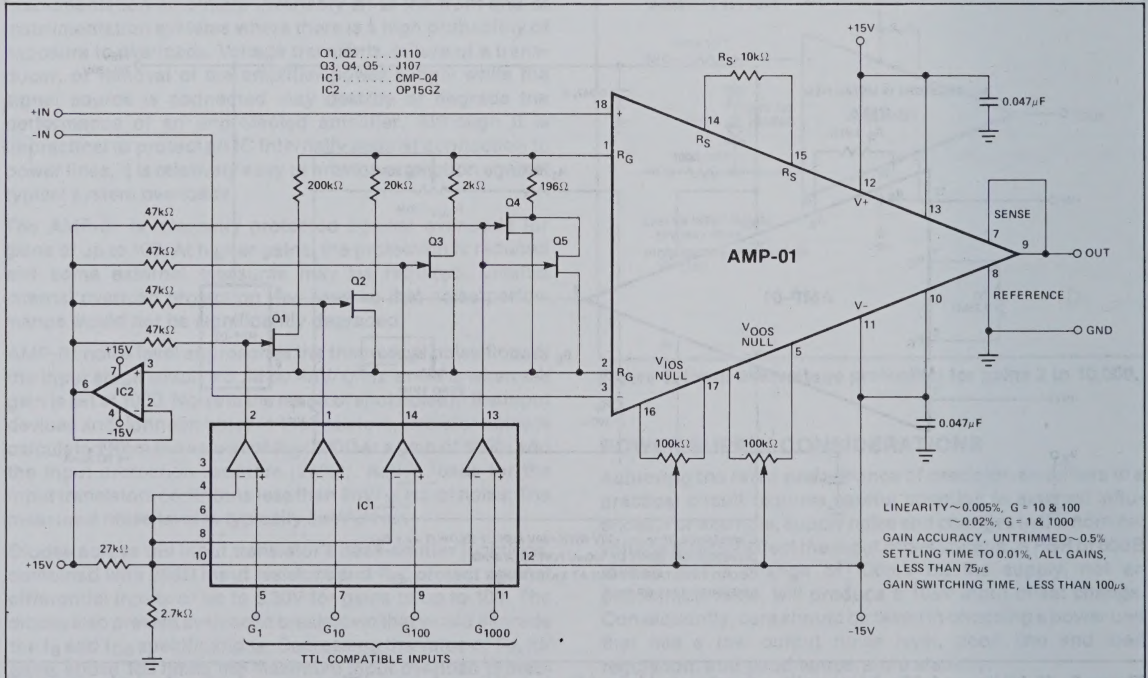
COMPLIANCE OF I_{OUT}, +20V WITH +30V SUPPLY (OUTPUT w.r.t. 0_V)
DIFFERENTIAL INPUT OF 100mV FOR 16mA SPAN.
OUTPUT RESISTANCE ~ 5MΩ AT I_{OUT} = 20mA.
LINEARITY 0.01% OF SPAN.

Figure 8. 13-bit linear 4-20mA transmitter constructed by adding a voltage reference. Thermocouple signals can be accepted without preamplification.


0.047µF
10µF
+15V
10kΩ
14
R_S
18
+IN
+
15
R_S
12
V+
13
1
R_G
2kΩ
AMP-01
2
R_G
V-
10
11
3
-IN
2N4921
0.047µF
SENSE
7
100Ω
9
V_OUT
(±10V INTO 10Ω)
8
REFERENCE
2N4918
0.047µF
10µF
-15V

VOLTAGE GAIN, G = 100
POWER BANDWIDTH (-3dB), 60KHz
QUIESCENT CURRENT, 4mA
LINEARITY ~ 0.01% @ FULL
OUTPUT INTO 10Ω

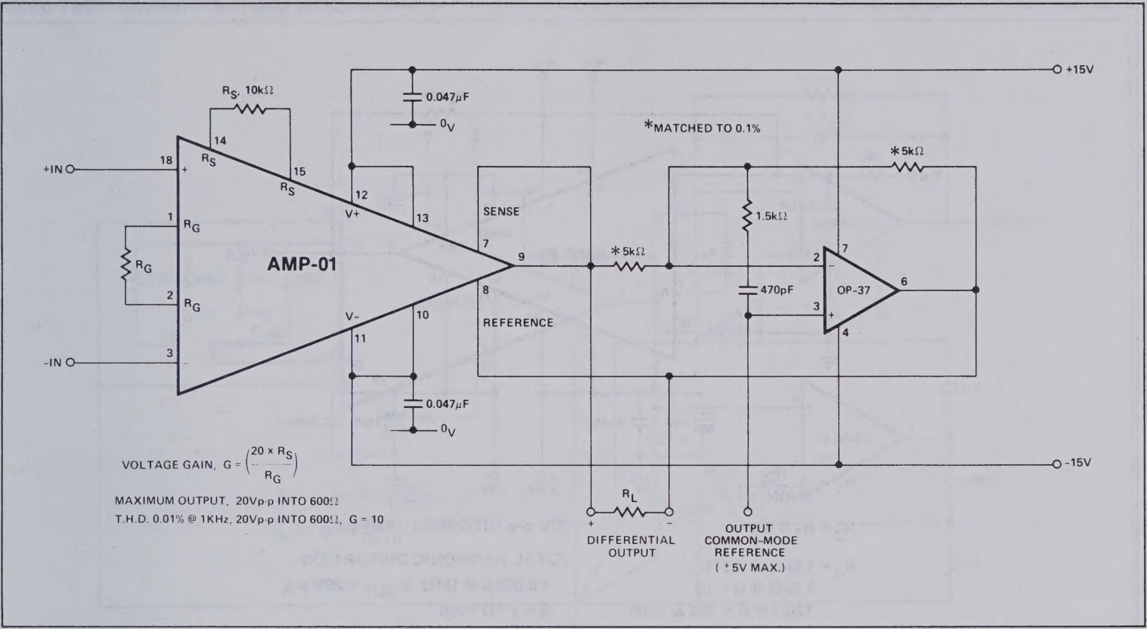
Figure 9. Adding two transistors increases output current to ±1A without affecting the quiescent current of 4mA. Power bandwidth is 60kHz.


+IN
-IN
200kΩ
20kΩ
2kΩ
196Ω
47kΩ
47kΩ
47kΩ
47kΩ
Q1
Q2
Q3
Q4
Q5
+15V
IC2
-15V
IC1
27kΩ
+15V
2.7kΩ
G_1
G_10
G_100
G_1000
TTL COMPATIBLE INPUTS
+15V
R_S, 10kΩ
0.047µF
18
14
R_S
15
R_S
12
V+
13
SENSE
7
9
OUT
AMP-01
8
REFERENCE
10
GND
V-
11
V_OOS NULL
5
V_IOS NULL
4
17
16
100kΩ
100kΩ
R_G
2
3
1
0.047µF
-15V

Q1, Q2 . . . . . J110
Q3, Q4, Q5 . . J107
IC1 . . . . CMP-04
IC2 . . . . OP15GZ

LINEARITY ~ 0.005%, G = 10 & 100
~ 0.02%, G = 1 & 1000
GAIN ACCURACY, UNTRIMMED ~ 0.5%
SETTLING TIME TO 0.01%, ALL GAINS,
LESS THAN 75µs
GAIN SWITCHING TIME, LESS THAN 100µs

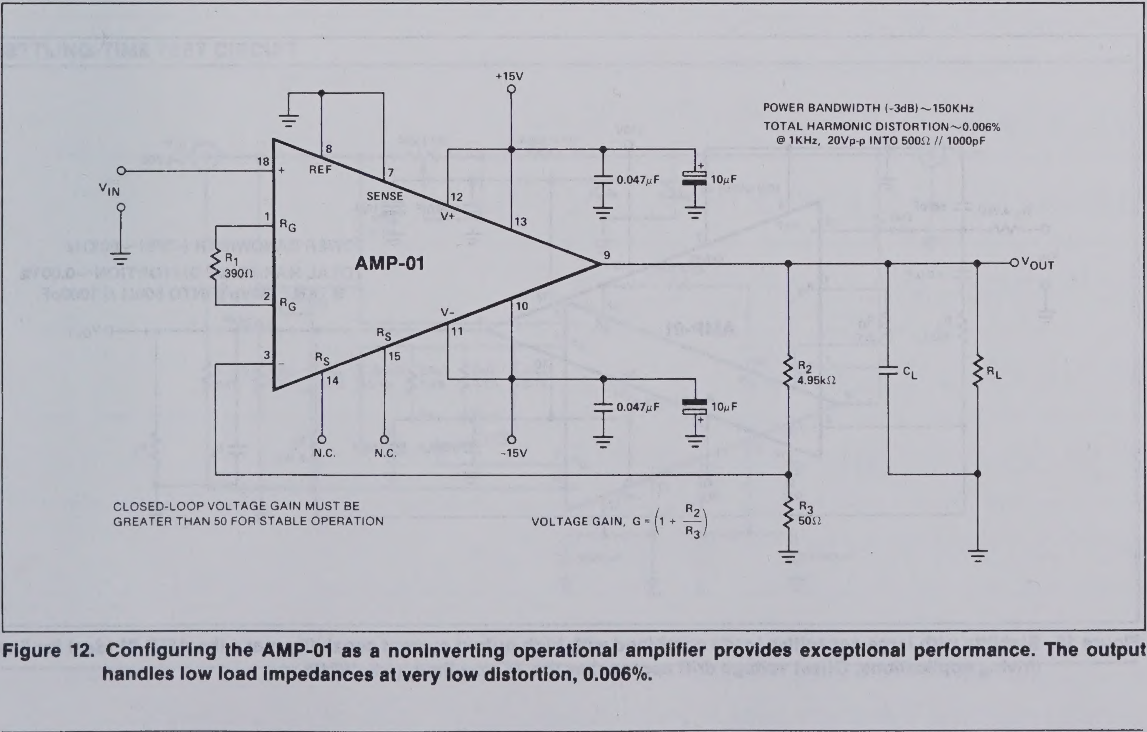
Figure 10. The AMP-01 makes an excellent programmable-gain instrumentation amplifier. Combined gain-switching and settling time to 13-bits falls below 100µs. Linearity is better than 12-bits over a gain range 1 to 1000.


R_S, 10kΩ
0.047μF
0V
*MATCHED TO 0.1%
+15V
+IN
18
+
14
R_S
15
R_S
12
V+
13
SENSE
7
*5kΩ
1.5kΩ
1
R_G
R_G
AMP-01
9
*5kΩ
2
–
7
470pF
OP-37
6
3
+
2
R_G
8
10
REFERENCE
4
–IN
3
–
V–
11
0.047μF
0V
–15V
R_L
+
–
DIFFERENTIAL OUTPUT
OUTPUT COMMON-MODE REFERENCE (±5V MAX.)

VOLTAGE GAIN, $G = \left(\frac{20 \times R_S}{R_G}\right)$

MAXIMUM OUTPUT, 20Vp-p INTO 600Ω
T.H.D. 0.01% @ 1KHz, 20Vp-p INTO 600Ω, G = 10

Figure 11. A differential input instrumentation amplifier with differential output replaces a transformer in many applications. The output will drive a 600Ω load at low distortion, (0.01%).


+15V
8
REF
18
+
7
SENSE
12
V+
13
0.047μF
+
10μF
V_{IN}
1
R_G
R_1
390Ω
AMP-01
9
V_{OUT}
2
R_G
10
V–
R_S
11
3
–
R_S
15
14
R_2
4.95kΩ
C_L
R_L
0.047μF
10μF
+
N.C.
N.C.
–15V
R_3
50Ω

POWER BANDWIDTH (-3dB) ~ 150KHz
TOTAL HARMONIC DISTORTION ~ 0.006%
@ 1KHz, 20Vp-p INTO 500Ω // 1000pF

CLOSED-LOOP VOLTAGE GAIN MUST BE GREATER THAN 50 FOR STABLE OPERATION

VOLTAGE GAIN, $G = \left(1 + \frac{R_2}{R_3}\right)$

Figure 12. Configuring the AMP-01 as a noninverting operational amplifier provides exceptional performance. The output handles low load impedances at very low distortion, 0.006%.

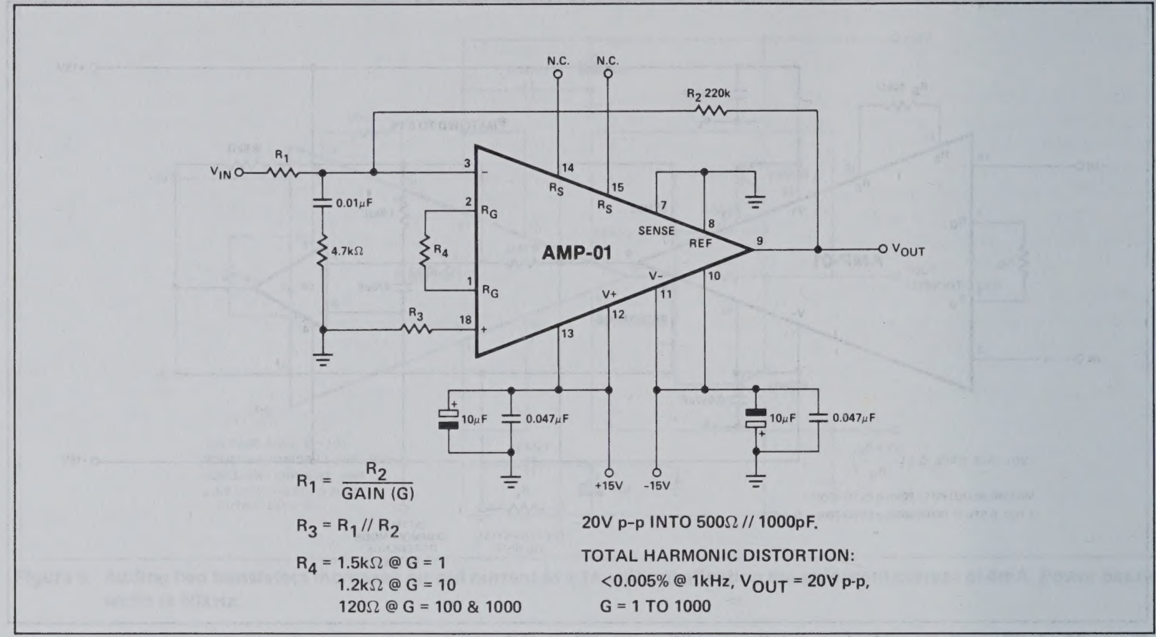

N.C.
N.C.
R_2 220k
R_1
V_{IN}
3
–
14
R_S
15
R_S
7
SENSE
8
REF
9
V_{OUT}
2
R_G
R_4
AMP-01
1
R_G
R_3
18
+
13
12
V+
V-
11
10
0.01µF
4.7kΩ
10µF
0.047µF
10µF
0.047µF
+15V
-15V
$R_1 = \frac{R_2}{\text{GAIN (G)}}$
$R_3 = R_1 // R_2$
R_4 = 1.5kΩ @ G = 1
1.2kΩ @ G = 10
120Ω @ G = 100 & 1000
20V p-p INTO 500Ω // 1000pF.
TOTAL HARMONIC DISTORTION:
<0.005% @ 1kHz, V_{OUT} = 20V p-p,
G = 1 TO 1000

Figure 13. The inverting operational amplifier configuration has excellent linearity over the gain range 1 to 1000, typically 0.005%. Offset voltage drift at unity gain is improved over the drift in the instrumentation amplifier configuration.

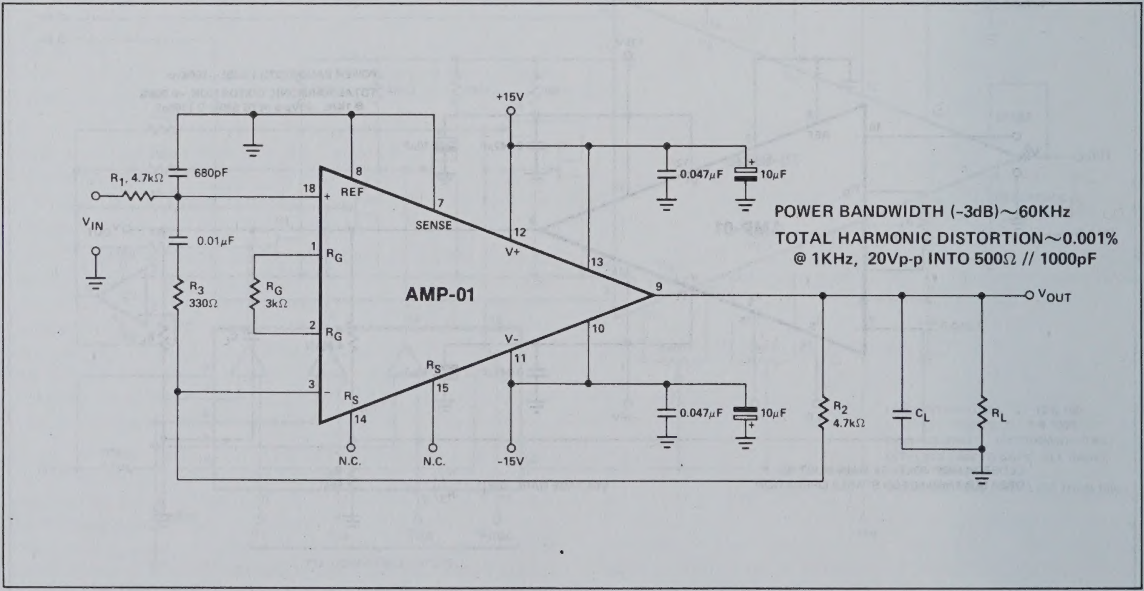
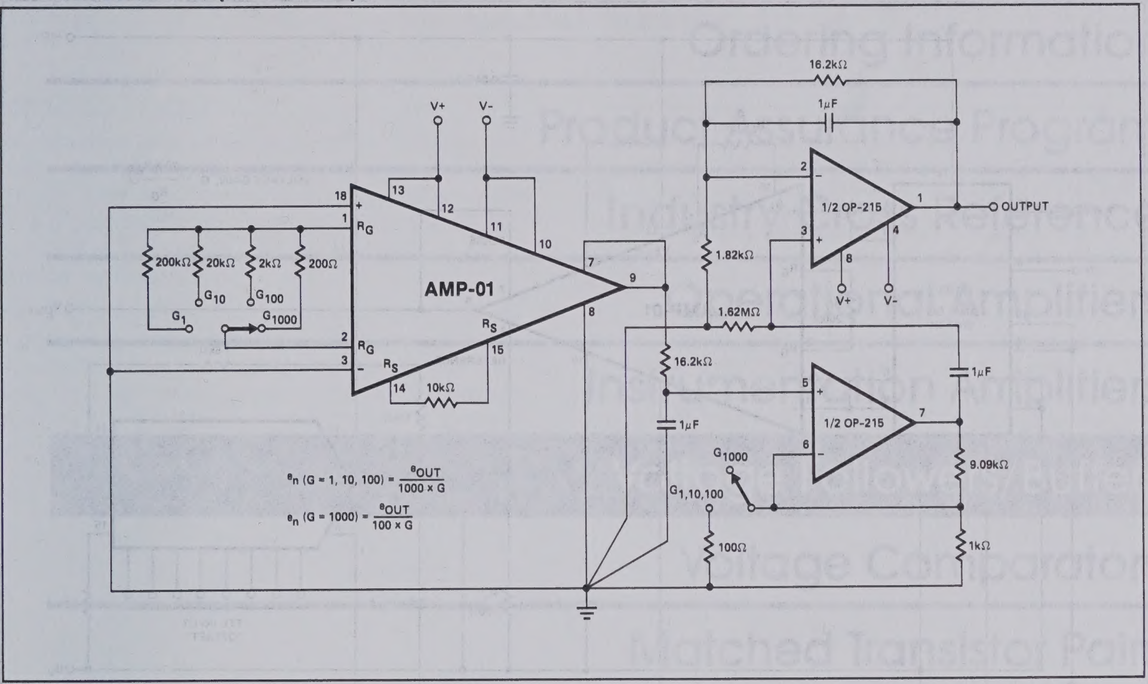
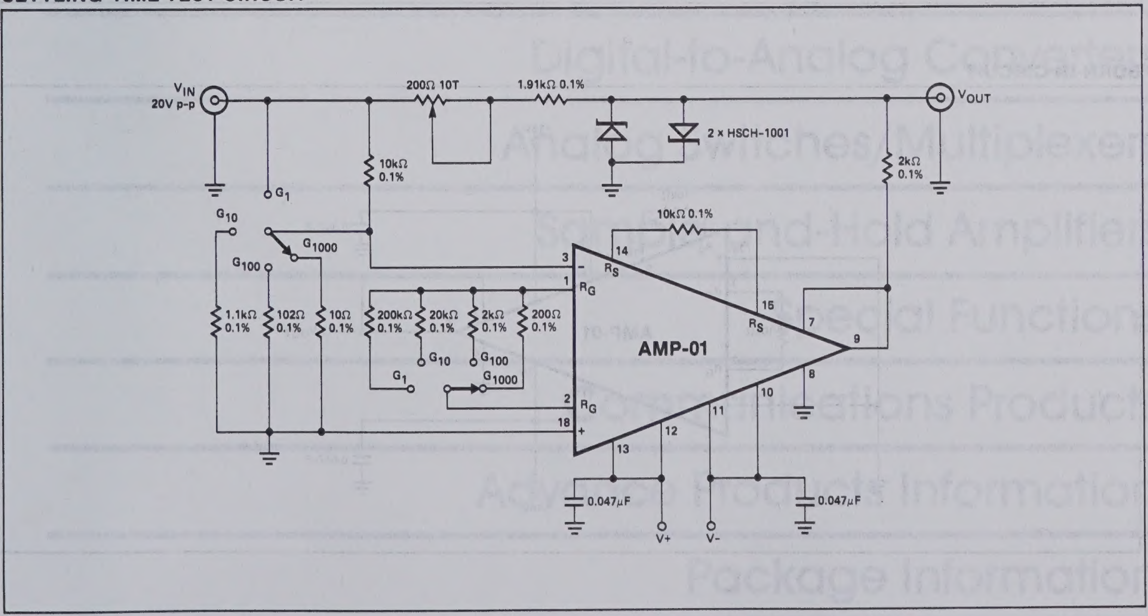

+15V
R_1, 4.7kΩ
680pF
V_{IN}
0.01µF
R_3 330Ω
R_G 3kΩ
18
+
REF
8
7
SENSE
12
V+
13
1
R_G
9
AMP-01
2
R_G
10
V-
11
R_S
15
3
–
R_S
14
N.C.
N.C.
-15V
0.047µF
10µF
0.047µF
10µF
R_2 4.7kΩ
C_L
R_L
V_{OUT}
POWER BANDWIDTH (-3dB)~60KHz
TOTAL HARMONIC DISTORTION~0.001%
@ 1KHz, 20Vp-p INTO 500Ω // 1000pF

Figure 14. Stability with large capacitive loads combined with high output current capability make the AMP-01 ideal for line driving applications. Offset voltage drift approaches the TCV_{IOS} limit, (0.3µV/°C).

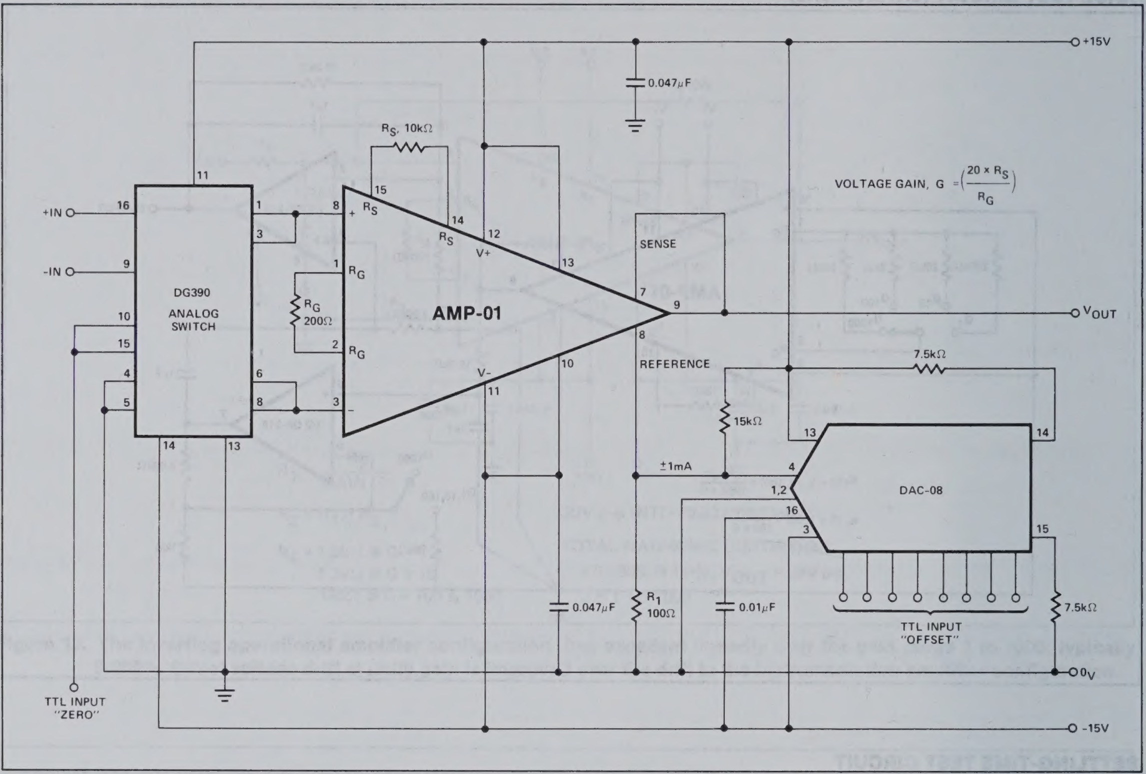
NOISE TEST CIRCUIT (0.1Hz to 10Hz)


V+
V-
AMP-01
18
1
2
3
13
12
11
10
7
9
8
15
14
+
−
RG
RG
RS
RS
200kΩ
20kΩ
2kΩ
200Ω
G1
G10
G100
G1000
10kΩ
16.2kΩ
1µF
1/2 OP-215
OUTPUT
1.82kΩ
1.62MΩ
16.2kΩ
1µF
1µF
1/2 OP-215
9.09kΩ
G1000
G1,10,100
100Ω
1kΩ
e_n (G = 1, 10, 100) = $\frac{e_{OUT}}{1000 \times G}$
e_n (G = 1000) = $\frac{e_{OUT}}{100 \times G}$

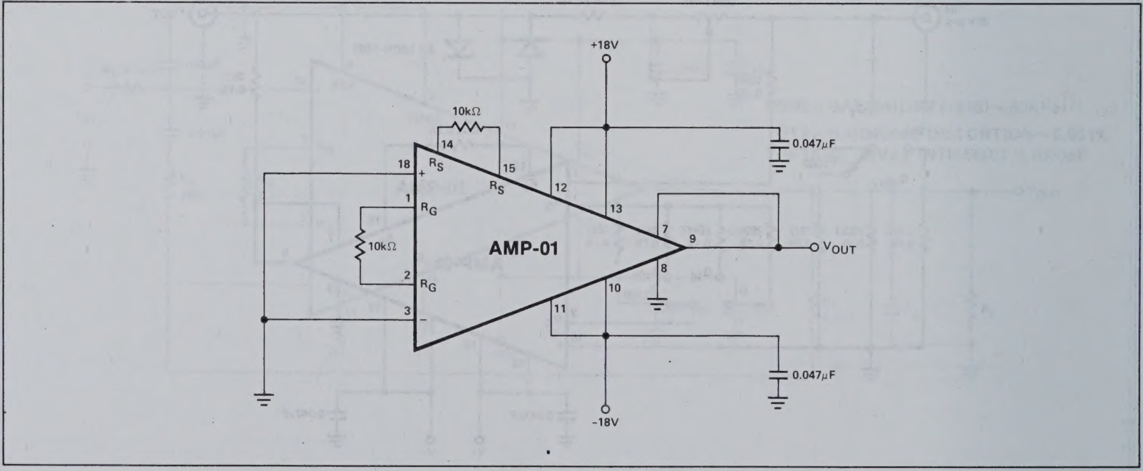
SETTLING-TIME TEST CIRCUIT


VIN
20V p-p
200Ω 10T
1.91kΩ 0.1%
2 × HSCH-1001
VOUT
2kΩ 0.1%
10kΩ 0.1%
G1
G10
G100
G1000
10kΩ 0.1%
1.1kΩ 0.1%
102Ω 0.1%
10Ω 0.1%
200kΩ 0.1%
20kΩ 0.1%
2kΩ 0.1%
200Ω 0.1%
G10
G100
G1
G1000
AMP-01
RS
RS
RG
RG
3
1
2
18
14
15
7
9
8
10
11
12
13
0.047µF
0.047µF
V+
V-

INSTRUMENTATION AMPLIFIER WITH AUTO-ZERO


+15V
0.047μF
R_S, 10kΩ
VOLTAGE GAIN, G = $\left(\frac{20 \times R_S}{R_G}\right)$
+IN
-IN
DG390
ANALOG
SWITCH
R_G
200Ω
AMP-01
+
−
R_S
R_G
V+
V-
SENSE
REFERENCE
V_{OUT}
7.5kΩ
15kΩ
±1mA
DAC-08
R_1
100Ω
0.047μF
0.01μF
7.5kΩ
TTL INPUT
"OFFSET"
TTL INPUT
"ZERO"
0V
-15V
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
1,2

BURN-IN CIRCUIT


+18V
10kΩ
0.047μF
R_S
R_G
10kΩ
AMP-01
+
−
V_{OUT}
0.047μF
-18V
1
2
3
7
8
9
10
11
12
13
14
15
18

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VOLTAGE FOLLOWERS—BUFFERS

Introduction 7-3

BUF-03 7-4
High-Speed Voltage Follower/Buffer

VOLTAGE FOLLOWERS BUFFERS

INTRODUCTION

The function of a unity-gain buffer is to accurately reproduce the input signal under widely-varying load conditions. To do this, buffers must have high input impedance, wide bandwidth, and high output drive. Offsets and gain error need to be minimized.

The buffer function can be implemented by use of general-purpose operational amplifiers connected as unity-gain voltage followers, but higher performance can be obtained by optimizing a circuit specifically for buffering. A design dedicated to unity-gain buffering and using no feedback can provide better frequency response. In addition, output current can be increased substantially beyond that of conventional IC operational amplifiers.

The BUF-03 is a high-speed, unity-gain IC that is optimized for the buffer function. A FET input provides high input impedance. On-chip zener-zap trimming is used to reduce the offset voltage. The output stage is designed to supply approximately 70mA of peak current. These features combine to make the BUF-03 an IC analog buffer of unique capability.

BUF-03 HIGH-SPEED VOLTAGE FOLLOWER/BUFFER

FEATURES

- **Very High Slew Rate** 250V/μsec
- **Wide Bandwidth** 63MHz
- **Load Drive Current** .... 70mA Peak
- **Easily Drives Large Capacitive Loads Without Oscillation**
- **High Input Resistance** .... $5 \times 10^{11}\Omega$
- **Low Output Resistance** 2Ω
- **Very Low Bias Current (Warmed-Up)** 150pA
- **Low Offset Voltage** 2mV
- **Unity Gain** 0.997V/V
- **Excellent Gain Linearity** 0.015%

GENERAL DESCRIPTION

The BUF-03 is the first very high-speed monolithic voltage follower. Featuring performance previously unobtainable in a monolithic unit, it offers a combination of both exceptional speed and excellent input/output specifications. Implemented in an open-loop circuit employing source followers and emitter followers, the BUF-03 utilizes a quasi-quad FET input structure to optimize both speed and D.C. input characteristics. On-chip zener-zap trimming is used to achieve low offset voltage while careful biasing throughout results in excellent gain linearity over the full input voltage range.

Applications for which the BUF-03 is well-suited include high-speed line drivers, isolation amplifiers for driving reactive loads, and high-speed sample-hold circuits.

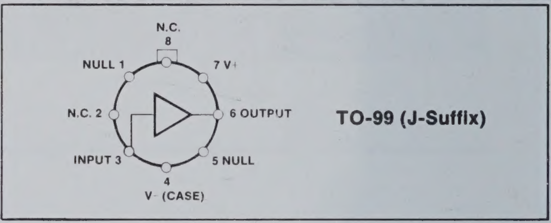
ORDERING INFORMATION†

$T_A = 25°C$ V_{OS} MAX (mV)	PACKAGE TO-99 8-PIN	OPERATING TEMPERATURE RANGE
6	BUF03AJ*	MIL
6	BUF03EJ	COM
15	BUF03BJ*	MIL
15	BUF03FJ	COM

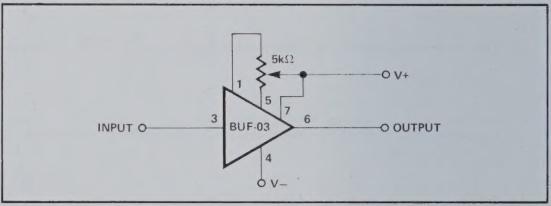
*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

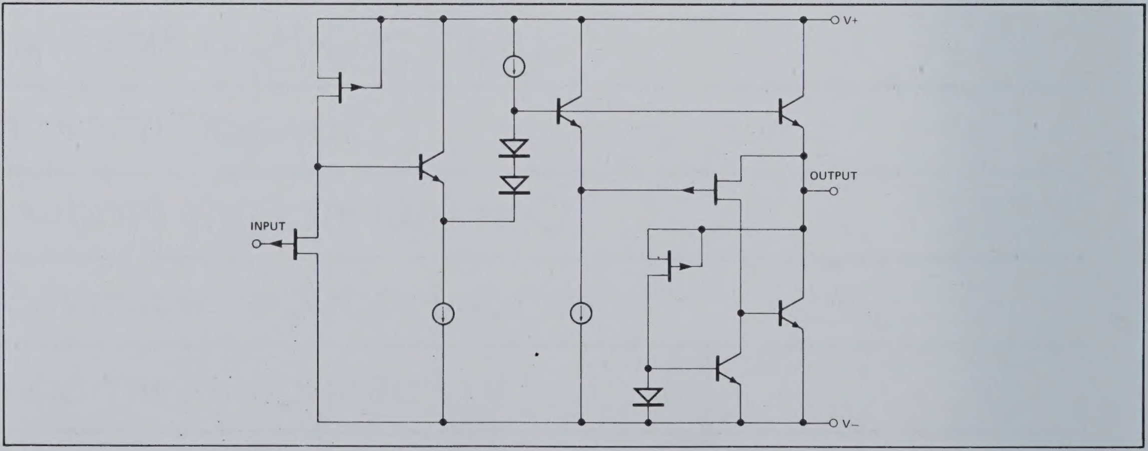
PIN CONNECTIONS



OPTIONAL OFFSET NULLING CIRCUIT



SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note)

Supply Voltage (V+ to V−)	36V
Internal Power Dissipation (P_d) (see curves)	
in still air, no heat sink	1.05W
with heat sink, $\theta_{JA} = 90°C/W$	1.40W
Input Voltage (for $V_S < \pm18V$, maximum input voltage is equal to supply)	±18V
Continuous Output Current	70mA
Peak Output Current	100mA
Short-Circuit Protection (Maximum P_d or T_j not to be exceeded)	Indefinite at 80mA
Maximum Junction Temperature (T_j)	175°C
Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	
BUF-03A, BUF-03B	−55°C to +125°C
BUF-03E, BUF-03F	0°C to +70°C
Lead Temperature (Soldering, 60 sec)	300°C
DICE Junction Temperature (T_j)	−65°C to +175°C

NOTE: Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $T_A = 25°C$, $T_{CHIP} = 75°C$, device fully warmed-up, unless otherwise noted. (Note 1)

			BUF-03A/E			BUF-03B/F			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
AC SPECIFICATIONS									
Slew Rate	SR	$R_L \geq 2k\Omega$, $C_L = 50pF$	220	250	—	180	250	—	V/μsec
Power Bandwidth	PBW	$V_{IN} = 10V_{p-p}$, $R_L \geq 2k\Omega$	—	9	—	—	8	—	MHz
Bandwidth	BW	$\Delta V_{IN} = \leq 2V_{p-p}$	—	63	—	—	50	—	MHz
Settling Time	t_S	To 0.1%, ±10V step	—	90	—	—	100	—	nsec
Capacitive Load Capability	C_{LOAD}	No Oscillations	—	1	—	—	1	—	μF
Propagation Delay	t_d	Step Input	—	7	—	—	7	—	nsec
Rise Time	t_r	$\Delta V = 0.5V$	—	7	—	—	7	—	nsec
Wide Band Input Noise Voltage	V_n	DC to 50MHz	—	350	—	—	400	—	μV_{RMS}
Input Noise Voltage Density	e_n	f = 10kHz	—	50	—	—	60	—	$nV/\sqrt{Hz}$
DC SPECIFICATIONS									
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	—	2	6	—	4	15	mV
Input Bias Current	I_B		—	150	400	—	180	700	pA
Input Resistance	R_{IN}		—	5×10^{11}		—	4×10^{11}	—	Ω
Voltage Gain ($V_{IN} = \pm10V$)	A_{VO}	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	0.9960 0.9945 0.9925	0.9975 0.9960 0.9945	— — —	0.9940 0.9930 0.9905	0.9970 0.9950 0.9930	— — —	V/V
Nonlinearity (Note 2)	NL	$V_{IN} = \pm10V$, $R_L \geq 2k\Omega$ $V_{IN} = \pm7V$, $R_L \geq 1k\Omega$	— —	0.015 0.013	0.023 0.023	— —	0.017 0.015	0.03 0.03	%F.S.
Maximum Output Error	OUT_{error}	$V_{IN} = +10V, 0V, -10V$ $R_S = 0$ to $20k\Omega$ $R_L \geq 2k\Omega$ in all combinations	—	40	60	—	50	85	mV
Power Supply Rejection Ratio	PSRR	$V_S = \pm6V$ to $\pm18V$	—	0.10	0.71	—	0.15	1.42	mV/V
Supply Current	I_{SY}	No Load	—	19	25	—	19	25	mA
Peak Load Current	$I_{L(PK)}$		—	70	—	—	70	—	mA
Output Resistance	R_O		—	2	—	—	2	—	Ω
Offset Voltage Nulling Range	ΔV_{OS}	$R_P \geq 1k\Omega$	—	±80	—	—	±80	—	mV
Input Voltage Range (Reduced Accuracy)	IVR		—	±11.5	—	—	±11.5	—	V

NOTES:

1. The BUF-03 package thermal resistance, in still air, is 145°C/W (45°C/W junction-to-case, 100°C/W case-to-ambient). The chip temperature of 75°C is achieved by reducing the case-to-ambient thermal resistance to 45°C/W. An inexpensive heat sink, such as the Thermalloy 2271 or 6203, is recommended for use in this application. In addition, if the device is operated in a forced-air environment, or is attached to a PC board which has good thermal conductivity, the chip temperature may be further reduced. If no heat sinking is used, the chip temperature (in still air) may exceed 105°C. The effect of this elevated temperature will be to increase the input bias current by a factor of eight, increase the V_{OS} specification by $TCV_{OS} \times 30°C$, and reduce device speed by 10%.
2. Nonlinearity is computed using linear regression techniques with data from five points (e.g., −10V, −5V, 0V, +5V, and +10V for ±10V full-scale linearity).

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \le T_A \le +125°C$, $T_{CHIP}(MAX) = +165°C$, device fully warmed-up, unless otherwise noted. (Note 1)

			BUF-03A			BUF-03B			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Slew Rate	SR	$R_L \ge 2k\Omega$, $C_L = 50pF$	—	220	—	—	220	—	V/μsec
Input Offset Voltage	V_{OS}	$R_S \le 2k\Omega$	—	6	20	—	10	35	mV
Average Input Offset Voltage Drift	TCV_{OS}	$R_S \le 2k\Omega$, (Note 2)	—	50	100	—	90	170	μV/°C
Input Bias Current	I_B	$T_A = +125°C$	—	25	75	—	30	90	nA
Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$, $V_{IN} = \pm 10V$	0.9920	0.9955	—	0.9902	0.9942	—	V/V
Gain Drift with Temperature			—	5	—	—	8	—	ppm/°C
Power Supply Rejection Ratio	PSRR	$V_S = \pm 7V$ to $\pm 15V$	—	0.15	1.26	—	0.20	2.24	mV/V
Supply Current	I_{SY}	$T_A = +125°C$	—	18	24	—	18	24	mA

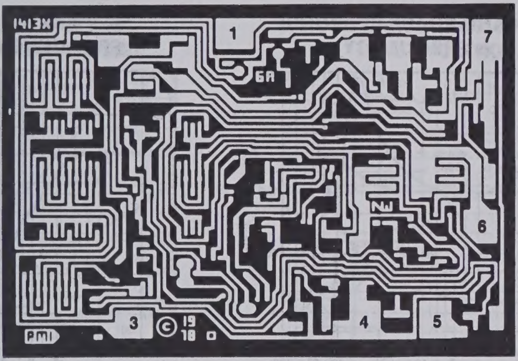
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $0°C \le T_A \le +70°C$, $T_{CHIP}(MAX) = +120°C$, device fully warmed-up, unless otherwise noted.

			BUF-03E			BUF-03F			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Slew Rate	SR	$R_L \ge 2k\Omega$	—	240	—	—	240	—	V/μsec
Input Offset Voltage	V_{OS}	$R_S \le 2k\Omega$, $C_L = 50pF$	—	4	14	—	7	28	mV
Average Input Offset Voltage Drift	TCV_{OS}	$R_S \le 2k\Omega$, (Note 2)	—	40	90	—	80	150	μV/°C
Input Bias Current	I_B	$T_A = +70°C$	—	1.5	5	—	1.8	8	nA
Voltage Gain ($V_{IN} = \pm 10V$)	A_{VO}	$R_L \ge 2k\Omega$	0.9935	0.9958	—	0.9918	0.9946	—	V/V
Gain Drift with Temperature			—	5	—	—	8	—	ppm/°C
Power Supply Rejection Ratio	PSRR	$V_S = \pm 7V$ to $\pm 15V$	—	0.12	1	—	0.16	1.78	mV/V
Supply Current	I_{SY}	$T_A = +70°C$	—	19	25	—	19	25	mA

NOTES:

1. In order to operate the device at an ambient temperature of +125° C, more extensive heat sinking must be used to ensure that the chip temperature never exceeds the absolute maximum of +175° C. The chip temperature of +165° C is achieved by reducing the case-to-ambient thermal resistance to 30° C/W (e.g., Thermalloy 2227).
2. Guaranteed by design.

DICE CHARACTERISTICS



1. NULL
3. INPUT
4. NEGATIVE SUPPLY
5. NULL
6. OUTPUT
7. POSITIVE SUPPLY

DIE SIZE 0.070 × 0.048 inch, 3360 sq. mils
(1.78 × 1.22 mm, 2.17 sq. mm)

For additional DICE information refer to Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_j = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	BUF-03N LIMIT	BUF-03G LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	6	15	mV MAX
Slew Rate (Note 1)	SR	$R_L \geq 2k\Omega$, $C_L = 50pF$	220	180	V/μsec MIN
Voltage Gain	A_{VO}	$R_L \geq 10k\Omega$, $V_{IN} = \pm 10V$	0.9960	0.9940	V/V MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 6V$ to $\pm 18V$	0.71	1.42	mV/V MAX
Supply Current	I_{SY}	No Load	25	25	mA MAX

Note: Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

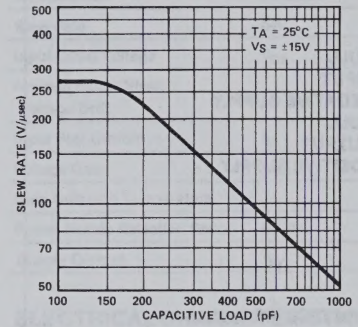
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_j = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	BUF-03N TYPICAL	BUF-03G TYPICAL	UNITS
Peak Load Current	$I_L(PK)$		70	70	mA
Input Bias Current	I_B		40	60	pA
Input Resistance	R_{IN}		5×10^{11}	5×10^{11}	Ω
Output Resistance	R_O		2	2	Ω
Offset Voltage Nulling Range	ΔV_{OS}	$R_P \geq 1k\Omega$	±80	±80	mV
Input Voltage Range (Reduced Accuracy)	IVR		±11.5	±11.5	V
Power Bandwidth	PBW	$V_{IN} = 10V_{p-p}$, $R_L \geq 2k\Omega$	9	8	MHz
Bandwidth	BW	$\Delta V_{IN} \leq 2V_{p-p}$	63	55	MHz
Settling Time	t_S	To 0.1%, ±10V step	90	100	ns
Capacitive Load Capacity	C_{LOAD}	No Oscillations	1	1	μF
Propagation Delay	t_d	Step Input	7	7	ns
Rise Time	t_r	$\Delta V_{IN} = 0.5V$	7	7	ns
Wide Band Input Noise Voltage	V_n	DC to 50MHz	350	400	μV_{RMS}
Input Noise Voltage Density	e_n	f = 10kHz	50	60	$nV/\sqrt{Hz}$

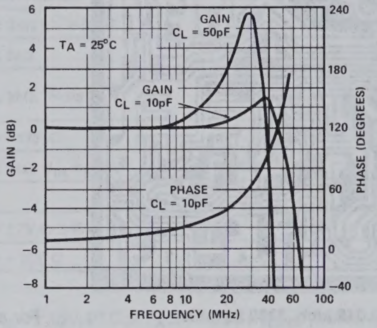
NOTE:
1. Sample tested.

TYPICAL PERFORMANCE CHARACTERISTICS

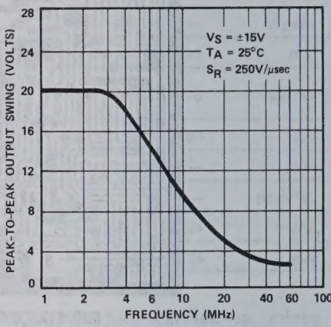
SLEW RATE vs CAPACITIVE LOAD



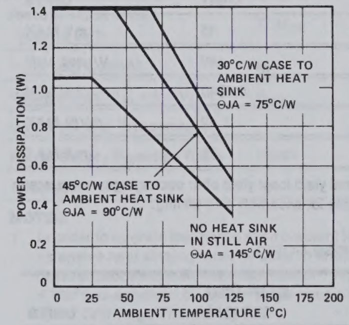
GAIN AND PHASE RESPONSE vs FREQUENCY



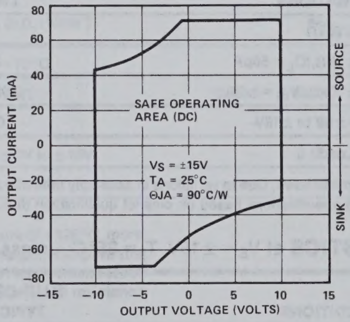
LARGE-SIGNAL FREQUENCY RESPONSE



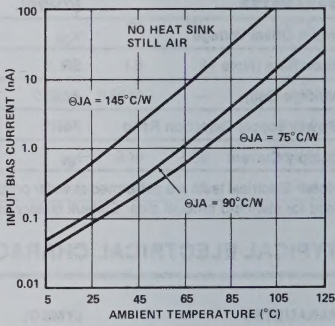
MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



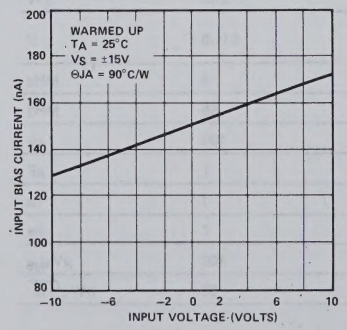
OUTPUT CURRENT vs OUTPUT VOLTAGE



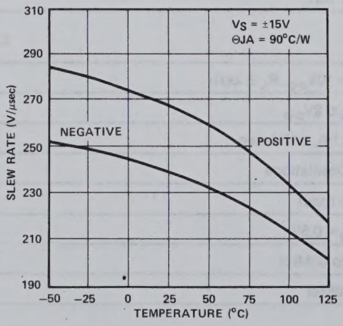
INPUT BIAS CURRENT vs TEMPERATURE (WARMED-UP)



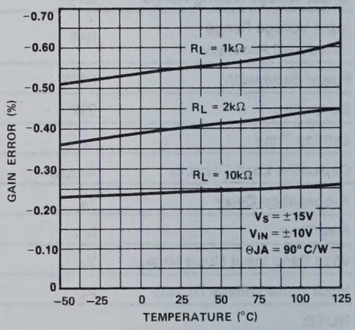
INPUT BIAS CURRENT vs INPUT VOLTAGE



SLEW RATE vs TEMPERATURE

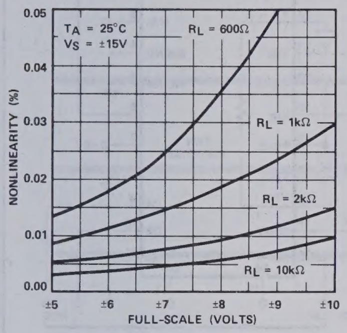


GAIN ERROR vs TEMPERATURE

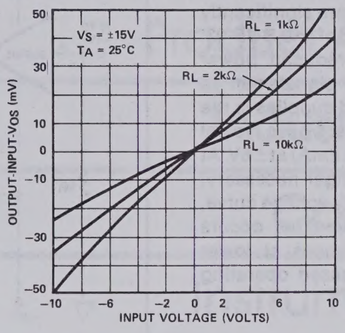


TYPICAL PERFORMANCE CHARACTERISTICS

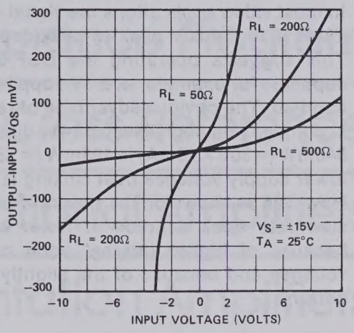
NONLINEARITY vs FULL-SCALE VOLTAGE



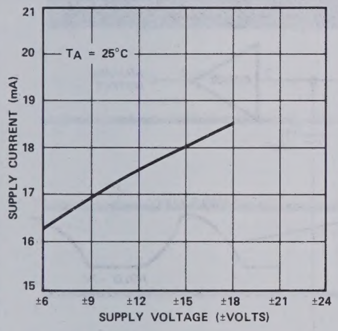
GAIN ERROR vs INPUT VOLTAGE



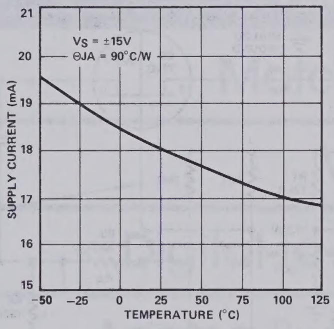
GAIN ERROR vs INPUT VOLTAGE



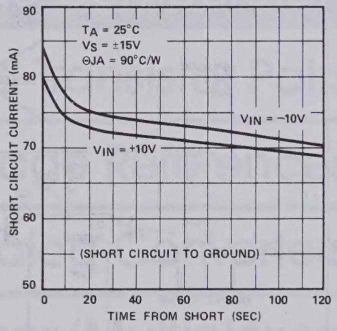
SUPPLY CURRENT vs SUPPLY VOLTAGE



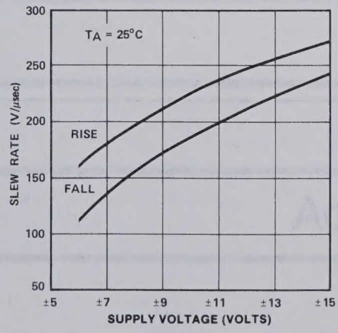
SUPPLY CURRENT vs TEMPERATURE



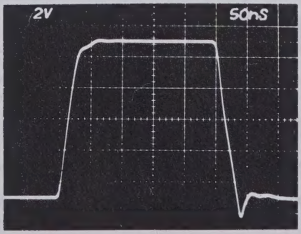
OUTPUT SHORT-CIRCUIT CURRENT vs TIME



SLEW RATE vs SUPPLY VOLTAGE



SLEW RATE

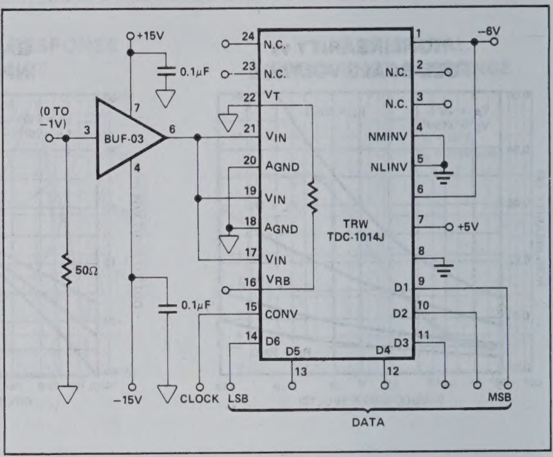


APPLICATIONS INFORMATION

OPERATING THE BUF-03 AT REDUCED POWER SUPPLIES

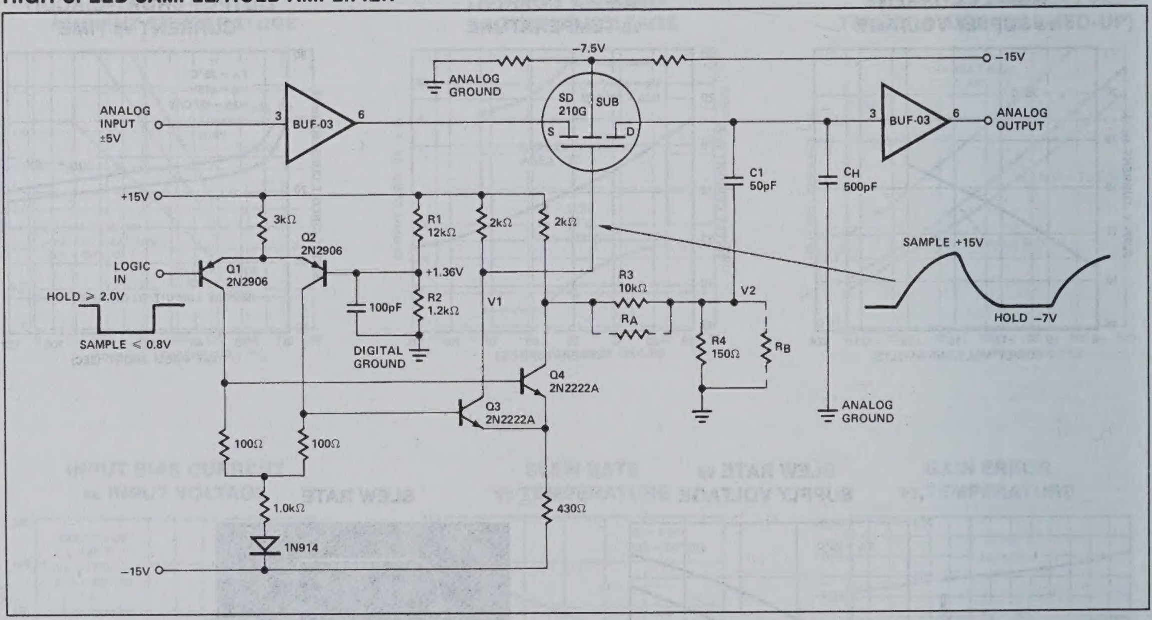
In most video applications the signal levels are significantly lower than the 20V peak-to-peak capability of the BUF-03. This suggests operating the BUF-03 at reduced power supplies; for example, at ±6V supplies ±2V signals can be handled. The obvious advantage of reduced supplies is the accompanying decrease in power dissipation: from a typical 540mW (=30V×18mA) to 195mW (=12V×16.2mA) at ±6V. At lower supply voltages heat sinking is no longer necessary. However, as shown on the slew rate vs supply voltage curve, slew rate does degrade at lower supplies. This occurs because of higher internal node capacitances at lower voltages and because of the slightly decreased operating current.

HIGH-SPEED 6-BIT A/D BUFFER



+15V
0.1µF
(0 TO −1V)
3
BUF-03
7
6
4
50Ω
0.1µF
−15V
CLOCK
LSB
MSB
DATA
24 N.C.
23 N.C.
22 VT
21 VIN
20 AGND
19 VIN
18 AGND
17 VIN
16 VRB
15 CONV
14 D6
13 D5
12 D4
11 D3
10 D2
9 D1
8
7 +5V
6
5 NLINV
4 NMINV
3 N.C.
2 N.C.
1 −6V
TRW TDC-1014J

HIGH-SPEED SAMPLE/HOLD AMPLIFIER



ANALOG INPUT ±5V
3
BUF-03
6
−7.5V
ANALOG GROUND
−15V
SD 210G
SUB
S
D
C1 50pF
CH 500pF
3
BUF-03
6
ANALOG OUTPUT
+15V
3kΩ
Q2 2N2906
R1 12kΩ
2kΩ
2kΩ
LOGIC IN
Q1 2N2906
+1.36V
HOLD ≥ 2.0V
SAMPLE ≤ 0.8V
100pF
R2 1.2kΩ
V1
R3 10kΩ
RA
V2
R4 150Ω
RB
DIGITAL GROUND
SAMPLE +15V
HOLD −7V
Q4 2N2222A
Q3 2N2222A
ANALOG GROUND
100Ω
100Ω
1.0kΩ
1N914
430Ω
−15V

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Quad Low-Power Voltage Comparators

VOLTAGE COMPARATORS

INTRODUCTION

A comparator provides a logic output indicating the amplitude relationship between two analog signal inputs.

When selecting a comparator, certain device parameters must be considered for proper design and application. These parameters are:

V_{OS} (Input Offset Voltage)
Response Time
Slew Rate
PSRR (Power Supply Rejection Ratio)
I_B (Input Bias Current)
CMVR (Common-Mode Voltage Range)
Output Configuration
Voltage Gain

The input offset voltage (V_{OS}) for a comparator should be as small as possible because in a high gain circuit it is the dominating factor that determines the exact threshold level. For this reason, comparators should be nulled or a Precision Comparator used so that the input differential voltage is as close to zero as practical when the output is at the logic switching threshold.

The voltage gain (A_V) determines the sensitivity and threshold accuracy of a comparator. For the ideal comparator, the gain could be considered infinite; and an extremely small voltage applied between the two inputs will cause a change in the output. In practice, some minimum voltage variation will be required at the input to effect a change in the output state. This minimum sensitivity will be determined from the voltage gain of the comparator. The relationship is as follows:

$$\Delta V_{IN(MIN)} = \frac{\Delta V_O}{A_V}$$

The quantity ΔV_O which is the difference between the high and low state of the output is generally chosen to be 2.5V to insure the matching of the comparator with the TTL load.

Precision Monolithics' comparator product line has expanded to five devices. The CMP-01 is a fast precision comparator with low offset voltage. The CMP-02 offers the CMP-01's offset voltage performance along with lower input bias currents.

The quad CMP-04 offers both low power and low offset voltages. Existing "139" type applications can be upgraded by the pin compatible CMP-04. The PM-139/239/339 devices provide equal performance to "139/239/339" type comparators.

The CMP-05 brings together superior input specifications with very fast response times. This combination makes the CMP-05 the ideal choice in high-accuracy 10 and 12-bit data systems.

DEFINITIONS

Average Offset Current Drift (TCI_{OS}) — The ratio of the change in the input offset current to the change in temperature producing it.

Average Offset Voltage Drift (TCV_{OS}) — The ratio of the change in the input offset voltage to the change in temperature producing it.

Average Offset Voltage Drift With External Trimming (TCV_{OSN}) — The ratio of the change in the input offset voltage to the change in temperature producing it, with the input offset voltage trimmed to zero at room temperature.

Common-Mode Rejection Ratio (CMRR) — The ratio of differential voltage gain to common-mode voltage gain, expressed in dB. CMRR is measured as the ratio of the change in common-mode voltage divided by the change in input offset voltage.

$$\text{CMRR} = 20 \log \left(\frac{A_{V(DIFF)}}{A_{V(CM)}} \right) = 20 \log \left(\frac{\Delta CMV}{\Delta V_{OS}} \right)$$

Common-Mode Voltage Range (CMVR) — The range of common-mode voltage on the input terminals for which operation within specifications is assured.

VOLTAGE COMPARATORS

Differential Input Resistance (R_{IN}) — The resistance looking into either input terminal with the other grounded.

Differential Input Voltage — The range of voltage between the input terminals for which operation within specifications is assured.

Input Bias Current (I_B) — The average of the two input currents, with the inputs tied together.

Input Offset Current (I_{OS}) — The difference between the currents into the two input terminals when the output is within a specified voltage range.

Input Offset Voltage (V_{OS}) — The voltage applied between the input terminals to obtain a specified output voltage range.

Input Slew Rate — The maximum rate of change in differential and/or common-mode input voltage which the input stage can follow.

Input To Output High Propagation Delay (tpd +) — The time measured between the input signal's V_{OS} crossing and the output voltage's 50% low-to-high transition point. Specified for a given input voltage step size and overdrive.

Input To Output Low Propagation Delay (tpd−) — The time measured between the input signal's V_{OS} crossing and the output voltage's 50% high-to-low transition point. Specified for a given input voltage step size and overdrive.

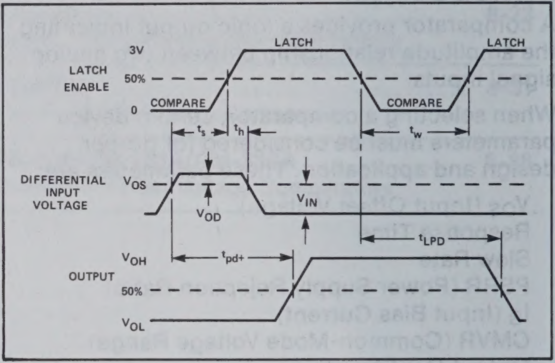
Latch Disable Propagation Delay (t_{LPD}) — The time measured between the 50% transition points of the latch enable signal and the output signal transition point.

Latch Hold Time (t_h) — The amount of time measured from 50% of the latch enable signal to the comparator-input trip-point crossing.

Latch Pulse Width (t_w) — The width of the latch enable pulse measured between the 50% points of the rising and falling pulse edges.

Latch Set-Up Time (t_s) — The amount of time measured from the comparator-input trip-point crossing to 50% of the latch enable control.

Switching Time Waveforms



Offset Voltage Adjustment Range — The change in offset voltage that can be obtained by adjusting a specified external nulling potentiometer.

Output Leakage Current (I_{LEAK}) — The current into the output terminal with a given output voltage and input drive equal to or greater than a specified value.

Output Sink Current (I_{SINK}) — The maximum negative current that can be delivered by the comparator.

Overdrive (V_{OD}) — The input step voltage (V_{IN}) of specified size drives the comparator from some initial input voltage to an input level just barely in excess of that required to bring the output from its high or low state to the logic threshold voltage. This excess is defined as the voltage overdrive.

Positive Output Voltage (V_{OH}) — The high output voltage level with a given load and an input drive equal to a specified value.

Power Supply Rejection Ratio (PSRR) — The ratio of the maximum change in input offset voltage to the specified change in power supply voltage.

Response Time (t_r) — The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. Logic threshold is defined as the voltage at the output of the comparator at which the loading logic circuitry changes its digital state, or, as 1.4V when the loading logic circuitry is not used.

Saturation Voltage (V_{OL}) — The low output voltage level with a given sink current and an input drive equal to a specified value.

Supply Currents — The currents required from the positive or negative supplies to operate the comparator without a load.

Voltage Gain (A_V) — The ratio of the change in output voltage (over a specified range) to the change in differential input voltage producing it.

CMP-01

FAST PRECISION COMPARATOR

FEATURES

- **Fast Response Time .... 180ns Max**
- **High Input Slew Rate 92V/μs**
- **Low Offset Voltage .... 0.3mV Typical, 0.8mV Max**
- **Low Offset Current .... 4nA Typical, 25nA Max**
- **Low Offset Drift .... 1μV/°C, 30pA/°C**
- **Standard Power Supplies .... +5V or ±5V to ±18V**
- **Guaranteed Operation from Single +5V Supply**
- **No Pull-Up Resistor Required for TTL Drive**
- **Wired OR Capability**
- **Fits 111, 106, 710 Sockets**
- **Easy Offset Nulling .... Single 2kΩ Potentiometer**
- **Easy to Use .... Free from Oscillations**

ORDERING INFORMATION†

+25°C V_{OS} (mV)	HERMETIC TO-99 8-PIN	HERMETIC DIP 8-PIN	PLASTIC DIP 8-PIN	OPERATING TEMPERATURE RANGE
0.8	CMP01J*	CMP01Z*	—	MIL
0.8	CMP01EJ	CMP01EZ	CMP01EP	COM
2.8	CMP01CJ	CMP01CZ	CMP01CP	COM

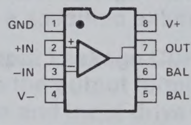
*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

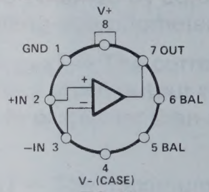
GENERAL DESCRIPTION

The CMP-01 is a monolithic fast precision voltage comparator using an advanced NPN-Schottky Barrier Diode process. It features fast response time to both large and small input signals, while maintaining excellent input characteristics. The CMP-01 is capable of operating over a wide range of supply voltages including single ended 5 volt supply. The large output current sinking and high output voltage capability assure good application flexibility, while the combination of fast response, high accuracy, and freedom from oscillation assure performance in precision level detectors and 12 and 13-bit A/D converters. The CMP-01 is pin-compatible to earlier 111, 106, and 710 types. For applications requiring lower input offset and bias currents, refer to the CMP-02 data sheet.

PIN CONNECTIONS

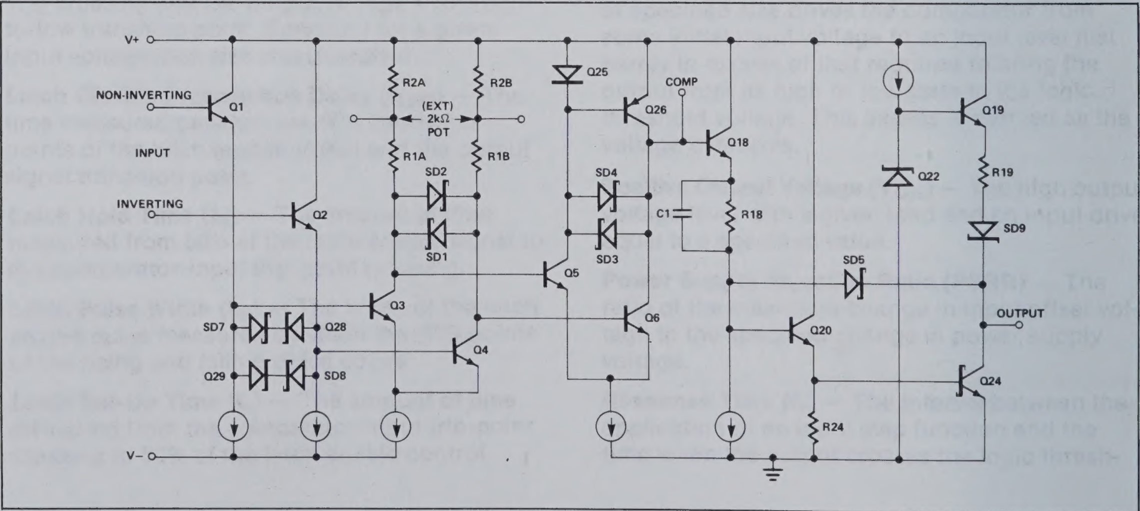

GND 1
+IN 2
−IN 3
V− 4
8 V+
7 OUT
6 BAL
5 BAL

8-PIN HERMETIC MINI-DIP
(Z-Suffix)
EPOXY MINI-DIP
(P-Suffix)


V+
8
GND 1
7 OUT
+IN 2
6 BAL
−IN 3
5 BAL
4
V- (CASE)

TO-99
(J-Suffix)

SIMPLIFIED SCHEMATIC


V+
NON-INVERTING
INPUT
INVERTING
V−
Q1
Q2
R2A
R2B
(EXT)
2kΩ
POT
R1A
R1B
SD2
SD1
Q3
Q4
SD7
Q28
Q29
SD8
Q25
COMP
Q26
Q18
SD4
SD3
C1
R18
Q5
Q6
Q20
SD5
R24
Q19
R19
Q22
SD9
OUTPUT
Q24

ABSOLUTE MAXIMUM RATINGS (Note 2)

Total Supply Voltage, V+ to V−	36V
Output to Ground	−5V to +32V
Output to Negative Supply Voltage	50V
Ground to Negative Supply Voltage	30V
Positive Supply Voltage to Ground	+30V
Positive Supply Voltage to Offset Null	0 to 2V
Power Dissipation (See Note 1)	500mW
Differential Input Voltage	±11V
Input Voltage ($V_S = \pm 15V$)	±15V
Output Sink Current (Continuous Operation)	75mA
Operating Temperature Range	
CMP-01	−55° C to +125° C
CMP-01E, CMP-01C	0° C to +70° C
DICE Junction Temperature (T_j)	−65° C to +150° C
Storage Temperature Range	−65° C to +150° C
P-Suffix	−65° C to +125° C
Lead Temperature (Soldering, 60 sec)	300° C
Output Short-Circuit Duration — to ground	Indefinite
to V+	1 Minute

NOTES:

1. Maximum package power dissipation vs. ambient temperature.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80° C	7.1mW/° C
Epoxy Mini-DIP (P)	36° C	5.6mW/° C
Hermetic Mini-DIP (Z)	75° C	6.7mW/° C

2. Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25° C$, unless otherwise noted.

			CMP-01 CMP-01E			CMP-01C			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$, (Note 1)	—	0.3	0.8	—	0.4	2.8	mV
Input Offset Current	I_{OS}	(Note 1)	—	4	25	—	5	80	nA
Input Bias Current	I_B		—	350	600	—	400	900	nA
Differential Input Resistance	R_{IN}	(Note 2)	3	14	—	1	10	—	MΩ
Voltage Gain	A_V	$V_O = 0.4V$ to 2.4V, (Notes 1, 2)	200	500	—	100	500	—	V/mV
Response Time (Note 3)	t_r	100mV step, 5mV Overdrive							ns
		No Load (No Pull-Up)	—	110	180	—	110	180	
		5kΩ to 5v (Pull-Up)	—	110	—	—	110	—	
		TTL Fan-Out = 4, No Pull-Up	—	110	—	—	110		
		5V Step 5mV Overdrive							
		No Load (No Pull-Up)	—	160	—	—	160	—	
		5kΩ to 5v (Pull-Up)	—	160	—	—	160	—	
		TTL Fan-Out = 4, No Pull-Up	—	160	—	—	160	—	
Input Slew Rate			—	92	—	—	92	—	V/μs
Input Voltage Range	CMVR		±12.5	±13	—	±12.5	±13	—	V
Common-Mode Rejection Ratio	CMRR		94	110	—	90	110	—	dB
Power Supply Rejection Ratio	PSRR	$5V \leq V_{S+} \leq 18V$, $-18V \leq V_{S-} \leq 0V$	80	100	—	74	98	—	dB
Positive Output Voltage	V_{OH}	$V_{IN} \geq 3mV$, $I_O = 320\mu A$	2.4	3.2	—	—	—	—	V
		$V_{IN} \geq 3mV$, $I_O = 240\mu A$	—	—	—	2.4	3.4	—	
		$V_{IN} \geq 3mV$, $I_O = 0mA$	2.4	4.8	—	2.4	4.8	—	
Saturation Voltage	V_{OL}	$V_{IN} \leq -10mV$, $I_{sink} = 0mA$	—	0.16	0.4	—	0.16	0.4	V
		$V_{IN} \leq -10mV$, $I_{sink} \leq 6.4mA$	—	0.3	0.45	—	0.31	0.45	
		$V_{IN} \leq -10mV$, $I_{sink} \leq 12mA$ (CMP-01 only)	—	0.36	0.5	—	—	—	
Output Leakage Current	I_{LEAK}	$V_{IN} \geq 10mV$, $V_O = +30V$	—	0.03	2	—	0.05	8	μA
Positive Supply Current	I+	$V_{IN} \leq -10mV$	—	5.6	8	—	5.6	8.5	mA
Negative Supply Current	I−	$V_{IN} \leq -10mV$	—	1.3	2.2	—	1.3	2.2	mA
Power Dissipation	P_d	$V_{IN} \leq -10mV$	—	103	153	—	103	161	mW
Offset Voltage Adjustment Range		Nulling Pot ≥ 2kΩ	—	±5	—	—	±5	—	mV

NOTES:

1. These parameters are specified as the maximum values required to drive the output between the logic levels of 0.4V and 2.4V with a 1kΩ load tied to +5V; thus, these parameters define an error band which takes into account the worst case effects of voltage gain and input impedance.
2. Guaranteed by design.
3. Sample tested.

ELECTRICAL CHARACTERISTICS at $V_{S+} = 5V$, $V_{S-} = 0V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-01 CMP-01E			CMP-01C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \le 5k\Omega$, (Note 1)	—	0.4	1.5	—	0.5	3.5	mV
Input Offset Current	I_{OS}	(Note 1)	—	3	21	—	4	65	nA
Input Bias Current	I_B		—	250	500	—	300	720	nA
Voltage Gain	A_V	$V_O = 0.4V$ to 2.4V, (Notes 1, 2)	—	50	—	—	50	—	V/mV
Response Time	t_r	100mV Step, 5mV Overdrive 5kΩ to 5V (Pull-Up) TTL Fan-Out = 4, 5kΩ to 5V (Pull-Up)	— —	150 150	— —	— —	150 150	— —	ns
Input Voltage Range	CMVR		1.8	1.7-3.8	3.5	1.8	1.7-3.8	3.5	V
Saturation Voltage	V_{OL}	$V_{IN} \le -10mV$, $I_{sink} \le 6.4mA$	—	0.3	0.45	—	0.3	0.45	V
Positive Supply Current	I+	$V_{IN} \le -10mV$	—	2.3	3.2	—	2.4	3.8	mA
Power Dissipation	P_d	$V_{IN} \le -10mV$	—	11.5	16	—	12	19	mW

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \le T_A \le 125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-01			UNITS
			MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \le 5k\Omega$, (Note 1) $V_{S+} = 5V$, $V_{S-} = 0V$, (Note 1)	— —	0.5 0.6	1.6 2.8	mV
Average Input Offset Voltage Drift Without External Trim With External Trim	TCV_{OS} TCV_{OSn}	$R_S = 50\Omega$	— —	1.5 1	— —	µV/°C
Input Offset Current	I_{OS}	$T_A = +125°C$, (Note 1) $T_A = -55°C$, (Note 1)	— —	4 5	25 45	nA
Average Input Offset Current Drift	TCI_{OS}	$+25°C \le T_A \le +125°C$ $-55°C \le T_A \le +25°C$	— —	12 35	— —	pA/°C
Input Bias Current	I_B	$T_A = +125°C$ $T_A = -55°C$	— —	330 550	600 1400	nA
Voltage Gain	A_V	$V_O = 0.4V$ to 2.4V, (Notes 1, 2)	100	500	—	V/mV
Response Time	t_r	100mV Step, 5mV Overdrive, (Note 2) $T_A = +125°C$, No Load $T_A = -55°C$, No Load	— —	220 100	— —	ns
Input Voltage Range	CMVR		±12	±13	—	V
Common-Mode Rejection Ratio	CMRR		88	106	—	dB
Power Supply Rejection Ratio	PSRR	$5V \le V_{S+} \le 15V$, $-15V \le V_{S-} \le 0V$	75	96	—	dB
Positive Output Voltage	V_{OH}	$V_{IN} \ge 4mV$, $I_O = 200\mu A$	2.4	3	—	V
Saturation Voltage	V_{OL}	$V_{IN} \le -10mV$, $I_{sink} = 0mA$ $V_{IN} \le -10mV$, $I_{sink} = 6.4mA$	— —	0.20 0.32	0.4 0.5	V

NOTES:

1. These parameters are specified as the maximum values required to drive the output between the logic levels of 0.4V and 2.4V with a 1kΩ load tied to +5V; thus, these parameters define an error band which takes into account the worst case effects of voltage gain and input impedance.
2. Guaranteed by design.

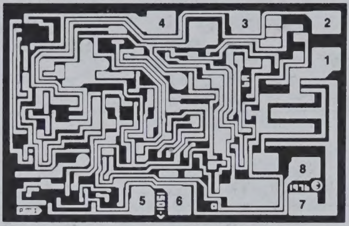
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $0°C \le T_A \le 70°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-01E MIN	CMP-01E TYP	CMP-01E MAX	CMP-01C MIN	CMP-01C TYP	CMP-01C MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \le 5k\Omega$, (Note 1) $V_{S+} = 5V$, $V_{S-} = 0V$, (Note 1)	— —	0.4 0.5	1.4 2.4	— —	0.5 0.6	3.5 4.3	mV
Average Input Offset Voltage Drift Without External Trim With External Trim	 TCV_{OS} TCV_{OSn}	$R_S = 50\Omega$	 — —	 1.5 1.0	 — —	 — —	 1.8 1.2	 — —	µV/°C
Input Offset Current	I_{OS}	$T_A = +70°C$, (Note 1) $T_A = 0°C$, (Note 1)	— —	4 5	25 45	— —	5 6	80 120	nA
Average Input Offset Current Drift	TCI_{OS}	$+25°C \le T_A \le +70°C$ $0°C \le T_A \le +25°C$	— —	12 35	— —	— —	12 40	— —	pA/°C
Input Bias Current	I_B	$T_A = +70°C$ $T_A = 0°C$	— —	330 400	600 950	— —	340 450	900 1200	nA
Voltage Gain	A_V	$V_O = 0.4V$ to $2.4V$, (Notes 1, 2)	100	500	—	70	500	—	V/mV
Response Time	t_r	100mV Step, 5mV Overdrive $T_A = +70°C$, No Load $T_A = 0°C$, No Load	 — —	 150 100	 — —	 — —	 150 100	 — —	ns
Input Voltage Range	CMVR		±12.0	±13.3	—	±12.0	±13.3	—	V
Common-Mode Rejection Ratio	CMRR		90	108	—	86	108	—	dB
Power Supply Rejection Ratio	PSRR	$5V \le V_{S+} \le 15V$, $-15V \le V_{S-} \le 0V$	77	98	—	70	88	—	dB
Positive Output Voltage	V_{OH}	$V_{IN} \ge 4mV$, $I_O = 200\mu A$	2.4	3.2	—	2.4	3.2	—	V
Saturation Voltage	V_{OL}	$V_{IN} \le -10mV$, $I_{sink} = 0$ $V_{IN} \le -10mV$, $I_{sink} = 6.4mA$	— —	0.17 0.3	0.4 0.5	— —	0.17 0.31	0.4 0.5	V

NOTES:

1. These parameters are specified as the maximum values required to drive the output between the logic levels of 0.4V and 2.4V with a 1kΩ load tied to +5V; thus, these parameters define an error band which takes into account the worst case effects of voltage gain and input impedance.
2. Guaranteed by design.

DICE CHARACTERISTICS



**DIE SIZE 0.065 × 0.042 inch, 2730 sq. mils
(1.651 × 1.069 mm, 1.761 sq. mm)**

1. **GROUND**
2. **NONINVERTING INPUT**
3. **INVERTING INPUT**
4. **NEGATIVE SUPPLY (SUBSTRATE)**
5. **BALANCE**
6. **BALANCE**
7. **OUTPUT**
8. **POSITIVE SUPPLY**

For additional DICE information refer to Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$.

PARAMETER	SYMBOL	CONDITIONS	CMP-01N LIMIT	CMP-01GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$, (Note 1)	0.8	2.8	mV MAX
Input Offset Current	I_{OS}	(Note 1)	25	80	nA MAX
Input Bias Current	I_B		600	900	nA MAX
Differential Input Resistance	R_{IN}	(Note 2)	3	1	MΩ MIN
Input Voltage Range	CMVR		±12.5	±12.5	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm CMVR$	94	90	dB MIN
Power Supply Rejection Ratio	PSRR	$5V \leq V_S+ \leq 18V$ $-18V \leq V_S- \leq 0V$	80	74	dB MIN
Positive Output Voltage	V_{OH}	$V_{IN} \geq 3mV$, $I_O = 320\mu A$ $V_{IN} \geq 3mV$, $I_O = 240\mu A$	2.4 —	— 2.4	V MIN
Saturation Voltage	V_{OL}	$I_{sink} = 6.4mA$	0.45	0.45	V MAX
Output Leakage Current	I_{LEAK}	$V_{IN} \geq 10mV$, $V_O = 30V$	2	8	μA MAX
Positive Supply Current	I+	$V_{IN} \leq -10mV$	8.0	8.5	mA MAX
Negative Supply Current	I−	$V_{IN} \leq -10mV$	2.2	2.2	mA MAX
Power Consumption	P_d	$V_{IN} \leq -10mV$	153	161	mW MAX

NOTES:

1. These parameters are specified as the maximum values required to drive the output between the logic levels of 0.4V and 2.4V with a 1kΩ load tied to +5V; thus, these parameters define an error band which takes into account the worst case effects of voltage gain and input impedance.
2. Guaranteed by design.

WAFER TEST LIMITS at $V_S+ = 5V$ and $V_S- = 0V$, $T_A = 25°C$.

PARAMETER	SYMBOL	CONDITIONS	CMP-01N LIMIT	CMP-01GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$	1.5	3.5	mV MAX
Input Offset Current	I_{OS}		21	65	nA MAX

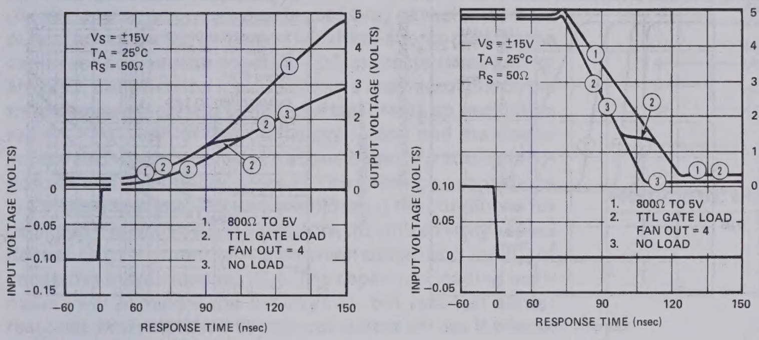
Note: Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, and 25°C.

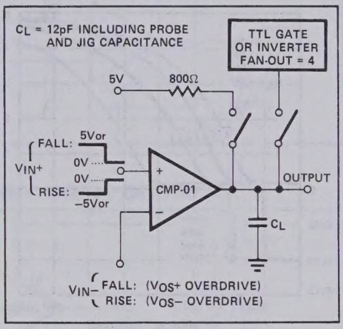
PARAMETER	SYMBOL	CONDITIONS	CMP-01N TYPICAL	CMP-01GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}	$R_S = 50\Omega$	1.5	1.8	μV/°C
Average Input Offset Current Drift	TCI_{OS}		35	40	pA/°C
Response Time	t_r	100mV Step, 5mV Overdrive No Load (No Pull-Up), $T_A = 25°C$	110	110	ns

TYPICAL PERFORMANCE CHARACTERISTICS

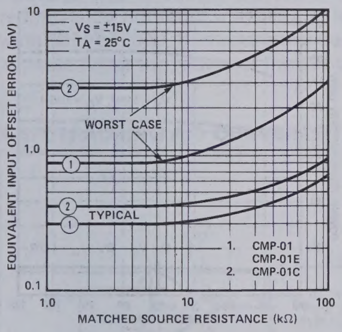
RESPONSE TIME, 100mV STEP, 5mV OVERDRIVE, VARIOUS LOADS



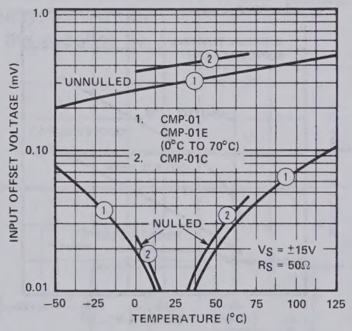
RESPONSE TIME TEST CIRCUIT


CL = 12pF INCLUDING PROBE AND JIG CAPACITANCE
TTL GATE OR INVERTER FAN-OUT = 4
5V
800Ω
FALL:
5Vor
VIN+
0V
0V
RISE:
−5Vor
+
−
CMP-01
OUTPUT
CL
VIN−
FALL: (VOS+ OVERDRIVE)
RISE: (VOS− OVERDRIVE)

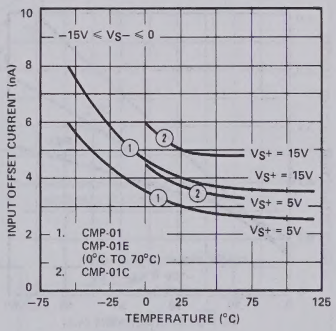
INPUT OFFSET ERROR vs SOURCE RESISTANCE



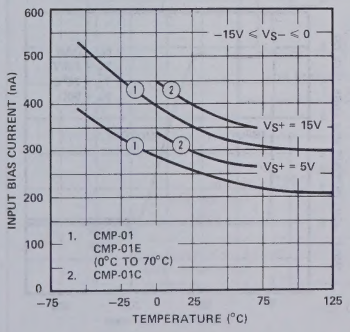
OFFSET VOLTAGE vs TEMPERATURE



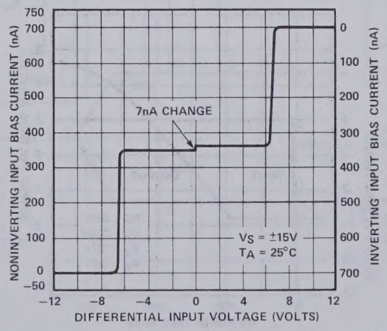
INPUT OFFSET CURRENT vs TEMPERATURE



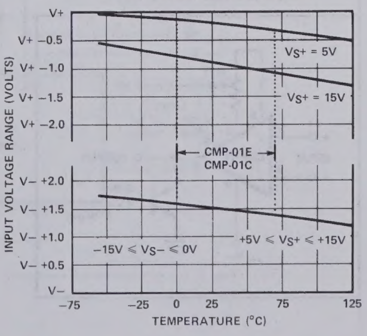
INPUT BIAS CURRENT vs TEMPERATURE



INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE

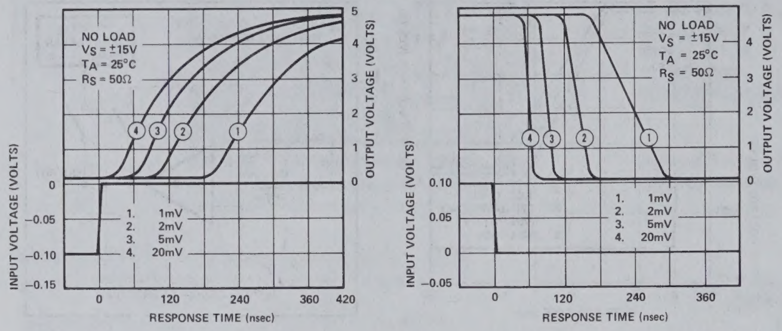


INPUT VOLTAGE RANGE vs TEMPERATURE

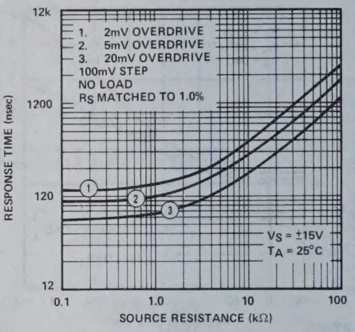


TYPICAL PERFORMANCE CHARACTERISTICS

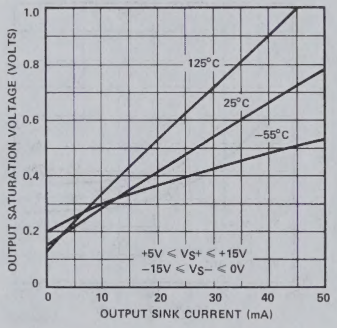
RESPONSE TIME FOR 100mV STEP AND VARIOUS INPUT OVERDRIVES



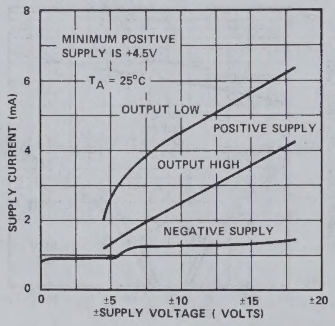
RESPONSE TIME vs SOURCE RESISTANCE



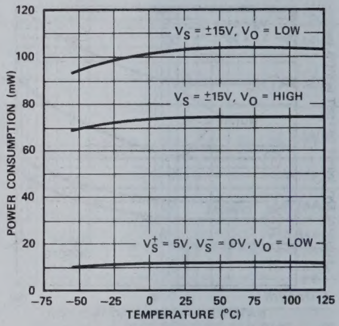
SATURATION VOLTAGE vs SINK CURRENT



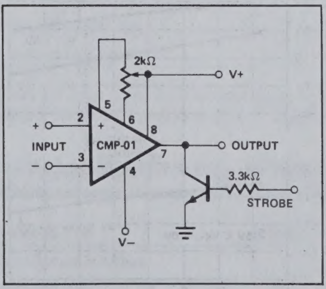
SUPPLY CURRENT vs SUPPLY VOLTAGE



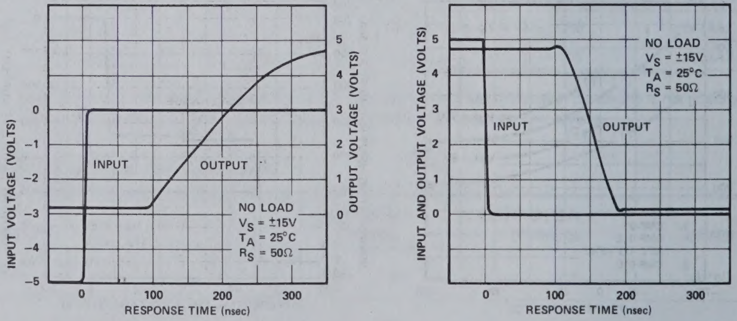
POWER CONSUMPTION vs TEMPERATURE



OFFSET TRIMMING AND STROBE CIRCUIT


2kΩ
V+
5
6
8
2
3
4
7
+
−
INPUT
CMP-01
OUTPUT
3.3kΩ
STROBE
V−

RESPONSE TIME FOR 5V STEP AND 5mV OVERDRIVE



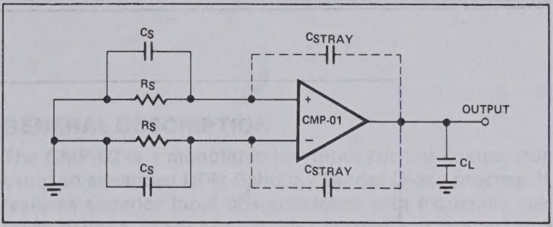
APPLICATIONS INFORMATION

The CMP-01 provides fast response times even with small overdrives; to achieve this performance requires very high gain at high frequencies. The CMP-01 is completely free of oscillations; however, small values of stray capacitance from output to input when combined with high-source resistances can cause an unstable condition. DC characteristics are not affected, but when the input is within a few microvolts of the transition level, certain conditions can create an oscillation region. The width of this oscillatory region and the size of source resistance where oscillations begin is a strong function of the stray coupling present. The following suggestions are offered as a guide towards minimizing the conditions for oscillation: matched source resistors, minimized stray capacitances (e.g., a ground plane between output and input), or capacitive output loading (C_L). The capacitive loading techniques will eliminate the oscillations, but result in slower response time. Matched bypass capacitors across the input resistors also can eliminate the instability,

$$\text{and if } C_S \geq 20\text{pF}\left(\frac{\text{maximum step size}}{\text{minimum overdrive}}\right)$$

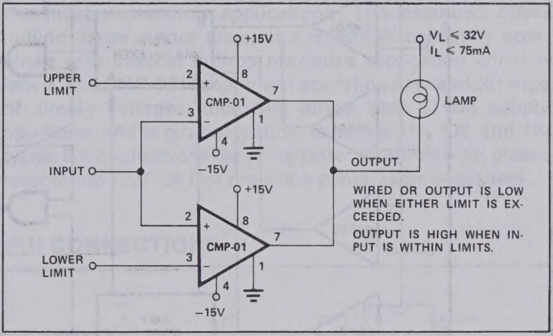
the response time will approximate the response time for low values of R_S. It should be noted that the offset nulling terminals do not require bypassing for stability. As with all wideband circuits, it is recommended that the supplies be bypassed near the socket of the device.

MINIMIZING OSCILLATION



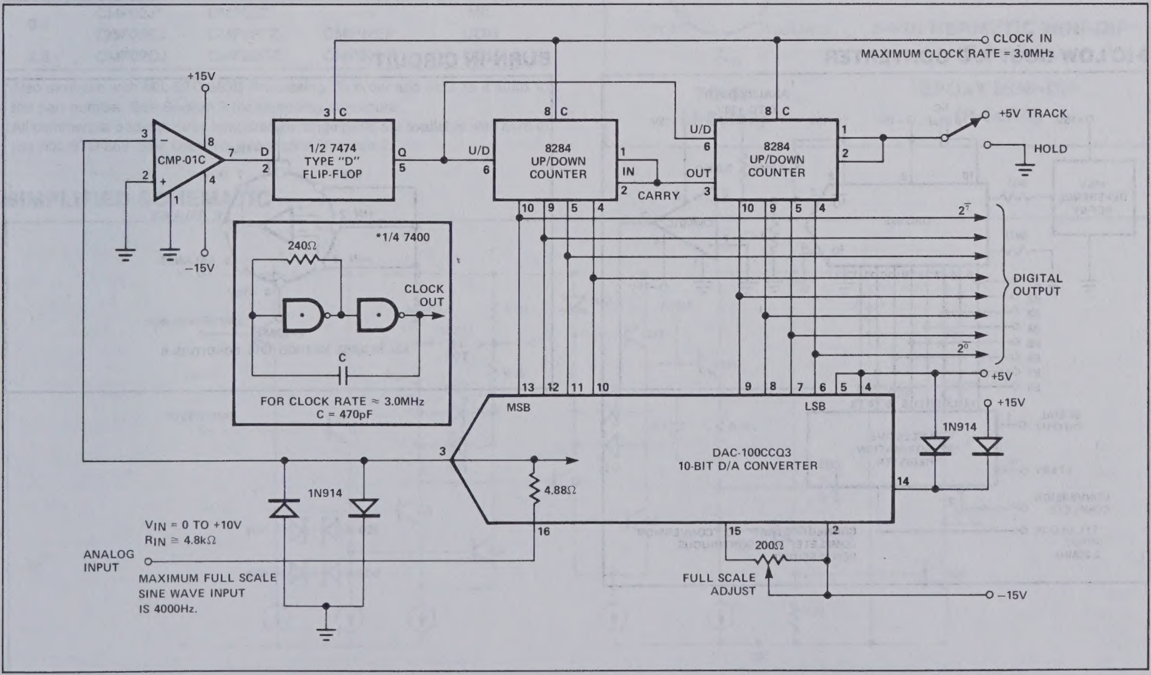
CS
CSTRAY
RS
RS
CMP-01
OUTPUT
CS
CSTRAY
CL

PRECISION, DUAL LIMIT, GO/NO GO TESTER



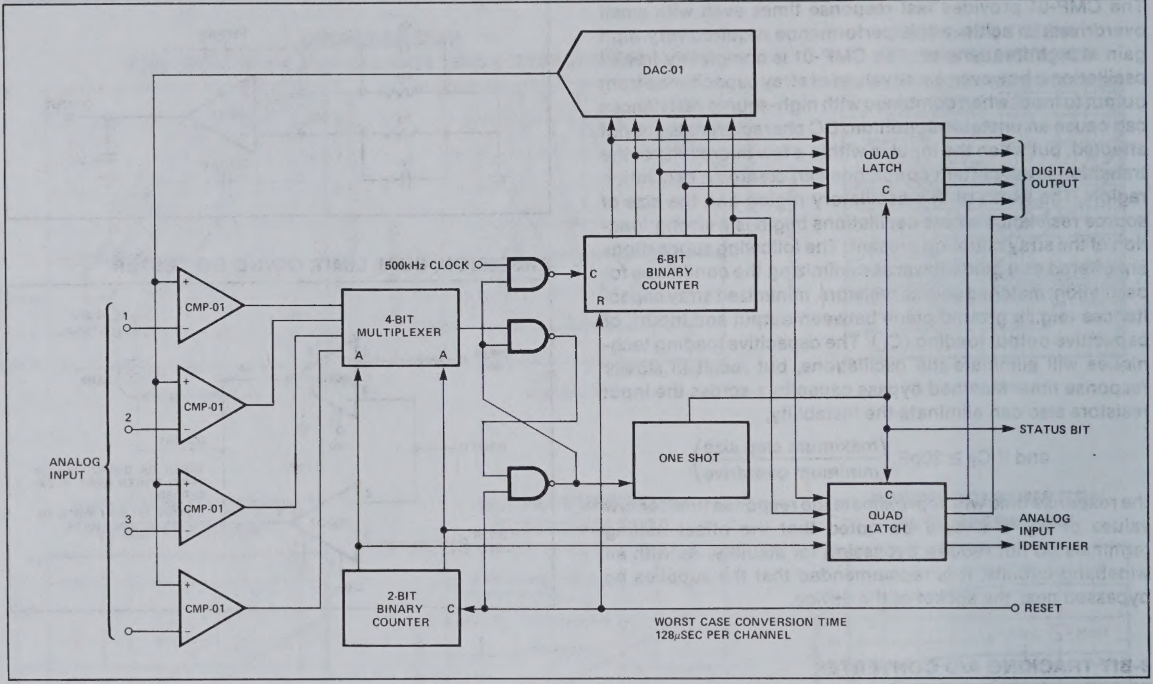
+15V
VL ≤ 32V
IL ≤ 75mA
UPPER LIMIT
CMP-01
LAMP
INPUT
-15V
OUTPUT
+15V
WIRED OR OUTPUT IS LOW WHEN EITHER LIMIT IS EXCEEDED.
OUTPUT IS HIGH WHEN INPUT IS WITHIN LIMITS.
LOWER LIMIT
CMP-01
-15V

8-BIT TRACKING A/D CONVERTER



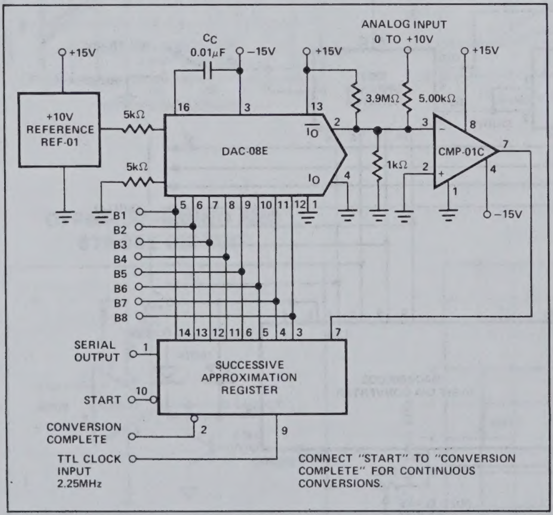
CLOCK IN
MAXIMUM CLOCK RATE = 3.0MHz
+15V
CMP-01C
-15V
1/2 7474 TYPE "D" FLIP-FLOP
D
Q
U/D
8284 UP/DOWN COUNTER
IN
CARRY
OUT
U/D
8284 UP/DOWN COUNTER
+5V TRACK
HOLD
*1/4 7400
240Ω
CLOCK OUT
C
FOR CLOCK RATE ≈ 3.0MHz C = 470pF
2⁷
2⁰
DIGITAL OUTPUT
+5V
+15V
1N914
MSB
LSB
DAC-100CCQ3 10-BIT D/A CONVERTER
4.88Ω
1N914
VIN = 0 TO +10V
RIN ≅ 4.8kΩ
ANALOG INPUT
MAXIMUM FULL SCALE SINE WAVE INPUT IS 4000Hz.
200Ω
FULL SCALE ADJUST
-15V

4-CHANNEL DIGITALLY MULTIPLEXED RAMPED A/D CONVERTER


DAC-01
QUAD LATCH
C
DIGITAL OUTPUT
500kHz CLOCK
C
6-BIT BINARY COUNTER
R
CMP-01
CMP-01
CMP-01
CMP-01
1
2
3
ANALOG INPUT
4-BIT MULTIPLEXER
A
A
ONE SHOT
STATUS BIT
C
QUAD LATCH
ANALOG INPUT IDENTIFIER
2-BIT BINARY COUNTER
C
RESET

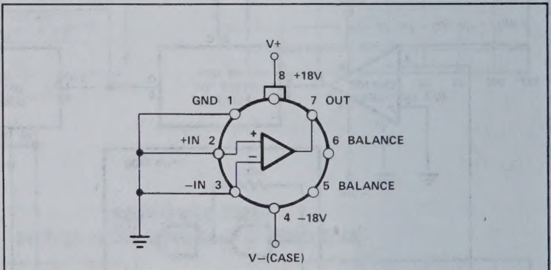
WORST CASE CONVERSION TIME 128μSEC PER CHANNEL

3 IC LOW COST A/D CONVERTER


+15V
CC
0.01μF
−15V
+15V
ANALOG INPUT 0 TO +10V
+15V
+10V REFERENCE REF-01
5kΩ
5kΩ
16
3
13
DAC-08E
IO
IO
2
4
3.9MΩ
5.00kΩ
1kΩ
3
2
8
7
4
1
CMP-01C
−15V
5 6 7 8 9 10 11 12
B1
B2
B3
B4
B5
B6
B7
B8
14 13 12 11 6 5 4 3
7
SERIAL OUTPUT
1
SUCCESSIVE APPROXIMATION REGISTER
START
10
CONVERSION COMPLETE
2
9
TTL CLOCK INPUT 2.25MHz

CONNECT "START" TO "CONVERSION COMPLETE" FOR CONTINUOUS CONVERSIONS.

BURN-IN CIRCUIT


V+
8 +18V
GND 1
7 OUT
+IN 2
6 BALANCE
−IN 3
5 BALANCE
4 −18V
V−(CASE)

MIL-STD-883, METHOD 1015, CONDITION B

LOW-INPUT-CURRENT PRECISION COMPARATOR

CMP-02

FEATURES

- **Low Offset Voltage .... 0.3mV Typ, 0.8mV Max**
- **Low Offset Current .... 0.3nA Typ, 3nA Max**
- **Low Bias Current .... 28nA Typ, 50nA Max**
- **Low Offset Drift .... 1μV/° C, 4pA/° C**
- **High Gain .... 200,000 Min**
- **High CMRR .... 110dB Typ, 94dB Min**
- **High Input Impedance 16MΩ**
- **Fast Response Time .... 190ns Typ, 270ns Max**
- **Standard Power Supplies .... +5V or ±5V to ±18V**
- **Guaranteed Operation from Single +5V**
- **No Pull-Up Resistor Required for TTL Drive**
- **Wired OR Capability**
- **Fits 111, 106, 710 Sockets**
- **Easy Offset Nulling .... Single 2kΩ Potentiometer**
- **Easy to Use .... Free from Oscillations**

ORDERING INFORMATION†

	PACKAGE			
	HERMETIC			
+25° C V_{OS} (mV)	TO-99 8-PIN	DIP 8-PIN	PLASTIC DIP 8-PIN	OPERATING TEMPERATURE RANGE
0.8	CMP02J*	CMP02Z*	—	MIL
	CMP02EJ	CMP02EZ	CMP02EP	COM
2.8	CMP02CJ	CMP02CZ	CMP02CP	COM

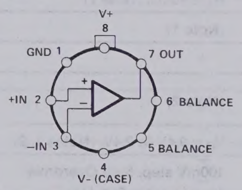
*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

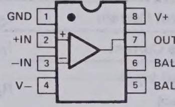
GENERAL DESCRIPTION

The CMP-02 is a monolithic low input current comparator using an advanced NPN-Schottky Barrier Diode process. It features superior input characteristics with extremely low offset voltage, offset current, bias current and temperature drift. High common-mode and power supply rejection plus good response time contribute to excellent performance in the most demanding applications. The balanced offset nulling, large output drive, and wired-OR capability combined with internal pull-up maximize application convenience. The CMP-02 is capable of operating over a wide range of supply voltages, including single plus 5 volt supply operation, and is pin-compatible to earlier 111, 106, and 710 types. For applications requiring faster response time, please refer to the CMP-01 fast precision comparator data sheet.

PIN CONNECTIONS


V+
8
GND 1
7 OUT
+IN 2
6 BALANCE
–IN 3
5 BALANCE
4
V– (CASE)

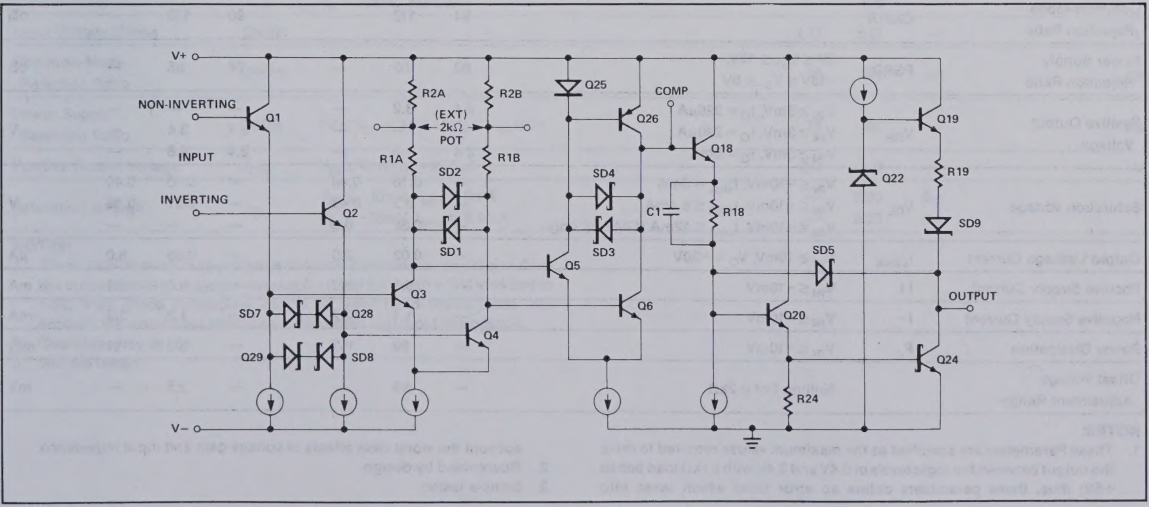
TO-99
(J-Suffix)


GND 1
+IN 2
–IN 3
V– 4
8 V+
7 OUT
6 BALANCE
5 BALANCE

8-PIN HERMETIC MINI-DIP
(Z-Suffix)

EPOXY MINI-DIP
(P-Suffix)

SIMPLIFIED SCHEMATIC


V+
NON-INVERTING
INPUT
INVERTING
Q1
Q2
R2A
R2B
(EXT)
2kΩ
POT
R1A
R1B
SD2
SD1
Q25
COMP
Q26
Q18
SD4
SD3
C1
R18
Q5
Q3
Q4
Q6
SD7
Q28
Q29
SD8
SD5
Q20
R24
Q19
R19
Q22
SD9
OUTPUT
Q24
V–

ABSOLUTE MAXIMUM RATINGS (Note 2)

Total Supply Voltage, V+ to V−	36V
Output to Ground	−5V to +32V
Output to Negative Supply Voltage	50V
Ground to Negative Supply Voltage	30V
Positive Supply Voltage to Ground	30V
Positive Supply Voltage to Offset Null	0 to 2V
Power Dissipation (See Note 1)	500mW
Differential Input Voltage	±11V
Input Voltage ($V_S = \pm 15V$)	±15V
Output Sink Current (Continuous Operation)	75mA
Operating Temperature Range	
CMP-02	−55° C to +125° C
CMP-02E, CMP-02C	0° C to +70° C
DICE Junction Temperature (T_j)	−65° C to +150° C
Storage Temperature Range	−65° C to +150° C
P-Suffix	−65° C to +125° C
Lead Temperature (Soldering, 60 sec)	300° C
Output Short-Circuit Duration — to ground	Indefinite
to V+	1 Minute

NOTES:

1. Maximum package power dissipation vs. ambient temperature.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80° C	7.1mW/° C
Mini-DIP (P)	36° C	5.6mW/° C
Hermetic Mini-DIP (Z)	75° C	6.7mW/° C

2. Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-02 CMP-02E			CMP-02C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$, (Note 1)	—	0.3	0.8	—	0.4	2.8	mV
Input Offset Voltage	V_{OS}	$R_S \leq 50k\Omega$, (Note 1)	—	0.3	0.9	—	0.4	3	mV
Input Offset Current	I_{OS}	(Note 1)	—	0.3	3.0	—	0.4	15	nA
Input Bias Current	I_B		—	28	50	—	35	100	nA
Differential Input Resistance	R_{IN}	(Note 2)	5	16	—	1.5	12	—	MΩ
Voltage Gain	A_V	$V_O = 0.4V$ to 2.4V, (Notes 1, 2)	200	500	—	100	500	—	V/mV
Response Time (Note 3)	t_r	100mV step, 5mV Overdrive							ns
		No Load (No Pull-Up)	—	190	270	—	190	270	
		5kΩ to 5V (Pull-Up)	—	190	—	—	190	—	
		TTL Fan-Out = 4, No Pull-Up	—	190	—	—	190	—	
Input Slew Rate			—	15	—	—	15	—	V/μs
Input Voltage Range	CMVR		±12.5	±13.0	—	±12.5	±13.0	—	V
Common-Mode Rejection Ratio	CMRR		94	110	—	90	110	—	dB
Power Supply Rejection Ratio	PSRR	$5V \leq V_{S+} \leq 18V$, $-18V \leq V_{S-} \leq 0V$	80	100	—	74	98	—	dB
Positive Output Voltage	V_{OH}	$V_{IN} \geq 3mV$, $I_O = 320\mu A$	2.4	3.2	—	—	—	—	V
		$V_{IN} \geq 3mV$, $I_O = 240\mu A$	—	—	—	2.4	3.4	—	
		$V_{IN} \geq 3mV$, $I_O = 0mA$	2.4	4.8	—	2.4	4.8	—	
Saturation Voltage	V_{OL}	$V_{IN} \leq -10mV$, $I_{sink} = 0mA$	—	0.16	0.40	—	0.16	0.40	V
		$V_{IN} \leq -10mV$, $I_{sink} \leq 6.4mA$	—	0.3	0.45	—	0.31	0.45	
		$V_{IN} \leq -10mV$, $I_{sink} \leq 12mA$ (CMP-02 only)	—	0.36	0.5	—	—	—	
Output Leakage Current	I_{LEAK}	$V_{IN} \geq 10mV$, $V_O = +30V$	—	0.03	2.0	—	0.05	8.0	μA
Positive Supply Current	I+	$V_{IN} \leq -10mV$	—	5.5	8.0	—	5.6	8.5	mA
Negative Supply Current	I−	$V_{IN} \leq -10mV$	—	1.1	2.2	—	1.2	2.2	mA
Power Dissipation	P_d	$V_{IN} \leq -10mV$	—	99	153	—	102	161	mW
Offset Voltage Adjustment Range		Nulling Pot ≥ 2kΩ	—	±5	—	—	±5	—	mV

NOTES:

1. These Parameters are specified as the maximum values required to drive the output between the logic levels of 0.4V and 2.4V with a 1kΩ load tied to +5V; thus, these parameters define an error band which takes into account the worst case effects of voltage gain and input impedance.
2. Guaranteed by design.
3. Sample tested.

ELECTRICAL CHARACTERISTICS at $V_S = 5V$, $V_{S-} = 0V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-02 CMP-02E MIN	 TYP	 MAX	CMP-02C MIN	 TYP	 MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \le 5k\Omega$, (Note 1)	—	0.4	1.5	—	0.5	3.5	mV
Input Offset Current	I_{OS}	(Note 1)	—	0.25	3	—	0.35	14	nA
Input Bias Current	I_B		—	24	45	—	30	90	nA
Voltage Gain	A_V	$V_O = 0.4V$ to $2.4V$, (Notes 1, 2)	—	50	—	—	50	—	V/mV
Response Time	t_r	100mV Step, 5mV Overdrive 5kΩ to 5V (Pull-Up)	—	250	—	—	250	—	ns
		TTL Fan-Out = 4, 5kΩ to 5V	—	250	—	—	250	—	
Input Voltage Range	CMVR		1.8-3.5	1.7-3.8	—	1.8-3.5	1.7-3.8	—	V
Saturation Voltage	V_{OL}	$V_{IN} \le -3.5mV$, $I_{sink} \le 6.4mA$	—	0.3	0.45	—	0.3	0.45	V
Positive Supply Current	I+	$V_{IN} \le -10mV$	—	2.2	3	—	2.3	3.6	mA
Power Dissipation	P_d	$V_{IN} \le -10mV$	—	11	15	—	11.5	18	mW

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \le T_A \le 125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-02 MIN	 TYP	 MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \le 5k\Omega$, (Note 1)	—	0.4	1.6	mV
		$V_{S+} = 5V$, $V_{S-} = 0V$, (Note 1)	—	0.5	2.8	
Average Input Offset Voltage Drift						
Without External Trim	TCV_{OS}	$R_S = 50\Omega$	—	1.5	—	µV/°C
With External Trim	TCV_{OSn}	$R_S = 50\Omega$	—	1.0	—	
Input Offset Current	I_{OS}	$T_A = +125°C$, (Note 1)	—	0.3	4	nA
		$T_A = -55°C$, (Note 1)	—	0.4	12	
Average Input Offset Current Drift	TCI_{OS}	$+25°C \le T_A \le +125°C$	—	2	—	pA/°C
		$-55°C \le T_A \le +25°C$	—	4	—	
Input Bias Current	I_B	$T_A = +125°C$	—	25	50	nA
		$T_A = -55°C$	—	45	120	
Voltage Gain	A_V	$V_O = 0.4V$ to $2.4V$, (Notes 1, 2)	100	500	—	V/mV
Response Time	t_r	100mV Step, 5mV Overdrive $T_A = +125°C$, No Load	—	310	—	ns
		$T_A = -55°C$, No Load	—	155	—	
Input Voltage Range	CMVR		±12	±13	—	V
Common-Mode Rejection Ratio	CMRR		88	106	—	dB
Power Supply Rejection Ratio	PSRR	$5V \le V_{S+} \le 15V$, $-15V \le V_{S-} \le 0V$	75	96	—	dB
Positive Output Voltage	V_{OH}	$V_{IN} \ge 4mV$, $I_O = 200\mu A$	2.4	3	—	V
Saturation Voltage	V_{OL}	$V_{IN} \le -10mV$, $I_{sink} = 0mA$	—	0.20	0.4	V
		$V_{IN} \le -10mV$, $I_{sink} = 6.4mA$	—	0.32	0.5	

NOTES:

1. These Parameters are specified as the maximum values required to drive the output between the logic levels of 0.4V and 2.4V with a 1kΩ load tied to +5V; thus, these parameters define an error band which takes into account the worst case effects of voltage gain and input impedance.
2. Guaranteed by design.
3. Sample tested.

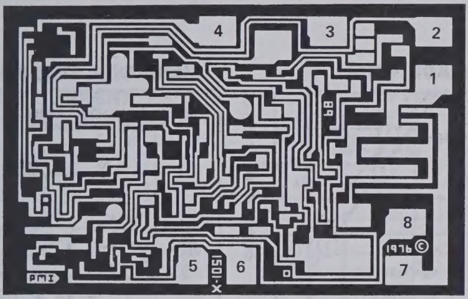
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $0°C \leq T_A \leq 70°C$, unless otherwise noted.

			CMP-02E			CMP-02C			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$, (Note 1)	—	0.4	1.4	—	0.5	3.5	mV
		$V_{S+} = 5V$, $V_{S-} = 0V$, (Note 1)	—	0.5	2.4	—	0.6	4.3	
Average Input Offset Voltage Drift									
Without External Trim	TCV_{OS}	$R_S = 50\Omega$	—	1.5	—	—	1.8	—	µV/°C
With External Trim	TCV_{OSn}	$R_S = 50\Omega$	—	1	—	—	1.2	—	
Input Offset Current	I_{OS}	$T_A = +70°C$, (Note 1)	—	0.3	3	—	0.4	15	nA
		$T_A = 0°C$, (Note 1)	—	0.4	6	—	0.5	25	
Average Input Offset Current Drift	TCI_{OS}	$+25°C \leq T_A \leq +70°C$	—	2	—	—	3	—	pA/°C
		$0°C \leq T_A \leq +25°C$	—	4	—	—	5	—	
Input Bias Current	I_B	$T_A = +70°C$	—	26	50	—	33	100	nA
		$T_A = 0°C$	—	34	80	—	42	160	
Voltage Gain	A_V	$V_O = 0.4V$ to $2.4V$, (Notes 1, 2)	100	500	—	70	500	—	V/mV
Response Time	t_r	100mV Step, 5mV Overdrive							ns
		$T_A = +70°C$, No Load	—	225	—	—	225	—	
		$T_A = 0°C$, No Load	—	180	—	—	180	—	
Input Voltage Range	CMVR		±12.0	±13	—	±12	±13	—	V
Common-Mode Rejection Ratio	CMRR		90	108	—	86	108	—	dB
Power Supply Rejection Ratio	PSRR	$5V \leq V_{S+} \leq 15V$, $-15V \leq V_{S-} \leq 0V$	77	98	—	70	88	—	dB
Positive Output Voltage	V_{OH}	$V_{IN} \geq 4mV$, $I_O = 200\mu A$	2.4	3.2	—	2.4	3.2	—	V
Saturation Voltage	V_{OL}	$V_{IN} \leq -10mV$, $I_{sink} = 0$	—	0.17	0.4	—	0.17	0.4	V
		$V_{IN} \leq -10mV$, $I_{sink} = 6.4mA$	—	0.30	0.5	—	0.31	0.5	

NOTES:

1. These Parameters are specified as the maximum values required to drive the output between the logic levels of 0.4V and 2.4V with a 1kΩ load tied to +5V; thus, these parameters define an error band which takes into account the worst case effects of voltage gain and input impedance.
2. Guaranteed by design.
3. Sample tested.

DICE CHARACTERISTICS



1. GROUND
2. NONINVERTING INPUT
3. INVERTING INPUT
4. NEGATIVE SUPPLY (SUBSTRATE)
5. BALANCE
6. BALANCE
7. OUTPUT
8. POSITIVE SUPPLY

DIE SIZE 0.065 × 0.042 inch, 2730 sq. mils
(1.651 × 1.069 mm, 1.761 sq. mm)

For additional DICE information refer to Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$.

PARAMETER	SYMBOL	CONDITIONS	CMP-02N TYPICAL	CMP-02GR TYPICAL	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$ $R_S \leq 50k\Omega$	0.8 0.9	2.8 3	mV MAX
Input Offset Current	I_{OS}		3	15	nA MAX
Input Bias Current	I_B		50	100	nA MAX
Differential Input Resistance	R_{IN}		5	1.5	MΩ MIN
Input Voltage Range	CMVR		±12.5	±12.5	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm CMVR$	94	90	dB MIN
Power Supply Rejection Ratio	PSRR	$5V \leq V_S+ \leq 18V$ $-18V \leq V_S- \leq 0V$	80	74	dB MIN
Positive Output Voltage	V_{OH}	$V_{IN} \geq 3mV$, $I_O = 320\mu A$ $V_{IN} \geq 3mV$, $I_O = 240\mu A$	2.4 —	— 2.4	V MIN
Saturation Voltage	V_{OL}	$I_{sink} = 6.4mA$	0.45	0.45	V MAX
Output Leakage Current	I_{LEAK}	$V_{IN} \geq 10mV$, $V_O = 30V$	2	8	μA MAX
Positive Supply Current	I+	$V_{IN} \leq -10mV$	8	8.5	mA MAX
Negative Supply Current	I−	$V_{IN} \leq -10mV$	2.2	2.2	mA MAX
Power Consumption	P_d	$V_{IN} \leq -10mV$	153	161	mW MAX

WAFER TEST LIMITS at $V_S+ = 5V$ and $V_S- = 0V$, $T_A = 25°C$.

PARAMETER	SYMBOL	CONDITIONS	CMP-02N LIMIT	CMP-02GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$	1.5	3.5	mV MAX
Input Offset Current	I_{OS}		3	14	nA MAX

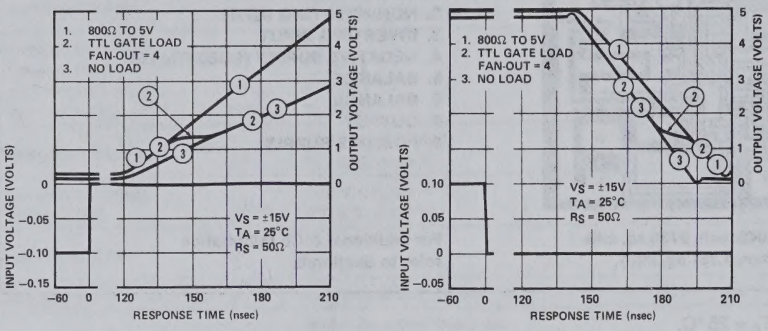
Note: Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$.

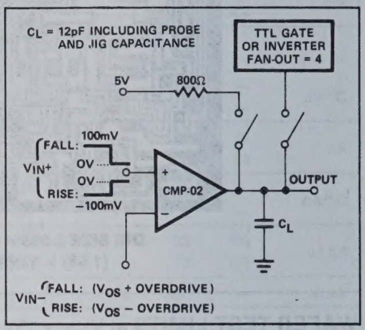
PARAMETER	SYMBOL	CONDITIONS	CMP-02N TYPICAL	CMP-02GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}	$R_S = 50\Omega$	1.5	1.8	μV/°C
Average Input Offset Current Drift	TCI_{OS}		4	5	pA/°C
Response Time	t_r	100mV Step, 5mV Overdrive No Load (No Pull-Up), $T_A = 25°C$	190	190	ns

TYPICAL PERFORMANCE CHARACTERISTICS

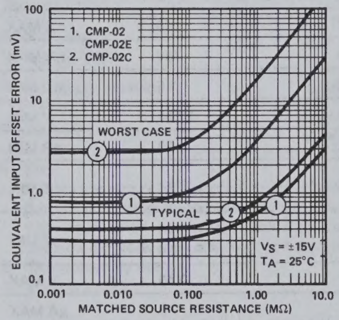
RESPONSE TIME, 100mV STEP, 5mV OVERDRIVE, VARIOUS LOADS



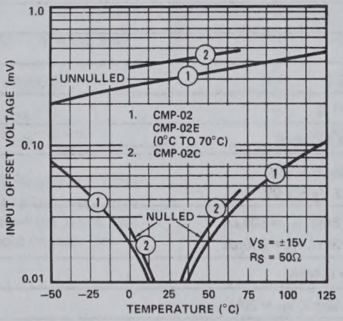
RESPONSE TIME TEST CIRCUIT


CL = 12pF INCLUDING PROBE AND JIG CAPACITANCE
TTL GATE OR INVERTER FAN-OUT = 4
5V
800Ω
FALL: 100mV
OV
VIN+
OV
RISE: −100mV
CMP-02
OUTPUT
CL
VIN− FALL: (VOS + OVERDRIVE)
RISE: (VOS − OVERDRIVE)

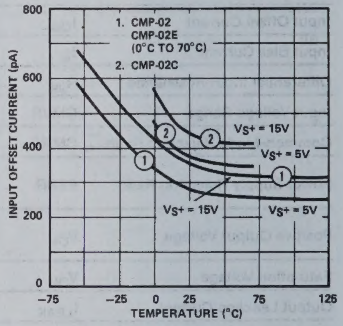
INPUT OFFSET ERROR vs SOURCE RESISTANCE



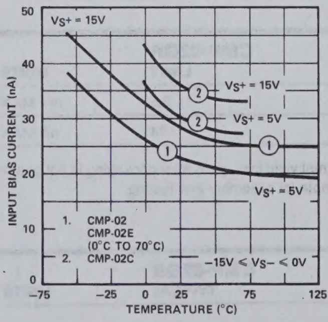
OFFSET VOLTAGE vs TEMPERATURE



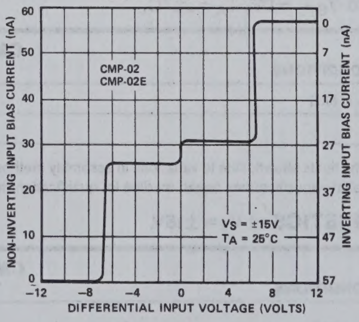
INPUT OFFSET CURRENT vs TEMPERATURE



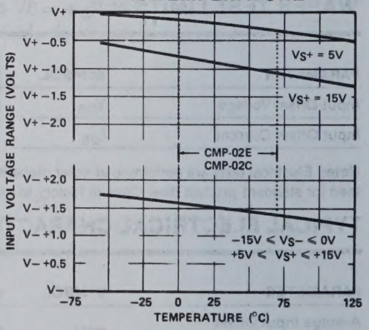
INPUT BIAS CURRENT vs TEMPERATURE



INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE

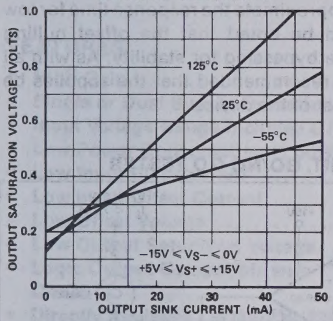


INPUT VOLTAGE RANGE vs TEMPERATURE

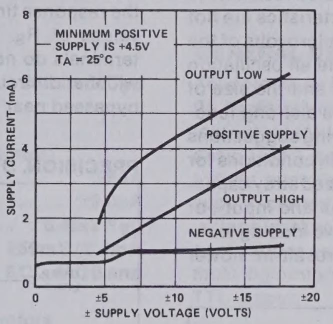


TYPICAL PERFORMANCE CHARACTERISTICS

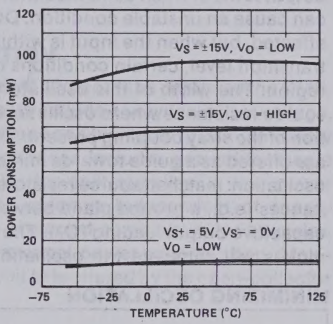
SATURATION VOLTAGE vs SINK CURRENT



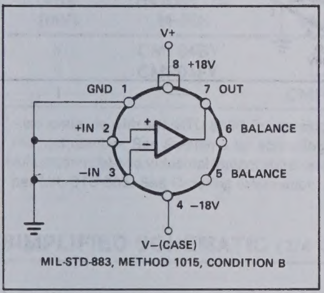
SUPPLY CURRENT vs SUPPLY VOLTAGE



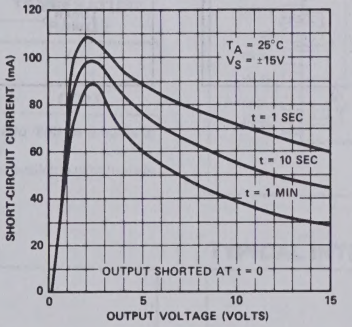
POWER CONSUMPTION vs TEMPERATURE



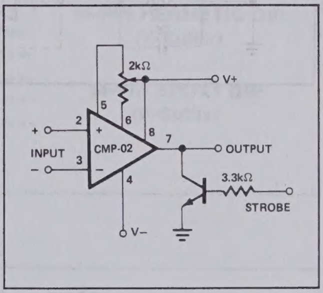
STANDARD BURN-IN CIRCUIT


V+
8 +18V
GND 1
7 OUT
+IN 2
6 BALANCE
−IN 3
5 BALANCE
4 −18V
V−(CASE)
MIL-STD-883, METHOD 1015, CONDITION B

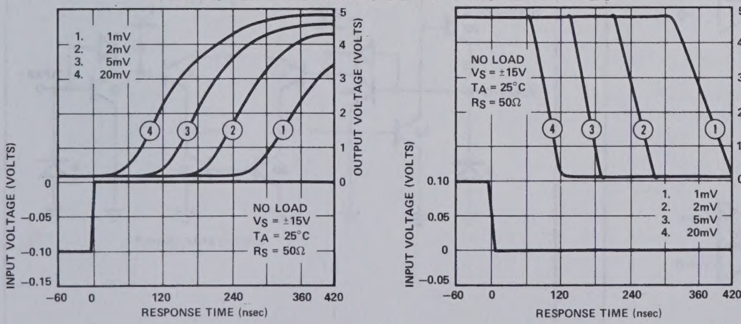
OUTPUT SHORT-CIRCUIT CURRENT vs OUTPUT VOLTAGE



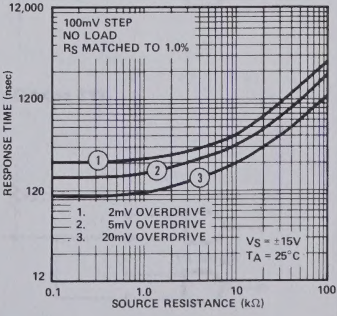
OFFSET TRIMMING AND STROBE CIRCUITS


2kΩ
V+
+
INPUT
−
2
3
5
6
8
7
CMP-02
4
OUTPUT
3.3kΩ
STROBE
V−

RESPONSE TIME, 100mV STEP AND VARIOUS INPUT OVERDRIVES



RESPONSE TIME vs SOURCE RESISTANCE



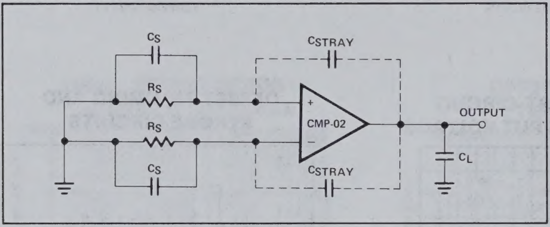
APPLICATIONS INFORMATION

The CMP-02 provides fast response times even with small overdrives; to achieve this performance requires very high gain at high frequencies. The CMP-02 is completely free of oscillations; however, small values of stray capacitance from output to input when combined with high-source resistances can cause an unstable condition. DC characteristics are not affected, but when the input is within a few microvolts of the transition level, certain conditions can create an oscillation region. The width of this oscillatory region and the size of source resistance where oscillations begin is a strong function of the stray coupling present. The following suggestions are offered as a guide towards minimizing the conditions for oscillation: matched source resistors, minimized stray capacitances (e.g., a ground plane between output and input), or capacitive output loading (C_L). The capacitive loading techniques will eliminate the oscillations, but result in slower response time. Matched bypass capacitors across the input resistors also can eliminate the instability,

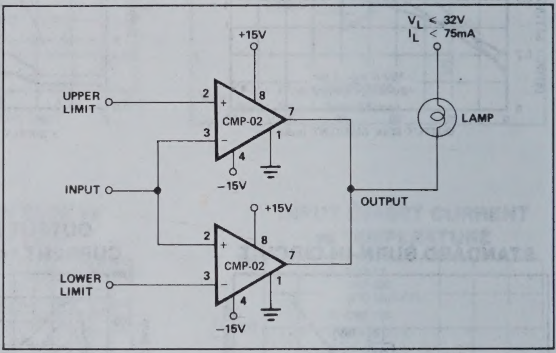
$$\text{and if } C_S \ge 20\text{pF}\left(\frac{\text{maximum step size}}{\text{minimum overdrive}}\right)$$

the response time will approximate the response time for low values of R_S. It should be noted that the offset nulling terminals do not require bypassing for stability. As with all wideband circuits, it is recommended that the supplies be bypassed near the socket of the device.

MINIMIZING OSCILLATION



PRECISION, DUAL LIMIT, GO/NO GO TESTER



QUAD LOW-POWER PRECISION COMPARATOR

CMP-04

FEATURES

- **High Gain .... 200V/mV Typ**
- **Single or Dual Supply Operation**
- **Input Voltage Range Includes Ground**
- **Low Power Consumption (1.5mW/Comparator)**
- **Low Input Bias Current 25nA**
- **Low Input Offset Current .... ±2.0nA**
- **Low Offset Voltage .... ±0.4mV Typ**
- **Low Output Saturation Voltage .... 250mV @ 4mA**
- **Logic Output Compatible with TTL, DTL, ECL, MOS and CMOS**
- **Directly Replaces LM139/239/339 Comparators**

ORDERING INFORMATION†

25°C V_{OS} (mV)	DIP PACKAGE HERMETIC 14-PIN	PLASTIC 14-PIN	OPERATING TEMPERATURE RANGE
1	CMP04BY*	—	MIL
1	CMP04FY	—	IND
1	—	CMP04FP	COM

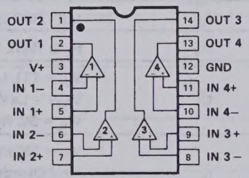
*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

GENERAL DESCRIPTION

Four precision independent comparators comprise the CMP-04. Performance highlights include a very low offset voltage, low output saturation voltage and high gain in a single supply design. The input voltage range includes ground for single supply operation and V− for split supplies. A low power supply current of 2mA, which is independent of supply voltage, makes this the preferred comparator for precision applications requiring minimal power consumption. Maximum logic interface flexibility is offered by the open-collector TTL output.

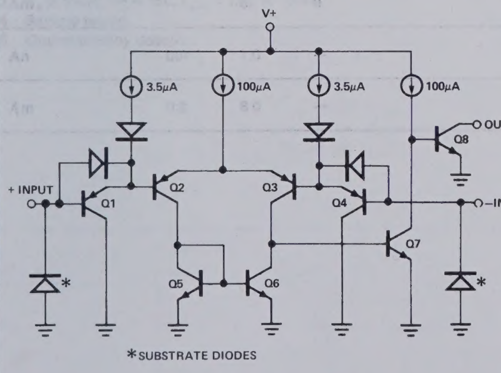
PIN CONNECTIONS


OUT 2 1
OUT 1 2
V+ 3
IN 1− 4
IN 1+ 5
IN 2− 6
IN 2+ 7
14 OUT 3
13 OUT 4
12 GND
11 IN 4+
10 IN 4−
9 IN 3+
8 IN 3−
1
2
3
4

14-PIN HERMETIC DIP (Y-Suffix)

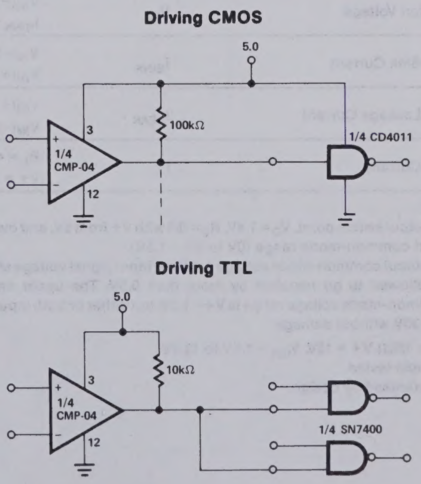
14-PIN EPOXY DIP (P-Suffix)

SIMPLIFIED SCHEMATIC (1/4 CMP-04)


V+
3.5μA
100μA
3.5μA
100μA
OUTPUT
Q8
+ INPUT
Q1
Q2
Q3
Q4
−INPUT
Q7
Q5
Q6
*
*

*SUBSTRATE DIODES

TYPICAL INTERFACE


Driving CMOS
5.0
100kΩ
3
+
1/4
CMP-04
−
12
1/4 CD4011
Driving TTL
5.0
10kΩ
3
+
1/4
CMP-04
−
12
1/4 SN7400

ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage	36V or ±18V
Differential Input Voltage	$36V_{DC}$
Input Voltage	−0.3V to +36V
Power Dissipation (Note 1)	500mW
Operating Temperature Range	
CMP-04FY	−25°C to +85°C
CMP-04BY	−55°C to +125°C
CMP-04FP	0°C to +70°C
DICE Junction Temperature (T_j)	−65°C to +150°C
Storage Temperature Range	−65°C to +150°C
P-Suffix	−65°C to +125°C
Input Current ($V_{IN} < -3.0V$)	50mA
Output Short Circuit to GND	Continuous
Lead Temperature (Soldering, 60 sec)	300°C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.
2. Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
Hermetic DIP (Y)	100°C	10mW/°C
Plastic DIP (P)	50°C	6mW/°C

ELECTRICAL CHARACTERISTICS at V+ = +5V, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-04B/F MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S = 0\Omega$, $R_L = 5.1k\Omega$ $V_O = 1.4V$, (Note 1)	—	0.4	1	mV
Input Offset Current	I_{OS}	$I_{IN}(+) - I_{IN}(-)$ $R_L = 5.1k\Omega$ $V_O = 1.4V$	—	2	10	nA
Input Bias Current	I_B	$I_{IN}(+)$ or $I_{IN}(-)$	—	25	100	nA
Voltage Gain	A_V	$R_L \geq 15k\Omega$, V+ = 15V, (Note 5)	80	200	—	V/mV
Large-Signal Response Time	t_r	V_{IN} = TTL Logic Swing $V_{REF} = 1.4V$, (Note 4) $V_{RL} = 5V$, $R_L = 5.1k\Omega$	—	300	—	ns
Small-Signal Response Time	t_r	$V_{IN} = 100mV$ Step, (Note 4) 5mV Overdrive $V_{RL} = 5V$, $R_L = 5.1k\Omega$	—	1.3	—	µs
Input Voltage Range	CMVR	(Note 2)	0	—	V+ −1.5	V
Common-Mode Rejection Ratio	CMRR	(Notes 3, 5)	80	100	—	dB
Power Supply Rejection Ratio	PSRR	V+ = +5V to 18V, (Note 5)	80	100	—	dB
Saturation Voltage	V_{OL}	$V_{IN}(-) \geq 1V$, $V_{IN}(+) = 0$, $I_{SINK} \leq 4mA$	—	250	400	mV
Output Sink Current	I_{SINK}	$V_{IN}(-) \geq 1V$, $V_{IN}(+) = 0$, $V_O \leq 1.5V$	6	16	—	mA
Output Leakage Current	I_{LEAK}	$V_{IN}(+) \geq 1V$, $V_{IN}(-) = 0$, $V_O = 5V$	—	0.1	100	nA
Supply Current	I+	$R_L = \infty$, All Comps V+ = 30V	—	0.8	2.0	mA

NOTES:

1. At output switch point, $V_O = 1.4V$, $R_S = 0\Omega$ with V+ from 5V; and over the full input common-mode range (0V to V+ − 1.5V).
2. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ − 1.5V, but either or both inputs can go to +30V without damage.
3. $R_L \geq 15k\Omega$ V+ = 15V, V_{CM} = 1.5V to 13.5V.
4. Sample tested.
5. Guaranteed by design.

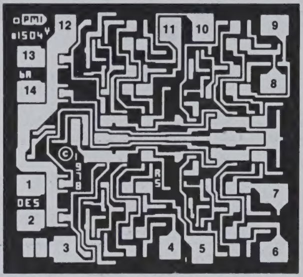
ELECTRICAL CHARACTERISTICS at V+ = +5V. For CMP-04BY, $-55°C \le T_A \le 125°C$. For CMP-04FY, $-25°C \le T_A \le 85°C$. For CMP-04FP, $0°C \le T_A \le 70°C$, unless otherwise noted.

			CMP-04B/F (Note 3)			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}	$R_S = 0\Omega$, $R_L = 5.1k\Omega$ $V_O = 1.4V$, (Note 1)	—	1	2	mV
Input Offset Current	I_{OS}	$I_{IN}(+) - I_{IN}(-)$ $R_L = 5.1k\Omega$ $V_O = 1.4V$	—	4	20	nA
Input Bias Current	I_B	$I_{IN}(+)$ or $I_{IN}(-)$	—	40	200	nA
Voltage Gain	A_V	$R_L \ge 15k\Omega$, V+ = 15V, (Note 5)	70	125	—	V/mV
Large-Signal Response Time	t_r	V_{IN} = TTL Logic Swing $V_{REF} = 1.4V$, (Note 4) $V_{RL} = 5V$, $R_L = 5.1k\Omega$	—	300	—	ns
Small-Signal Response Time	t_r	$V_{IN} = 100mV$ Step, (Note 4) 5mV Overdrive $V_{RL} = 5V$, $R_L = 5.1k\Omega$	—	1.3	—	μs
Input Voltage Range	CMVR	(Note 2)	0	—	V+ −1.5	V
Common-Mode Rejection Ratio	CMRR	(Notes 3, 5)	60	100	—	dB
Power Supply Rejection Ratio	PSRR	V+ = +5V to 18V	80	100	—	dB
Saturation Voltage	V_{OL}	$V_{IN}(-) \ge 1V$, $V_{IN}(+) = 0$, $I_{SINK} \le 4mA$	—	250	700	mV
Output Sink Current	I_{SINK}	$V_{IN}(-) \ge 1V$, $V_{IN}(+) = 0$, $V_O \le 1.5V$	5	16	—	mA
Output Leakage Current	I_{LEAK}	$V_{IN}(+) \ge 1V$, $V_{IN}(-) = 0$, $V_O = 5V$	—	0.1	200	nA
Supply Current	I+	$R_L = \infty$, All Comps V+ = 30V	—	1.2	3.0	mA

NOTES:

1. At output switch point, $V_O = 1.4V$, $R_S = 0\Omega$ with V+ from 5V; and over the full input common-mode range (0V to V+ − 1.5V).
2. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ − 1.5V, but either or both inputs can go to +30V without damage.
3. $R_L \ge 15k\Omega$, V+ = 15V, V_{CM} = 1.5V to 13.5V.
4. Sample tested.
5. Guaranteed by design.

DICE CHARACTERISTICS



DIE SIZE 0.052 × 0.056 inch, 2912 sq. mils
(1.32 × 1.42 mm, 1.88 sq. mm)

1. OUTPUT (2)
2. OUTPUT (1)
3. POSITIVE SUPPLY
4. INVERTING INPUT (1)
5. NONINVERTING INPUT (1)
6. INVERTING INPUT (2)
7. NONINVERTING INPUT (2)
8. INVERTING INPUT (3)
9. NONINVERTING INPUT (3)
10. INVERTING INPUT (4)
11. NONINVERTING INPUT (4)
12. GROUND (SUBSTRATE)
13. OUTPUT (4)
14. OUTPUT (3)

For additional DICE information refer to Section 2.

WAFER TEST LIMITS at $V+ = +5V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-04N LIMIT	CMP-04G LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S = 0\Omega$, $R_L = 5.1k\Omega$ $V_O = 1.4V$, (Note 1)	1	2	mV MAX
Input Offset Current	I_{OS}	$I_{IN}(+) - I_{IN}(-)$ $R_L = 5.1k\Omega$ $V_O = 1.4V$	10	25	nA MAX
Input Bias Current	I_B	$I_{IN}(+)$ or $I_{IN}(-)$, (Note 1)	100	100	nA MAX
Voltage Gain	A_V	$R_L \geq 15k\Omega$, $V+ = 15V$, (Note 3)	80	50	V/mV MIN
Input Voltage Range	CMVR	(Notes 2, 3)	$V+ - 1.5$	$V+ - 1.5$	V MAX
Common-Mode Rejection Ratio	CMRR	(Note 4)	80	80	dB MIN
Power Supply Rejection Ratio	PSRR	$V+ = 5V$ to $+18V$	80	80	dB MIN
Saturation Voltage	V_{OL}	$V_{IN}(-) \geq 1V$, $V_{IN}(+) = 0$, $I_{SINK} \leq 4mA$	400	400	mV MAX
Output Sink Current	I_{SINK}	$V_{IN}(-) \geq 1V$, $V_{IN}(+) = 0$, $V_O \leq 1.5V$	6	6	mA MIN
Output Leakage Current	I_{LEAK}	$V_{IN}(+) \geq 1V$, $V_{IN}(-) = 0$, $V_O = 5V$	100	100	nA MAX
Supply Current	$I+$	$R_L = \infty$, All Comps $V+ = 30V$	2	2	mA MAX

Note: Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

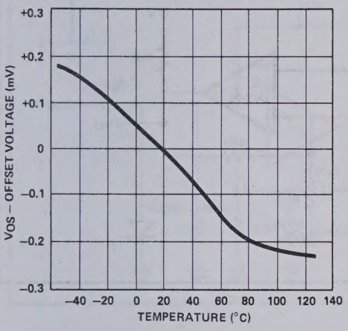
TYPICAL ELECTRICAL CHARACTERISTICS at $V+ = +5V$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-04N TYPICAL	CMP-04G TYPICAL	UNITS
Large-Signal Response Time	t_r	V_{IN} = TTL Logic Swing $V_{REF} = 1.4V$, (Note 5) $V_{RL} = 5V$, $R_L = 5.1k\Omega$	300	300	ns
Small-Signal Response Time	t_r	$V_{IN} = 100mV$ Step, (Note 5) 5mV Overdrive $V_{RL} = 5V$, $R_L = 5.1k\Omega$	1.3	1.3	µs

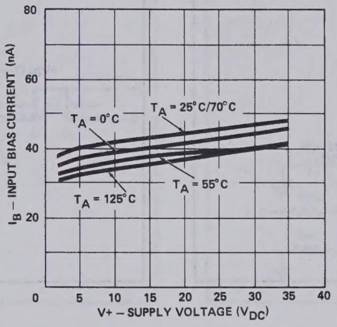
NOTES:
1. At output switch point, $V_O = 1.4V$, $R_S = 0\Omega$ with V+ from 5V; and over the full input common-mode range (0V to $V+ - 1.5V$).
2. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V+ - 1.5V$, but either or both inputs can go to +30V without damage.
3. Guaranteed by design.
4. $R_L \geq 15k\Omega$. $V_{CM} = 1.5V$ to $13.5V$.
5. Sample tested.

TYPICAL PERFORMANCE CHARACTERISTICS

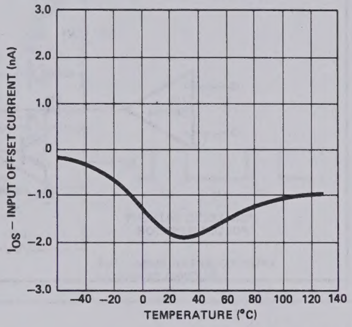
OFFSET VOLTAGE vs TEMPERATURE



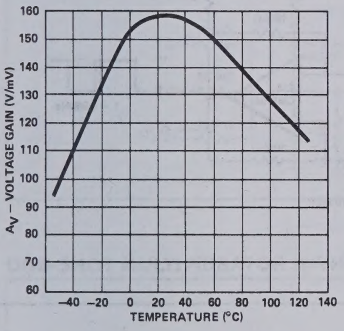
INPUT BIAS CURRENT vs V+ AND TEMPERATURE



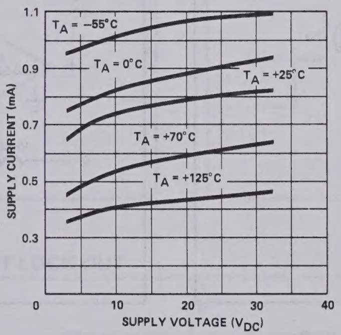
INPUT OFFSET CURRENT vs TEMPERATURE



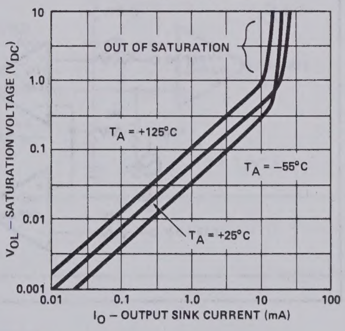
VOLTAGE GAIN vs TEMPERATURE



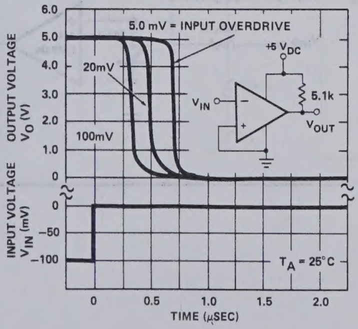
SUPPLY CURRENT vs SUPPLY VOLTAGE



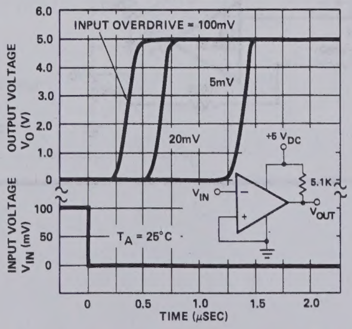
OUTPUT VOLTAGE vs OUTPUT CURRENT AND TEMPERATURE



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES — NEGATIVE TRANSITION

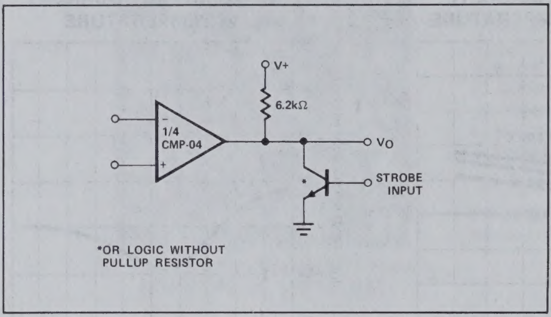


RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES — POSITIVE TRANSITION

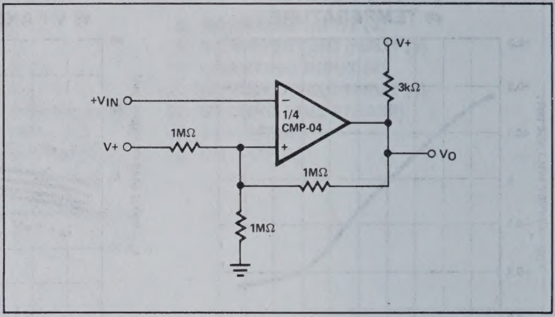


TYPICAL APPLICATIONS

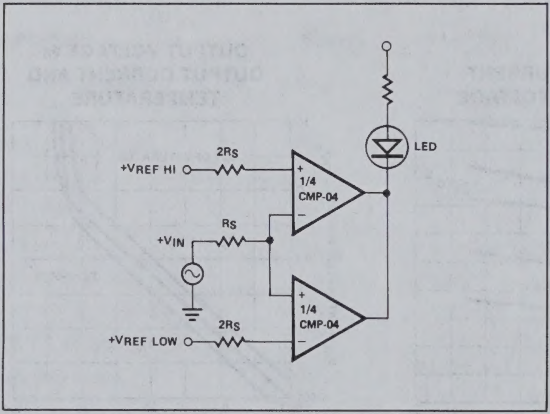
OUTPUT STROBING


V+
6.2kΩ
1/4
CMP-04
VO
*
STROBE INPUT
*OR LOGIC WITHOUT PULLUP RESISTOR

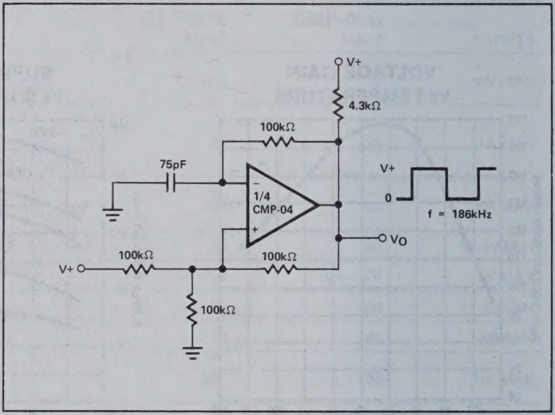
INVERTING COMPARATOR WITH HYSTERESIS


V+
3kΩ
+VIN
1/4
CMP-04
V+
1MΩ
VO
1MΩ
1MΩ

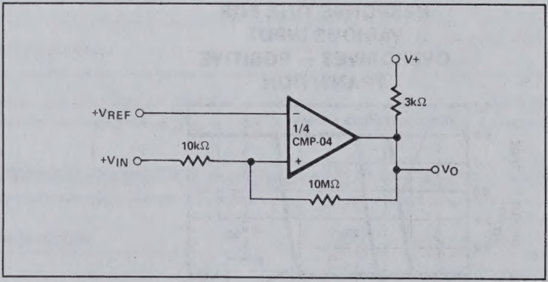
LIMIT COMPARATOR


LED
2RS
+VREF HI
1/4
CMP-04
RS
+VIN
1/4
CMP-04
2RS
+VREF LOW

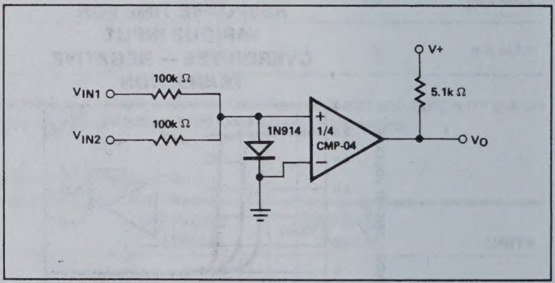
SQUAREWAVE OSCILLATOR


V+
4.3kΩ
100kΩ
75pF
1/4
CMP-04
V+
0
f = 186kHz
VO
V+
100kΩ
100kΩ
100kΩ

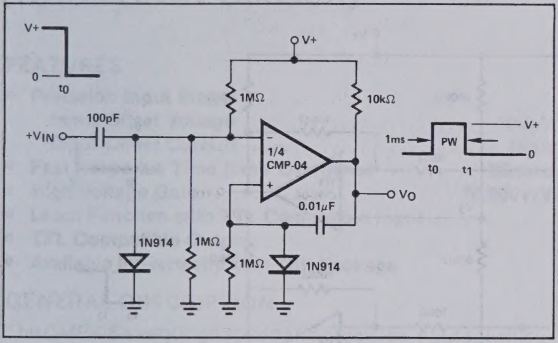
NONINVERTING COMPARATOR WITH HYSTERESIS


V+
3kΩ
+VREF
1/4
CMP-04
+VIN
10kΩ
VO
10MΩ

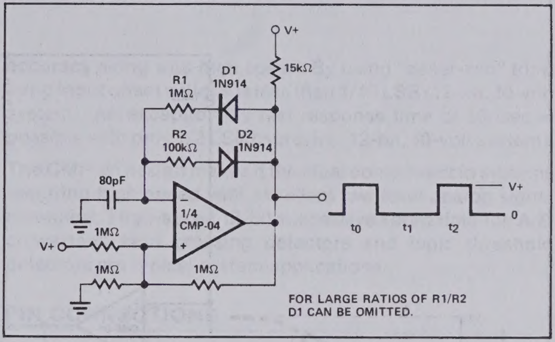
COMPARING INPUT VOLTAGES OF OPPOSITE POLARITY


V+
5.1k Ω
VIN1
100k Ω
VIN2
100k Ω
1N914
1/4
CMP-04
VO

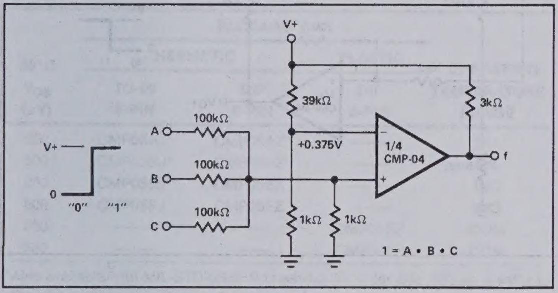
ONE-SHOT MULTIVIBRATOR


V+
0
t0
V+
1MΩ
10kΩ
100pF
+VIN
1ms
PW
V+
0
t0
t1
1/4
CMP-04
VO
0.01μF
1N914
1MΩ
1MΩ
1N914

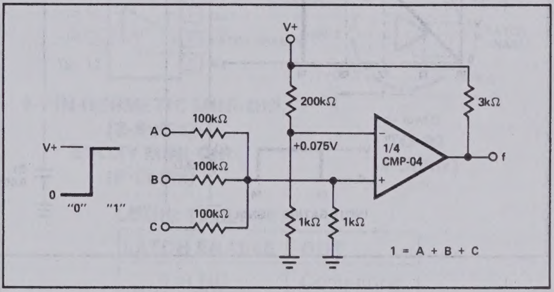
PULSE GENERATOR


V+
15kΩ
D1
1N914
R1
1MΩ
R2
100kΩ
D2
1N914
80pF
1/4
CMP-04
V+
t0
t1
t2
0
V+
1MΩ
1MΩ
1MΩ
FOR LARGE RATIOS OF R1/R2
D1 CAN BE OMITTED.

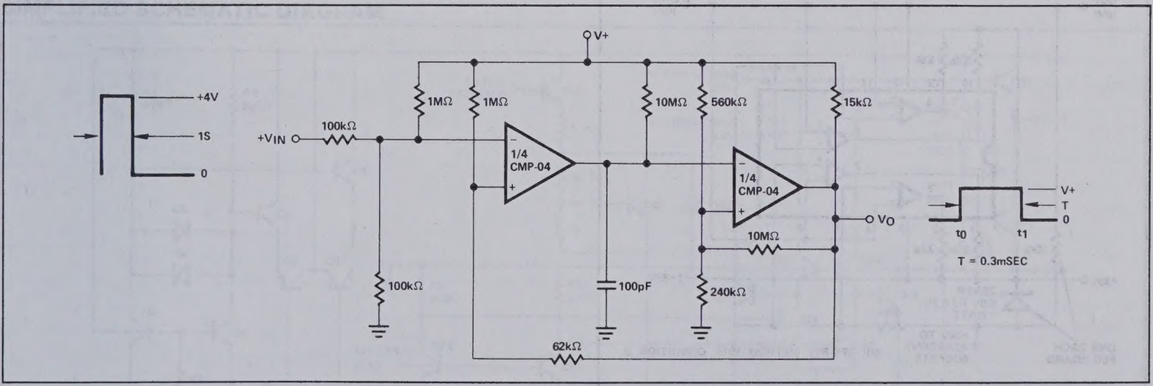
AND GATE


V+
39kΩ
3kΩ
100kΩ
A
+0.375V
1/4
CMP-04
f
V+
100kΩ
B
0
"0"
"1"
100kΩ
C
1kΩ
1kΩ
1 = A • B • C

OR GATE

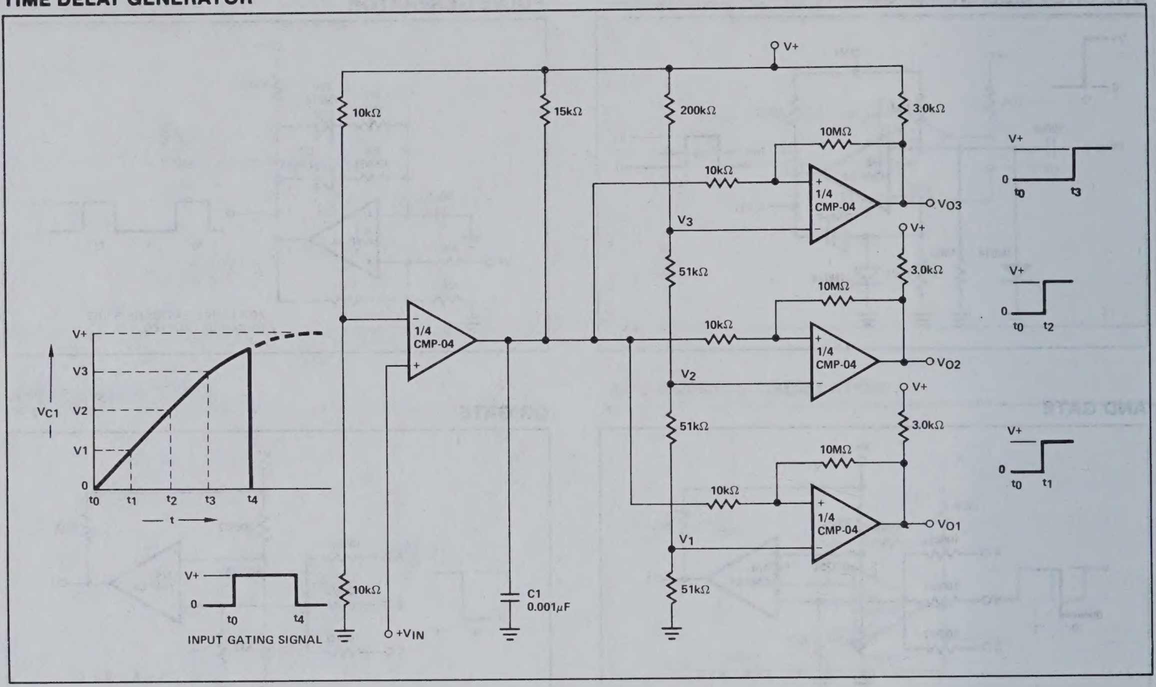

V+
200kΩ
3kΩ
100kΩ
A
+0.075V
1/4
CMP-04
f
V+
100kΩ
B
0
"0"
"1"
100kΩ
C
1kΩ
1kΩ
1 = A + B + C

ONE-SHOT MULTIVIBRATOR WITH INPUT LOCK OUT

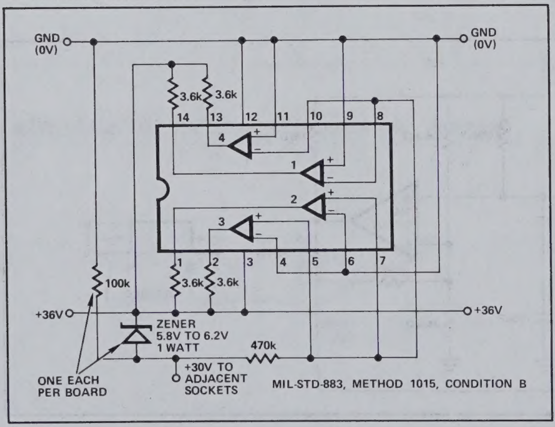

+4V
1S
0
V+
1MΩ
1MΩ
10MΩ
560kΩ
15kΩ
+VIN
100kΩ
1/4
CMP-04
1/4
CMP-04
VO
V+
T
0
t0
t1
T = 0.3mSEC
10MΩ
100kΩ
100pF
240kΩ
62kΩ

TYPICAL APPLICATIONS

TIME DELAY GENERATOR


V+
10kΩ
15kΩ
200kΩ
3.0kΩ
10MΩ
10kΩ
1/4 CMP-04
VO3
V3
51kΩ
VO2
V2
VO1
V1
10kΩ
C1 0.001μF
+VIN
V+
V3
VC1
V2
V1
0
t0 t1 t2 t3 t4
t
V+
0
t0 t4
INPUT GATING SIGNAL
V+ 0 t0 t3
V+ 0 t0 t2
V+ 0 t0 t1

BURN-IN CIRCUIT


GND (0V)
GND (0V)
3.6k
3.6k
14 13 12 11 10 9 8
4
1
2
3
1 2 3 4 5 6 7
100k
3.6k
3.6k
+36V
+36V
ZENER 5.8V TO 6.2V 1 WATT
470k
+30V TO ADJACENT SOCKETS
ONE EACH PER BOARD
MIL-STD-883, METHOD 1015, CONDITION B

HIGH-SPEED PRECISION COMPARATOR (WITH LATCH CIRCUIT)

CMP-05

FEATURES

- **Precision Input Stage**
  - **Input Offset Voltage 100µV**
  - **Input Offset Current 15nA**
- **Fast Response Time (5mV Overdrive) 35nsec**
- **High Voltage Gain 16,000V/V**
- **Latch Function with TTL Compatible Input**
- **TTL Compatible Output**
- **Available in Hermetic Mini-DIP Package**

GENERAL DESCRIPTION

The CMP-05's very high speed and precision input specifications make it the ideal comparator in systems needing 12-bit accuracy along with high speed. By using "zener-zap" trimming input offset voltage is less than 1/10 LSB (12-bit, 10-volt system). An exceptionally fast response time of 50nsec is possible with only 1/2 LSB overdrive (12-bit, 10-volt system).

The CMP-05 design makes it the ideal component in systems requiring high speed with excellent low-level analog signal resolution. High-speed 12-bit successive approximation A/D converters, zero crossing detectors and logic threshold detectors are typical system applications.

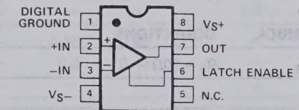
ORDERING INFORMATION

25°C	PACKAGE			
	HERMETIC		PLASTIC	OPERATING
V_{OS} (µV)	TO-99 8-PIN	DIP 8-PIN	DIP 8-PIN	TEMPERATURE RANGE
250	CMP05AJ*	CMP05AZ*	——	MIL
600	CMP05BJ*	CMP05BZ*	——	MIL
250	CMP05EJ	CMP05EZ	——	IND
600	CMP05FJ	CMP05FZ	——	IND
250	——	——	CMP05EP	COM
600	——	——	CMP05FP	COM

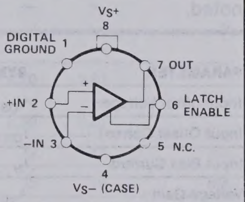
*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

PIN CONNECTIONS


DIGITAL GROUND
+IN
−IN
$V_{S}-$
1
2
3
4
8
7
6
5
$V_{S}+$
OUT
LATCH ENABLE
N.C.

8-PIN HERMETIC MINI-DIP (Z-Suffix)
EPOXY MINI-DIP (P-Suffix)

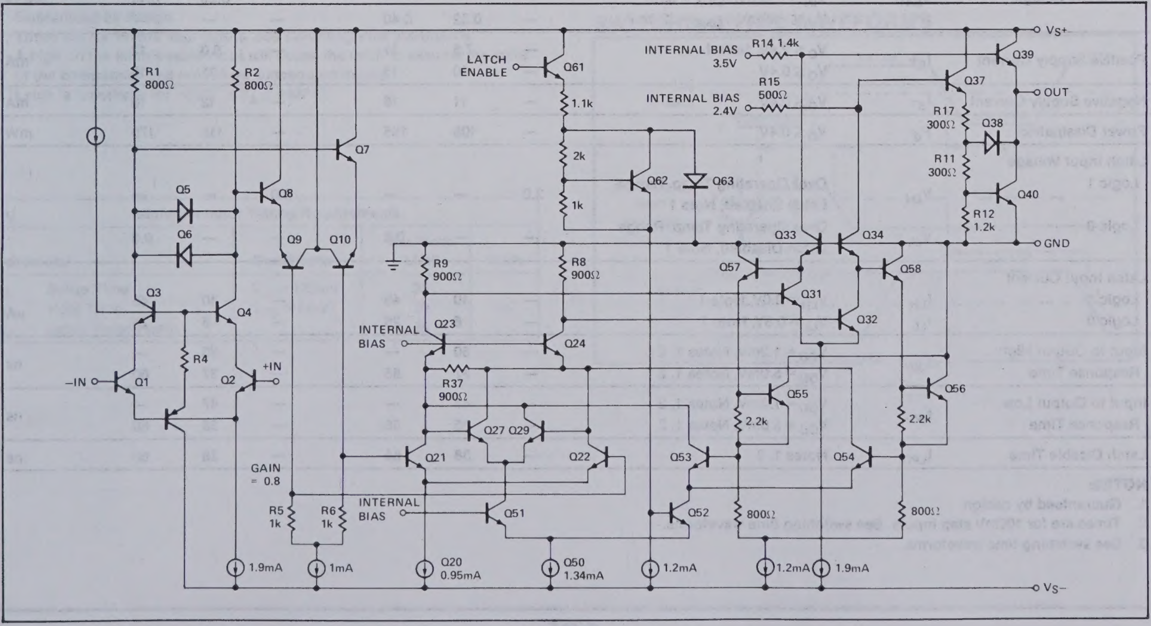

Vs+
8
DIGITAL GROUND 1
7 OUT
+IN 2
6 LATCH ENABLE
−IN 3
5 N.C.
4
Vs− (CASE)

TO-99 (J-Suffix)

LOGIC TABLE

LATCH ENABLE	OUT
0 or NC	Comparing
1	Latched

SIMPLIFIED SCHEMATIC DIAGRAM


R1 800Ω
R2 800Ω
Q7
Q5
Q8
Q6
Q9
Q10
Q3
Q4
R4
−IN
Q1
Q2
+IN
GAIN = 0.8
R5 1k
R6 1k
1.9mA
1mA
LATCH ENABLE
Q61
1.1k
2k
1k
Q62
Q63
R9 900Ω
R8 900Ω
INTERNAL BIAS
Q23
Q24
R37 900Ω
Q27 Q29
Q21
Q22
INTERNAL BIAS
Q51
Q20 0.95mA
Q50 1.34mA
INTERNAL BIAS 3.5V
R14 1.4k
INTERNAL BIAS 2.4V
R15 500Ω
Q33
Q34
Q57
Q58
Q31
Q32
Q55
Q56
2.2k
2.2k
Q53
Q54
Q52
800Ω
800Ω
1.2mA
1.2mA
1.9mA
Vs+
Q39
Q37
OUT
R17 300Ω
Q38
R11 300Ω
Q40
R12 1.2k
GND
Vs−

ABSOLUTE MAXIMUM RATINGS (Note 2)

Positive Supply Voltage	+6V
Negative Supply Voltage	−18V
Power Dissipation (Note 1)	500mW
Differential Input Voltage	±5V
Latch Enable Input Voltage	−0.5V to V+ Supply
Operating Temperature Range	
CMP-05A/B (J or Z Package) (Note 3)	−55°C to +125°C
CMP-05E/F (J or Z Package)	−25°C to +85°C
CMP-05E/F (P Package)	0°C to +70°C
DICE Junction Temperature (T_j)	−65°C to +150°C
Storage Temperature Range	−65°C to +150°C
P-Suffix	−65°C to +125°C
Lead Temperature (Soldering, 60 sec)	300°C
Output Short Circuit Duration — to ground	Indefinite
— to V+ = 5.0V	1 Minute

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
Epoxy Mini-DIP (P)	36°C	5.6mW/°C
Hermetic Mini-DIP (Z)	75°C	6.7mW/°C

NOTES:
1. See table for maximum ambient temperature rating and derating factor.
2. Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.
3. Latch is functional for $-55°C \le T_A \le +85°C$.

ELECTRICAL CHARACTERISTICS at $V_S+ = 5.0V$, $V_S- = -5.0V$, $T_A = 25°C$ and Latch Enable grounded, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-05A/E MIN	CMP-05A/E TYP	CMP-05A/E MAX	CMP-05B/F MIN	CMP-05B/F TYP	CMP-05B/F MAX	UNITS
Input offset Voltage	V_{OS}	$R_S = 50\Omega$	—	100	250	—	200	600	μV
Input Offset Current	I_{OS}		—	15	80	—	30	150	nA
Input Bias Current	I_B		—	0.6	1.2	—	0.8	1.8	μA
Voltage Gain	A_{VO}	Note 1	8	16	—	7	14	—	V/mV
Input Voltage Range	CMVR	Note 1	±3.0	±3.3	—	±3.0	±3.3	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 3.0V$, Note 1	86	91	—	84	89	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.75V$ to $V_S = \pm 5.25V$	—	51	126	—	64	126	μV/V
		$V_S+ = 5V$, $V_S- = -5V$ to $-15V$	—	15	51	—	18	63	
Output High Voltage	V_{OH}	$V_{IN} \ge 10mV$, $I_O = 0\mu A$	2.4	2.9	—	2.4	2.9	—	V
		$V_{IN} \ge 10mV$, $I_O = 320\mu A$	2.4	2.9	—	—	—	—	
		$V_{IN} \ge 10mV$, $I_O = 200\mu A$	—	—	—	2.4	2.9	—	
Saturation Voltage	V_{SAT}	$V_{IN} \le -10mV$, $I_{SINK} = 0mA$	—	0.13	0.40	—	0.13	0.40	V
		$V_{IN} \le -10mV$, $I_{SINK} = 8mA$	—	—	—	—	0.28	0.40	
		$V_{IN} \le -10mV$, $I_{SINK} = 12.8mA$	—	0.32	0.40	—	—	—	
Positive Supply Current	I_S+	$V_O \le 2.4V$, Note 1	—	7.5	11	—	8.0	12	mA
		$V_O \le 0.4V$	—	10	15	—	11	16	
Negative Supply Current	I_S-	$V_O \le 0.4V$	—	11	16	—	12	18	mA
Power Dissipation	P_d	$V_O \le 0.4V$	—	105	155	—	115	170	mW
Latch Input Voltage									
Logic 1	V_{LH}	Over Operating Temp. Range Latch Enabled, Note 1	2.0	—	—	2.0	—	—	V
Logic 0	V_{LL}	Over Operating Temp. Range Latch Disabled, Note 1	—	—	0.8	—	—	0.8	
Latch Input Current									
Logic 1	I_{LH}	$V_{LH} = 3.0V$, Note 1	—	10	45	—	10	45	μA
Logic 0	I_{LL}	$V_{LL} = 0.8V$, Note 1	—	6	25	—	6	25	
Input to Output High Response Time	t_{pd+}	$V_{OD} = 1.2mV$, Notes 1, 2	—	50	—	—	50	—	ns
		$V_{OD} = 5.0mV$, Notes 1, 2	—	37	55	—	37	60	
Input to Output Low Response Time	t_{pd-}	$V_{OD} = 1.2mV$, Notes 1, 2	—	47	—	—	47	—	ns
		$V_{OD} = 5.0mV$, Notes 1, 2	—	35	55	—	35	60	
Latch Disable Time	t_{LPD}	Notes 1, 3	—	38	55	—	38	60	ns

NOTES:
1. Guaranteed by design.
2. Times are for 100mV step inputs. See switching time waveforms.
3. See switching time waveforms.

ELECTRICAL CHARACTERISTICS at $V_S+ = 5.0V$, $V_S- = -5.0V$, and Latch Enable grounded. For CMP-05A/B, $-55°C \le T_A \le 125°C$. For CMP-05E/F; $-25°C \le T_A \le 85°C$ (J, Z Packages) and $0°C \le T_A \le 70°C$ (P Package), unless otherwise noted.

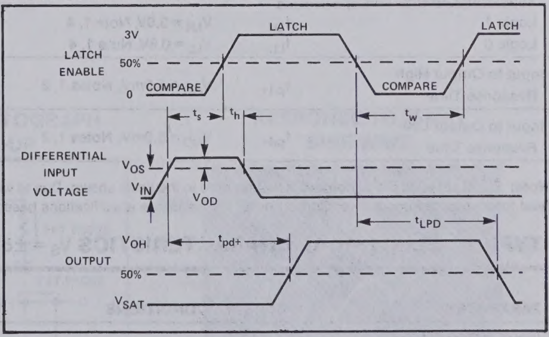
			CMP-05A/E			CMP-05B/F			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input offset Voltage	V_{OS}	$R_S = 50\Omega$	—	0.25	0.80	—	0.40	1.5	mV
Input Offset Voltage Drift	TCV_{OS}		—	1.5	7.5	—	2.5	15	µV/°C
Input Offset Current	I_{OS}		—	40	250	—	70	400	nA
Input Bias Current	I_B		—	1.1	2.5	—	1.5	3.8	µA
Voltage Gain	A_{VO}	Note 1	6	11	—	5	10	—	V/mV
Input Voltage Range	CMVR	Note 1	±2.9	±3.2	—	±2.9	±3.2	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 2.9V$, Note 1	83	90	—	80	88	—	dB
Power Supply Rejection Ratio	PSRR	$\pm 4.75V \le V_S \le \pm 5.25V$	—	63	178	—	80	252	µV/V
Output High Voltage	V_{OH}	$V_{IN} \ge 10mV$, $I_O = 0\mu A$ $V_{IN} \ge 10mV$, $I_O = 240\mu A$ $V_{IN} \ge 10mV$, $I_O = 160\mu A$	2.4 2.4 —	— — —	— — —	2.4 — 2.4	— — —	— — —	V
Saturation Voltage	V_{SAT}	$V_{IN} \le -10mV$, $I_{SINK} = 0mA$ $V_{IN} \le -10mV$, $I_{SINK} = 9.6mA$ $V_{IN} \le -10mV$, $I_{SINK} = 6.4mA$	— — —	0.18 0.2 —	0.40 0.40 —	— — —	0.20 — 0.30	0.40 — 0.40	V
Positive Supply Current	I_S+	$V_O \le 0.4V$	—	11	16	—	12	17	mA
Negative Supply Current	I_S-	$V_O \le 0.4V$	—	12	17	—	13	19	mA
Power Dissipation	P_d	$V_O \le 0.4V$	—	115	165	—	125	180	mW
Latch Input Current									
Logic 1	I_{LH}	$V_{LH} = 3V$, Note 1, 4	—	18	90	—	18	90	µA
Logic 0	I_{LL}	$V_{LL} = 0.8V$, Note 1, 4	—	10	50	—	10	50	
Input to Output High Response Time	t_{pd+}	$V_{OD} = 1.2mV$, Notes 1, 2 $V_{OD} = 5.0mV$, Notes 1, 2	— —	125 92	— —	— —	125 92	— —	ns
Input to Output Low Response Time	t_{pd-}	$V_{OD} = 1.2mV$, Notes 1, 2 $V_{OD} = 5.0mV$, Notes 1, 2	— —	115 88	— —	— —	115 88	— —	ns
Latch Disable Time	t_{LPD}	Notes 1, 2, 4	—	38	—	—	38	—	ns

NOTES:

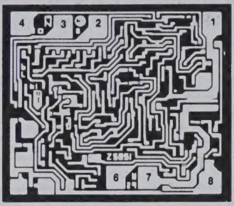
1. Guaranteed by design.
2. Times are for 100mV step inputs. See switching time waveforms.
3. A high on the latch enable input will cause the latch to assume the state of the comparator and not follow subsequent inputs.
4. Latch is functional for $-55°C \le T_A \le +85°C$.

Minimum Input Timing Requirements				
Parameter		Conditions	Minimum Limit	Units
t_S	Setup Time	$V_{IN} = 100mV$	35	ns
t_h	Hold Time	$V_{OD} = 5mV$	10	
t_w	Latch Pulse Width		25	

SWITCHING TIME WAVEFORMS



DICE CHARACTERISTICS



1. **DIGITAL GROUND**
2. **NONINVERTING INPUT**
3. **INVERTING INPUT**
4. **NEGATIVE SUPPLY (SUBSTRATE)**
6. **LATCH ENABLE**
7. **OUTPUT**
8. **POSITIVE SUPPLY**

For additional DICE information refer to Section 2.

DIE SIZE 0.051 × 0.045 inch, 2295 sq. mils
(1.295 × 1.143mm, 1.481 sq. mm)

WAFER TEST LIMITS at $V_S = \pm 5V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-05N LIMIT	CMP-05G LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	250	600	µV MAX
Input Offset Current	I_{OS}		80	150	nA MAX
Input Bias Current	I_B		1.2	1.8	µA MAX
Voltage Gain	A_{VO}	Note 1	8	7	V/mV MIN
Input Voltage Range	CMVR	Note 1	±3.0	±3.0	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 2.9V$ Note 1	83	80	dB MIN
Power Supply Rejection Ratio	PSRR	$\pm 4.75 \leq V_S \leq \pm 5.25$	126	178	µV/V MAX
		$V_S+ = 5V$, $V_S- = -5V$ to $-15V$	51	63	
Positive Output Voltage	V_{OH}	$V_{IN} \geq 10mV$, $I_O = 0\mu A$	2.4	2.4	V MIN
Saturation Voltage	V_{SAT}	$V_{IN} \leq 10mV$, $I_O = 0\mu A$	0.4	0.4	V MAX
Positive Supply Current	I+	$V_O \leq 0.4V$	15	16	mA MAX
Negative Supply Current	I−	$V_O \leq 0.4V$	16	18	mA MAX
Negative Supply Current	I−	$V- = -15V$, $V_O \leq 0.4V$	18	20	mA MAX
Latch Input Voltage					
Logic 1	V_{LH}	Latch Enabled	2.0	2.0	V MIN
Logic 0	V_{LL}	Latch Disabled	0.8	0.8	V MAX
Latch Input Current					
Logic 1	I_{LH}	$V_{LH} = 3.0V$, Note 1, 4	45	45	µA MAX
Logic 0	I_{LL}	$V_{LL} = 0.8V$, Note 1, 4	25	25	
Input to Output High Response Time	t_{pd+}	$V_{OD} = 5.0mV$, Notes 1, 2	55	60	ns MAX
Input to Output Low Response Time	t_{pd-}	$V_{OD} = 5.0mV$, Notes 1, 2	55	60	ns MAX

Note: Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

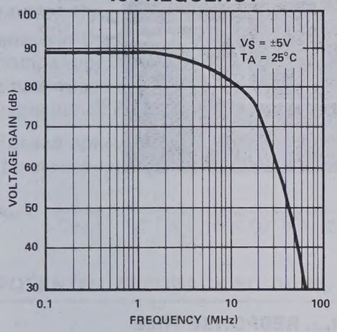
TYPICAL ELECTRICAL CHARACTERISTICS $V_S = \pm 5V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-05N TYPICAL	CMP-05G TYPICAL	UNITS
Input to Output High Response Time	t_{pd+}	$V_{OD} = 1.2mV$, Note 2	50	50	ns
Input to Output Low Response Time	t_{pd-}	$V_{OD} = 1.2mV$, Note 2	47	47	ns
Latch Disable Time	t_{LPD}	Note 3, 4	38	38	ns

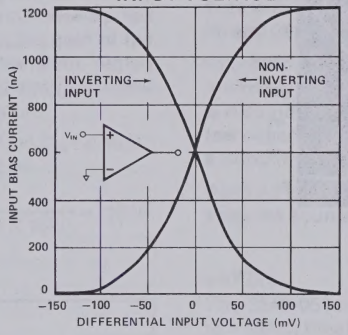
NOTES:
1. Guaranteed by design.
2. Times are for 100mv step inputs.
3. See switching time waveforms.
4. Latch is functional for $-55°C \leq T_A \leq 85°C$.

TYPICAL PERFORMANCE CHARACTERISTICS

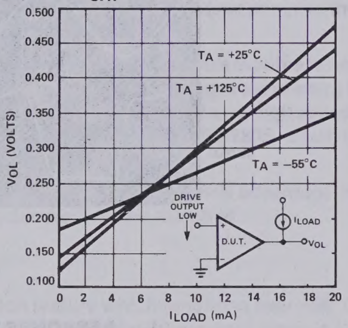
VOLTAGE GAIN vs FREQUENCY



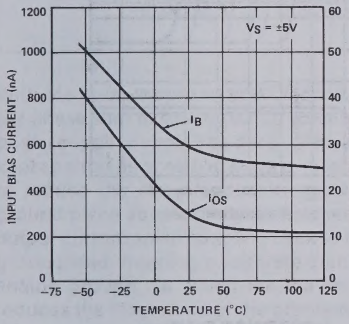
INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE



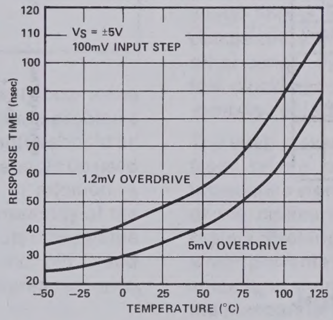
VSAT vs LOAD CURRENT



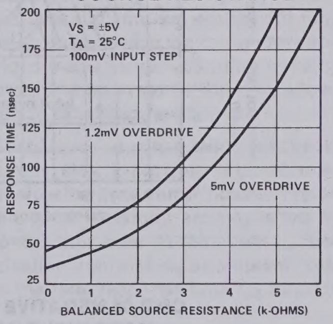
INPUT CURRENTS vs TEMPERATURE



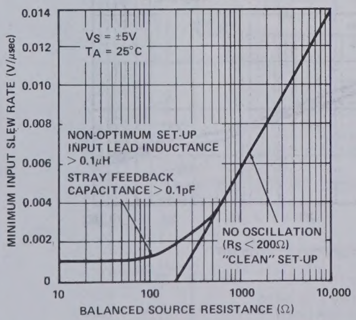
RESPONSE TIME vs TEMPERATURE



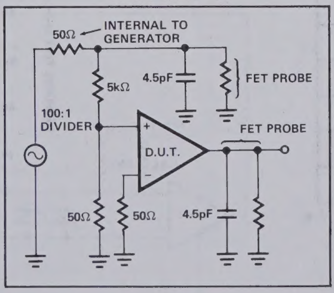
RESPONSE TIME vs BALANCED SOURCE RESISTANCE



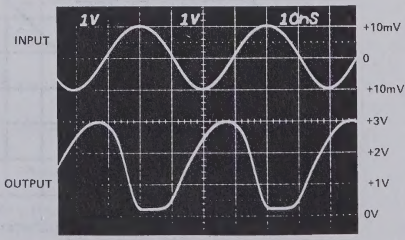
MINIMUM INPUT SIGNAL SLEW RATE vs BALANCED SOURCE RESISTANCE



RESPONSE PHOTOGRAPH TEST SET-UP

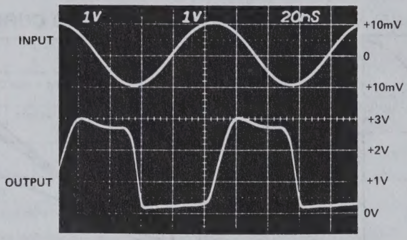

50Ω
INTERNAL TO GENERATOR
5kΩ
4.5pF
FET PROBE
100:1 DIVIDER
+
−
D.U.T.
FET PROBE
50Ω
50Ω
4.5pF

RESPONSE TO 25MHz SINE WAVE

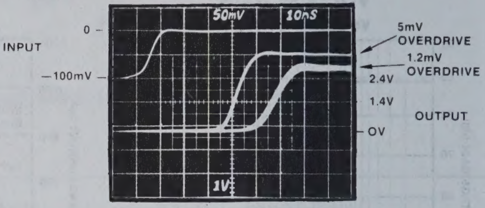


TYPICAL PERFORMANCE CHARACTERISTICS

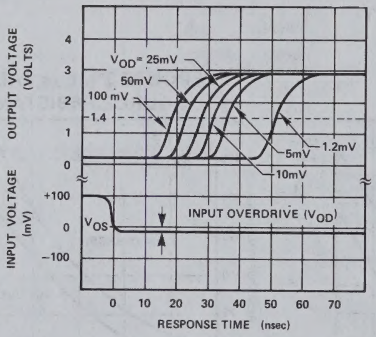
RESPONSE TO 10MHz SINE WAVE



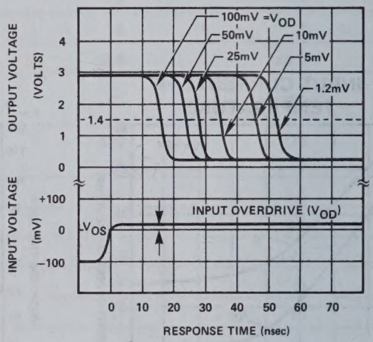
RESPONSE TIME TO 5mV AND 1.2mV (= 1/2 LSB) OVERDRIVES



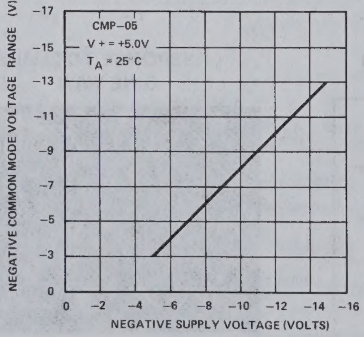
t_{pd+} RESPONSE TIME



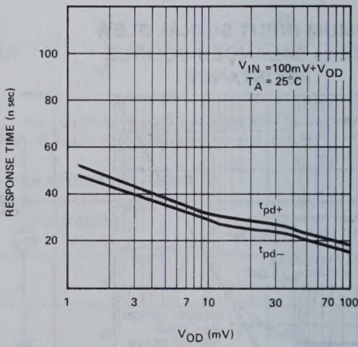
t_{pd-} RESPONSE TIME



CMP-05 NEGATIVE COMMON-MODE INPUT RANGE vs NEGATIVE SUPPLY



RESPONSE TIME vs OVERDRIVE VOLTAGE



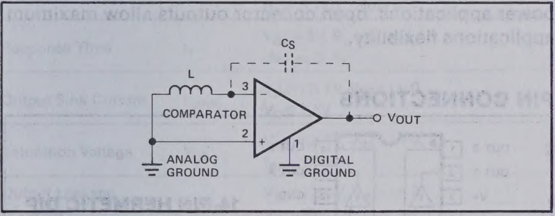
APPLICATION INFORMATION

The CMP-05 is a very accurate device providing fast response time even with small—Microvolt level—overdrives. To achieve this performance requires high gain at high frequencies. As shown in the voltage gain versus frequency curve, the gain—bandwidth product of the CMP-05 is 1.5×10^{11} Hz. It maintains its full gain to approximately 8MHz and rolls off at a very fast rate beyond that frequency due to the fact that five poles occur in the 30 to 60MHz range. At 30MHz the gain of the comparator is still 2000. Therefore, in the transition region small values of source lead inductance and stray feedback capacitance can cause an oscillatory condition.

For example (in the figure below) with $L = 0.1\mu H$, $C_S = 0.15pF$, the closed-loop gain of the circuit at 30MHz is:

$$A_V = \frac{1}{LC_S\omega^2} = \frac{1}{10^{-7} \times 0.15 \times 10^{-12} \times (2\pi \times 30 \times 10^6)^2} = 1880$$

POTENTIAL FEEDBACK SOURCES



With the open-loop gain at 2000 oscillation will occur since the phase shift exceeds 180° C. To minimize these problems power supplies should be decoupled, lead lengths should be kept as short as possible, and a ground plane should be used to reduce the stray feedback capacitance. In addition, a ground plane substantially diminishes the possibility of the output current spike coupling back to the inputs through the ground lead. Keeping a separate digital ground (pin 1) and analog ground (to which the inputs are referenced) also reduces the magnitude of the problem.

Fortunately, in high-speed circuitry the comparator inputs will be driven at a fast rate, in which case no transition region oscillations will occur. As the minimum slew rate versus source resistance curve indicates, if the input is driven at a rate exceeding 6mV/μsec, no oscillations will occur with source resistors of less than 1kΩ. Examples of "clean" transitions can be observed in the photographs of the response time with 5mV and 1.2mV overdrives, and the response to the 10 and 25MHz input signals.

In order to not degrade its speed the CMP-05's inputs are not internally clamped. If large differential voltages are present it is recommended that the inputs be clamped with high speed, low capacitance diodes such as the H.P. 5082-2835, which is a Schottky Diode.

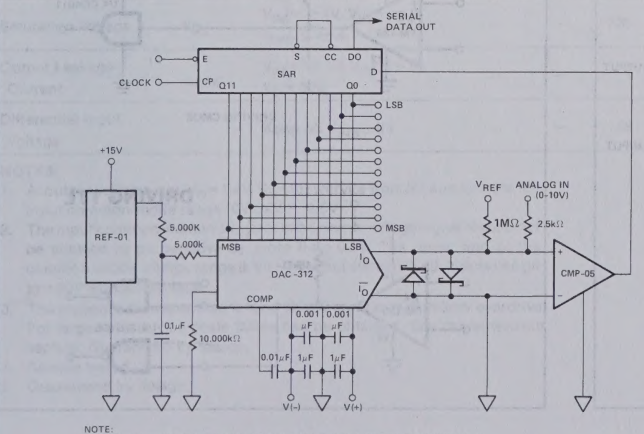
As in all high-speed devices, it is to the user's advantage to keep the source impedances low and matched.

LATCH

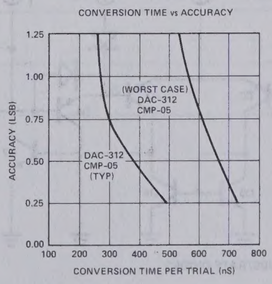
The CMP-05 has a latch feature which functions over −55° C to +85° C. When the latch is enabled, the output stays in its existing logic state regardless of the input signal. The input timing requirements of the latch are presented in the Switching Time Waveforms. The latch opens up a broader applications area at no sacrifice in total system speed. Effectively, the latch allows high speed sampling of comparison decisions. This is important in automatic test equipment limit comparators, in measuring pods used in logic analyzers and other similar synchronous measurement circuitry needing fast clocking frequencies. The latch pulse width t_w allows sampling of input signals to take place in 25nsec.

The latch prevents self oscillation (due to positive feedback) from taking place when slowly-moving high-source-impedance signals pass thru the linear amplification region of the comparator. This is successfully accomplished by rapidly strobing the comparator near its minimum t_w time which prevents self oscillation from making a complete cycle since t_w is shorter than the total response time t_{pd} through the comparator.

12-BIT FAST A/D CONVERTER



NOTE:
DEVICE(S) CONNECTED TO ANALOG INPUT MUST BE CAPABLE OF SOURCING 4.0mA.
A BUFFER (eg. BUF-02) MAY BE REQUIRED.



CONVERSION TIME (nS)	TYP	WORST CASE
SAR	33	55
CMP-05	92	125
TOTAL	375nS	680nS
× 13	4.9μS	8.8μS

PM-139/PM-139A/PM-339A QUAD LOW-POWER VOLTAGE COMPARATORS

FEATURES

- **Single or Dual Supply Operation**
- **Input Voltage Range Includes Ground**
- **Low Power Consumption (2mW/Comparator)**
- **Low Input Bias Current 25nA**
- **Low Input Offset Current .... ±5nA**
- **Low Offset Voltage .... ±2mV**
- **Low Output Saturation Voltage (250mV @ 4mA)**
- **Logic Outputs Compatible with TTL, DTL, ECL, MOS and CMOS**
- **Directly replaces LM139 and LM139A/339A Comparators**

ORDERING INFORMATION†

+25°C V_{OS} (mV)	PACKAGE Is 14-PIN HERMETIC DIP	OPERATING TEMPERATURE RANGE
±2*	PM139AY*	MIL
±5*	PM139Y*	MIL
±2	PM339AY	COM

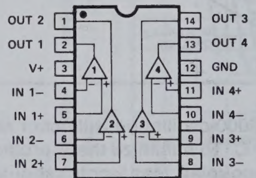
*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

GENERAL DESCRIPTION

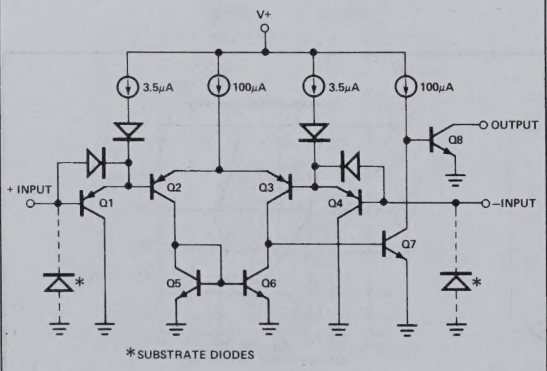
The PM-139 has four independent voltage comparators, each with precision DC specifications. Low offset voltage, bias current, power consumption and output saturation voltage are offered in a design that features single power supply operation. The input voltage range includes ground for convenient single supply operation. The 2mA power supply current, independent of supply voltage — coupled with the single supply operation, makes this comparator ideal for low power applications. open collector outputs allow maximum applications flexibility.

PIN CONNECTIONS


OUT 2
OUT 1
V+
IN 1–
IN 1+
IN 2–
IN 2+
OUT 3
OUT 4
GND
IN 4+
IN 4–
IN 3+
IN 3–
1
2
3
4
5
6
7
8
9
10
11
12
13
14

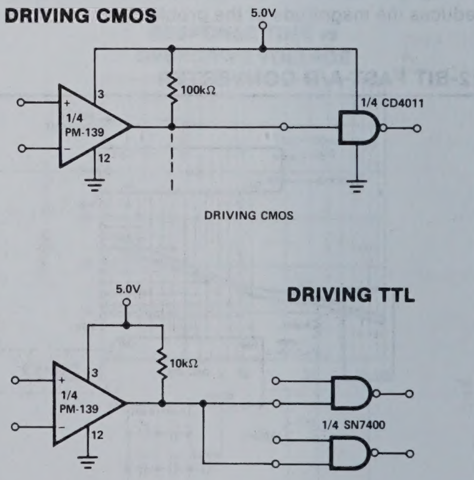
14-PIN HERMETIC DIP (Y-Suffix)

SIMPLIFIED SCHEMATIC (ONE COMPARATOR)


V+
3.5μA
100μA
3.5μA
100μA
OUTPUT
Q8
+ INPUT
Q1
Q2
Q3
Q4
–INPUT
Q7
Q5
Q6
*
*

*SUBSTRATE DIODES

TYPICAL INTERFACE


DRIVING CMOS
5.0V
100kΩ
1/4 CD4011
3
1/4 PM-139
12
+
–
DRIVING CMOS
DRIVING TTL
5.0V
10kΩ
3
1/4 PM-139
12
+
–
1/4 SN7400

ELECTRICAL CHARACTERISTICS at $V+ = +5V$, $T_A = 25°C$, unless otherwise noted.

			PM-139A			PM-339A			PM-139			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset voltage	V_{OS}	(Note 1)	—	1	2	—	1	2	—	2	5	mV
Input Bias Current	I_B	$I_{IN}(+)$ or $I_{IN}(-)$ with Output in Linear Range	—	25	100	—	25	250	—	25	100	nA
Input Offset Current	I_{OS}	$I_{IN}(+)$ or $I_{IN}(-)$	—	3	25	—	5	50	—	3	25	nA
Input Common-Mode Voltage Range	CMVR	(Notes 2, 5)	0	—	$V+ -1.5$	0	—	$V+ -1.5$	0	—	$V+ -1.5$	V
Supply Current	I_S	$R_L = \infty$ on all Comparators $V+ = 30V$	—	0.8	2	—	0.8	2	—	0.8	2	mA
Voltage Gain	A_{VO}	$R_L \geq 15k\Omega$, $V+ = 15V$ (to support large V_O swing) (Note 5)	50	200	—	50	200	—	50	200	—	V/mV
Large-Signal Response Time	t_r	V_{IN} = TTL Logic Swing, $V_{REF} = 1.4V$, $V_{RL} = 5V$, $R_L = 5.1k\Omega$, (Note 4)	—	300	—	—	300	—	—	300	—	ns
Response Time	t_r	$V_{RL} = 5V$, $R_L = 5.1k\Omega$ (Notes 3, 4)	—	1.3	—	—	1.3	—	—	1.3	—	μs
Output Sink Current	I_{SINK}	$V_{IN}(-) \geq 1V$, $V_{IN}(+) = 0$, $V_O \leq 1.5V$	6	16	—	6	16	—	6	16	—	mA
Saturation Voltage	V_{OL}	$V_{IN}(-) \geq 1V$, $V_{IN}(+) = 0$, $I_{SINK} \leq 4mA$	—	250	400	—	250	400	—	250	400	mV
Output Leakage Current	I_{LEAK}	$V_{IN}(+) \geq 1V$, $V_{IN}(-) = 0$, $V_O = 30V$	—	0.1	—	—	0.1	—	—	0.1	—	nA

ELECTRICAL CHARACTERISTICS at $V+ = +5V$, $-55°C \leq T_A \leq +125°C$ for PM-139/139A and $0°C \leq T_A \leq +70°C$ for PM-339A, unless otherwise noted.

			PM-139A			PM-339A			PM-139			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}	(Note 1)	—	—	4	—	—	4	—	—	9	mV
Input Offset Current	I_{OS}	$I_{IN}(+)$ or $I_{IN}(-)$	—	—	100	—	—	150	—	—	100	nA
Input Bias Current	I_B	$I_{IN}(+)$ OR $I_{IN}(-)$ with Output in Linear Range	—	—	300	—	—	400	—	—	300	nA
Input Common-Mode Voltage Range	CMVR	(Notes 3, 5)	0	—	$V+ -2$	0	—	$V+ -2$	0	—	$V+ -2$	V
Saturation Voltage	V_{OL}	$V_{IN}(-) \geq 1V$, $V_{IN}(+) = 0$, $I_{SINK} \leq 4mA$	—	—	700	—	—	700	—	—	700	mV
Output Leakage Current	I_{LEAK}	$V_{IN}(+) \geq 1V$, $V_{IN}(-) = 0$, $V_O = 30V$	—	—	1	—	—	1	—	—	1	μA
Differential Input Voltage		Keep All $V_{IN's} \geq 0V$	—	—	36	—	—	36	—	—	36	V

NOTES:

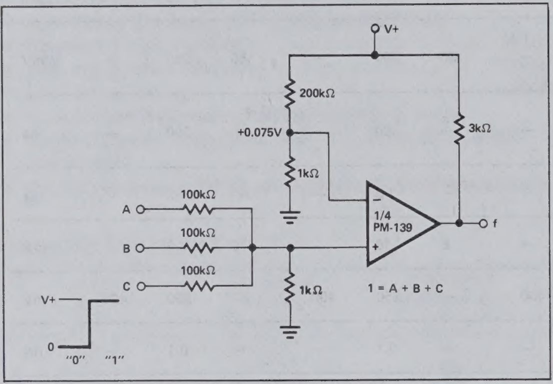
1. At output switch point, $V_O = 1.4V$, $R_S = 0\Omega$ with $V+$ from 5V, and over the full input common-mode range (0V to $V+ -1.5V$).
2. The input common-mode voltage or either input voltage signal should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V+ -1.5V$, but either or both inputs can go to +30V without damage.
3. The response time specified is for a 100mV input step with 5mV overdrive. For larger overdrive signals 300ns can be obtained. See characteristics section. Guaranteed by design.
4. Sample tested.
5. Guaranteed by design.

ABSOLUTE MAXIMUM RATINGS

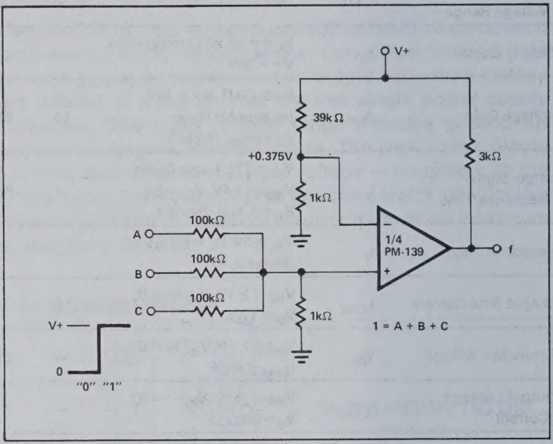
Supply Voltage, V+	36V or ±18V
Differential Input Voltage	36V
Input Voltage	−0.3V to +36V
Power Dissipation Hermetic DIP	500mW
Derate Above 100° C	10mW/° C
Output Short-Circuit to Ground	Continuous
Input Current ($V_{IN} < -0.3V$)	50mA
Operating Temperature Range	
PM-339A	0° C to +70° C
PM-139A/139	−55° C to +125° C
Storage Temperature Range	−65° C to +150° C
Lead Temperature (Soldering, 60 sec)	300° C

TYPICAL APPLICATIONS

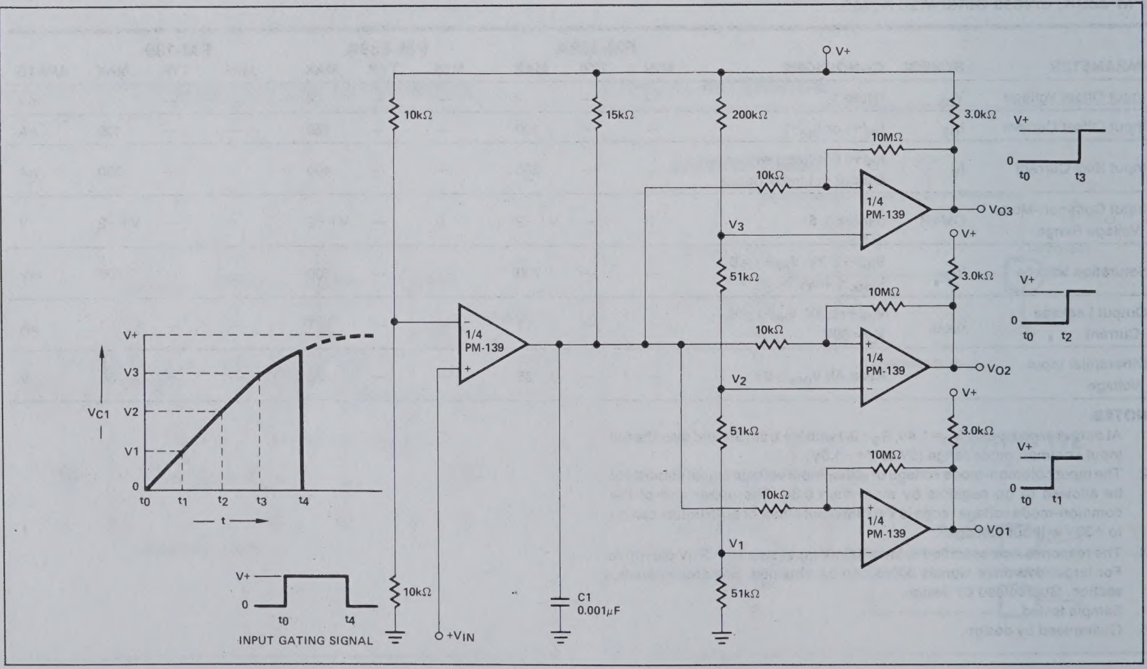
OR GATE


V+
200kΩ
3kΩ
+0.075V
1kΩ
100kΩ
A
100kΩ
B
100kΩ
C
1/4 PM-139
f
1kΩ
1 = A + B + C
V+
0
"0" "1"

AND GATE

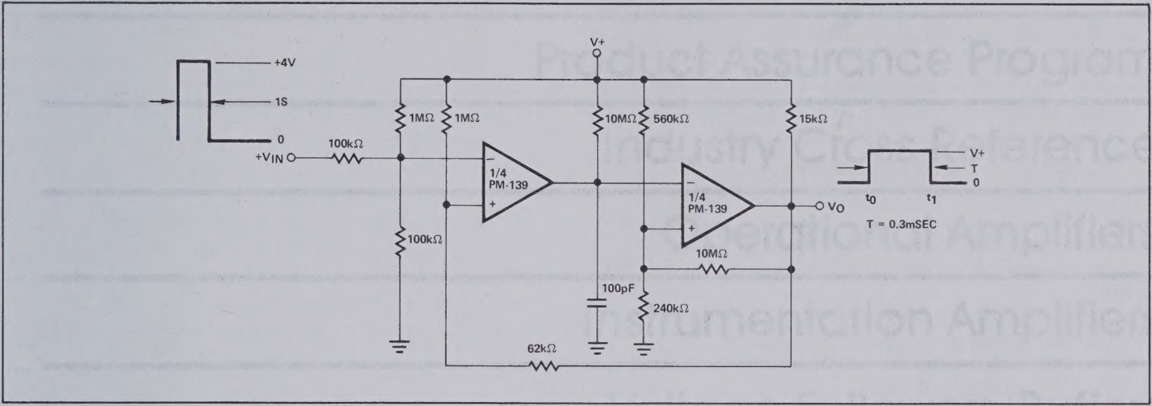

V+
39kΩ
3kΩ
+0.375V
1kΩ
100kΩ
A
100kΩ
B
100kΩ
C
1/4 PM-139
f
1kΩ
1 = A + B + C
V+
0
"0" "1"

TIME DELAY GENERATOR

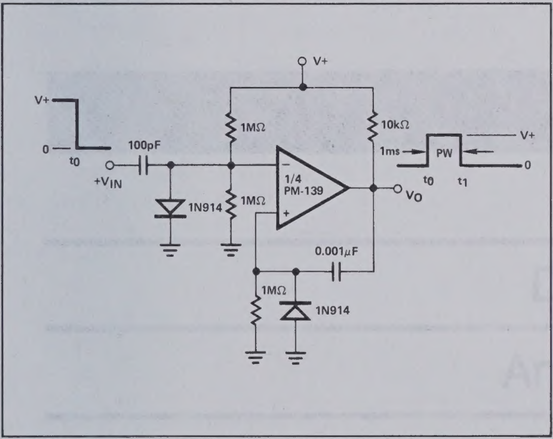

V+
10kΩ
15kΩ
200kΩ
3.0kΩ
10MΩ
10kΩ
1/4 PM-139
V3
VO3
V+
0
t0 t3
51kΩ
3.0kΩ
10MΩ
10kΩ
1/4 PM-139
V2
VO2
V+
0
t0 t2
51kΩ
3.0kΩ
10MΩ
10kΩ
1/4 PM-139
V1
VO1
V+
0
t0 t1
51kΩ
1/4 PM-139
V+
V3
VC1
V2
V1
0
t0 t1 t2 t3 t4
t
V+
0
t0 t4
INPUT GATING SIGNAL
10kΩ
+VIN
C1 0.001µF

TYPICAL APPLICATIONS

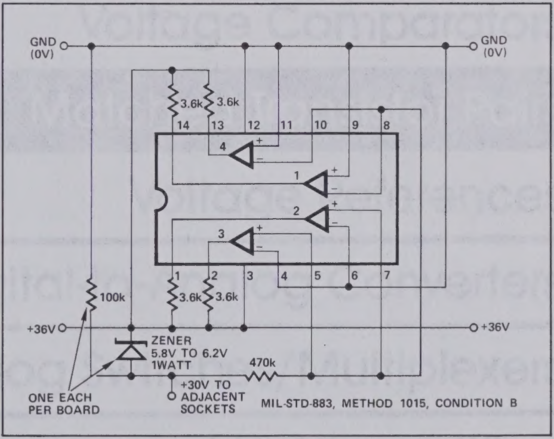
ONE-SHOT MULTIVIBRATOR WITH INPUT LOCK-OUT


+4V
1S
0
+VIN
100kΩ
1MΩ
1MΩ
100kΩ
1/4 PM-139
V+
10MΩ
560kΩ
15kΩ
100pF
1/4 PM-139
10MΩ
240kΩ
62kΩ
VO
V+
T
0
t0
t1
T = 0.3mSEC

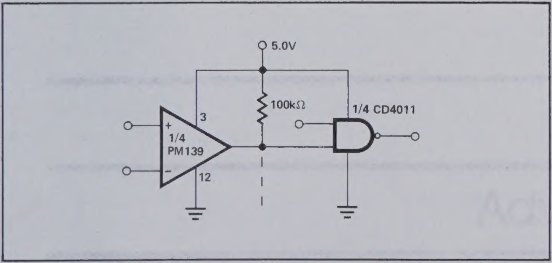
ONE-SHOT MULTIVIBRATOR


V+
0
t0
+VIN
100pF
1N914
1MΩ
1MΩ
V+
1/4 PM-139
10kΩ
VO
0.001μF
1MΩ
1N914
1ms
PW
V+
0
t0
t1

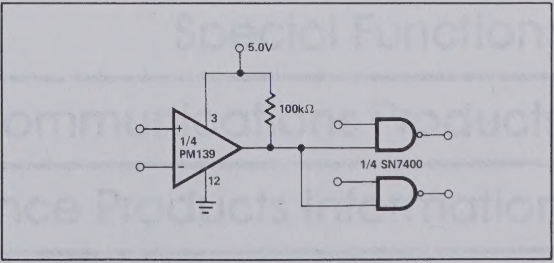
BURN-IN CIRCUIT


GND (0V)
GND (0V)
3.6k
3.6k
14
13
12
11
10
9
8
4
1
2
3
1
2
3
4
5
6
7
100k
3.6k
3.6k
+36V
+36V
ZENER 5.8V TO 6.2V 1WATT
470k
+30V TO ADJACENT SOCKETS
ONE EACH PER BOARD
MIL-STD-883, METHOD 1015, CONDITION B

DRIVING CMOS


5.0V
100kΩ
1/4 CD4011
3
1/4 PM139
12

DRIVING TTL


5.0V
100kΩ
3
1/4 PM139
12
1/4 SN7400

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Matched Monolithic Dual Transistor

MAT-02 .... **16-8**
Matched Monolithic Dual Transistor
Note: See Advance Products Information

MATCHED TRANSISTOR PAIRS

INTRODUCTION

Monolithic dual transistors feature inherently close matching of electrical parameters and very low thermal differentials. In addition, the PMI duals are specifically designed for low offset voltage, low offset voltage drift, low noise, and high gain, all over a wide range of collector current. Monolithic duals optimized for amplifier input use provide the best possible input stage performance. These duals are excellent for use in high-performance audio systems, high-gain instrumentation amplifiers, and precision current mirrors.

These dual transistors were also designed for minimal base-to-emitter resistance which makes log conformity excellent. For an ideal transistor, the base-to-emitter voltage is equal to $(kT/q)\ \ln\ (I_C/I_S)$. An added term, $I_C\ r_{BE}$, causes departure from this idealized logarithmic relationship. The new MAT-02 has very low r_{BE} over a wide range of collector current. Circuits for squaring, RMS-to-DC conversion, and logarithmic amplification can be accurately implemented through use of the low-r_{BE} MAT-02. The MAT-02 preliminary data sheet is shown in the Advanced Products Section.

The well-defined relationship between V_{BE} and collector current can also be used for temperature sensing or for generating bandgap-reference voltages. The low noise, low offsets, and high gain combined with a wide operating range for collector current make these monolithic duals very useful for a diverse range of applications.

DEFINITIONS

Average Offset Current Drift (TCI_{OS}) — The ratio of the change in I_{OS} to the change in temperature producing it.

Average Offset Voltage Drift (TCV_{OS}) — The ratio of the change in V_{OS} to the change in temperature producing it.

Bias Current (I_B) — The average of the base currents at a specified collector voltage and current.

Broadband Noise Voltage (e_{nRMS}) — The root-mean-square noise voltage referred to the input over a specified bandwidth at a specified collector voltage and current.

Current Gain Match (Δh_{FE}) — The difference in h_{FE} between the transistors at a specified voltage and current, expressed as a percentage of the lower of the two h_{FE}'s.

$$\left(1 - \frac{h_{FE1}}{h_{FE2}}\right) \times 100$$

Excess Emitter Resistance (r_{BE}) — The effective resistance between the base and emitter terminals of each transistor.

Noise Voltage (e_{np-p}) — The peak-to-peak noise voltage referred to the input over a specified bandwidth at a specified collector voltage and current.

Noise Voltage Density (e_n) — The rms noise voltage referred to the input in a 1Hz band surrounding a specified frequency, measured at a specified collector voltage and current.

Offset Current (I_{OS}) — The difference between the base currents at a specified collector voltage and current.

Offset Current Change ($\Delta I_{OS}/\Delta V_{CB}$) — The ratio of the change in offset current to the change in collector-base voltage producing it.

Offset Voltage (V_{OS}) — The difference between the base-emitter voltages (V_{BE1}-V_{BE2}) at a specified collector voltage and current.

MATCHED TRANSISTOR PAIRS

Parameter Comparison Table ($I_C = 10\mu A$) for MAT-02

Device	BV_{CEO} Min (V)	V_{OS} Max (mV)	TCV_{OS} Max ($\mu V/^\circ C$)	h_{FE} Min	I_{OS} Max (nA)	TCI_{OS} Max ($pA/^\circ C$)
MAT-02A/E**	40	.05	0.3	400	0.5	90
MAT-02B/F**	40	.15	1	300	1.3	150
LM194	40	.05	0.3	300	0.7	N.C.
LM394	40	.15	1	200	2.0	N.C.
MAT-01AH	45	0.1	0.5	500	0.6	90
MAT-01GH	45	0.5	1.8	250	3.2	150
LM114A	45	0.5	2.0	500	2.0	—
LM114	45	2.0	10	250	10	—
LM115A	60	0.5	2.0	250	2.0	—
LM115	60	2.0	10	250	10	—
AD810*	35	3.0	15	100	2.0	600
AD811*	45	1.5	7.5	200	10	300
AD812*	35	1.0	5.0	400	2.5	300
AD813*	45	0.5	2.5	200	5	300
AD818*	20	1.0	5.0	200	10	300

*Discontinued

**Temperature range for A-grade and B-grade is −55° C to +125° C; temperature range for E-grade and F-grade is −25° C to +85° C.

Parameter Comparison Table ($I_C = 10\mu A$) for MAT-01 to 2N-Types

Device	BV_{CEO} Min (V)	V_{OS} Max (mV)	TCV_{OS} Max ($\mu V/^\circ C$)	h_{FE} Min	$\%h_{FE}$ Match Max	I_{OS} Max (nA)	TCI_{OS} Max ($pA/^\circ C$)
MAT-01GH	45	0.5	1.8	250	8	3.2	150
2N2639	45	5.0	10	50	10	20	1000
2N2640	45	10	20	50	20	40	2000
2N2642	45	5.0	10	100	10	10	500
2N2643	45	10	20	100	20	20	375
2N2915	45	3.0	10	60	10	17	600
2N2915A	45	2.0	5.0	60	15	26	900
2N2916	45	5.0	10	150	10	7	N.C.
2N2916A	45	2.0	5.0	150	15	10	300
2N2917	45	10	20	60	20	17	1450
2N2918	45	5.0	20	150	20	7	750
2N2919	60	3.0	10	60	10	17	600
2N2919A	60	1.5	5.0	60	10	17	600
2N2920	60	3.0	10	150	10	7	N.C.
2N2920A	60	1.5	5.0	150	10	7	300
2N2060	60	5.0	10	25	10	40	N.C.
2N2060A	60	3.0	5.0	25	10	40	N.C.
2N2060B	60	1.5	5.0	25	10	40	N.C.

Notes: 1. TCI_{OS} Max and I_{OS} Max calculated from published data.
2. N.C. = Insufficient published data to calculate.
3. All of above are physically interchangeable pin-for-pin with MAT-01 and MAT-02 series.

MATCHED MONOLITHIC DUAL TRANSISTOR

MAT-01

FEATURES

- **Low V_{OS} (V_{BE} Match) .... 40μV Typ**
  100μV Max
- **Low TCV_{OS} .... 0.5μV/° C Max**
- **High h_{FE} .... 500 Min**
- **Excellent h_{FE} Linearity from 10nA to 10mA**
- **Low Noise Voltage .... $0.23\mu V_{p\text{-}p}$ — 0.1Hz to 10Hz**
- **High Breakdown .... 45V Min**

GENERAL DESCRIPTION

The MAT-01 is a monolithic dual NPN transistor. An exclusive Silicon Nitride "Triple-Passivation" process provides excellent stability of critical parameters over both temperature and time. Matching characteristics include offset voltage of 40μV, temperature drift of 0.15μV/° C, and h_{FE} matching of 0.7%. Very high h_{FE} is provided over a six decade range of collector current, including an exceptional h_{FE} of 590 at a collector current of only 10nA. The high gain at low collector current makes the MAT-01 ideal for use in low-power, low-level input stages.

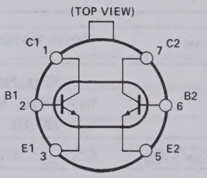
ORDERING INFORMATION†

$T_A = 25°C$ V_{OS} MAX (mV)	PACKAGE	OPERATING TEMPERATURE RANGE
0.1	MAT01AH*	MIL
0.5	MAT01GH*	MIL

*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

PIN CONNECTIONS



TO-78
(H-Suffix)

NOTE: Substrate is connected to case

ABSOLUTE MAXIMUM RATINGS (Note 4)

Collector-Base Voltage (BV_{CBO})	
MAT-01AH, GH, N	45V
Collector-Emitter Voltage (BV_{CEO})	
MAT-01AH, GH, N	45V
Collector-Collector Voltage (BV_{CC})	
MAT-01AH, GH, N	45V
Emitter-Emitter Voltage (BV_{EE})	
MAT-01AH, GH, N	45V
Emitter-Base Voltage (BV_{EBO}) (Note 1)	5V
Collector Current (I_C)	25mA
Emitter Current (I_E)	25mA
Total Power Dissipation	
Case Temperature ≤ 40° C (Note 2)	1.8W
Ambient Temperature ≤ 70° C (Note 3)	500mW
Operating Ambient Temperature	−55° C to +125° C
Operating Junction Temperature	−55° C to +150° C
Storage Temperature	−65° C to +150° C
Lead Temperature (Soldering, 60 sec)	300° C
DICE Junction Temperature	−65° C to +150° C

NOTES:

1. Application of reverse bias voltages in excess of rating shown can result in degradation of h_{FE} and h_{FE} matching characteristics. Do not attempt to measure BV_{EBO} greater than the 5V rating shown.
2. Rating applies to applications using heat sinking to control case temperature. Derate linearly at 16.4mW/° C for case temperatures above 40° C.
3. Rating applies to applications not using heat sinking; device in free air only. Derate linearly at 6.3mW/° C for ambient temperatures above 70° C.
4. Absolute maximum ratings apply to both DICE and packaged devices.

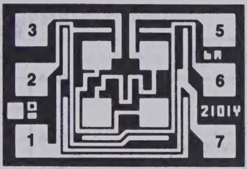
ELECTRICAL CHARACTERISTICS at $V_{CB} = 15V$, $I_C = 10\mu A$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-01AH MIN	MAT-01AH TYP	MAT-01AH MAX	MAT-01GH MIN	MAT-01GH TYP	MAT-01GH MAX	UNITS
Breakdown Voltage	BV_{CEO}	$I_C = 100\mu A$	45	—	—	45	—	—	V
Offset Voltage	V_{OS}		—	0.04	0.1	—	0.10	0.5	mV
Offset Voltage Stability									
First Month	V_{OS}/Time	(Note 1)	—	2.0	—	—	2.0	—	μV/Mo
Long-Term		(Note 2)	—	0.2	—	—	0.2	—	
Offset Current	I_{OS}		—	0.1	0.6	—	0.2	3.2	nA
Bias Current	I_B		—	13	20	—	18	40	nA
Current Gain	h_{FE}	$I_C = 10nA$	—	590	—	—	430	—	
		$I_C = 10\mu A$	500	770	—	250	560	—	
		$I_C = 10mA$	—	840	—	—	610	—	
Current Gain Match	Δh_{FE}	$I_C = 10\mu A$	—	0.7	3.0	—	1.0	8.0	%
		$100nA \leq I_C \leq 10mA$	—	0.8	—	—	1.2	—	
Low Frequency Noise Voltage	$e_{np\text{-}p}$	0.1Hz to 10Hz (Note 3)	—	0.23	0.4	—	0.23	0.4	$\mu V_{p\text{-}p}$
Broadband Noise Voltage	e_{nRMS}	1Hz to 10kHz	—	0.60	—	—	0.60	—	μV_{RMS}
Noise Voltage Density	e_n	$f_O = 10Hz$ (Note 3)	—	7.0	9.0	—	7.0	9.0	$nV/\sqrt{Hz}$
		$f_O = 100Hz$ (Note 3)	—	6.1	7.6	—	6.1	7.6	
		$f_O = 1000Hz$ (Note 3)	—	6.0	7.5	—	6.0	7.5	
Offset Voltage Change	$\Delta V_{OS}/\Delta V_{CB}$	$0 \leq V_{CB} \leq 30V$	—	0.5	3.0	—	0.8	8.0	μV/V
Offset Current Change	$\Delta I_{OS}/\Delta V_{CB}$	$0 \leq V_{CB} \leq 30V$	—	2	15	—	3	70	pA/V
Collector-Base Leakage Current	I_{CBO}	$V_{CB} = 30V$, $I_E = 0$ (Notes 3, 4)	—	15	50	—	25	200	pA
Collector-Emitter Leakage Current	I_{CES}	$V_{CE} = 30V$, $V_{BE} = 0$ (Notes 3, 4)	—	50	200	—	90	400	pA
Collector-Collector Leakage Current	I_{CC}	$V_{CC} = 30V$, (Note 3)	—	20	200	—	30	400	pA
Collector Saturation Voltage	$V_{CE(SAT)}$	$I_B = 0.1mA$, $I_C = 1mA$	—	0.12	0.20	—	0.12	0.25	V
		$I_B = 1mA$, $I_C = 10mA$	—	0.8	—	—	0.8	—	
Gain-Bandwidth Product	f_T	$V_{CE} = 10V$, $I_C = 10mA$	—	450	—	—	450	—	MHz
Output Capacitance	C_{ob}	$V_{CE} = 15V$, $I_E = 0$	—	2.8	—	—	2.8	—	pF
Collector-Collector Capacitance	C_{CC}	$V_{CC} = 0$	—	8.5	—	—	8.5	—	pF

ELECTRICAL CHARACTERISTICS at $V_{CB} = 15V$, $I_C = 10\mu A$, $-55°C \leq T_A \leq +125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-01AH MIN	MAT-01AH TYP	MAT-01AH MAX	MAT-01GH MIN	MAT-01GH TYP	MAT-01GH MAX	UNITS
Offset Voltage	V_{OS}		—	0.06	0.15	—	0.14	0.70	mV
Average Offset Voltage Drift	TCV_{OS}	(Note 5)	—	0.15	0.50	—	0.35	1.8	μV/° C
Offset current	I_{OS}		—	0.9	8.0	—	1.5	15.0	nA
Average Offset Current Drift	TCI_{OS}	(Note 5)	—	10	90	—	15	150	pA/° C
Bias Current	I_B		—	28	60	—	36	130	nA
Current Gain	h_{FE}		167	400	—	77	300	—	
Collector-Base Leakage Current	I_{CBO}	$T_A = 125°C$, $V_{CB} = 30V$, $I_E = 0$ (Notes 3, 4)	—	15	80	—	25	200	nA
Collector-Emitter Leakage Current	I_{CES}	$T_A = 125°C$, $V_{CE} = 30V$, $V_{BE} = 0$ (Notes 3, 4)	—	50	300	—	90	400	nA
Collector-Collector Leakage Current	I_{CC}	$T_A = 125°C$, $V_{CC} = 30V$ (Note 3)	—	30	200	—	50	400	nA

DICE CHARACTERISTICS



1. COLLECTOR (1)
2. BASE (1)
3. EMITTER (1)
5. EMITTER (2)
6. BASE (2)
7. COLLECTOR (2)

DIE SIZE 0.035 × 0.025 inch, 875 sq. mils
(0.89 × 0.64 mm, 0.58 sq. mm)

For additional DICE information refer to Section 2.

WAFER TEST LIMITS at $V_{CB} = 15V$ and $I_C = 10\mu A$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-01N LIMITS	UNITS
Breakdown Voltage	BV_{CEO}	$I_C = 100\mu A$	45	V MIN
Offset Voltage	V_{OS}		0.5	mV MAX
Offset Current	I_{OS}		3.2	nA MAX
Bias Current	I_B		40	nA MAX
Current Gain	h_{FE}		250	MIN
Current Gain Match	Δh_{FE}		8.0	% MAX
Offset Voltage Change	$\Delta V_{OS}/\Delta V_{CB}$	$0 \leq V_{CB} \leq 30V$	8.0	µV/V MAX
Offset Current Change	$\Delta I_{OS}/\Delta V_{CB}$	$0 \leq V_{CB} \leq 30V$	70	pA/V MAX
Collector Saturation Voltage	$V_{CE(SAT)}$	$I_B = 0.1mA$, $I_C = 1mA$	0.25	V MAX

Note: Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_{CB} = 15V$ and $I_C = 10\mu A$, $T_A = 25°C$, unless otherwise noted.

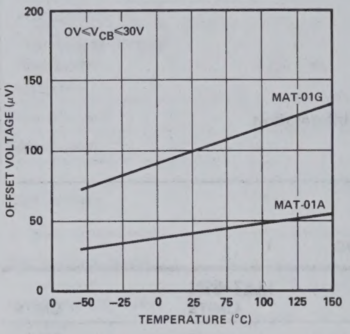
PARAMETER	SYMBOL	CONDITIONS	MAT-01N TYPICAL	UNITS
Average Offset Voltage Drift	TCV_{OS}		0.35	µV/°C
Average Offset Current Drift	TCI_{OS}		15	pA/°C
Collector-Emitter-Leakage Current	I_{CES}	$V_{CE} = 30V$, $V_{BE} = 0$	90	pA
Collector-Base-Leakage Current	I_{CBO}	$V_{CB} = 30V$, $I_E = 0$	25	pA
Gain Bandwidth Product	f_T	$V_{CE} = 10V$, $I_C = 10mA$	450	MHz
Offset Voltage Stability	$\Delta V_{OS}/T$	First Month (Note 1) Long-Term (Note 2)	2.0 0.2	µV/Mo

NOTES:

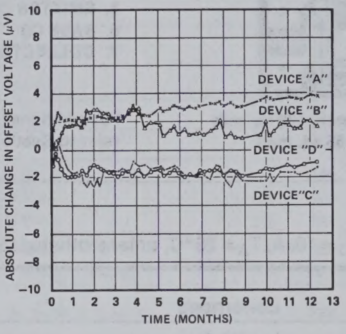
1. Exclude first hour of operation to allow for stabilization.
2. Parameter describes long-term average drift after first month of operation.
3. Sample tested.
4. The collector-base (I_{CBO}) and collector-emitter (I_{CEO}) leakage currents may be reduced by a factor of two to ten times by connecting the substrate (package) to a potential which is lower than either collector voltage.
5. Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

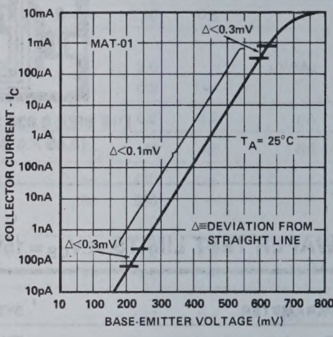
OFFSET VOLTAGE vs TEMPERATURE



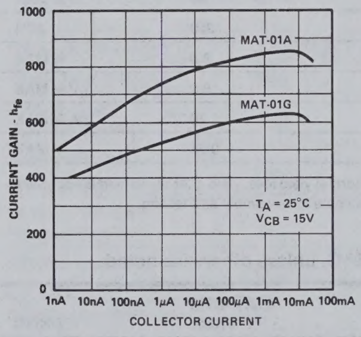
OFFSET VOLTAGE vs TIME



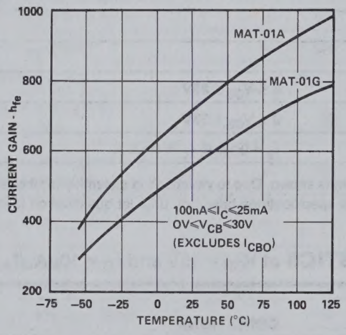
BASE-EMITTER VOLTAGE vs COLLECTOR CURRENT



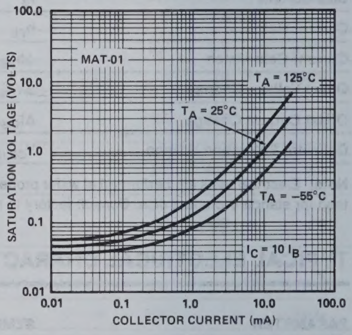
CURRENT GAIN vs COLLECTOR CURRENT



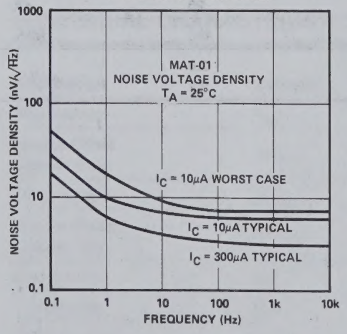
CURRENT GAIN vs TEMPERATURE



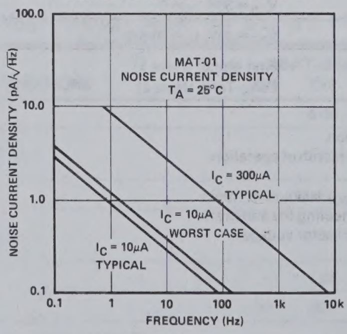
SATURATION VOLTAGE vs COLLECTOR CURRENT



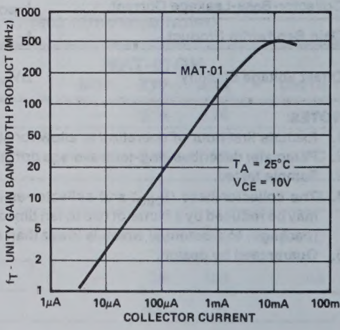
NOISE VOLTAGE



NOISE CURRENT DENSITY

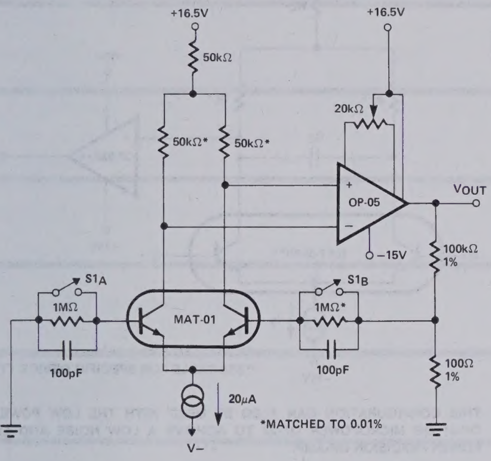


GAIN-BANDWIDTH vs COLLECTOR CURRENT



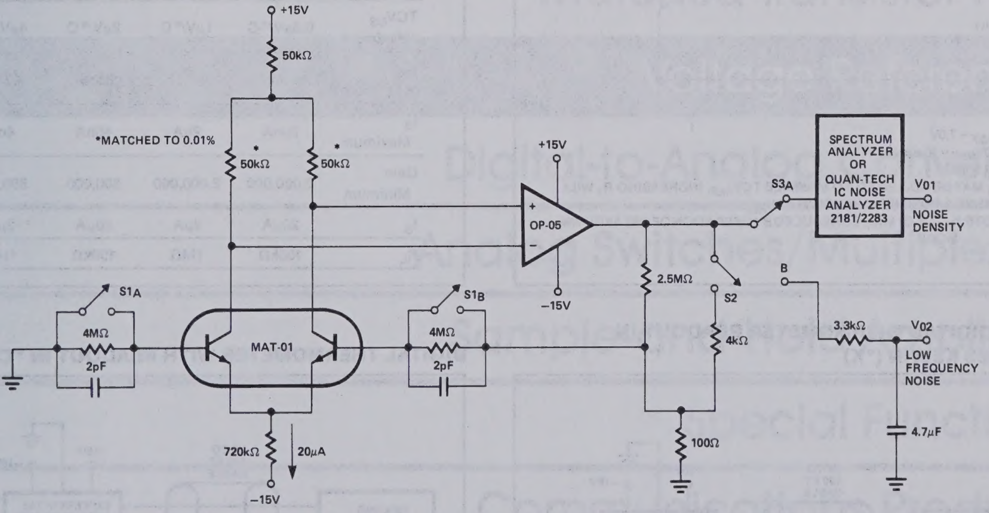
MAT-01 TEST CIRCUITS

MAT-01 MATCHING MEASUREMENT CIRCUIT


+16.5V
50kΩ
+16.5V
20kΩ
50kΩ*
50kΩ*
+
OP-05
−
VOUT
−15V
100kΩ
1%
S1A
1MΩ
MAT-01
S1B
1MΩ*
100pF
100pF
100Ω
1%
20μA
*MATCHED TO 0.01%
V−

TEST	SI_A	SI_B	UNITS	
V_{OS}	X	X	V_{OUT_1}	1 volt per mV
I_{OS}	O	O	$V_{OUT_2} - V_{OUT_1}$	1 volt per nA

MAT-01 NOISE MEASUREMENT CIRCUIT


+15V
50kΩ
*MATCHED TO 0.01%
50kΩ
50kΩ
+15V
+
OP-05
−
−15V
SPECTRUM ANALYZER OR QUAN-TECH IC NOISE ANALYZER 2181/2283
S3A
V01
NOISE DENSITY
B
2.5MΩ
S2
4kΩ
3.3kΩ
V02
LOW FREQUENCY NOISE
S1A
4MΩ
2pF
MAT-01
S1B
4MΩ
2pF
100Ω
4.7μF
720kΩ
20μA
−15V

TEST	SI_A	SI_B	S_2	S_3	READING
Noise Voltage Density (Per Transistor)	X	X	X	A	$V_{01}/\sqrt{2}$
Noise Current Density (Per Transistor)	O	O	X	A	$V_{01}/(\sqrt{2} \times 4M\Omega)$
Low Frequency Noise (Referred to Input)	X	X	O	B	V_{02} PEAK-TO-PEAK 25,000

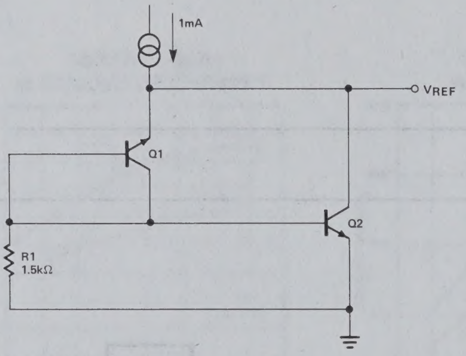
APPLICATION NOTES

Application of reverse bias voltages to the emitter-base junctions in excess of ratings (5V) may result in degradation of h_{FE} and h_{FE} matching characteristics. Circuit designs should be checked to ensure that reverse bias voltages above 5V cannot be applied during such transient conditions as at circuit turn-on and turn-off.

Stray thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can prevent realization of the predicted drift performance. Both input terminals should be maintained at the same temperature, preferably close to the temperature of the device's package.

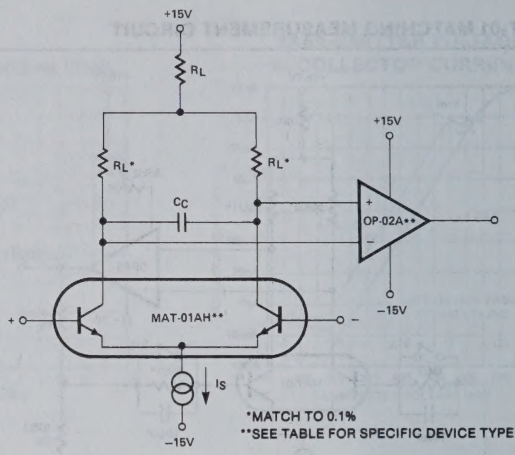
TYPICAL APPLICATIONS

PRECISION REFERENCE


1mA
VREF
Q1
Q2
R1
1.5kΩ

$V_{REF} \approx 7.0V$
$TCV_{REF} \approx 10ppm/°C$
$R_O \approx 40\Omega$
R_1 MAY BE ADJUSTED TO MINIMIZE TCV_{REF}. INCREASING R_1 WILL CAUSE A POSITIVE CHANGE IN TCV_{REF}.
NOTE: h_{FE} OF Q1 WILL BE REDUCED BY OPERATION OF BREAKDOWN MODE.

PRECISION OPERATIONAL AMPLIFIERS

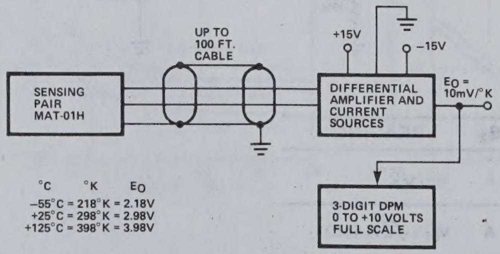

+15V
RL
RL*
RL*
CC
+15V
+
OP-02A**
−
−15V
+
MAT-01AH**
−
IS
−15V

*MATCH TO 0.1%
**SEE TABLE FOR SPECIFIC DEVICE TYPE

THIS CONFIGURATION CAN ALSO BE USED WITH THE LOW POWER OP-21 OR MICROPOWER OP-22 TO ACHIEVE A LOW NOISE AND LOW POWER PRECISION OP-AMP.

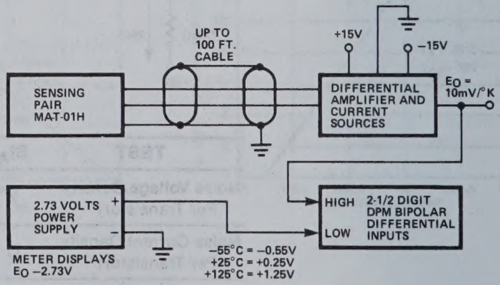
	MAT-01AH OP-02A	MAT-01AH OP-02A	MAT-01GH OP-02	MAT-01GH OP-02
V_{OS} Maximum	0.15mV	0.27mV	0.65mV	1.2mV
TCV_{OS} Maximum	0.6μV/°C	1μV/°C	2μV/°C	4μV/°C
I_{OS} Maximum	0.8nA	0.1nA	3.2nA	0.32nA
I_B Maximum	20nA	2nA	40nA	4nA
Gain Minimum	2,000,000	2,000,000	800,000	800,000
I_S	20μA	2μA	20μA	2μA
R_L	100kΩ	1MΩ	100kΩ	1MΩ

BASIC DIGITAL THERMOMETER READOUT IN DEGREES KELVIN (°K)


SENSING PAIR MAT-01H
UP TO 100 FT. CABLE
+15V
−15V
DIFFERENTIAL AMPLIFIER AND CURRENT SOURCES
EO = 10mV/°K
3-DIGIT DPM 0 TO +10 VOLTS FULL SCALE

°C	°K	EO
−55°C =	218°K =	2.18V
+25°C =	298°K =	2.98V
+125°C =	398°K =	3.98V

DIGITAL THERMOMETER WITH READOUT IN °C


SENSING PAIR MAT-01H
UP TO 100 FT. CABLE
+15V
−15V
DIFFERENTIAL AMPLIFIER AND CURRENT SOURCES
EO = 10mV/°K
2.73 VOLTS POWER SUPPLY
+
−
HIGH
LOW
2-1/2 DIGIT DPM BIPOLAR DIFFERENTIAL INPUTS

METER DISPLAYS EO −2.73V

−55°C = −0.55V
+25°C = +0.25V
+125°C = +1.25V

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Instrumentation Amplifiers 6
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Matched Transistor Pairs 9
Voltage References 10
Digital-to-Analog Converters 11
Analog Switches/Multiplexers 12
Sample-and-Hold Amplifiers 13
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Communications Products 15
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Sales Offices, Representatives and Distributors 18

VOLTAGE REFERENCES

Introduction **10-3**

Definitions **10-3**

REF-01 .... **10-4**
+10V Precision Voltage Reference

REF-02 .... **10-11**
+5V Precision Voltage Reference/
Temperature Transducer

REF-05 .... **10-20**
+5V Precision Voltage Reference

REF-10 .... **10-26**
+10V Precision Voltage Reference

INTRODUCTION

Voltage references provide a constant output voltage irrespective of changes in input voltage, output current, or temperature. References are needed in such diverse equipment as power supplies, panel meters, calibration standards, precision current sources, data conversion systems, and control set-point circuits.

Line regulation, load regulation (output impedance), and temperature coefficient specifications indicate how close a reference will be to an ideal voltage source. Line regulation specifies reference-output-voltage vs. input-voltage changes. Output voltage changes due to load current variations are reflected by load regulation specifications. Temperature coefficient specifications indicate output voltage variation over temperature.

PMI references use the bandgap principle which sums voltages with negative and positive temperature coefficients to yield a stable output voltage over temperature. A transistor base-emitter-junction voltage (V_{BE}) exhibits a negative temperature coefficient. Two transistors operating with unequal current densities will have different V_{BE}s and the difference, ΔV_{BE}, exhibits a positive temperature coefficient. When ΔV_{BE} is amplified and added to V_{BE}, a near-zero temperature coefficient results if the sum equals 1.23V. The 1.23V level is then amplified to provide stable output voltages of +5.00V or +10.00V. The bandgap technique has the advantages of low power consumption, low noise, and excellent long-term stability.

PMI's zener-zapping technique allows for trimming of the ΔV_{BE} amplification factor to ensure low output voltage temperature coefficients. Additional zapping trims the output's absolute value to within specified limits.

The REF-01 and REF-02 are stable +10.00V and +5.00V monolithic bandgap voltage references. Output voltages are adjustable with small effect on output-voltage temperature coefficients. The REF-02 provides an additional output voltage that has a linear temperature dependence.

The REF-05 and REF-10 are premium versions of the REF-01 and REF-02 that have guaranteed long-term stability and MIL-STD-883 processing. Extensive testing over a long period of time, combined with tight control of processing, has enabled PMI to specify limits on output change with time.

DEFINITIONS

Line Regulation — The ratio of the change in output voltage to the change in input (line) voltage producing it. It includes the effects of self-heating.

Load Regulation — The ratio of the change in output voltage to the change in load current. It includes the effects of self-heating.

Output Change With Temperature (ΔV_{OT}) — The absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of the typical output voltage.

$$\Delta V_{OT} = \left| \frac{V_{MAX} - V_{MIN}}{V_O\ (\text{Typical})} \right| \times 100$$

Output Temperature Coefficient (TCV_O) — The ratio of output change with temperature variation to the specified temperature range expressed in ppm/°C. For example, TCV_O is defined as ΔV_{OT} divided by the temperature range; i.e.,

$$TCV_O(0^\circ C \text{ to } +70^\circ C) = \frac{\Delta V_{OT}(0^\circ C \text{ to } +70^\circ C)}{70^\circ C}$$

$$\text{and } TCV_O(-55^\circ C \text{ to } +125^\circ C) = \frac{\Delta V_{OT}(-55^\circ C \text{ to } +125^\circ C)}{180^\circ C}$$

Output Turn-On Settling Time (t_{ON}) — The time required for the output voltage to reach its final value within a specified error band after application of V_{IN}.

Output Voltage Noise ($e_{np\text{-}p}$) — The peak-to-peak output noise voltage within a specified frequency band.

Quiescent Supply Current (I_{SY}) — The current required from the supply to operate the device with no load.

REF-01

+10V PRECISION VOLTAGE REFERENCE

FEATURES

- **10 Volt Output** .... ±0.3%
- **Adjustment Range** .... ±3%
- **Excellent Temperature Stability** .... 3ppm/°C
- **Low Noise** .... $20\mu V_{p\text{-}p}$
- **Low Supply Current** .... 1.4mA Max
- **Wide Input Voltage Range** .... 13V to 33V
- **High Load-Driving Capability** 20mA
- **No External Components**
- **Short-Circuit Proof**
- **MIL-STD-883 Screening Available**

ORDERING INFORMATION†

$T_A = 25°C$ ΔV_O MAX (mV)	PACKAGE TO-99 8-PIN	PACKAGE HERMETIC DIP 8-PIN	PACKAGE PLASTIC DIP 8-PIN	OPERATING TEMPERATURE RANGE
± 30	REF01AJ*	REF01AZ*		MIL
± 30	REF01EJ	REF01EZ		COM
± 50	REF01J*	REF01Z*		MIL
± 50	REF01HJ	REF01HZ	REF01HP	COM
±100	REF01CJ	REF01CZ	REF01CP	COM

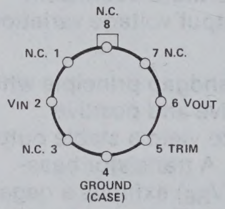
*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

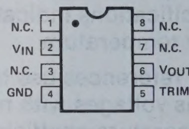
GENERAL DESCRIPTION

The REF-01 precision voltage reference provides a stable +10V output which can be adjusted over at ±3% range with minimal effect on temperature stability. Single-supply operation over an input voltage range of 12V to 40V, low current drain of 1mA, and excellent temperature stability are achieved with an improved bandgap design. Low cost, low noise, and low power make the REF-01 an excellent choice whenever a stable voltage reference is required. Applications include D/A and A/D converters, portable instrumentation, and digital voltmeters. Full military temperature range devices with screening to MIL-STD-883 are available. For guaranteed long-term drift see the REF-10 data sheet.

PIN CONNECTIONS


N.C. 8
N.C. 1
7 N.C.
VIN 2
6 VOUT
N.C. 3
5 TRIM
4
GROUND (CASE)

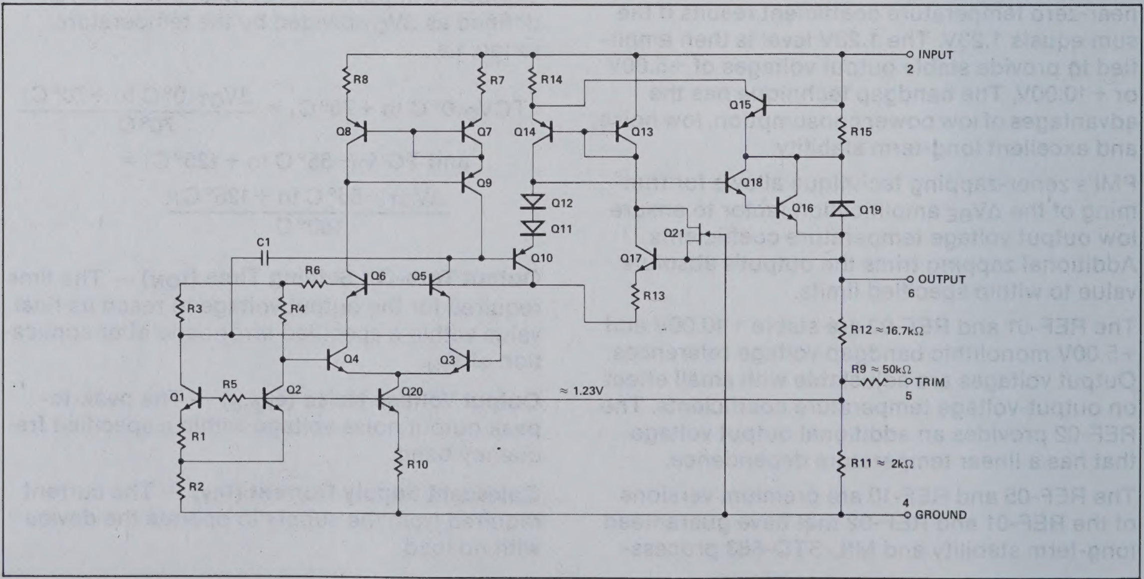
TO-99
(J-Suffix)


N.C. 1
VIN 2
N.C. 3
GND 4
8 N.C.
7 N.C.
6 VOUT
5 TRIM

EPOXY MINI-DIP
(P-Suffix)

8-PIN HERMETIC DIP
(Z-Suffix)

SIMPLIFIED SCHEMATIC


INPUT 2
R8
R7
R14
Q15
R15
Q8
Q7
Q14
Q13
Q9
Q18
Q12
Q16
Q19
Q11
C1
Q21
Q10
Q17
R6
Q6
Q5
OUTPUT 6
R13
R3
R4
R12 ≈ 16.7kΩ
Q4
Q3
R9 ≈ 50kΩ
TRIM 5
R5
Q2
Q20
≈ 1.23V
Q1
R1
R10
R11 ≈ 2kΩ
R2
4 GROUND

ABSOLUTE MAXIMUM RATINGS (Note 2)

Input Voltage
REF-01, A, E, H, All DICE 40V
REF-01C 30V
Power Dissipation (Note 1) 500mW
Output Short-Circuit Duration
(to Ground or V_{IN}) .... Indefinite
Storage Temperature Range
J and Z Packages .... −65° C to +150° C
P Package .... −65° C to +125° C
Operating Temperature Range
REF-01A, REF-01 .... −55° C to +125° C
REF-01E, REF-01H
REF-01C .... 0° C to +70° C
DICE Junction Temperature (T_j) .... −65° C to +150° C
Lead Temperature (Soldering, 60 sec.) .... 300° C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80° C	7.1mW/° C
8-Pin Hermetic DIP (Z)	75° C	6.7mW/° C
8-Pin Plastic DIP (P)	36° C	5.6mW/° C

2. Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_{IN} = +15V$, $T_A = 25°C$, unless otherwise noted.

			REF-01A/E			REF-01/H			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Output Voltage	V_O	$I_L = 0$	9.97	10.00	10.03	9.95	10.00	10.05	V
Output Adjustment Range	ΔV_{trim}	$R_p = 10k\Omega$	±3.0	±3.3	—	±3.0	±3.3	—	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 6)	—	20	30	—	20	30	μV_{p-p}
Line Regulation (Note 4)		$V_{IN} = 13V$ to 33V	—	0.006	0.010	—	0.006	0.010	%/V
Load Regulation (Note 4)		$I_L = 0$ to 10mA	—	0.005	0.008	—	0.006	0.010	%/mA
Turn-on Settling Time	t_{on}	To ±0.1% of final value	—	5	—	—	5	—	μs
Quiescent Supply Current	I_{SY}	No Load	—	1.0	1.4	—	1.0	1.4	mA
Load Current	I_L		10	21	—	10	21	—	mA
Sink Current	I_S		−0.3	−0.5	—	−0.3	−0.5	—	mA
Short-Circuit Current	I_{SC}	$V_O = 0$	—	30	—	—	30	—	mA

ELECTRICAL CHARACTERISTICS at $V_{IN} = +15V$, $-55°C \le T_A \le +125°C$ and $I_L = 0mA$, unless otherwise noted.

			REF-01A/E			REF-01/H			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Ouput Voltage Change with Temperature (Notes 1, 2)	ΔV_{OT}	$0°C \le T_A \le +70°C$ $-55°C \le T_A \le +125°C$	— —	0.02 0.06	0.06 0.15	— —	0.07 0.18	0.17 0.45	%
Output Voltage Temperature Coefficient	TCV_O	(Note 3)	—	3.0	8.5	—	10.0	25.0	ppm/° C
Change in V_O Temperature Coefficient with Output Adjustment		$R_p = 10k\Omega$	—	0.7	—	—	0.7	—	ppm/%
Line Regulation ($V_{IN} = 13V$ to 33V) (Note 4)		$0°C \le T_A \le +70°C$ $-55°C \le T_A \le +125°C$	— —	0.007 0.009	0.012 0.015	— —	0.007 0.009	0.012 0.015	%/V
Load Regulation ($I_L = 0$ to 8mA) (Note 4)		$0°C \le T_A \le +70°C$ $-55°C \le T_A \le +125°C$	— —	0.006 0.007	0.010 0.012	— —	0.007 0.009	0.012 0.015	%/mA

NOTES:

1. ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 10V:

$$\Delta V_{OT} = \left| \frac{V_{MAX} - V_{MIN}}{10V} \right| \times 100$$

2. ΔV_{OT} specification applies trimmed to +10.000V or untrimmed.
3. TCV_O is defined as ΔV_{OT} divided by the temperature range, i.e.,

$$TCV_O\,(0° \text{ to } +70°C) = \frac{\Delta V_{OT}\,(0° \text{ to } +70°C)}{70°C}$$

$$\text{and } TCV_O\,(-55° \text{ to } +125°C) = \frac{\Delta V_{OT}\,(-55° \text{ to } +125°C)}{180°C}$$

4. Line and Load Regulation specifications include the effect of self heating.
5. Guaranteed by design.
6. Sample tested.

ELECTRICAL CHARACTERISTICS at $V_{IN} = +15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	REF-01C MIN	 TYP	 MAX	UNITS
Output Voltage	V_O	$I_L = 0mA$	9.90	10.00	10.10	V
Output Adjustment Range	ΔV_{trim}	$R_p = 10k\Omega$	±2.7	±3.3	—	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 6)	—	25	35	μV_{p-p}
Line Regulation (Note 4)		$V_{IN} = 13V$ to $30V$	—	0.009	0.015	%/V
Load Regulation (Note 4)		$I_L = 0$ to $8mA$ $I_L = 0$ to $4mA$	— —	0.006 0.006	0.015 0.015	%/mA
Turn-on Settling Time	t_{ON}	To ±0.1% of final value	—	5	—	μs
Quiescent Supply Current	I_{SY}	No Load	—	1.0	1.6	mA
Load Current	I_L		8	21	—	mA
Sink Current	I_S		−0.2	−0.5	—	mA
Short-Circuit Current	I_{SC}	$V_O = 0$	—	30	—	mA

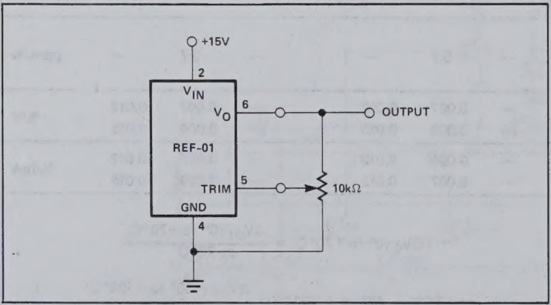
ELECTRICAL CHARACTERISTICS at $V_{IN} = +15V$, $0°C \leq T_A \leq +70°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	REF-01C MIN	 TYP	 MAX	UNITS
Ouput Voltage Change with Temperature	ΔV_{OT}	(Notes 1 and 2)	—	0.14	0.45	%
Output Voltage Temperature Coefficient	TCV_O	(Note 3)	—	20	65	ppm/°C
Change in V_O Temperature Coefficient with Output Adjustment		$R_p = 10k\Omega$	—	0.7	—	ppm/%
Line Regulation (Note 4)		$V_{IN} = 13V$ to $30V$	—	0.011	0.018	%/V
Load Regulation (Note 4)		$I_L = 0$ to $5mA$	—	0.008	0.018	%/mA

NOTES:

1. ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 10V:
$$\Delta V_{OT} = \left| \frac{V_{MAX} - V_{MIN}}{10V} \right| \times 100$$
2. ΔV_{OT} specification applies trimmed to +10.000V or untrimmed.
3. TCV_O is defined as ΔV_{OT} divided by the temperature range, i.e.,
$$TCV_O = \frac{\Delta V_{OT}}{70°C}$$
4. Line and Load Regulation specifications include the effect of self heating.
5. Guaranteed by design.
6. Sample tested.

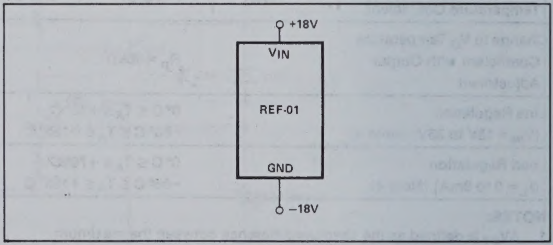
OUTPUT ADJUSTMENT



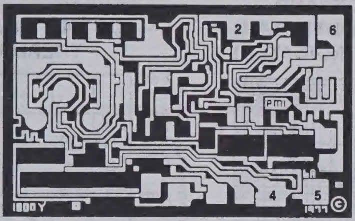
The REF-01 trim terminal can be used to adjust the output voltage over a 10V ±300mV range. This feature allows the system designer to trim system errors by setting the reference to a voltage other than 10V. Of course, the output can also be set to exactly 10.000V, or to 10.240V for binary applications.

Adjustment of the output does not significantly affect the temperature performance of the device. The temperature coefficient change is approximately 0.7 ppm/°C for 100mV of output adjustment.

BURN-IN CIRCUIT



DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)



2. INPUT VOLTAGE (V_{IN})
4. GROUND
5. TRIM
6. OUTPUT VOLTAGE (V_{OUT})

DIE SIZE 0.063 × 0.040 inch, 2520 sq. mils
(1.60 × 1.02 mm, 1.63 sq. mm)

For additional DICE information refer to Section 2.

WAFER TEST LIMITS at $V_S = +15V$, $T_A = 25°C$ for REF-01N and REF-01G devices; $T_A = 125°C$ for REF-01NT and REF-01GT devices, unless otherwise noted. (Note 1)

PARAMETER	SYMBOL	CONDITIONS	REF-01NT LIMIT	REF-01N LIMIT	REF-01GT LIMIT	REF-01G LIMIT	UNITS
Output Voltage	V_O	$I_L = 0$	10.05 9.95	10.03 9.97	10.10 9.90	10.05 9.95	V MAX V MIN
Output Adjustment Range	V_{trim}	$R_P = 10k\Omega$	—	±3.0	—	±3.0	% MIN
Line Regulation		$V_{IN} = 13V$ to $33V$	0.015	0.01	0.015	0.01	%/V MAX

Note: Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

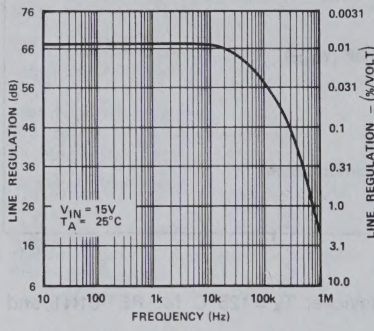
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = +15V$, $T_A = 25° C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	REF-01NT TYPICAL	REF-01N TYPICAL	REF-01GT TYPICAL	REF-01G TYPICAL	UNITS
Load Regulation		$I_L = 0$ to $10mA$ $I_L = 0$ to $8mA$, NT, GT @ +125° C	0.007	0.005	0.009	0.006	%/mA
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz	20	20	20	20	μV_{p-p}
Turn-On Settling Time	t_{ON}	To ±0.1% of Final Value NT, GT @ +125° C	7.5	5.0	7.5	5.0	µs
Quiescent Current	I_{SY}	No Load, NT, GT @ +125° C	1.4	1.0	1.4	1.0	mA
Load Current	I_L		21	21	21	21	mA
Sink Current	I_S		–0.5	–0.5	–0.5	–0.5	mA
Short-Circuit Current	I_{SC}	$V_O = 0$	30	30	30	30	mA
Output Voltage Temperature Coefficient	TCV_O		10	10	10	10	ppm/° C

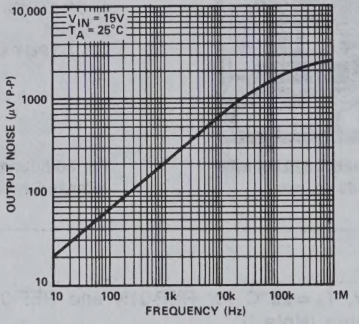
NOTE:
1. For +25° C specifications of REF-01NT and REF-01GT, see REF-01N and REF-01G respectively.

TYPICAL PERFORMANCE CHARACTERISTICS

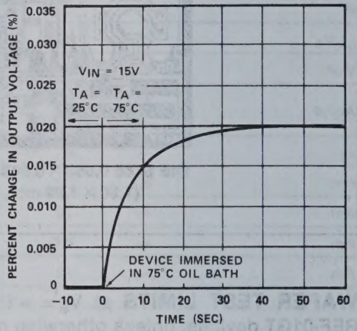
LINE REGULATION vs FREQUENCY



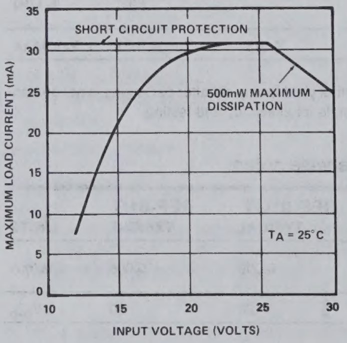
OUTPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



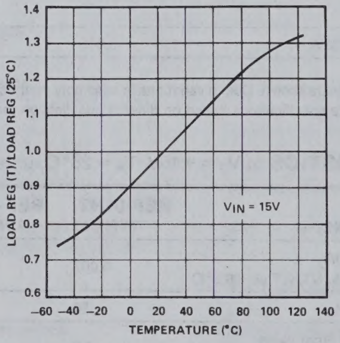
OUTPUT CHANGE DUE TO THERMAL SHOCK



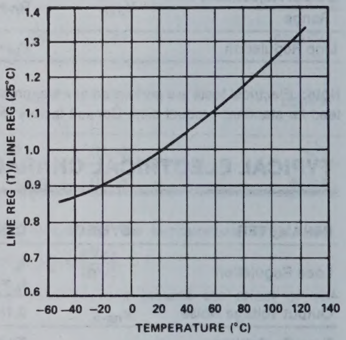
MAXIMUM LOAD CURRENT vs INPUT VOLTAGE



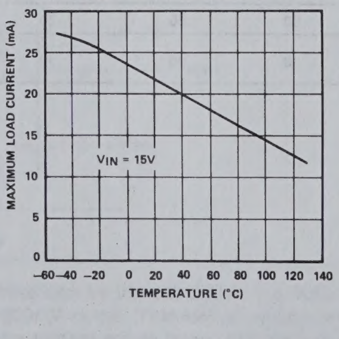
NORMALIZED LOAD REGULATION (ΔI_L = 10mA) vs TEMPERATURE



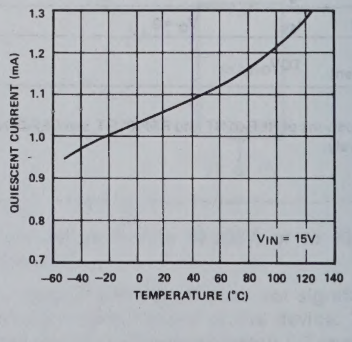
NORMALIZED LINE REGULATION vs TEMPERATURE



MAXIMUM LOAD CURRENT vs TEMPERATURE

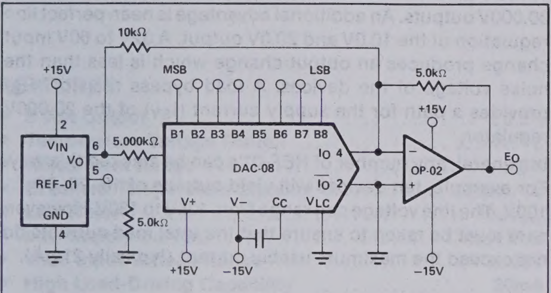


QUIESCENT CURRENT vs TEMPERATURE



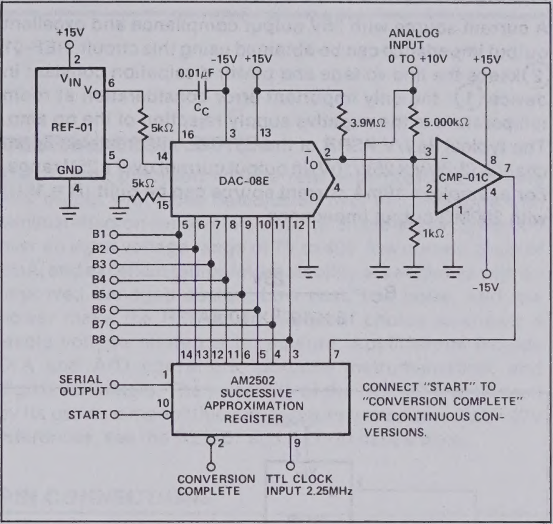
TYPICAL APPLICATIONS

D/A CONVERTER REFERENCE


+15V
2
V_{IN}
V_O
6
5
REF-01
GND
4
10kΩ
5.000kΩ
5.0kΩ
MSB
LSB
B1 B2 B3 B4 B5 B6 B7 B8
DAC-08
I_O 4
$\overline{I_O}$ 2
V+
V−
C_C
V_{LC}
+15V
−15V
5.0kΩ
+15V
OP-02
−15V
E_O

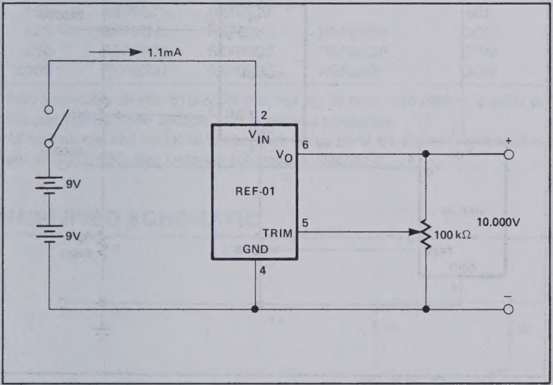
	B1	B2	B3	B4	B5	B6	B7	B8	E
POS. FULL-SCALE −1 LSB	1	1	1	1	1	1	1	1	+4.960
ZERO—SCALE	1	0	0	0	0	0	0	0	0.000
NEG. FULL-SCALE +1 LSB	0	0	0	0	0	0	0	1	−4.960
NEG. FULL-SCALE	0	0	0	0	0	0	0	0	−5.000

A/D CONVERTER REFERENCE

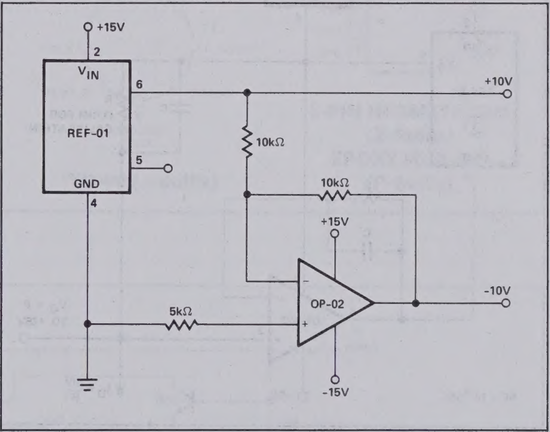

+15V
2
V_{IN}
V_O
6
REF-01
5
GND
4
0.01μF
C_C
−15V
+15V
5kΩ
16
3
13
14
5kΩ
15
DAC-08E
I_O
$\overline{I_O}$
2
4
5 6 7 8 9 10 11 12 1
ANALOG INPUT 0 TO +10V
+15V
3.9MΩ
5.000kΩ
3
2
8
7
CMP-01C
4
1
1kΩ
−15V
B1
B2
B3
B4
B5
B6
B7
B8
14 13 12 11 6 5 4 3
7
SERIAL OUTPUT
1
START
10
AM2502 SUCCESSIVE APPROXIMATION REGISTER
2
9
CONVERSION COMPLETE
TTL CLOCK INPUT 2.25MHz

CONNECT "START" TO "CONVERSION COMPLETE" FOR CONTINUOUS CONVERSIONS.

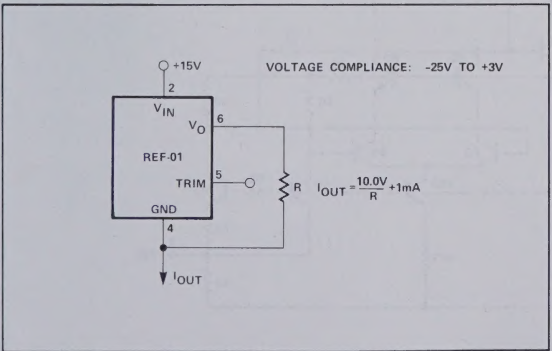
PRECISION CALIBRATION STANDARD


1.1mA
9V
9V
2
V_{IN}
V_O
6
REF-01
5
TRIM
GND
4
+
100kΩ
10.000V
−

±10V REFERENCE


+15V
2
V_{IN}
6
REF-01
5
GND
4
+10V
10kΩ
10kΩ
+15V
OP-02
−10V
5kΩ
−15V

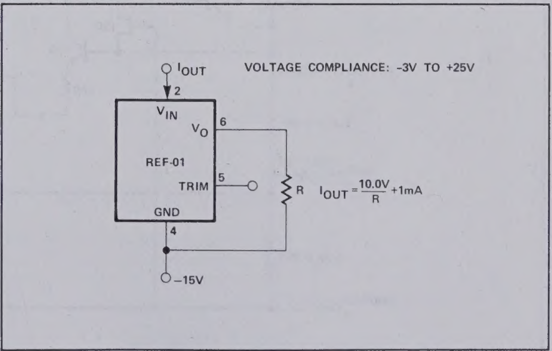
CURRENT SOURCE


+15V
2
V_{IN}
V_O
6
REF-01
5
TRIM
GND
4
R
I_{OUT}

VOLTAGE COMPLIANCE: -25V TO +3V

$I_{OUT} = \frac{10.0V}{R} + 1mA$

CURRENT SINK


I_{OUT}
2
V_{IN}
V_O
6
REF-01
5
TRIM
GND
4
R
−15V

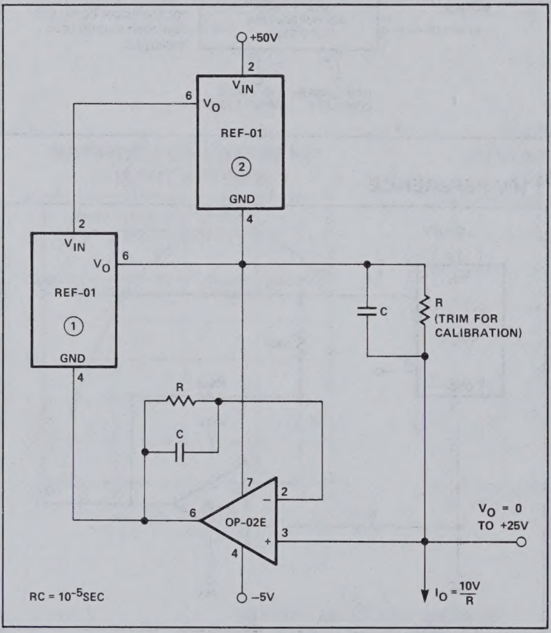
VOLTAGE COMPLIANCE: -3V TO +25V

$I_{OUT} = \frac{10.0V}{R} + 1mA$

PRECISION CURRENT SOURCE

A current source with 25V output compliance and excellent output impedance can be obtained using this circuit. REF-01 ② keeps the line voltage and power dissipation constant in device ①; the only important error consideration at room temperature is the negative supply rejection of the op amp. The typical 3μV/V PSRR of the OP-02E will create an 8ppm change (3μV/V × 25V/10V) in output current over a 25V range. For example, a 10mA current source can be built (R = 1kΩ) with 300MΩ output impedance.

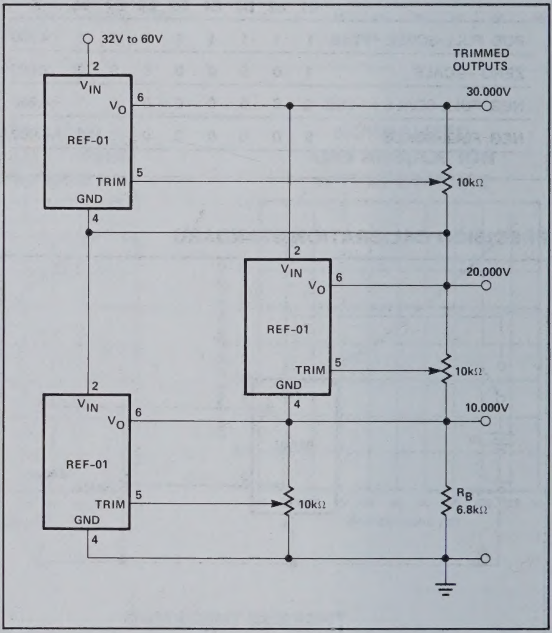
$$R_O = \frac{25V}{8 \times 10^{-6} \times 10mA}$$


+50V
2
V_IN
6
V_O
REF-01
②
GND
4
2
V_IN
V_O
6
REF-01
①
GND
4
C
R
(TRIM FOR CALIBRATION)
R
C
7
2
6
OP-02E
3
4
V_O = 0 TO +25V
RC = 10^-5SEC
−5V
I_O = 10V/R

REFERENCE STACK WITH EXCELLENT LINE REGULATION

Three REF-01's can be stacked to yield 10.000, 20.000, and 30.000V outputs. An additional advantage is near-perfect line regulation of the 10.0V and 20.0V output. A 32V to 60V input change produces an output change which is less than the noise voltage of the devices. A load bypass resistor (R_B) provides a path for the supply current (I_{SY}) of the 20.000V regulator.

In general, any number of REF-01's can be stacked this way. For example, ten devices will yield outputs of 10, 20, 30 . . . 100V. The line voltage can range from 105V to 130V. However, care must be taken to ensure that the total load currents do not exceed the maximum usable current (typically 21mA).


32V to 60V
TRIMMED OUTPUTS
2
V_IN
V_O
6
REF-01
TRIM
5
GND
4
30.000V
10kΩ
2
V_IN
V_O
6
REF-01
TRIM
5
GND
4
20.000V
10kΩ
2
V_IN
V_O
6
REF-01
TRIM
5
GND
4
10.000V
10kΩ
R_B
6.8kΩ

+5V PRECISION VOLTAGE REFERENCE/ TEMPERATURE TRANSDUCER

REF-02

FEATURES

- **5 Volt Output .... ±0.3%**
- **Temperature Voltage Output .... 2.1mV/°C**
- **Adjustment Range .... ±6%**
- **Excellent Temperature Stability .... 3ppm/°C**
- **Low Noise .... $10\mu V_{p-p}$**
- **Low Supply Current .... 1.4mA Max**
- **Wide Input Voltage Range .... 8V to 33V**
- **High Load-Driving Capability 20mA**
- **No External Components**
- **Short-Circuit Proof**
- **MIL-STD-883 Screening Available**

ORDERING INFORMATION†

$T_A = 25°C$ ΔV_O MAX (mV)	PACKAGE TO-99 8-PIN	HERMETIC DIP 8-PIN	PLASTIC DIP 8-PIN	OPERATING TEMPERATURE RANGE
±15	REF02AJ*	REF02AZ*	–	MIL
±15	REF02EJ	REF02EZ		COM
±25	REF02J*	REF02Z*		MIL
±25	REF02HJ	REF02HZ	REF02HP	COM
±50	REF02CJ	REF02CZ	REF02CP	COM
±100	REF02DJ	REF02DZ	REF02DP	COM

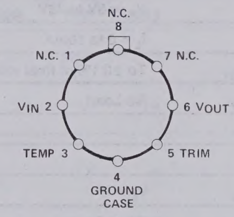
*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

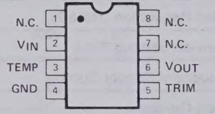
GENERAL DESCRIPTION

The REF-02 precision voltage reference provides a stable +5V output which can be adjusted over at ±6% range with minimal effect on temperature stability. Single-supply operation over an input voltage range of 7V to 40V, low current drain of 1mA, and excellent temperature stability are achieved with an improved bandgap design. Low cost, low noise, and low power make the REF-02 an excellent choice whenever a stable voltage reference is required. Applications include D/A and A/D converters, portable instrumentation, and digital voltmeters. The versatility of the REF-02 is enhanced by its use as a monolithic temperature transducer. For +10V references, see the REF-01 and REF-10 data sheets.

PIN CONNECTIONS

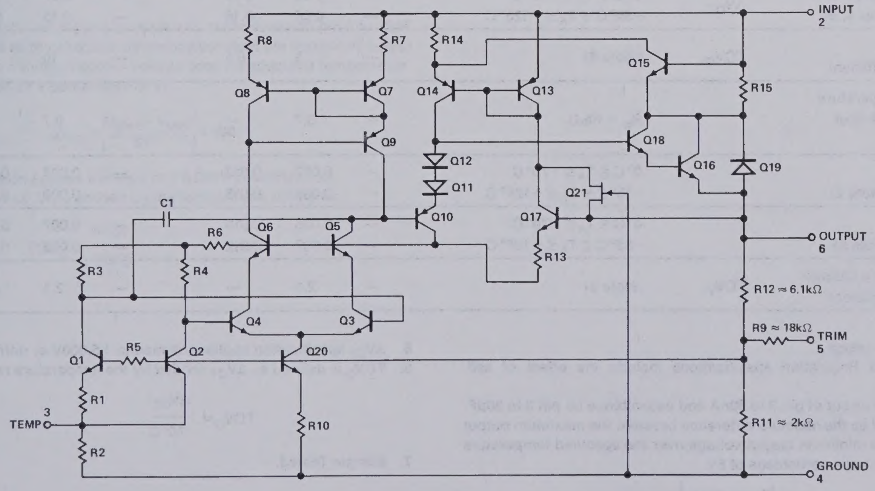

N.C.
8
N.C. 1
7 N.C.
VIN 2
6 VOUT
TEMP 3
5 TRIM
4
GROUND
CASE

TO-99 (J-Suffix)


N.C. 1
VIN 2
TEMP 3
GND 4
8 N.C.
7 N.C.
6 VOUT
5 TRIM

8-PIN HERMETIC DIP (Z-Suffix)
EPOXY MINI-DIP (P-Suffix)

SIMPLIFIED SCHEMATIC


INPUT
2
R8
R7
R14
Q15
R15
Q8
Q7
Q14
Q13
Q9
Q18
Q12
Q16
Q19
Q11
Q21
C1
Q10
Q17
R6
Q6
Q5
OUTPUT
6
R13
R3
R4
R12 ≈ 6.1kΩ
Q4
Q3
R9 ≈ 18kΩ
TRIM
5
R5
Q1
Q2
Q20
R1
3
TEMP
R10
R11 ≈ 2kΩ
R2
GROUND
4

ABSOLUTE MAXIMUM RATINGS (Note 2)

Input Voltage	
REF-02 A, E, H, All DICE	40V
REF-02 C, D	30V
Power Dissipation (Note 1)	500mW
Output Short-Circuit Duration (to Ground or V_{IN})	Indefinite
Storage Temperature Range	
J and Z Packages	−65°C to +150°C
P Package	−65°C to +125°C
Operating Temperature Range	
REF-02A, REF-02	−55°C to +125°C
REF-02E, REF-02H	0°C to +70°C
REF-02C, REF-02D	0°C to +70°C
Lead Temperature (Soldering, 60 sec)	300°C
DICE Junction Temperature (T_j)	−65°C to +150°C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C
8-Pin Plastic DIP (P)	36°C	5.6mW/°C

2. Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_{IN} = +15V$, $T_A = +25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	REF-02A/E MIN	REF-02A/E TYP	REF-02A/E MAX	REF-02/H MIN	REF-02/H TYP	REF-02/H MAX	UNITS
Output Voltage	V_O	$I_L = 0$	4.985	5.000	5.015	4.975	5.000	5.025	V
Output Adjustment Range	ΔV_{trim}	$R_p = 10k\Omega$	±3	±6	—	±3	±6	—	%
Output Voltage Noise	$e_{np\text{-}p}$	0.1Hz to 10Hz (Note 7)	—	10	15	—	10	15	$\mu V_{p\text{-}p}$
Line Regulation (Note 2)		$V_{IN} = 8V$ to $33V$	—	0.006	0.010	—	0.006	0.010	%/V
Load Regulation (Note 2)		$I_L = 0$ to $10mA$	—	0.005	0.010	—	0.006	0.010	%/mA
Turn-on Settling Time	t_{ON}	To ±0.1% of final value	—	5	—	—	5	—	μs
Quiescent Supply Current	I_{SY}	No Load	—	1.0	1.4	—	1.0	1.4	mA
Load Current	I_L		10	21	—	10	21	—	mA
Sink Current	I_S		−0.3	−0.5	—	−0.3	−0.5	—	mA
Short-Circuit Current	I_{SC}	$V_O = 0$	—	30	—	—	30	—	mA
Temperature Voltage Output	V_T	(Note 3)	—	630	—	—	630	—	mV

ELECTRICAL CHARACTERISTICS at $V_{IN} = +15V$, $-55°C \leq T_A \leq \pm 125°C$ for REF-02A and REF-02, $0°C \leq T_A \leq +70°C$ for REF-02E and REF-02H, $I_L = 0mA$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	REF-02A/E MIN	REF-02A/E TYP	REF-02A/E MAX	REF-02/H MIN	REF-02/H TYP	REF-02/H MAX	UNITS
Ouput Voltage Change with Temperature (Notes 4, 5)	ΔV_{OT}	$0°C \leq T_A \leq +70°C$ $-55°C \leq T_A \leq +125°C$	— —	0.02 0.06	0.06 0.15	— —	0.07 0.18	0.17 0.45	%
Output Voltage Temperature Coefficient	TCV_O	(Note 6)	—	3	8.5	—	10	25	ppm/°C
Change in V_O Temperature Coefficient with Output Adjustment		$R_p = 10k\Omega$	—	0.7	—	—	0.7	—	ppm/%
Line Regulation ($V_{IN} = 8$ to $33V$) (Note 2)		$0°C \leq T_A \leq +70°C$ $-55°C \leq T_A \leq +125°C$	— —	0.007 0.009	0.012 0.015	— —	0.007 0.009	0.012 0.015	%/V
Load Regulation ($I_L = 0$ to $8mA$) (Note 2)		$0°C \leq T_A \leq +70°C$ $-55°C \leq T_A \leq +125°C$	— —	0.006 0.007	0.010 0.012	— —	0.007 0.009	0.012 0.015	%/mA
Temperature Voltage Output Temperature Coefficient	TCV_T	(Note 3)	—	2.1	—	—	2.1	—	mV/°C

NOTES:

1. Guaranteed by design.
2. Line and Load Regulation specifications include the effect of self heating.
3. Limit current in or out of pin 3 to 50nA and capacitance on pin 3 to 30pF.
4. ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 5V.

$$\Delta V_{OT} = \left| \frac{V_{MAX} - V_{MIN}}{5V} \right| \times 100$$

5. ΔV_{OT} specification applies trimmed to +5.000V or untrimmed.
6. TCV_O is defined as ΔV_{OT} divided by the temperature range, i.e.,

$$TCV_O = \frac{\Delta V_{OT}}{70°C}$$

7. Sample Tested.

ELECTRICAL CHARACTERISTICS at $V_{IN} = +15V$, $T_A = 25°C$, unless otherwise noted.

			REF-02C			REF-02D			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Output Voltage	V_O	$I_L = 0mA$	4.950	5.000	5.050	4.900	5.000	5.100	V
Output Adjustment Range	ΔV_{trim}	$R_p = 10k\Omega$	±2.7	±6.0	—	±2.0	±6.0	—	%
Output Voltage Noise	$e_{np\text{-}p}$	0.1Hz to 10Hz (Note 7)	—	12	18	—	12	—	$\mu V_{p\text{-}p}$
Line Regulation (Note 2)		$V_{IN} = 8V$ to 30V	—	0.009	0.015	—	0.010	0.04	%/V
Load Regulation (Note 2)		$I_L = 0$ to 8mA $I_L = 0$ to 4mA	— —	0.006 —	0.015 —	— —	— 0.015	— 0.04	%/mA
Turn-on Settling Time	t_{ON}	To ±0.1% of final value	—	5	—	—	5	—	μs
Quiescent Supply Current	I_{SY}	No Load	—	1.0	1.6	—	1.0	2.0	mA
Load Current	I_L		8	21	—	8	21	—	mA
Sink Current	I_S		−0.2	−0.5	—	−0.2	−0.5	—	mA
Short-Circuit Current	I_{SC}	$V_O = 0$	—	30	—	—	30	—	mA
Temperature Voltage Output	V_T	(Note 3)	—	630	—	—	630	—	mV

ELECTRICAL CHARACTERISTICS at $V_{IN} = +15V$, $0°C \leq T_A \leq +70°C$ and $I_L = 0mA$, unless otherwise noted.

			REF-02C			REF-02D			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Ouput Voltage Change with Temperature	ΔV_{OT}	(Notes 4 and 5)	—	0.14	0.45	—	0.49	1.7	%
Output Voltage Temperature Coefficient	TCV_O	(Note 6)	—	20	65	—	70	250	ppm/°C
Change in V_O Temperature Coefficient With Output Adjustment		$R_p = 10k\Omega$	—	0.7	—	—	0.7	—	ppm/%
Line Regulation (Note 2)		$V_{IN} = 8V$ to 30V	—	0.011	0.018	—	0.012	0.05	%/V
Load Regulation (Note 2)		$I_L = 0$ to 5mA	—	0.008	0.018	—	0.016	0.05	%/mA
Temperature Voltage Output Temperature Coefficient	TCV_T	(Note 3)	—	2.1	—	—	2.1	—	mV/°C

NOTES:

1. Guaranteed by design.
2. Line and Load Regulation specifications include the effect of self heating.
3. Limit current in or out of pin 3 to 50nA and capacitance on pin 3 to 30pF.
4. ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 5V.

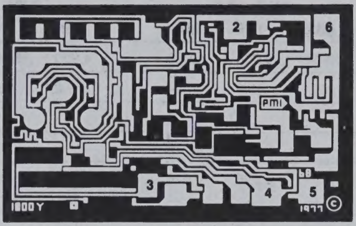
$$\Delta V_{OT} = \left| \frac{V_{MAX} - V_{MIN}}{5V} \right| \times 100$$

5. ΔV_{OT} specification applies trimmed to +5.000V or untrimmed.
6. TCV_O is defined as ΔV_{OT} divided by the temperature range, i.e.,

$$TCV_O = \frac{\Delta V_{OT}}{70°C}$$

7. Sample Tested.

DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)



DIE SIZE 0.063 × 0.040 inch, 2520 sq. mils
(1.60 × 1.02 mm, 1.63 sq. mm)

2. INPUT VOLTAGE (V_{IN})
3. TEMPERATURE TRANSDUCER OUTPUT VOLTAGE (TEMP)
4. GROUND
5. TRIM
6. OUTPUT VOLTAGE (V_{OUT})

For additional DICE information refer to Section 2.

WAFER TEST LIMITS at $V_S = +15V$, $T_A = 25°C$ for REF-02N and REF-02G devices; $T_A = 125°C$ for REF-02NT and REF-02GT devices, unless otherwise noted. (Note 3)

PARAMETER	SYMBOL	CONDITIONS	REF-02NT LIMIT	REF-02N LIMIT	REF-02GT LIMIT	REF-02G LIMIT	UNITS
Output Voltage	V_O	$I_L = 0$	4.975 5.025	4.985 5.015	4.950 5.050	4.975 5.025	V MIN V MAX
Output Adjustment Range	V_{trim}	$R_P = 10k\Omega$	—	±3	—	±3	% MIN
Line Regulation		$V_{IN} = 8V$ to $33V$	0.015	0.01	0.015	0.01	%/V MAX

Note: Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = +15V$, $T_A = +25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	REF-02NT TYPICAL	REF-02N TYPICAL	REF-02GT TYPICAL	REF-02G TYPICAL	UNITS
Temp. Voltage Output	V_T	(Notes 1, 2)	630	630	630	630	mV
Temp. Voltage Output Temp. Coefficient	TCV_T	(Notes 1, 2)	2.1	2.1	2.1	2.1	mV/°C
Output Voltage Temp. Coefficient	TCV_O		10	10	10	10	ppm/°C
Load Regulation		$I_L = 0$ to $10mA$ $I_L = 0$ to $8mA$, NT, GT @ +125°C	0.007	0.005	0.009	0.006	%/mA
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz	10	10	10	10	μV_{p-p}
Turn-On Settling Time	t_{ON}	To ±0.1% of final value, NT, GT @ +125°C	7.5	5.0	7.5	5.0	μs
Quiescent Supply Current	I_{SY}	No Load, NT, GT @ +125°C	1.4	1.0	1.4	1.0	mA
Load Current	I_L		21	21	21	21	mA
Sink Current	I_S		−0.5	−0.5	−0.5	−0.5	mA
Short-Circuit Current	I_{SC}	$V_O = 0$	30	30	30	30	mA

NOTES:

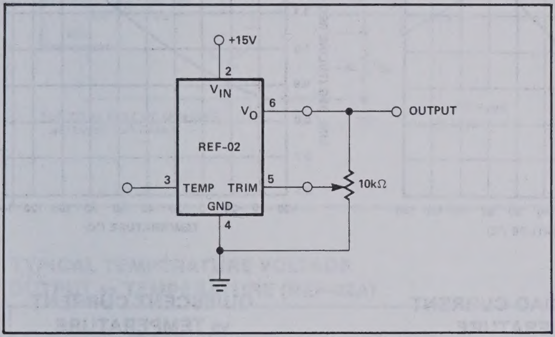
1. See AN-18 for detailed REF-02 thermometer applications information.
2. Limit current in or out of pin 3 to 50nA and capacitance on pin 3 to 30pF.
3. For +25° C specifications of REF-02NT and REF-02GT, See REF-02N and REF-02G respectively.

OUTPUT ADJUSTMENT

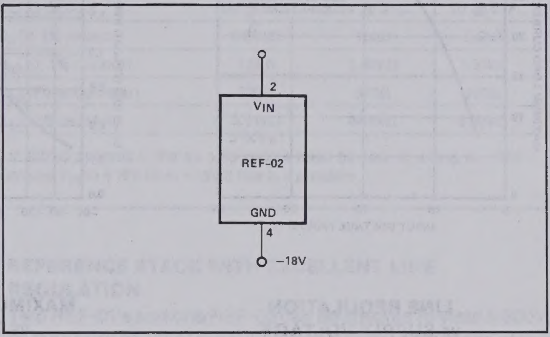
The REF-02 trim terminal can be used to adjust the output voltage over a 5V ±300mV range. This feature allows the system designer to trim system errors by setting the reference to a voltage other than 5V. Of course, the output can also be set to exactly 5.000V or to 5.12V for binary applications.

Adjustment of the output does not significantly affect the temperature performance of the device. Typically, the temperature coefficent change is 0.7ppm/° C for 100mV of output adjustment.

OUTPUT ADJUSTMENT CIRCUIT

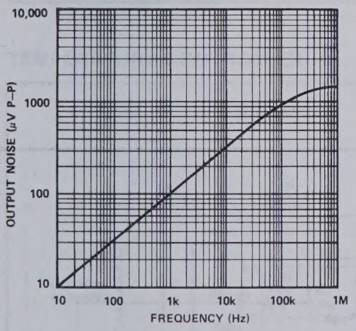


BURN-IN CIRCUIT

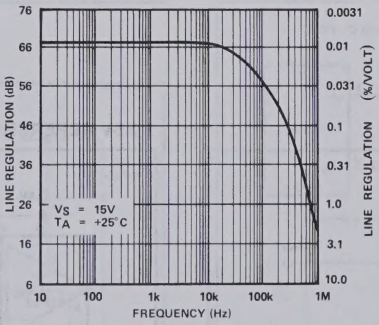


TYPICAL PERFORMANCE CHARACTERISTICS

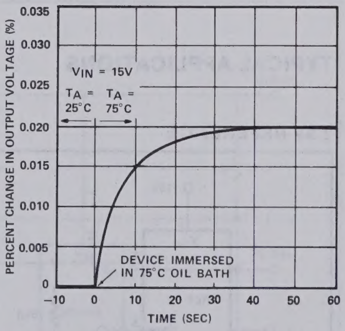
OUTPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



LINE REGULATION vs FREQUENCY

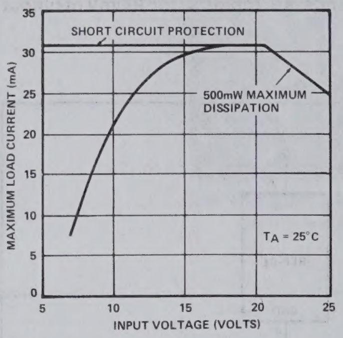


OUTPUT CHANGE DUE TO THERMAL SHOCK

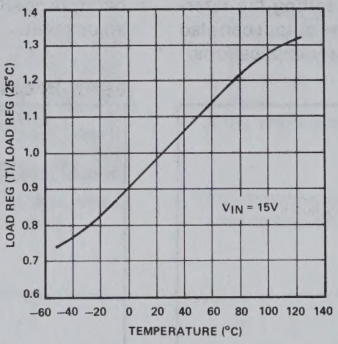


TYPICAL PERFORMANCE CHARACTERISTICS

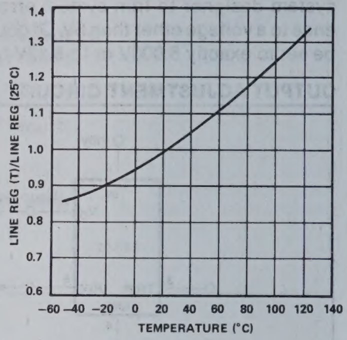
MAXIMUM LOAD CURRENT vs INPUT VOLTAGE



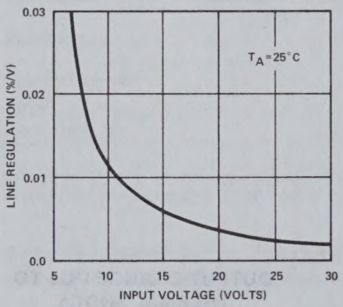
NORMALIZED LOAD REGULATION (ΔI_L = 10mA) vs TEMPERATURE



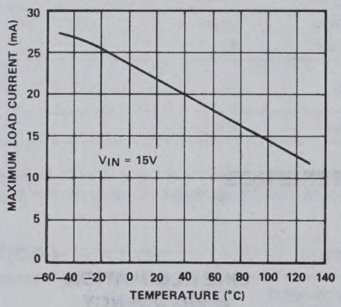
NORMALIZED LINE REGULATION vs TEMPERATURE



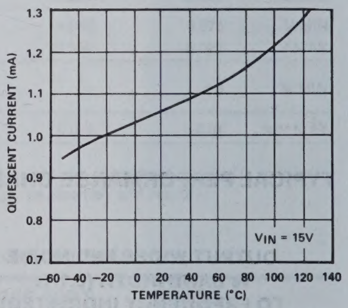
LINE REGULATION vs SUPPLY VOLTAGE



MAXIMUM LOAD CURRENT vs TEMPERATURE

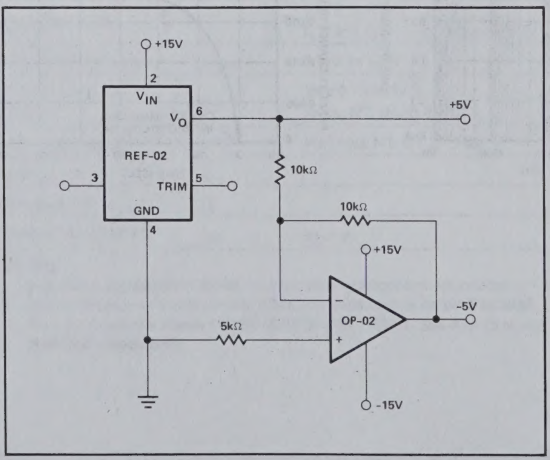


QUIESCENT CURRENT vs TEMPERATURE

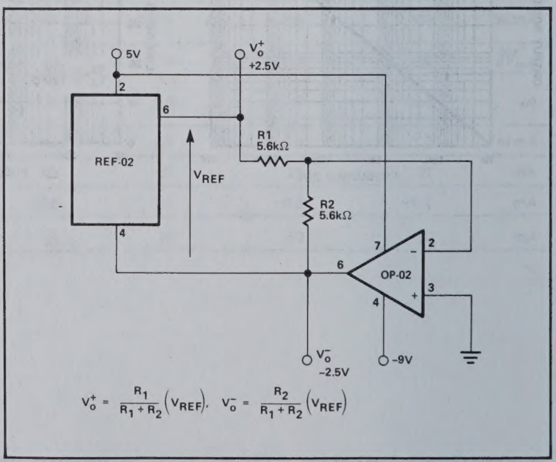


TYPICAL APPLICATIONS

±5V REFERENCE

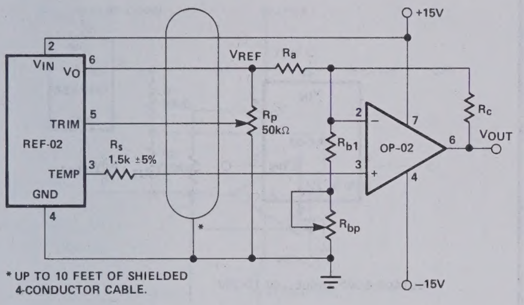

+15V
2
V_{IN}
V_O
6
REF-02
3
5
TRIM
GND
4
+5V
10kΩ
10kΩ
+15V
−
OP-02
+
−5V
5kΩ
−15V

±2.5V REFERENCE


5V
V_o^+
+2.5V
2
6
REF-02
V_{REF}
R1
5.6kΩ
R2
5.6kΩ
4
7
2
6
OP-02
3
4
−
+
V_o^-
−2.5V
−9V

$$V_o^+ = \frac{R_1}{R_1 + R_2}\left(V_{REF}\right), \quad V_o^- = \frac{R_2}{R_1 + R_2}\left(V_{REF}\right)$$

PRECISION TEMPERATURE TRANSDUCER WITH REMOTE SENSOR

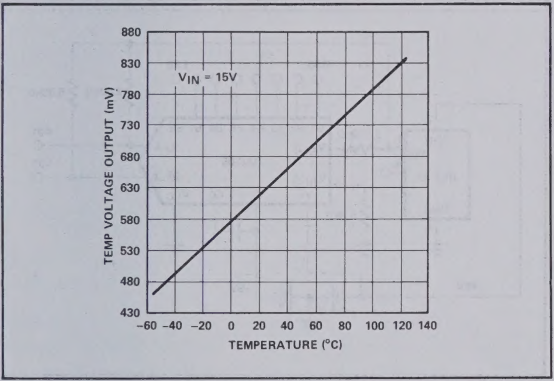

+15V
2
VIN
VO
6
VREF
Ra
Rc
5
TRIM
Rp
50kΩ
2
7
REF-02
Rs
1.5k ±5%
Rb1
OP-02
6
VOUT
3
TEMP
3
4
GND
4
Rbp
*
−15V

*UP TO 10 FEET OF SHIELDED 4-CONDUCTOR CABLE.

RESISTOR VALUES			
TCV_{OUT} SLOPE (S)	10mV/°C	100mV/°C	10mV/°F
TEMPERATURE RANGE	−55°C to +125°C	−55°C to +125°C	−67°F to +257°C
OUTPUT VOLTAGE RANGE	−0.55V to +1.25V	−5.5V to +12.5V*	−0.67V to +2.57V
ZERO-SCALE	0V @ 0°C	0V @ 0°C	0V @ 0°F
R_a (± 1% resistor)	9.09kΩ	15kΩ	7.5kΩ
R_{b1} (± 1% resistor)	1.5kΩ	1.82kΩ	1.21kΩ
R_{bp} (Potentiometer)	200Ω	500Ω	200Ω
R_c (±1% resistor)	5.11kΩ	84.5kΩ	8.25kΩ

*For 125°C operation, the op amp output must be able to swing to +12.5V, increase V_{IN} to +18V from +15V if this is a problem.

TYPICAL TEMPERATURE VOLTAGE OUTPUT vs TEMPERATURE (REF-02A)

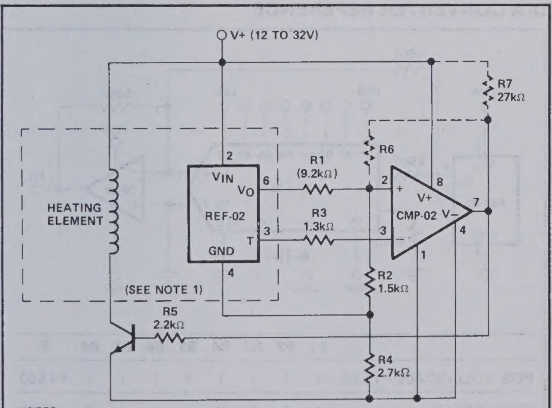


REFERENCE STACK WITH EXCELLENT LINE REGULATION

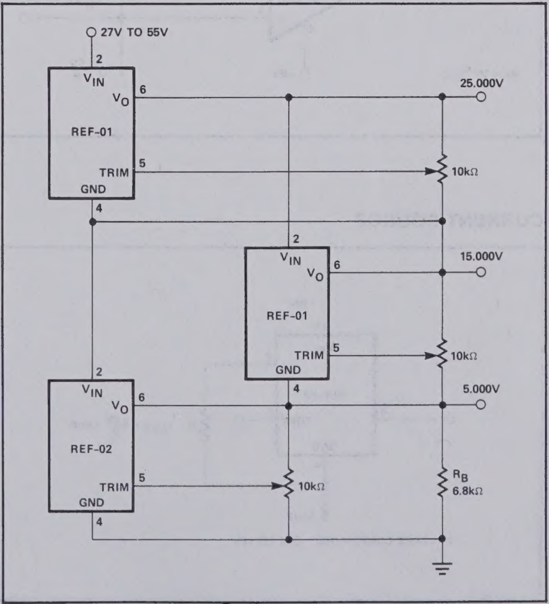
Two REF-01's and one REF-02 can be stacked to yield 5.000V, 15.000V and 25.000V outputs. An additional advantage of this circuit is near-perfect line regulation of the 5.0V and 15.0V outputs. A 27V to 55V input change produces an output change which is less than the noise voltage of the devices. A load bypass resistor (R_B) provides a path for the supply current (I_{SY}) of the 15.000V regulator.

In general, any number of REF-01's and REF-02's can be stacked this way. For example, ten devices will yield ten outputs in 5V or 10V steps. The line voltage can range from 100V to 130V. However, care must be taken to ensure that the total load currents do not exceed the maximum usable current (typically 21mA).

TEMPERATURE CONTROLLER


V+ (12 TO 32V)
R7
27kΩ
R6
2
R1
(9.2kΩ)
VIN
VO
6
2
+
8
V+
HEATING ELEMENT
REF-02
R3
1.3kΩ
CMP-02
V−
7
3
T
3
−
4
GND
1
4
R2
1.5kΩ
(SEE NOTE 1)
R5
2.2kΩ
R4
2.7kΩ

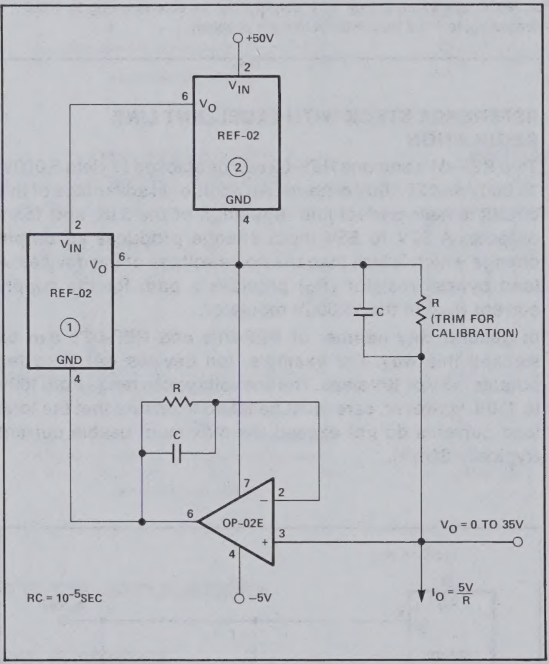
NOTES:
1. REF-02 SHOULD BE THERMALLY CONNECTED TO SUBSTANCE BEING HEATED.
2. NUMBERS IN PARENTHESES ARE FOR A SETPOINT TEMPERATURE OF 60°C.
3. R3 = R1‖R2‖R6


27V TO 55V
2
VIN
VO
6
25.000V
REF-01
TRIM
5
10kΩ
GND
4
2
VIN
VO
6
15.000V
REF-01
TRIM
5
10kΩ
GND
2
4
5.000V
VIN
VO
6
REF-02
TRIM
5
10kΩ
RB
6.8kΩ
GND
4

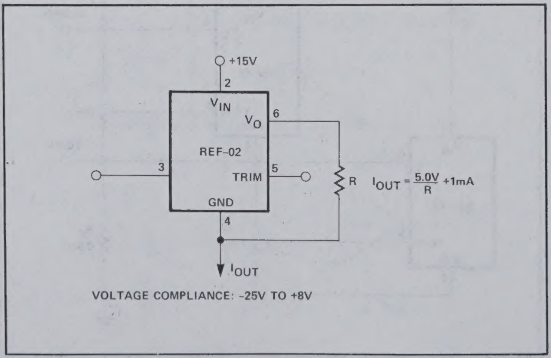
PRECISION CURRENT SOURCE

A current source with 35V output compliance and excellent output impedance can be obtained using this circuit. REF-02 ② keeps the line voltage and power dissipation constant in device ①; the only important error consideration at room temperature is the negative supply rejection of the op amp. The typical $3\mu V/V$ PSRR of the OP-02E will create a 20ppm change ($3\mu V/V \times 35V/5V$) in output current over a 35V range. For example, a 5mA current source can be built ($R = 1k\Omega$) with $350M\Omega$ output impedance.

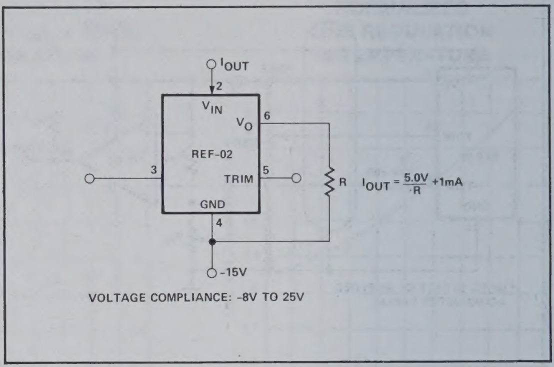
$$R_O = \frac{35V}{20 \times 10^{-6} \times 5mA}$$


+50V
2
VIN
6
VO
REF-02
②
GND
4
2
VIN
6
VO
REF-02
①
GND
4
C
R
(TRIM FOR CALIBRATION)
R
C
7
2
6
OP-02E
3
4
VO = 0 TO 35V
RC = 10⁻⁵SEC
−5V
IO = 5V/R

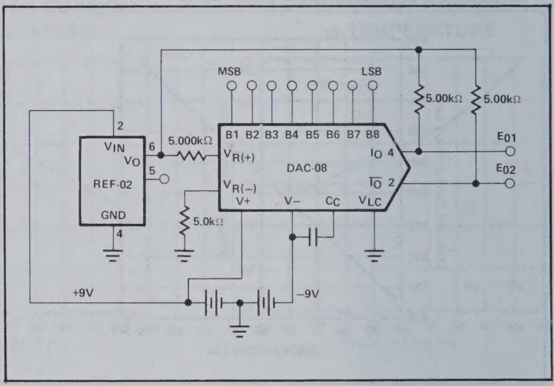
CURRENT SOURCE


+15V
2
VIN
VO
6
REF-02
3
5
TRIM
R
IOUT = 5.0V/R +1mA
GND
4
IOUT
VOLTAGE COMPLIANCE: -25V TO +8V

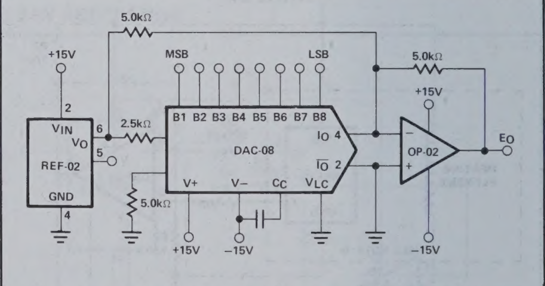
CURRENT SINK


IOUT
2
VIN
VO
6
REF-02
3
TRIM
5
R
IOUT = 5.0V/R +1mA
GND
4
-15V
VOLTAGE COMPLIANCE: -8V TO 25V

BATTERY OPERATED D/A CONVERTER REFERENCE

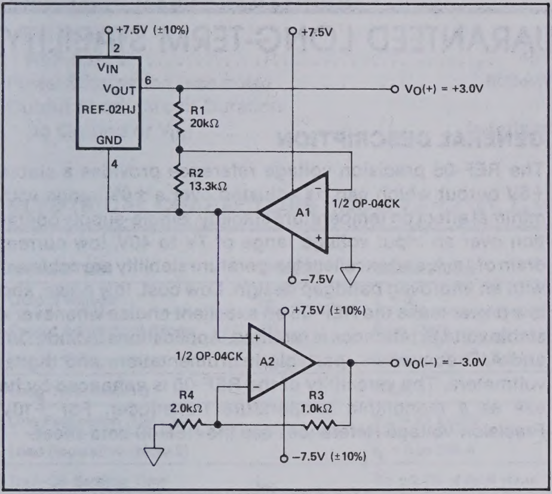

MSB
LSB
5.00kΩ
5.00kΩ
2
VIN
VO
6
5
REF-02
GND
4
5.000kΩ
B1 B2 B3 B4 B5 B6 B7 B8
VR(+)
IO 4
DAC-08
ĪO 2
VR(−)
V+
V−
CC
VLC
5.0kΩ
E01
E02
+9V
−9V

D/A CONVERTER REFERENCE

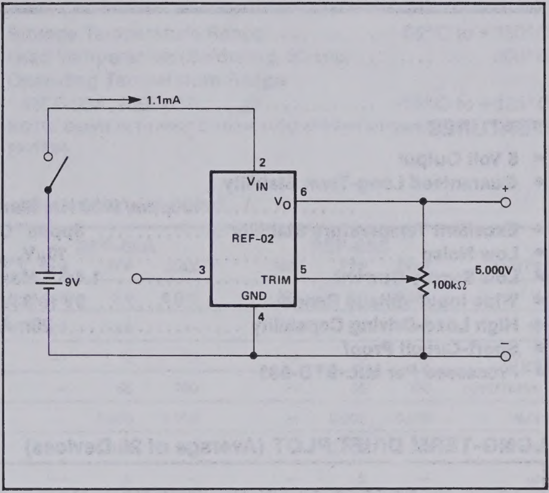

5.0kΩ
+15V
MSB
LSB
5.0kΩ
+15V
2
VIN
VO
6
5
REF-02
GND
4
2.5kΩ
B1 B2 B3 B4 B5 B6 B7 B8
IO 4
DAC-08
ĪO 2
V+
V−
CC
VLC
5.0kΩ
+15V
−15V
OP-02
EO
−15V

	B1	B2	B3	B4	B5	B6	B7	B8	E
POS. FULL-SCALE −1 LSB	1	1	1	1	1	1	1	1	+4.960
ZERO-SCALE	1	0	0	0	0	0	0	0	0.000
NEG. FULL-SCALE +1 LSB	0	0	0	0	0	0	0	1	−4.960
NEG. FULL-SCALE	0	0	0	0	0	0	0	0	−5.000

±3V REFERENCE


+7.5V (±10%)
2
VIN
VOUT
6
REF-02HJ
GND
4
+7.5V
VO(+) = +3.0V
R1
20kΩ
R2
13.3kΩ
A1
1/2 OP-04CK
−7.5V
+7.5V (±10%)
1/2 OP-04CK
A2
VO(−) = −3.0V
R4
2.0kΩ
R3
1.0kΩ
−7.5V (±10%)

PRECISION CALIBRATION STANDARD


1.1mA
2
VIN
VO
6
REF-02
3
TRIM
5
GND
4
9V
+
5.000V
100kΩ
−

REF-05 +5V PRECISION VOLTAGE REFERENCE

(GUARANTEED LONG-TERM STABILITY)

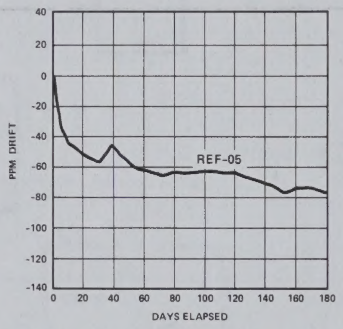
FEATURES

- **5 Volt Output**
- **Guaranteed Long-Term Stability .... 100ppm/1000 Hrs Max**
- **Excellent Temperature Stability .... 3ppm/°C**
- **Low Noise .... $10\mu V_{p-p}$**
- **Low Supply Current .... 1.4mA Max**
- **Wide Input Voltage Range .... 8V to 33V**
- **High Load-Driving Capability 20mA**
- **Short-Circuit Proof**
- **Processed Per MIL-STD-883**

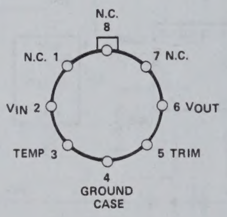
GENERAL DESCRIPTION

The REF-05 precision voltage reference provides a stable +5V output which can be adjusted over a ±6% range with minimal effect on temperature stability. Single-supply operation over an input voltage range of 7V to 40V, low current drain of 1mA, and excellent temperature stability are achieved with an improved bandgap design. Low cost, low noise, and low power make the REF-05 an excellent choice whenever a stable voltage reference is required. Applications include D/A and A/D converters, portable instrumentation, and digital voltmeters. The versatility of the REF-05 is enhanced by its use as a monolithic temperature transducer. For +10V Precision Voltage References see the REF-10 data sheet.

LONG-TERM DRIFT PLOT (Average of 20 Devices)



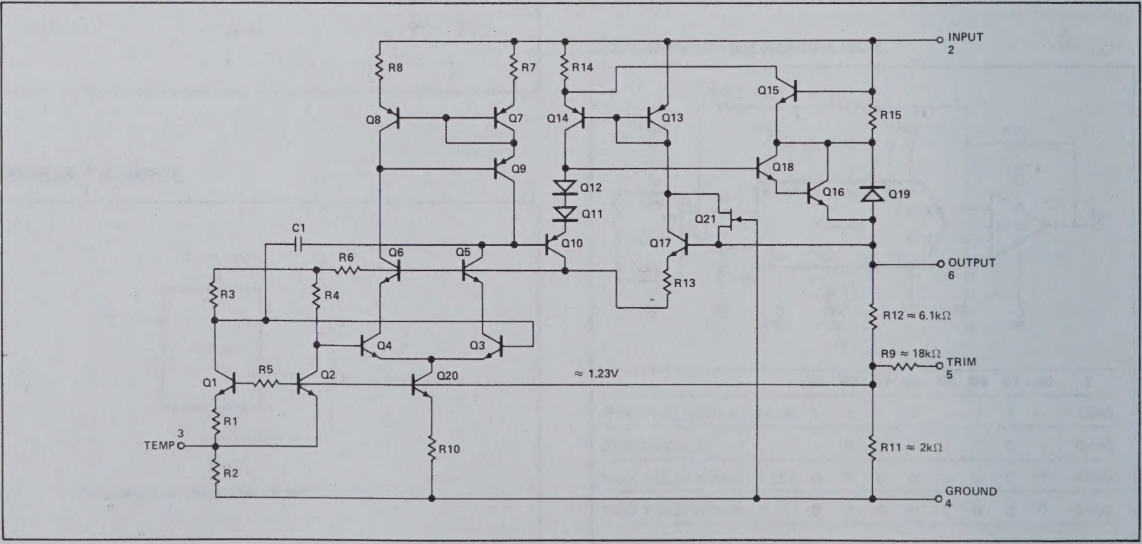
PIN CONNECTIONS



N.C. 8
N.C. 1
7 N.C.
VIN 2
6 VOUT
TEMP 3
5 TRIM
4 GROUND CASE

TO-99 (J-Suffix)
REF-05AJ/883
REF-05BJ/883

SIMPLIFIED SCHEMATIC



INPUT 2
R8
R7
R14
Q15
R15
Q8
Q7
Q14
Q13
Q9
Q18
Q12
Q16
Q19
Q11
Q21
C1
Q10
Q17
R6
Q6
Q5
OUTPUT 6
R3
R4
R13
R12 ≈ 6.1kΩ
Q4
Q3
R9 ≈ 18kΩ
TRIM 5
Q1
R5
Q2
Q20
≈ 1.23V
R1
TEMP 3
R10
R11 ≈ 2kΩ
R2
GROUND 4

ABSOLUTE MAXIMUM RATINGS

Input Voltage
REF-05A, B 40V
Power Dissipation (see note) 500mW
Output Short-Circuit Duration
(to Ground or V_{IN}) .... Indefinite

Storage Temperature Range .... −65° C to +150° C
Lead Temperature (Soldering, 60 sec) .... 300° C
Operating Temperature Range
REF-05A, REF-05B .... −55° C to +125° C

NOTE: Derate at 7.1mW/° C above 80° C ambient temperature for TO-99 (J) package.

ELECTRICAL CHARACTERISTICS at $V_{IN} = +15V$, $T_A = 25°C$, unless otherwise noted.

			REF-05A			REF-05B			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Output Voltage	V_O	$I_L = 0$	4.985	5.0	5.015	4.975	5.0	5.025	V
Output Adjustment Range	ΔV_{trim}	$R_P = 10k\Omega$	±3	±6	—	±3	±6	—	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 1)	—	10	15	—	10	15	μV_{p-p}
Long-Term Stability		(Note 1)	—	65	100	—	65	100	ppm/1kHrs
Line Regulation (Note 2)		$V_{IN} = 8V$ to $33V$	—	0.006	0.010	—	0.006	0.010	%/V
Load Regulation (Note 2)		$I_L = 0$ to $10mA$	—	0.005	0.010	—	0.006	0.010	%/mA
Turn-On Settling Time	t_{on}	To ±0.1% of final value	—	5	—	—	5	—	μs
Quiescent Supply Current	I_{SY}	No Load	—	1	1.4	—	1	1.4	mA
Load Current	I_L		10	21	—	10	21	—	mA
Sink Current	I_S		−0.3	−0.5	—	−0.3	−0.5	—	mA
Short-Circuit Current	I_{SC}	$V_O = 0$	—	30	—	—	30	—	mA
Temperature Voltage Output	V_T	(Note 3)	—	630	—	—	630	—	mV

ELECTRICAL CHARACTERISTICS at $V_{IN} = +15V$, $-55°C \le T_A \le +125°C$ and $I_L = 0mA$, unless otherwise noted.

			REF-05A			REF-05B			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Output Voltage Change with Temperature (Notes 4 & 5)	ΔV_{OT} ΔV_{OT}	$0°C \le T_A \le +70°C$ $-55°C \le T_A \le +125°C$	— —	0.02 0.06	0.06 0.15	— —	0.07 0.18	0.17 0.45	% %
Output Voltage Temperature Coefficient	TCV_O	(Note 6)	—	3	8.5	—	10	25	ppm/° C
Change in V_O Temperature Coefficient with Output Adjustment		$R_P = 10k\Omega$	—	0.7	—	—	0.7	—	ppm/%
Line Regulation ($V_{IN} = 8V$ to $33V$) (Note 2)		$0°C \le T_A \le +70°C$ $-55°C \le T_A \le +125°C$	— —	0.007 0.009	0.012 0.015	— —	0.007 0.009	0.012 0.015	%/V %/V
Load Regulation ($I_L = 0$ to $8mA$) (Note 2)		$0°C \le T_A \le +70°C$ $-55°C \le T_A \le +125°C$	— —	0.006 0.007	0.010 0.012	— —	0.007 0.009	0.012 0.015	%/mA %/mA
Temperature Voltage Output Temperature Coefficient	TCV_T	(Note 3)	—	2.1	—	—	2.1	—	mV/° C

NOTES:

1. Sample tested. Long-term stability is tested with power applied continuously.
2. Line and Load Regulation specifications include the effect of self heating.
3. Limit current in or out of pin 3 to 50nA and capacitance on pin 3 to 30pF.
4. ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 5V.

$$\Delta V_{OT} = \left| \frac{V_{MAX} - V_{MIN}}{5V} \right| \times 100$$

5. ΔV_{OT} specification applied trimmed to +5V or untrimmed.
6. TCV_O is defined as ΔV_{OT} divided by the temperature range, i.e.,

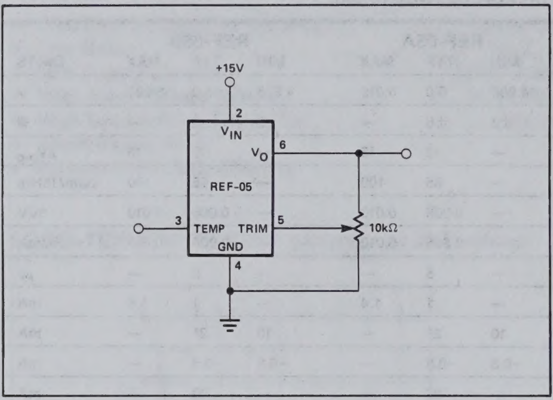
$$TCV_O = \frac{\Delta V_{OT}}{180°C}$$

OUTPUT ADJUSTMENT

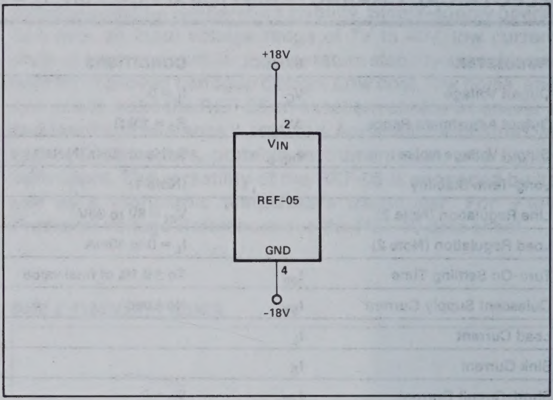
The REF-05 trim terminal can be used to adjust the output voltage over a 5V ±300mV range. This feature allows the system designer to trim system errors by setting the reference to a voltage other than 5V. Of course, the output can also be set to exactly 5V or to 5.12V for binary applications.

Adjustment of the output does not significantly affect the temperature performance of the device. Typically the temperature coefficient change is 0.7ppm/°C for 100mV of output adjustment.

OUTPUT ADJUSTMENT CIRCUIT

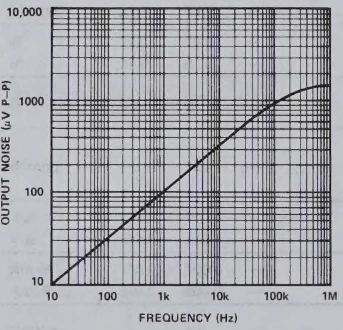


BURN-IN CIRCUIT

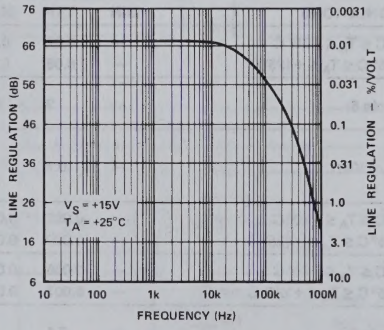


TYPICAL PERFORMANCE CHARACTERISTICS

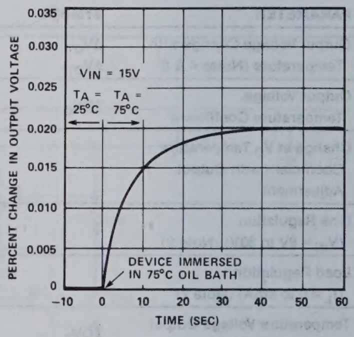
OUTPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



LINE REGULATION vs FREQUENCY

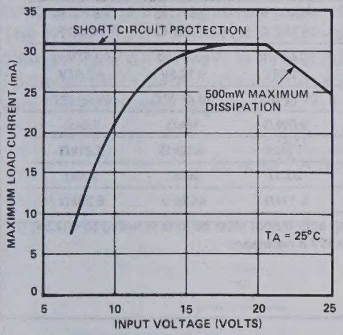


OUTPUT CHANGE DUE TO THERMAL SHOCK

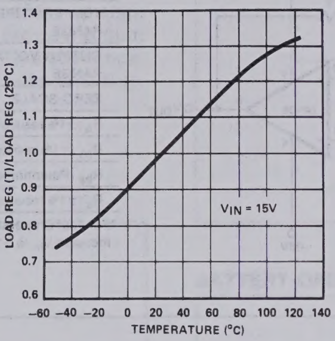


TYPICAL PERFORMANCE CHARACTERISTICS

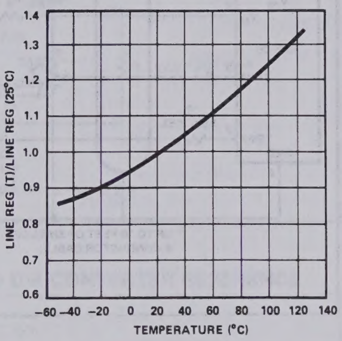
MAXIMUM LOAD CURRENT vs INPUT VOLTAGE



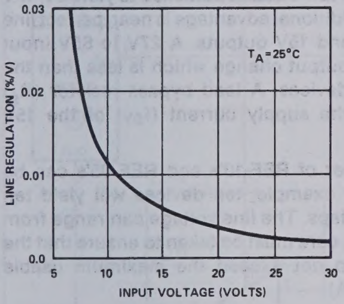
NORMALIZED LOAD REGULATION (ΔI_L = 10mA) vs TEMPERATURE



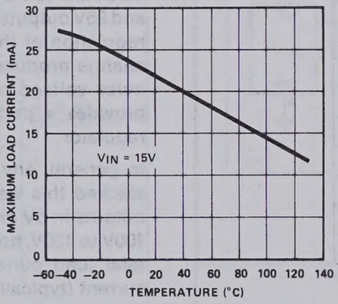
NORMALIZED LINE REGULATION vs TEMPERATURE



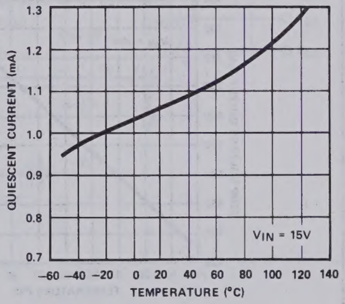
LINE REGULATION vs SUPPLY VOLTAGE



MAXIMUM LOAD CURRENT vs TEMPERATURE

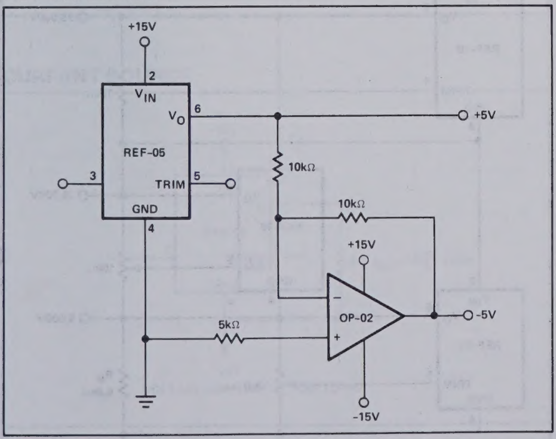


QUIESCENT CURRENT vs TEMPERATURE

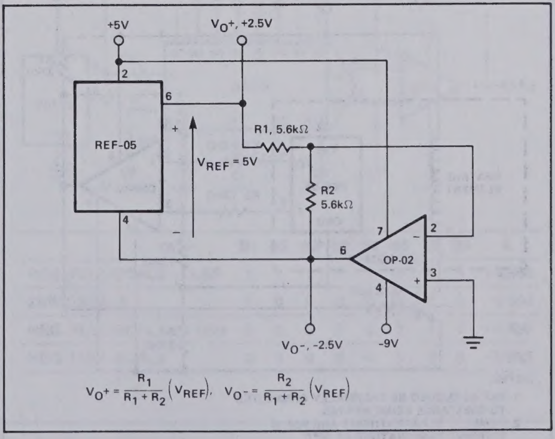


TYPICAL APPLICATIONS

±5V REFERENCE

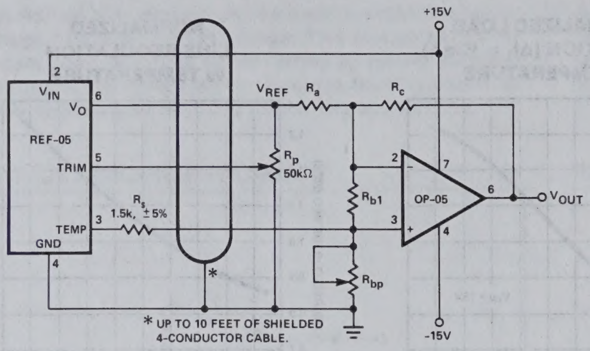

+15V
2
V_{IN}
V_O
6
REF-05
3
TRIM
5
GND
4
+5V
10kΩ
10kΩ
+15V
OP-02
−
+
-5V
5kΩ
-15V

±2.5V REFERENCE


+5V
V_O+, +2.5V
2
6
REF-05
+
V_{REF} = 5V
−
4
R1, 5.6kΩ
R2
5.6kΩ
7
2
6
OP-02
−
+
3
4
V_O−, -2.5V
-9V

$$V_{O^+} = \frac{R_1}{R_1+R_2}\left(V_{REF}\right), \quad V_{O^-} = \frac{R_2}{R_1+R_2}\left(V_{REF}\right)$$

PRECISION TEMPERATURE TRANSDUCER WITH REMOTE SENSOR


+15V
2
V_{IN}
6
V_O
REF-05
5
TRIM
R_s
1.5k, ±5%
3
TEMP
GND
4
V_{REF}
R_a
R_c
R_p
50kΩ
R_{b1}
R_{bp}
2
3
7
6
4
OP-05
V_{OUT}
-15V

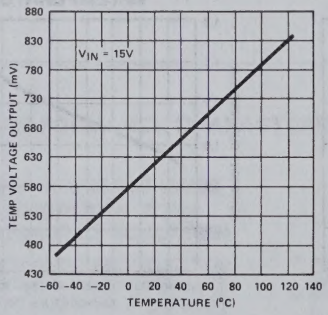
* UP TO 10 FEET OF SHIELDED 4-CONDUCTOR CABLE.

RESISTOR VALUES

TCV_{OUT} SLOPE (S)	10mV/°C	100mV/°C	10mV/°F
TEMPERATURE RANGE	−55°C to +125°C	−55°C to +125°C	−67°F to +257°F
OUTPUT VOLTAGE* RANGE	−0.55V to +1.25V	−5.5V to +12.5V	−0.67V to +2.57V
ZERO-SCALE	0V @ 0°C	0V @ 0°C	0V @ 0°F
R_a (±1% resistor)	9.09kΩ	15kΩ	7.5kΩ
R_{b1} (±1% resistor)	1.5kΩ	1.82kΩ	1.21kΩ
R_{bp} (Potentiometer)	200Ω	500Ω	200Ω
R_c (±1% resistor)	5.11kΩ	84.5kΩ	8.25kΩ

*For 125°C operation, the op amp output must be able to swing to +12.5V; increase V_{IN} to +18V from +15V if necessary.

TYPICAL TEMPERATURE VOLTAGE OUTPUT vs TEMPERATURE (REF-05A)

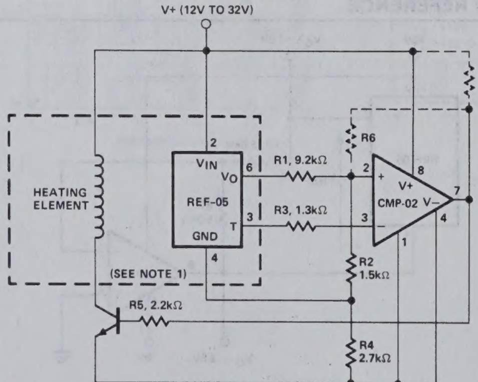


REFERENCE STACK WITH EXCELLENT LINE REGULATION

Two REF-10's and one REF-05 can be stacked to yield 5V, 15V and 25V outputs. An additional advantage is near-perfect line regulation of the 5V and 15V outputs. A 27V to 55V input change produces an output change which is less than the noise voltage of the devices. A load bypass resistor (R_g) provides a path for the supply current (I_{SY}) of the 15V regulator.

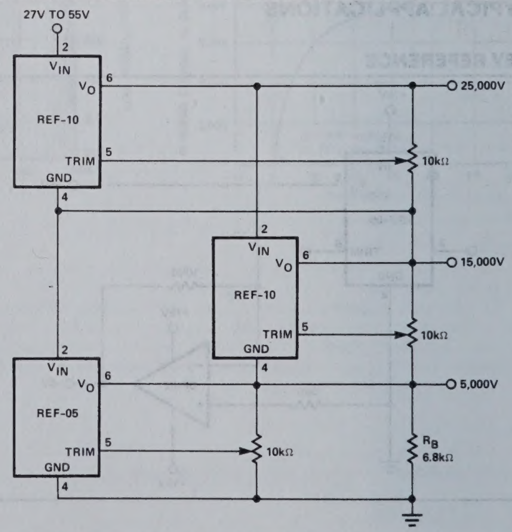
In general, any number of REF-10's and REF-05's can be stacked this way. For example, ten devices will yield ten outputs in 5V or 10V steps. The line voltage can range from 100V to 130V, however, care must be taken to ensure that the total load currents do not exceed the maximum usable current (typically 21mA).

TEMPERATURE CONTROLLER


V+ (12V TO 32V)
R7
27kΩ
R6
HEATING ELEMENT
2
V_{IN}
6
V_O
REF-05
3
T
GND
4
(SEE NOTE 1)
R1, 9.2kΩ
R3, 1.3kΩ
2
3
8
V+
CMP-02
V−
7
4
1
R2
1.5kΩ
R4
2.7kΩ
R5, 2.2kΩ

NOTES:

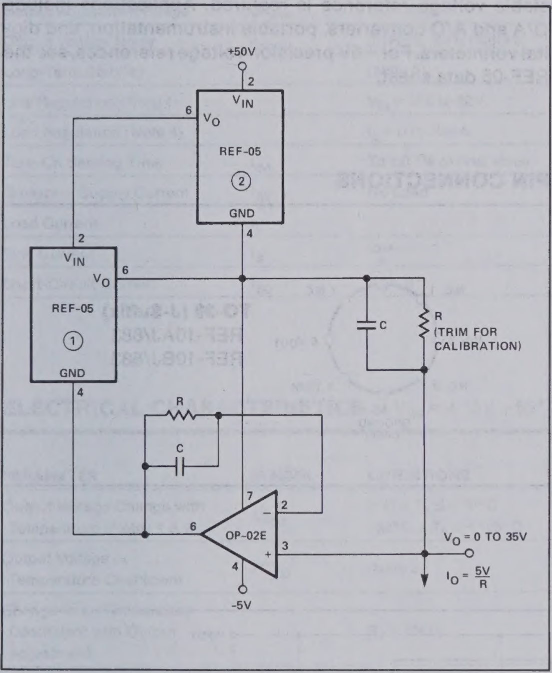
1. REF-02 SHOULD BE THERMALLY CONNECTED TO SUBSTANCE BEING HEATED.
2. NUMBERS IN PARENTHESES ARE FOR A SETPOINT TEMPERATURE OF 60°C.
3. R3 = R1||R2||R6


27V TO 55V
2
V_{IN}
6
V_O
REF-10
5
TRIM
GND
4
25,000V
10kΩ
2
V_{IN}
6
V_O
REF-10
5
TRIM
GND
4
15,000V
10kΩ
2
V_{IN}
6
V_O
REF-05
5
TRIM
GND
4
5,000V
10kΩ
R_B
6.8kΩ

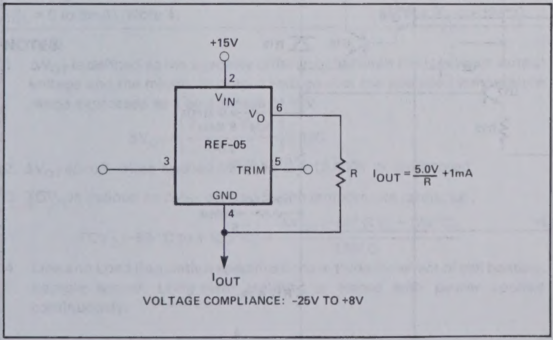
PRECISION CURRENT SOURCE

A current source with 35V output compliance and excellent output impedance can be obtained using this circuit. REF-05 ② keeps the line voltage and power dissipation constant in device ①; the only important error consideration at room temperature is the negative supply rejection of the op amp. The typical 3μV/V PSRR of the OP-02E will create a 20ppm change (3μV/V × 35V/5V) in output current over a 35V range. For example, a 5mA current source can be built (R = 1kΩ) with 350MΩ output impedance.

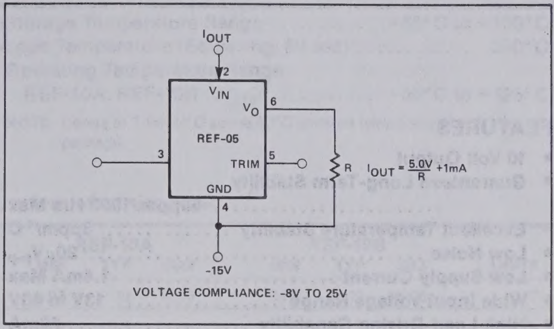
$$R_O = \frac{35V}{20 \times 10^{-6} \times 5mA}$$


+50V
2
V_{IN}
6
V_O
REF-05
②
GND
4
2
V_{IN}
6
V_O
REF-05
①
GND
4
C
R
(TRIM FOR CALIBRATION)
R
C
7
2
6
OP-02E
3
4
-5V
V_O = 0 TO 35V
$I_O = \frac{5V}{R}$

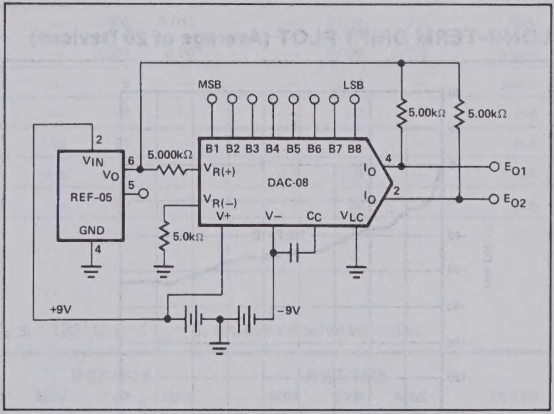
CURRENT SOURCE


+15V
2
V_{IN}
V_O
6
REF-05
3
5
TRIM
R
$I_{OUT} = \frac{5.0V}{R}$ +1mA
GND
4
I_{OUT}
VOLTAGE COMPLIANCE: -25V TO +8V

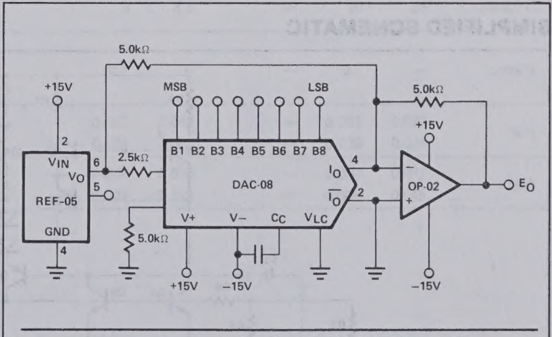
CURRENT SINK


I_{OUT}
2
V_{IN}
V_O
6
REF-05
3
5
TRIM
R
$I_{OUT} = \frac{5.0V}{R}$ +1mA
GND
4
-15V
VOLTAGE COMPLIANCE: -8V TO 25V

BATTERY-OPERATED D/A CONVERTER REFERENCE


MSB
LSB
5.00kΩ
5.00kΩ
2
V_{IN}
V_O
6
5
5.000kΩ
B1 B2 B3 B4 B5 B6 B7 B8
$V_{R(+)}$
$V_{R(-)}$
DAC-08
I_O
$\overline{I_O}$
4
2
E_{O1}
E_{O2}
REF-05
GND
4
5.0kΩ
V+
V−
CC
V_{LC}
+9V
-9V

D/A CONVERTER REFERENCE


5.0kΩ
+15V
MSB
LSB
5.0kΩ
+15V
2
V_{IN}
V_O
6
5
2.5kΩ
B1 B2 B3 B4 B5 B6 B7 B8
I_O
$\overline{I_O}$
4
2
DAC-08
OP-02
E_O
REF-05
GND
4
5.0kΩ
V+
V−
CC
V_{LC}
+15V
-15V
-15V

	B1	B2	B3	B4	B5	B6	B7	B8	E
POS. FULL-SCALE −1 LSB	1	1	1	1	1	1	1	1	+4.960
ZERO-SCALE	1	0	0	0	0	0	0	0	0.000
NEG. FULL-SCALE +1 LSB	0	0	0	0	0	0	0	1	−4.960
NEG. FULL-SCALE	0	0	0	0	0	0	0	0	-5.000

REF-10

+10V PRECISION VOLTAGE REFERENCE

(GUARANTEED LONG-TERM STABILITY)

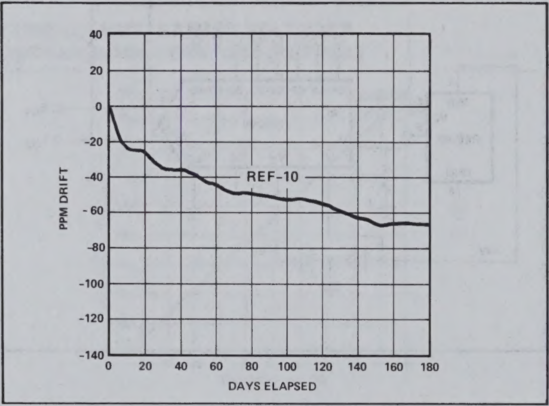
FEATURES

- **10 Volt Output**
- **Guaranteed Long-Term Stability .... 50ppm/1000 Hrs Max**
- **Excellent Temperature Stability .... 3ppm/°C**
- **Low Noise .... $20\mu V_{p-p}$**
- **Low Supply Current .... 1.4mA Max**
- **Wide Input Voltage Range .... 13V to 40V**
- **High Load-Driving Capability 20mA**
- **Short-Circuit Proof**
- **Processed Per MIL-STD-883**

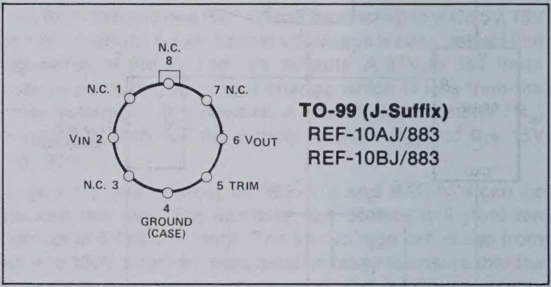
GENERAL DESCRIPTION

The REF-10 precision voltage reference provides a stable +10V output that can be adjusted over a ±3% range with minimal effect on temperature stability. Single-supply operation over an input voltage range of 13V to 40V, low current drain of 1mA, and excellent temperature stability are achieved with an improved bandgap design. Low cost, low noise, and low power make the REF-10 an excellent choice whenever a stable voltage reference is required. Applications include D/A and A/D converters, portable instrumentation, and digital voltmeters. For +5V precision voltage references, see the REF-05 data sheet.

LONG-TERM DRIFT PLOT (Average of 20 Devices)

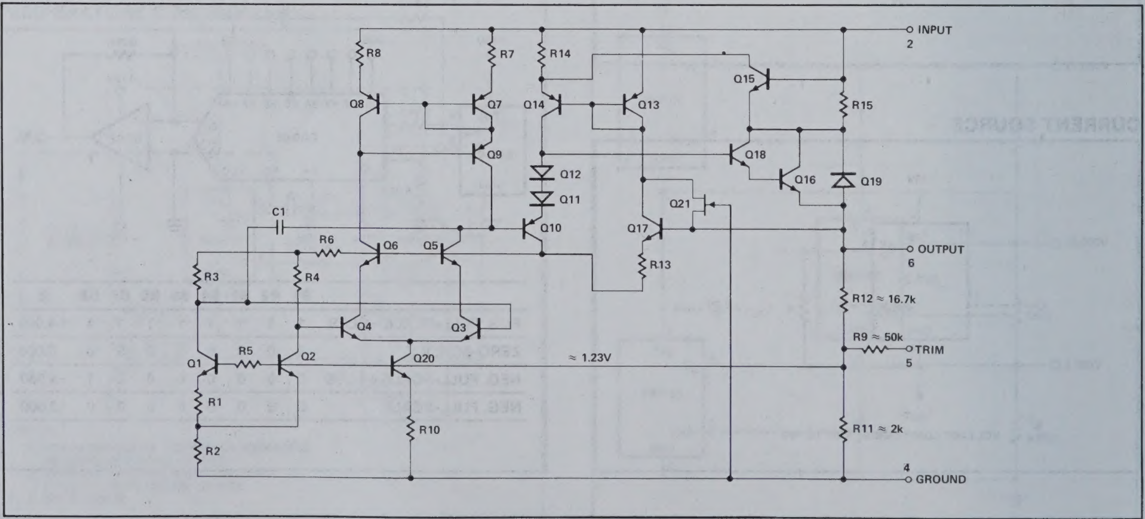


PIN CONNECTIONS


N.C. 8
N.C. 1
7 N.C.
VIN 2
6 VOUT
N.C. 3
5 TRIM
4 GROUND (CASE)

TO-99 (J-Suffix)
REF-10AJ/883
REF-10BJ/883

SIMPLIFIED SCHEMATIC


INPUT 2
R8
R7
R14
Q15
Q8
Q7
Q14
Q13
R15
Q9
Q18
Q12
Q16
Q19
Q11
Q21
C1
Q10
Q17
R6
Q6
Q5
OUTPUT 6
R3
R4
R13
R12 ≈ 16.7k
Q4
Q3
R9 ≈ 50k
TRIM 5
R5
Q1
Q2
Q20
≈ 1.23V
R1
R10
R11 ≈ 2k
R2
4 GROUND

ABSOLUTE MAXIMUM RATINGS

Input Voltage
REF-10A, B 40V
Power Dissipation (see note) 500mW
Output Short-Circuit Duration
(to Ground or V_{IN}) .... Indefinite

Storage Temperature Range .... −65° C to +150° C
Lead Temperature (Soldering, 60 sec) .... 300° C
Operating Temperature Range
REF-10A, REF-10B .... −55° C to +125° C

NOTE: Derate at 7.1mW/° C above 80° C ambient temperature for TO-99 (J) package.

ELECTRICAL CHARACTERISTICS at V_{IN} = +15V, T_A = 25° C, unless otherwise noted.

			REF-10A			REF-10B			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Output Voltage	V_O	$I_L = 0$	9.97	10	10.03	9.95	10	10.05	V
Output Adjustment Range	ΔV_{trim}	$R_P = 10k\Omega$	+3	±3.3	—	±3	±3.3	—	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 5)	—	20	30	—	20	30	μV_{p-p}
Long-Term Stability		(Note 5)	—	—	50	—	—	50	ppm/1000 Hrs
Line Regulation (Note 4)		V_{IN} = 13V to 33V	—	0.006	0.010	—	0.006	0.010	%/V
Load Regulation (Note 4)		I_L = 0 to 10mA	—	0.005	0.08	—	0.006	0.010	%/mA
Turn-On Settling Time	t_{on}	To ±0.1% of final value	—	5	—	—	5	—	μsec.
Quiescent Supply Current	I_{SY}	No Load	—	1.0	1.4	—	1.0	1.4	mA
Load Current	I_L		10	21	—	10	21	—	mA
Sink Current	I_S		−0.3	−0.5	—	−0.3	−0.5	—	mA
Short-Circuit Current	I_{SC}	$V_O = 0$	—	30	—	—	30	—	mA

ELECTRICAL CHARACTERISTICS at V_{IN} = +15V, −55° C ≤ T_A ≤ +125° C and $I_L = 0$, unless otherwise noted.

			REF-10A			REF-10B			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Output Voltage Change with Temperature (Notes 1 & 2)	ΔV_{OT}	0° C ≤ T_A ≤ +70° C −55° C ≤ T_A ≤ +125° C	— —	0.02 0.06	0.06 0.15	— —	0.07 0.18	0.17 0.45	%
Output Voltage Temperature Coefficient	TCV_O	(Note 3)	—	3	8.5	—	10	25	ppm/° C
Change in V_O Temperature Coefficient with Output Adjustment		$R_P = 10k\Omega$	—	0.7	—	—	0.7	—	ppm/%
Line Regulation (V_{IN} = 13V to 33V) (Note 4)		0° C ≤ T_A ≤ +70° C −55° C ≤ T_A ≤ +125° C	— —	0.007 0.009	0.012 0.015	— —	0.007 0.009	0.012 0.015	%/V
Load Regulation (I_L = 0 to 8mA) (Note 4)		0° C ≤ T_A ≤ +70° C −55° C ≤ T_A ≤ +125° C	— —	0.006 0.007	0.010 0.012	— —	0.007 0.009	0.012 0.015	%/mA

NOTES:

1. ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 10V.

$$\Delta V_{OT} = \left| \frac{V_{MAX} - V_{MIN}}{10V} \right| \times 100$$

2. ΔV_{OT} specification applied trimmed to +10.000V or untrimmed.
3. TCV_O is defined as ΔV_{OT} divided by the temperature range, i.e.,

$$TCV_O\,(-55°\,C \text{ to } +125°\,C) = \frac{\Delta V_{OT}\,(-55°\,C \text{ to } +125°\,C)}{180°\,C}$$

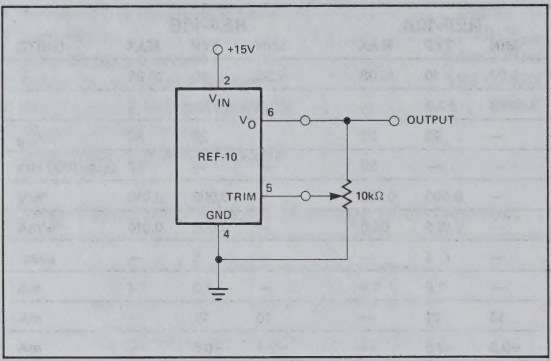
4. Line and Load Regulation specifications include the effect of self heating.
5. Sample tested. Long-term stability is tested with power applied continuously.

OUTPUT ADJUSTMENT

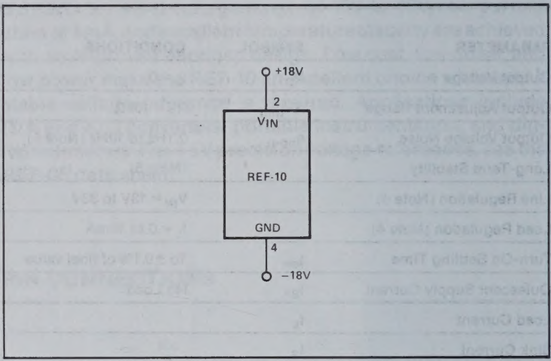
The REF-10 trim terminal can be used to adjust the output voltage over a 10V ±300mV range. This feature allows the system designer to trim system errors by setting the reference to a voltage other than 10V. Of course, the output can also be set to exactly 10.000V.

Adjustment of the output does not significantly affect the temperature performance of the device. Typically, the temperature coefficient change is 0.7ppm/° C per 100mV of output adjustment.

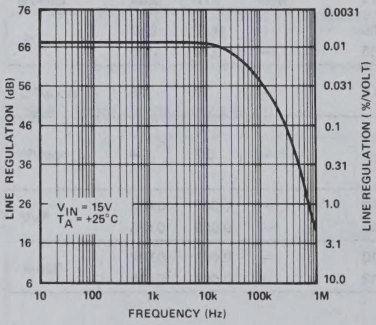
OUTPUT ADJUSTMENT CIRCUIT

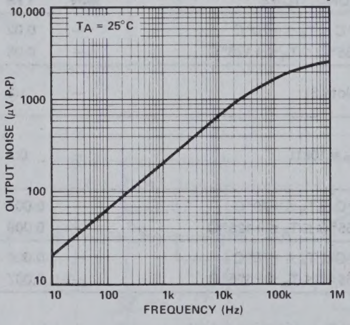


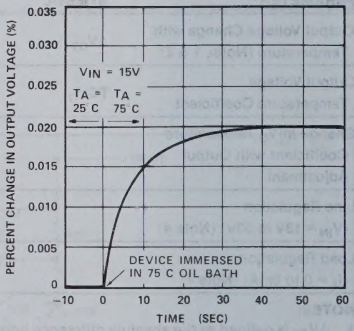
BURN-IN CIRCUIT



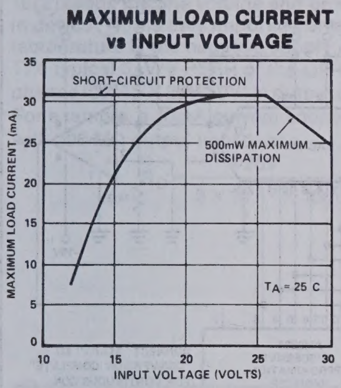
TYPICAL PERFORMANCE CHARACTERISTICS

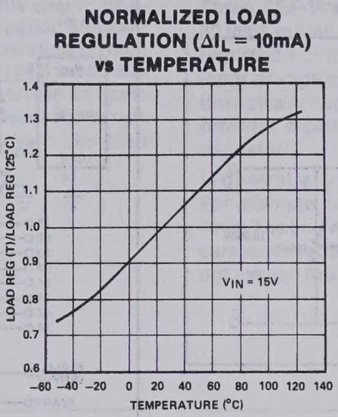

LINE REGULATION vs FREQUENCY

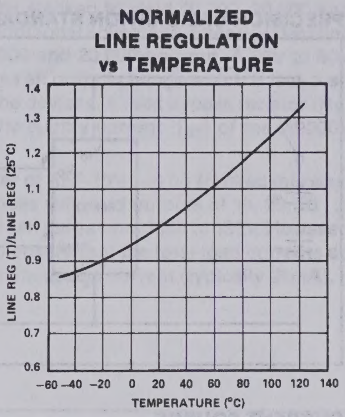

OUTPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)

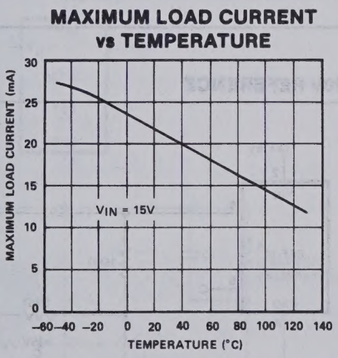

OUTPUT CHANGE DUE TO THERMAL SHOCK

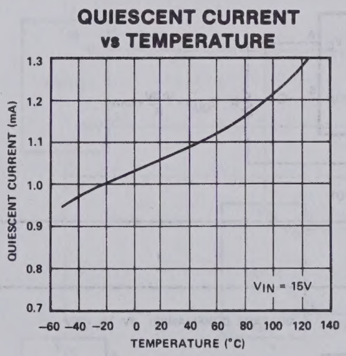
TYPICAL PERFORMANCE CHARACTERISTICS


MAXIMUM LOAD CURRENT vs INPUT VOLTAGE


NORMALIZED LOAD REGULATION (ΔI_L = 10mA) vs TEMPERATURE

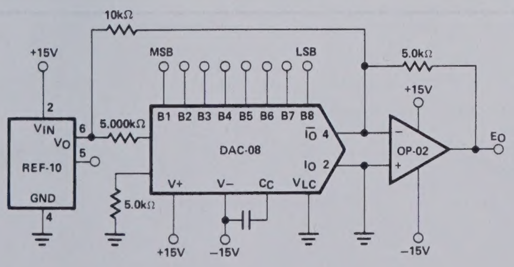

NORMALIZED LINE REGULATION vs TEMPERATURE


MAXIMUM LOAD CURRENT vs TEMPERATURE


QUIESCENT CURRENT vs TEMPERATURE

TYPICAL APPLICATIONS

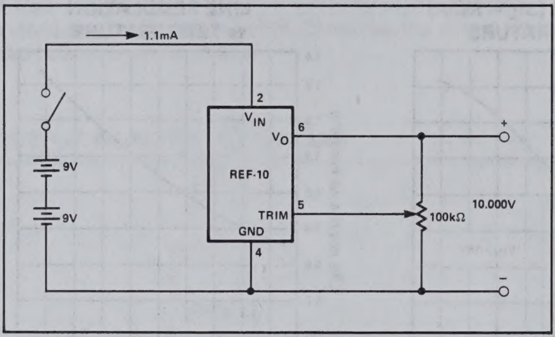
D/A CONVERTER REFERENCE


10kΩ
+15V
MSB
LSB
5.0kΩ
+15V
2
V_{IN}
V_O
6
5.000kΩ
5
REF-10
GND
4
B1 B2 B3 B4 B5 B6 B7 B8
DAC-08
$\overline{I_O}$ 4
I_O 2
V+
V−
C_C
V_{LC}
5.0kΩ
+15V
−15V
OP-02
−
+
E_O
−15V

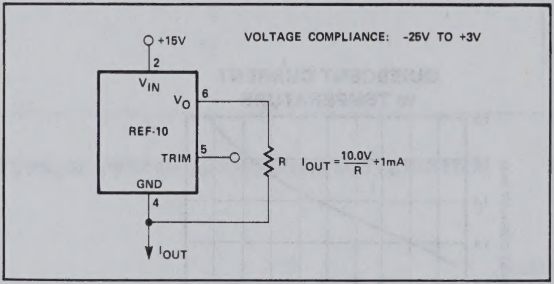
	B1	B2	B3	B4	B5	B6	B7	B8	E
POS FULL-SCALE − 1LSB	1	1	1	1	1	1	1	1	+4.960
ZERO-SCALE	1	0	0	0	0	0	0	0	0.000
NEG FULL-SCALE + 1LSB	0	0	0	0	0	0	0	1	−4.960
NEG FULL-SCALE	0	0	0	0	0	0	0	0	−5.000

TYPICAL APPLICATIONS

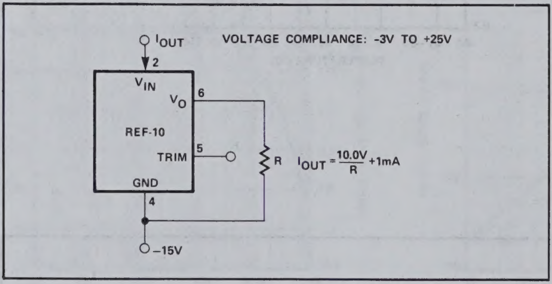
PRECISION CALIBRATION STANDARD


1.1mA
9V
9V
2
VIN
VO
6
REF-10
TRIM
5
GND
4
+
10.000V
100kΩ
−

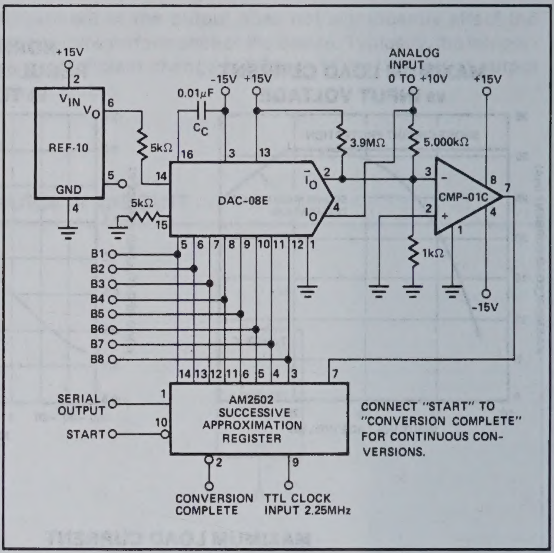
CURRENT SOURCE


+15V
VOLTAGE COMPLIANCE: -25V TO +3V
2
VIN
VO
6
REF-10
5
TRIM
GND
4
R
$I_{OUT} = \frac{10.0V}{R} + 1mA$
IOUT

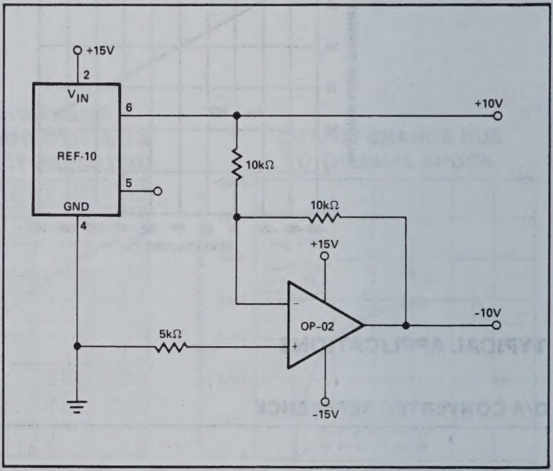
CURRENT SINK


IOUT
VOLTAGE COMPLIANCE: -3V TO +25V
2
VIN
VO
6
REF-10
5
TRIM
GND
4
R
$I_{OUT} = \frac{10.0V}{R} + 1mA$
−15V

A/D CONVERTER REFERENCE


+15V
2
VIN
VO
6
REF-10
GND
4
5
5kΩ
0.01µF
CC
−15V
+15V
16
3
13
14
DAC-08E
IO
IO
2
4
5kΩ
15
3.9MΩ
ANALOG INPUT 0 TO +10V
+15V
5.000kΩ
3
2
CMP-01C
8
7
4
1
1kΩ
−15V
B1
B2
B3
B4
B5
B6
B7
B8
5 6 7 8 9 10 11 12 1
14 13 12 11 6 5 4 3
7
SERIAL OUTPUT
1
START
10
AM2502 SUCCESSIVE APPROXIMATION REGISTER
2
9
CONVERSION COMPLETE
TTL CLOCK INPUT 2.25MHz
CONNECT "START" TO "CONVERSION COMPLETE" FOR CONTINUOUS CONVERSIONS.

±10V REFERENCE


+15V
2
VIN
6
REF-10
5
GND
4
+10V
10kΩ
10kΩ
+15V
−
OP-02
+
−10V
5kΩ
−15V

PRECISION CURRENT SOURCE

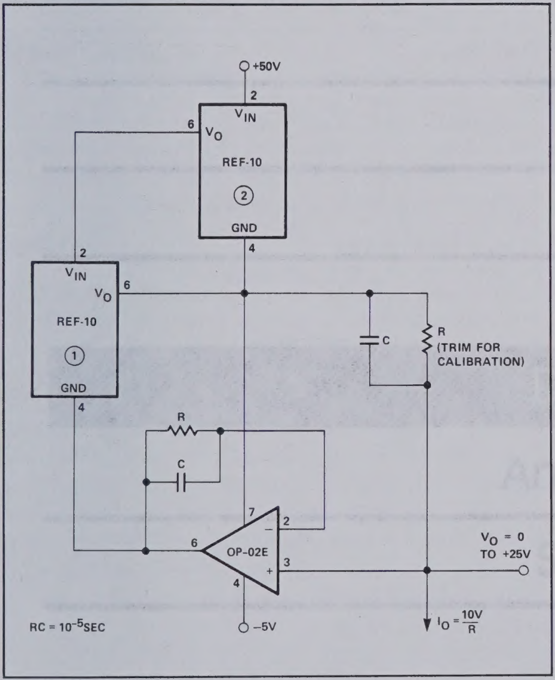
A current source with 25V output compliance and excellent output impedance can be obtained using this circuit. REF-10② keeps the line voltage and power dissipation constant in device①; the only important error consideration at room temperature is the negative supply rejection of the op amp. The typical 3μV/V PSRR of the OP-02E will create an 8ppm change (3μV/V × 25V/10V) in output current over a 25V range. For example, a 10mA current source can be built (R = 1kΩ) with 300 MΩ output impedance.

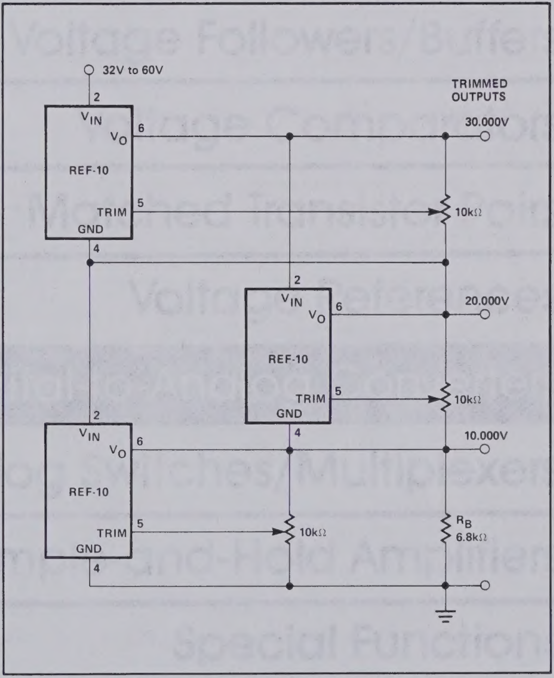
$$R_O = \frac{25V}{8 \times 10^{-6} \times 10mA}$$

REFERENCE STACK WITH EXCELLENT LINE REGULATION

Three REF-10's can be stacked to yield 10.000, 20.000 and 30.000V outputs. An additional advantage is near-perfect line regulation of the 10.000 and 20.000V output. A 32V to 60V input change produces an output change which is less than the noise voltage of the devices. A load bypass resistor (R_B) provides a path for the supply current (I_{SY}) of the 20.000V regulator.

In general, any number of REF-10's can be stacked this way. For example, ten devices will yield outputs of 10, 20, 30 . . . 100V. The line voltage can range from 105V to 130V. However, care must be taken to ensure that the total load currents do not exceed the maximum usable current (typically 21mA).


+50V
2
6
VIN
VO
REF-10
②
GND
4
2
VIN
VO
6
REF-10
①
GND
4
C
R
(TRIM FOR CALIBRATION)
R
C
7
2
6
OP-02E
3
4
VO = 0 TO +25V
IO = 10V/R
RC = 10⁻⁵SEC
–5V


32V to 60V
2
VIN
VO
6
REF-10
TRIM
5
GND
4
TRIMMED OUTPUTS
30.000V
10kΩ
2
VIN
VO
6
20.000V
REF-10
TRIM
5
GND
4
10kΩ
2
VIN
VO
6
10.000V
REF-10
TRIM
5
GND
4
10kΩ
RB
6.8kΩ

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Two's-Complement 10-Bit Voltage-Output D/A Converter

DAC-08 11-26
8-Bit High-Speed Multiplying D/A Converter

DAC-10 11-37
10-Bit High-Speed Multiplying D/A Converter

DAC-20 11-45
2-Digit BCD High-Speed Multiplying D/A Converter

DAC-86 11-53
COMDAC® Companding D/A Converter

DAC-88 11-61
COMDAC® Companding D/A Converter

DAC-89 11-70
COMDAC® Companding D/A Converter

DAC-100 11-79
10-Bit Current-Output D/A Converter

DAC-208 11-87
9-Bit Voltage-Output D/A Converter

DAC-210 11-91
11-Bit Voltage-Output D/A Converter

DAC-312 11-95
12-Bit High-Speed Multiplying D/A Converter

DAC-808 11-107
BYTEDAC® 8-Bit High-Speed "Microprocessor Compatible" Multiplying D/A Converter

DAC-888 11-118
BYTEDAC® 8-Bit High-Speed "Microprocessor Compatible" Multiplying D/A Converter

DAC-1508A/1408A 11-130
8-Bit Multiplying D/A Converters

PM-562 11-136
12-Bit Multiplying D/A Converter

JM-38510/11301/11302 11-140
JAN 8-Bit Multiplying D/A Converter

D/A CONVERTERS

INTRODUCTION

A D/A converter accepts a digital input and produces an analog output. The basic DAC consists of a voltage or current reference, binary weighted precision resistors, a set of electronic switches and a means of summing the weighted currents.

Three important criteria for selecting a good DAC are accuracy, speed and resolution. Other essential requirements to be considered are temperature stability, input coding, output format, reference requirements and power consumption.

PMI DACs use bipolar transistor technology. Some of the advantages these DACs offer are:

1. Bipolar technology allows a stable internal zener reference to be fabricated monolithically.
2. Reference servoed NPN current source transistors give high compliance, temperature stable outputs.
3. The bipolar transistor switches provided on PMI DACs have faster settling times than their FET counterparts.

DACs can be categorized by the type of analog output — a current or a voltage. "Complete" DACs have an on-board reference source, R-2R ladder network and current-to-voltage converting op amp on one monolithic IC. "Multiplying" DACs have access to the reference input pin allowing the user to multiply an analog quantity by a digital number.

Since introducing the first monolithic D/A converter in 1970, PMI has continually improved and updated its DAC line. PMI offers an extensive choice of DAC resolutions, coding formats, output configurations and temperature ranges. All of these products are characterized by high speed and temperature stable performance. Wide dynamic range and good zero resolution are offered by PMI's "companding" (compressing/expanding) D/A converter, the COMDAC®, in applications where a high-resolution linear DAC is not needed.

The selection guides following the definitions will aid you in quickly locating the appropriate DAC for your application.

DEFINITIONS— LINEAR DIGITAL-TO-ANALOG CONVERTERS

If the DAC output is a linear function of the digital input, the DAC is called a linear DAC. Otherwise it is called a nonlinear DAC. Most DACs are linear. The following definitions apply to linear DACs.

Absolute Accuracy — The absolute accuracy of a DAC is the difference between the actual *unadjusted* analog output and the ideal output that is expected when a *given* digital code is applied. Sources of error include full-scale error, zero-scale error, nonlinearity errors, and the drift of all these. Therefore, absolute accuracy includes all deviations from the ideal.

The absolute accuracy is usually specified at full-scale and at zero. The corresponding errors are called full-scale error (or gain error) and zero-scale error (or offset error). These errors are usually expressed in LSBs, % FSR, or in units of voltage or current.

Accuracy — Accuracy is the deviation of the actual unadjusted output of the DAC from the ideal output. It includes gain errors and offset errors. As shown in Figure 11.1, offset errors shift the transfer characteristic up or down the output axis and gain errors rotate it about the origin.

Relative Accuracy — Relative accuracy is the data converter specification that has the greatest variety of definitions from different manufacturers. Relative accuracy is the deviation of the analog output at any code from its ideal value after full-scale and zero-scale errors have been

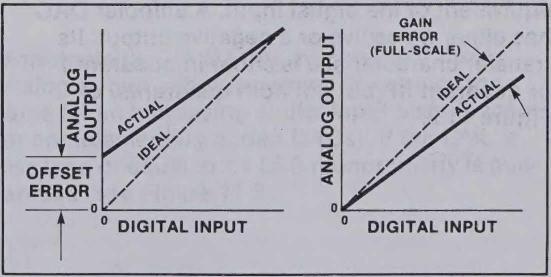


Figure 11.1 Gain and Offset Error Defined

calibrated out. Since the ideal discrete analog output values of a linear DAC corresponding to the digital input values lie on a straight line between zero and the ideal full-scale output, the relative accuracy of a DAC can be interpreted as a measure of integral nonlinearity. It is usually expressed in LSBs or % FSR.

It does NOT include gain errors or offset errors, which have been calibrated.

BCD — The abbreviation BCD stands for binary coded decimal. It is a binary code used to represent decimal numbers in which the digits 0 through 9 are coded using the 4-bit binary 8-4-2-1 code.

Binary — In the binary number system each digit can have one of two values; either zero or one. A binary number is represented in the positional notation system as:

$$N = A_n 2^n + A_{n-1} 2^{n-1} + \cdots + A_1 2^1 + A_0 2^0.$$

Where n = number of bits of resolution
A_n = zero or one

The least significant bit (LSB) usually appears rightmost and the most significant bit (MSB) leftmost. Note that the maximum value that can be represented by an n-bit binary number is $2^n - 1$.

Bit — The unit of binary information. It can have the value of zero or one.

Bipolar DAC — When the analog signal range includes both positive and negative values the system is said to be bipolar. The transfer characteristic of an ideal bipolar DAC is shown in Figure 11.2. The analog output consists of a series of discrete points that correspond to the analog equivalent of the digital input. A unipolar DAC has either a positive or a negative output. Its transfer characteristic is either in quadrant I or quadrant III (but not both quadrants) of Figure 11.2.

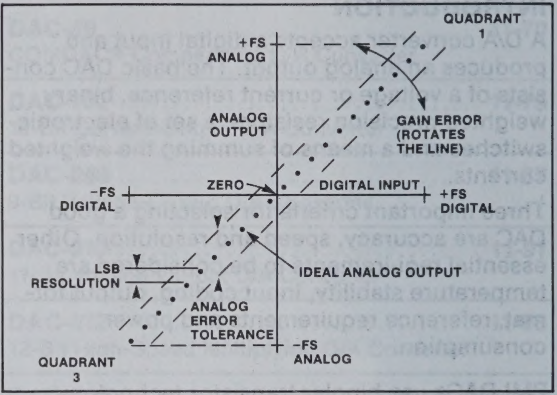

QUADRANT 1
+FS ANALOG
ANALOG OUTPUT
GAIN ERROR (ROTATES THE LINE)
ZERO
DIGITAL INPUT
−FS DIGITAL
+FS DIGITAL
LSB RESOLUTION
IDEAL ANALOG OUTPUT
ANALOG ERROR TOLERANCE
QUADRANT 3
−FS ANALOG

Figure 11.2 Bipolar D/A Converter

Differential Nonlinearity (DNL) — Differential nonlinearity is defined as the maximum deviation of the analog output between any two adjacent output states from the ideal 1 LSB step size. If the digital input code to a DAC is changed from its present code to either the next higher code or to the next lower code the analog output of an ideal DAC will increase or decrease by an amount of current or voltage equal to one LSB. The deviation of the actual "step size" from the ideal step size of 1 LSB is called differential nonlinearity error or DNL. DACs with DNL greater than ±1 LSB may be nonmonotonic. Maximum DNL error has an upper bound of twice the NL, but it can be less. This is illustrated in Figure 11.3.

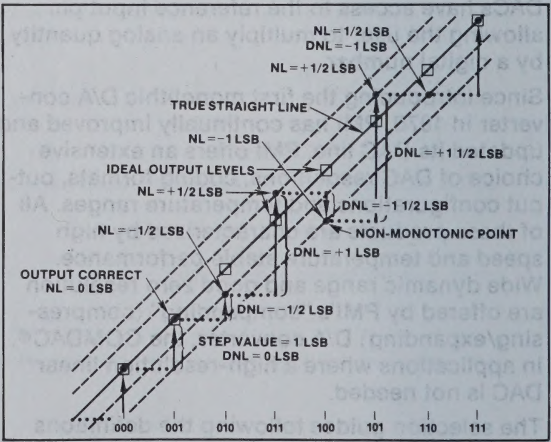

NL = 1/2 LSB
DNL = −1 LSB
NL = +1/2 LSB
TRUE STRAIGHT LINE
NL = −1 LSB
DNL = +1 1/2 LSB
IDEAL OUTPUT LEVELS
NL = +1/2 LSB
DNL = −1 1/2 LSB
NL = −1/2 LSB
NON-MONOTONIC POINT
DNL = +1 LSB
OUTPUT CORRECT
NL = 0 LSB
DNL = −1/2 LSB
STEP VALUE = 1 LSB
DNL = 0 LSB
000
001
010
011
100
101
110
111

Figure 11.3 Nonlinearity (NL) and Differential Nonlinearity (DNL)

Dynamic Range (DR) — The dynamic range of a DAC is the ratio of the largest output to the smallest output (excluding zero) expressed in decibels (dB). For linear DACs this ratio is 2^n, where n = number of bits of resolution.

$$\text{DR (in dB)} = 20 \text{ Log}_{10} 2^n$$

Errors — The performance of a DAC is determined by measuring the deviation of the actual analog output from the ideal expected output. In general, the adjustable analog output errors are full-scale or gain error and offset or zero-scale error. Nonadjustable errors include nonlinearity, differential nonlinearity, zero-scale symmetry, zero and full-scale temperature drift coefficients and power-supply sensitivity. The most meaningful nonadjustable error term is NONLINEARITY. The next most important nonadjustable error terms are full-scale drift and differential nonlinearity. A DAC that has a specified maximum nonlinearity of ±1/2 LSB over temperature will also be guaranteed to be monotonic. PMI specifies maximum nonlinearity over temperature for every DAC (except the DAC-03) to assure the designer of precision performance for the most demanding applications.

Full Scale (FS) — The full-scale output of a DAC is the maximum voltage or current that can be obtained from it. For a (natural) binary DAC the full-scale output occurs when the digital inputs are all ones. For an n-bit DAC the full-scale output will be $(2^n - 1)/2^n$ times the full-scale range (FSR, see definition).

Full-Scale Range (FSR) — The full-scale range of an n-bit DAC is that value which is divided into 2^n parts to determine the value of the LSB. The DAC output can never reach the full-scale range because the full-scale output will always be one LSB less than the full-scale range.

Functional Compliance — The functional compliance of a DAC is the voltage range over which the current output can be driven and for which the DAC output current will maintain the same relative accuracy (the output can change absolutely).

True Compliance — The true compliance of a DAC is the voltage range over which the current output can vary while the DAC maintains an absolute accuracy of ±1/2 LSB. The higher the DAC output impedance the better the voltage compliance will be.

Gain Drift — The variation of the full-scale value (voltage or current) is measured over the operating temperature range and is called gain drift. The gain drift is divided by the temperature range over which it is measured and expressed in PPM per degree centigrade.

Gain Error — The difference between the actual analog output range and the ideal analog output range expressed as a percent of full-scale or in terms of LSB value (see Figure 11.1) is called the gain error.

Glitch — A glitch is a switching transient appearing in the output during a code transition. Its value is expressed in volts (V × ns) or current (mA × ns) and time duration or in charge transferred (in Picocoulombs).

Least Significant Bit (LSB) — The analog value of the LSB is the smallest change that can occur in the output of a DAC. It corresponds to a one bit change in the binary input.

$$\text{LSB (Analog Value)} = \frac{\text{FSR}}{2^n} \left[\begin{array}{l}\text{Expressed in} \\ \text{Voltage or Current}\end{array}\right]$$

Where FSR = Full-Scale Range
n = number of bits

Most Significant Bit (MSB) — The analog value of the MSB is the largest incremental output change obtainable by switching a single input bit.

$$\text{MSB (Analog Value)} = \frac{\text{FSR}}{2} \left[\begin{array}{l}\text{Expressed in} \\ \text{Voltage or Current}\end{array}\right]$$

Monotonicity — A DAC is monotonic if the analog output either increases or remains the same for an increasing digital input code (except for complementary coded DACs). If the DNL is less than or equal to ±1 LSB monotonicity is guaranteed (see Figure 11.3).

Multiplying DACs — The DAC multiplies an analog reference by a digital word. Some DACs can multiply only positive digital words by a positive reference. This is known as single quadrant (quadrant I, see Figure 11.4) operation. Two quadrant operation (quadrants I and III) can be performed by a DAC that usually operates in quadrant I by offsetting it by a negative MSB (1/2 of FSR) so that the MSB becomes the sign bit.

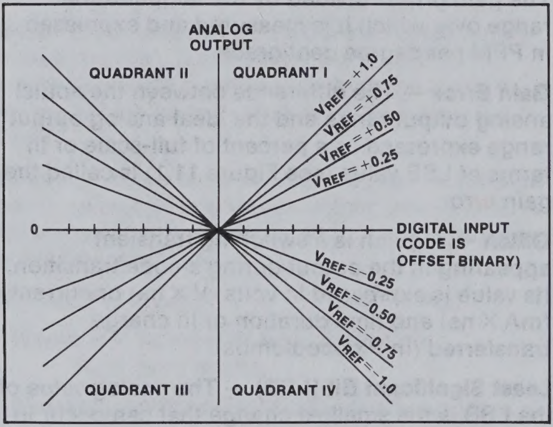


Figure 11.4 DAC Transfer Curves

Nonlinearity (NL) or Integral Nonlinearity (INL) — This is the single most important DAC specification. PMI measures NL as the maximum deviation of the analog output (from the ideal) from a straight line drawn between the end points, expressed as a percent of full-scale range or in terms of LSBs.

Another method of specifying NL is by using a "best fit" straight line through the transfer characteristic and manipulating the line such that there are "approximately equal" maximum positive and negative deviations from the line. These two methods are illustrated in Figure 11.5 and it can be seen that the "best fit" method minimizes the error. This means that the end-point definition is a worst case method of specifying NL. Again, PMI uses end-point measurement to provide the user with the most conservative rating.

For DACs, a specification of ±1/2 LSB NL (by either definition) guarantees monotonicity and ±1 LSB maximum differential nonlinearity.

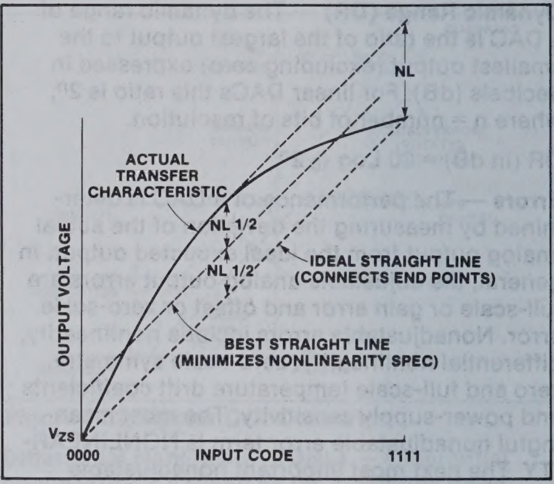


Figure 11.5 Nonlinearity

Offset Drift — The variation of the zero-scale offset (voltage or current) is measured over the operating temperature range and is called offset drift. The offset drift is divided by the temperature range over which it is measured and expressed in PPM per degree centigrade.

Output Resistance — Output resistance is the equivalent internal resistance for a current output D/A Converter as seen at its output. It is measured as the change in output current ΔI with the change in output voltage ΔV and, as such, is a direct measure of the true output voltage compliance.

Besides the compliance consideration, low output resistance can lead to V_{OS} drift problems when used with a current-to-voltage converting amplifier. In this case, the DAC output resistance forms a gain setting resistive divider with the feedback resistor, which effectively amplifies V_{OS} drift by the factor $\left(\frac{R_F}{R_0}+1\right)$.

Power Supply Sensitivity — The change in the output of the converter due to a change in the power supply value is called the power supply sensitivity. This may be expressed as a percent of full-scale range per one percent change in the power supply or as a percent of full-scale per volt of power supply change. Normally this is specified at DC, it is sometimes specified over a given frequency range.

Resolution — The resolution of a DAC is the number of states (2^n) that the FSR is divided (or resolved) into, where n is equal to the number of bits.

Settling Time — Settling time is the elapsed time for the analog output to reach its final value within a specified error band after the corresponding digital input code has been changed. It is usually specified for a full-scale change and measured from the 50% point of the logic input change to the time the output reaches its final value within the specified error band. See Figure 11.6.

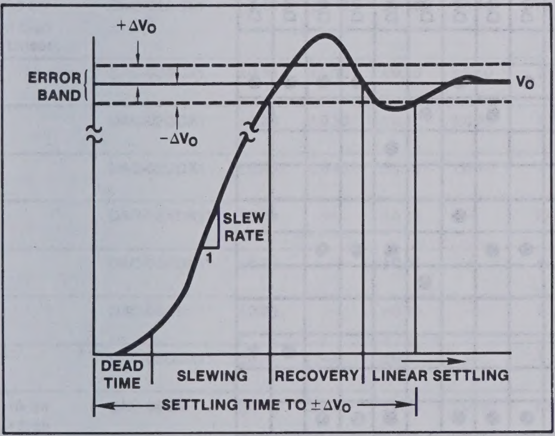


Figure 11.6 Settling Time Measurement

Zero-Scale Or Offset Error (ZS) — The zero-scale error is the error at analog zero for a data converter operating in the unipolar mode.

Zero-Scale Symmetry Error — This definition applies only to sign-magnitude DACs. It is the change in the analog output produced by switching the sign bit with a zero code input to the magnitude bits. It is expressed in units of voltage, current, or in fractions of an LSB.

DEFINITIONS—COMPANDING DACs

The companding (COMDAC®) DACs that PMI manufactures are the DAC-86, DAC-88, and the DAC-89. They are constructed such that the more significant bits of the digital input have a larger than binary relationship to the less significant bits. This decreases the resolution of the more significant bits, which increases the analog signal range. The effect of this is to compress more data into the more significant bits.

Chord — The mathematical formula describing the DAC transfer function is implemented by performing a piecewise linear approximation of the function. The straight line segments used in the approximation are called chords.

Chord Endpoints — The digital code corresponding to the maximum analog output for a given chord is called the chord endpoint.

Dynamic Range (DR) — The dynamic range of a DAC is the ratio of the largest output to the smallest output (excluding zero) expressed in decibels (dB). For the COMDACs® this would be output ($I_{7,\,15}$) divided by output ($I_{0,\,1}$). This is then converted to dB using the formula:

$$DR = 20\ \mathrm{Log}_{10}\left(\frac{I_{7,\,15}}{I_{0,\,1}}\right)\ (\mathrm{dB})$$

Encode Current — The encode current is the difference between $I_{OE\,(+)}$ and $I_{OD\,(+)}$ or the difference between $I_{OE\,(-)}$ and $I_{OD\,(-)}$ at any code.

Full-Scale Symmetry Error — The full-scale symmetry error of a DAC is the difference between the maximum and the minimum analog output values. For the COMDACs® this is the difference between $I_{OD\,(-)}$ and $I_{OD\,(+)}$ or $I_{OE\,(+)}$ and $I_{OE\,(-)}$.

Output-Level Notation — Each output current level may be designated by the digital input code as $I_{C,S}$; where c = chord number and s = step number. For example, $I_{0,0}$ = zero scale current; $I_{0,1}$ = first step from zero; $I_{0,15}$ = endpoint of the first chord (C_0); and $I_{7,15}$ = full-scale current.

Steps — Each chord is divided into equal increments called steps.

Step Nonlinearity — This is the deviation of the actual step size from the ideal step size within a chord. In a linear DAC it corresponds to differential nonlinearity.

D/A CONVERTERS

DIGITAL-TO-ANALOG CONVERTER SELECTION GUIDE

PMI offers a complete line of digital-to-analog converters (DACs), all which are guaranteed to be monotonic over their operating temperature ranges, and some which have become industry standards. The DACs have been arranged in a matrix which highlights their primary characteristics so that the user can easily narrow the selection according to specific requirements. More detailed specifications are then tabulated in each product group.

	Voltage Output						Current Output								
												µP Comp.		Companding	
	DAC-01	DAC-02, DAC-03	DAC-05	DAC-06	DAC-208	DAC-210	DAC-08	DAC-10	DAC-20	DAC-100	DAC-312	DAC-808	DAC-888	DAC-86	DAC-88, DAC-89
Resolution															
6-Bits	●														
8-Bits					●		●		●			●	●	●	●
10-Bits		●	●	●		●		●		●					
12-Bits											●				
Input Coding															
BCD									●						
Binary							●	●			●	●	●		
Complementary Binary	●									●					
Sign Magnitude		●	●		●	●									
Companding														●	●
Two's Complement				●											
Complementary Current Outputs							●	●	●		●	●	●		
Internal Reference	●	●	●	●	●	●				●					
Logic Threshold Control							●	●	●		●			●	●
JAN Qualified							●								
Operating Temp. Range															
Military	●		●	●	●	●	●	●		●	●	●	●		
Industrial										●		●		●	●
Commercial	●	●	●	●	●	●	●	●	●	●	●	●	●	●	

DAC SELECTION GUIDE

Voltage Output — Commercial Temperature Range (0° C to 70° C)

All specifications are minimum or maximum ratings unless otherwise indicated.

Resolution	PMI Part Number	Nonlinearity (% F.S.)		Zero-Scale Offset (% F.S.)		Monotonicity (Bits)		Gain T.C. (PPM/° C)		Settling Time (μs)	Output Voltage Range	Power Dissipation (mW)	Codes
		25° C	0° C to 70° C	25° C	0° C to 70° C	25° C	0° C to 70° C	Int. Ref.	Ext. Ref.				
6-Bit Linear	DAC-01CY	±0.40	±0.45	±0.25 typ	±0.25 typ	6	6	±160	—	3.0	±10V to ±11.89V	250	Complement Binary
	DAC-01HY	±0.40	±0.45	±0.40 typ	±0.40	6	6	±160	—	3.0	±10V to ±11.89V	250	Complement Binary
	DAC-01DY	±0.78	±0.78	±0.50 typ	±0.50	6	6	±160	—	3.0	±10V to ±11.89V	250	Complement Binary
8-Bit +Sign Linear	DAC-208EX	±0.1	±0.1	±0.1	±0.15	8	8	±40	±15 typ	0.75 typ	+5V or ±10V	290	Sign Magnitude
	DAC-208FX	±0.2	±0.2	±0.1	±0.1	8	8	±60	±30 typ	0.75 typ	+5V or ±10V	290	Sign Magnitude
10-Bit +Sign Linear	DAC-02ACX1	±0.10	±0.10	±0.10	±0.10	10	10	±60	±30 typ	2.0 typ	±10V to ±11.5V	300	Sign Magnitude
	DAC-02BCX1	±0.10	±0.10	±0.10	±0.10	9	9	±60	±30 typ	2.0 typ	±10V to ±11.5V	300	Sign Magnitude
	DAC-02CCX1	±0.20	±0.20	±0.10	±0.10	8	8	±60	±30 typ	2.0 typ	±10V to ±11.5V	300	Sign Magnitude
	DAC-02DDX1	±0.40	±0.40	±0.10	±0.10	7	7	±150	±30 typ	2.0 typ	±10V to ±11.5V	350	Sign Magnitude
	DAC-03ADX1*	±0.10	—	±0.10	—	10	—	±60 typ	±40 typ	2.0 typ	+10V to +11.5V	350	Natural Binary
	DAC-03BDX1*	±0.10	—	±0.10	—	9	—	±60 typ	±40 typ	2.0 typ	+10V to +11.5V	350	Natural Binary
	DAC-03CDX1*	±0.20	—	±0.10	—	8	—	±60 typ	±40 typ	2.0 typ	+10V to +11.5V	350	Natural Binary
	DAC-03DDX1*	±0.4	—	±0.1	—	7	—	±60 typ	±40 typ	2.0 typ	+10V +11.5V	350	Natural Binary
10-Bit +Sign Linear	DAC-05EX	±0.10	±0.20	±0.05	±0.10	10	10	±100	±30 typ	2.0 typ	±10V to ±11.5V	300	Sign Magnitude
	DAC-05GX	±0.40	±0.50	±0.05	±0.10	8	8	±100	±30 typ	2.0 typ	±10V to ±11.5V	300	Sign Magnitude
	DAC-06EX	±0.10	±0.20	±0.05	±0.10	10	10	±100	±30 typ	1.5 typ	±10V to ±11.5V	300	Two's Complement
	DAC-06FX	±0.20	±0.30	±0.05	±0.10	9	9	±100	±30 typ	1.5 typ	±10V to ±11.5V	300	Two's Complement
	DAC-06GX	±0.40	±0.40	±0.05	±0.10	8	8	±100	±30 typ	1.5 typ	±10V to ±11.5V	300	Two's Complement
	DAC-210EX	±0.05	±0.05	±0.05	±0.06	10	10	±40	±15 typ	1.5 typ	±10V to ±11.5V	290	Sign Magnitude
	DAC-210FX	±0.05	±0.1	±0.1	±0.1	10	10	±60	±30 typ	1.5 typ	±10V to ±11.5V	290	Sign Magnitude
	DAC-210GX	±0.1	—	—	—	9	9	±30 typ	±30 typ	1.5 typ	±10V to ±11.5V	290	Sign Magnitude

*DAC-03 available all grades with +5V output — use X2 suffix.

D/A CONVERTERS

DAC SELECTION GUIDE

Voltage Output — Military Temperature Range (−55° C to +125° C) These Products Available in 883B

All specifications are minimum or maximum ratings unless otherwise indicated.

Resolution	PMI Part Number	Nonlinearity (% F.S.) 25° C	Nonlinearity (% F.S.) −55° C to +125° C	Zero-Scale Offset (% F.S.) 25° C	Zero-Scale Offset (% F.S.) −55° C to +125° C	Monotonicity (Bits) 25° C	Monotonicity (Bits) −55° C to +125° C	Gain T.C. (PPM/° C) Int. Ref.	Gain T.C. (PPM/° C) Ext. Ref.	Settling Time (μs)	Output Voltage Range	Power Dissipation (mW)	Codes
6-Bit Linear	DAC-01AY	±0.20	±0.30	±0.25	±0.25	6	6	±80	—	3.0	±10V to ±11.75V	250	Complement Binary
	DAC-01Y	±0.40	±0.45	±0.25	±0.25	6	6	±80	—	3.0	±10V to ±11.75V	250	Complement Binary
	DAC-01BY	±0.40	±0.45	±0.25	±0.25	6	6	±120	—	3.0	±10V to ±11.75V	250	Complement Binary
	DAC-01FY	±0.40	±0.45	±0.40	±0.40	6	6	±80	—	3.0	±10V to ±11.75V	250	Complement Binary
8-Bit +Sign Linear	DAC-208AX	±0.1	±0.1	—	±0.1	8	8	±40	±15 typ	0.75	+5V or ±10V	290	Sign Magnitude
	DAC-208BX	±0.2	±0.2	—	±0.15	8	8	±60	±30 typ	0.75	+5V or ±10V	290	Sign Magnitude
10-Bit +Sign Linear	DAC-05AX1	±0.10	±0.20	±0.05	±0.10	10	10	±60	±30 typ	2.0 typ	±10V to ±11.75V	300	Sign Magnitude
	DAC-05CX1	±0.40	±0.50	±0.05	±0.10	8	8	±120	±30 typ	2.0 typ	±10V to ±11.75V	300	Sign Magnitude
	DAC-06BX	±0.20	±0.30	±0.05	±0.10	9	9	±90	±30 typ	1.5 typ	±10V to ±11.5V	300	Two's Complement
	DAC-06CX	±0.40	±0.50	±0.05	±0.10	8	8	±120	±30 typ	1.5 typ	±10V to ±11.5V	300	Two's Complement
	DAC-210AX	±0.05	±0.075	±0.05	±0.06	10	10	±40	±15 typ	1.5 typ	±10V to ±11.5V	325	Sign Magnitude
	DAC-210BX	±0.05	±0.10	±0.1	±0.1	10	10	±60	±30 typ	1.5 typ	±10V to ±11.5V	325	Sign Magnitude

DAC SELECTION GUIDE

Current Output — Commercial Temperature Range (0° C to 70° C)

All specifications are minimum or maximum ratings unless otherwise indicated.

Resolution	PMI Part Number	Nonlinearity (% F.S.) 25° C	Nonlinearity (% F.S.) 0° C to 70° C	Zero-Scale Offset (% F.S.) 25° C	Zero-Scale Offset (% F.S.) 0° C to 70° C	Monotonicity (Bits) 25° C	Monotonicity (Bits) 0° C to 70° C	Gain T.C. (PPM/° C) Int. Ref.	Gain T.C. (PPM/° C) Ext. Ref.	Settling Time (µs)	Output Compliance (Volts)	Output Impedance (MΩ)	Power Dissipation (mW)
8-Bit Linear	DAC-08HQ(HP)	±0.10	±0.10	0.05	0.05	8	8	—	±50	0.135	−10V to +18V	>20	174
	DAC-08EQ(EP)	±0.19	±0.19	0.10	0.10	8	8	—	±50	0.150	−10V to +18V	>20	174
	DAC-08CQ(CP)	±0.39	±0.39	0.20	0.20	8	8	—	±80	0.150	−10V to +18V	>20	174
	DAC-1408A-8Q(7P)	±0.19	±0.19	—	—	8	8	—	±20 typ	0.250	−5V to +0.5V		265
	DAC-1408A-7Q(7P)	±0.39	±0.39	—	—	7	7	—	±20 typ	0.250	−0.5V to +0.5V	—	265
	DAC-1408A-6Q	±0.78	±0.78	—	—	6	6	—	±20 typ	0.250	−0.5V to +0.5V		265
	DAC-20CQ(CP)	±0.50	±0.50	0.250	0.250	2 Digits	2 Digits	—	±80	0.150	−10V to +18V	>20	200
8-Bit Latched	DAC-808EX	±0.1	±0.1	0.1	0.1	9	8	—	±50	0.5	−5V to +8V	>20	170
	DAC-808FX	±0.19	±0.19	0.1	0.1	8	8	—	±80	0.5	−5V to +8V	>20	170
	DAC-808GX	±0.39	±0.39	0.1	0.1	8	8	—	±80	0.5	−5V to +8V	>20	170
	DAC-888EX	±0.1	±0.1	±0.1	±0.1	8	8	—	±50	0.25	−5V to +8V	—	190
	DAC-888FX	±0.19	±0.19	±0.1	±0.1	8	8	—	±80	0.25	−5V to +8V	—	190
10-Bit Linear	DAC-10FX	±0.05	±0.05	0.01	0.01	10	10	—	±25	0.135	−5.5V to +10V	—	460
	DAC-10GX	±0.1	±0.1	±0.01	±0.1	10	10	—	±50	150	−5.5V to +10V	—	460
	DAC-100ACQ3/Q4	±0.05	±0.05	0.013	0.013	10	10	±60	—	0.375	—	—	300
	DAC-100BCQ3/Q4	±0.10	±0.10	0.013	0.013	9	9	±60	—	0.300	—	—	300
	DAC-100CCQ3/Q4	±0.20	±0.20	0.013	0.013	8	8	±60	—	0.225	—	—	300
	DAC-100DDQ3/Q4	±0.30	±0.30	0.013	0.013	8	8	±120	—	0.150	—	—	300
12-Bit Linear	DAC-312FR	±0.025*	±0.025	±0.003	±0.003	12	12	—	±40	0.25	−5V to +10V	>10	375
	DAC-312ER	±0.012*	±0.12	±0.003	±0.003	12	12	—	±30	0.25	−5V to +10V	>10	375

*Differential Nonlinearity

DAC SELECTION GUIDE

Current Output — Industrial Temperature Range (−25° C to +85° C)

All specifications are minimum or maximum ratings unless otherwise indicated.

Resolution	PMI Part Number	Nonlinearity (% F.S.) 25° C	Nonlinearity (% F.S.) 0° C to +85° C	Zero-Scale Offset (% F.S.) 25° C	Zero-Scale Offset (% F.S.) 70° C to +85° C	Monotonicity (Bits) 25° C	Monotonicity (Bits) 0° C to +85° C	Gain T.C. (PPM/° C Int. Ref.	Gain T.C. (PPM/° C Ext. Ref.	Settling Time (μs)	Output Compliance (Volts)	Output Impedance (kΩ)	Power Dissipation (mW)
10-Bit Linear	DAC-100AAQ7/Q8	±0.05	±0.05	0.013	0.013	10	10	±15	—	0.375	—	500 typ	250
	DAC-100ABQ7/Q8	±0.05	±0.05	0.013	0.013	10	10	±30	—	0.375	—	500 typ	250
	DAC-100ACQ7/Q8	±0.05	±0.05	0.013	0.013	10	10	±60	—	0.375	—	500 typ	250
	DAC-100BBQ7/Q8	±0.10	±0.10	0.013	0.013	9	9	±30	—	0.300	—	500 typ	250
	DAC-100BCQ7/Q8	±0.10	0.10	0.013	0.013	9	9	±60	—	0.300	—	500 typ	250
	DAC-100CCQ7/Q8	±0.20	±0.20	0.013	0.013	8	8	±60	—	0.225	—	500 typ	250
	DAC-100DDQ7/Q8	±0.30	±0.30	0.013	0.013	8	8	±120	—	0.150	—	500 typ	250

Current Output — Military Temperature Range (−55° C to +125° C)

All specifications are minimum or maximum ratings unless otherwise indicated.

Resolution	PMI Part Number	Nonlinearity (% F.S.) 25° C	Nonlinearity (% F.S.) −55° C to +125° C	Zero-Scale Offset (% F.S.) 25° C	Zero-Scale Offset (% F.S.) −55° C to +125° C	Monotonicity (Bits) 25° C	Monotonicity (Bits) −55° C to +125° C	Gain T.C. (PPM/° C) Int. Ref.	Gain T.C. (PPM/° C) Ext. Ref.	Settling Time (μs)	Output Compliance (Volts)	Output Impedance (MΩ)	Power Dissipation (mW)
8-Bit Linear	DAC-08AQ	±0.10	±0.10	0.05	0.05	8	8	—	±50	0.135	−10V to +18V	>20 typ	174
	DAC-08Q	±0.19	±0.19	0.10	0.10	8	8	—	±80	0.150	−10V to +18V	>20 typ	174
	1508A-8Q	±0.19	±0.19	0.2	0.2	8	8	—	—	0.250 typ	−5V to +0.05V	—	265
8-Bit Latched	DAC-808AX	—	±0.1	0.1	0.1	8	8	—	±50	0.500	−5V to +8V	>20	170
	DAC-808BX	—	±0.19	0.1	0.1	8	8	—	±80	0.500	−5V to +8V	>20	170
	DAC-888AX	—	0.1	0.1	0.1	8	8	—	±50	0.250	−5V to +8V	>20	190
	DAC-888BX	—	0.19	0.1	0.1	8	8	—	±80	0.250	−5V to +8V	>20	190
10-Bit Linear	DAC-100ACQ5/Q6	±0.05	±0.05	0.013	0.013	10	10	±15	—	0.375	—	0.5 typ	300
	DAC-100BBQ5/Q6	±0.10	±0.12	0.013	0.013	9	9	±30	—	0.300	—	0.5 typ	300
	DAC-100BCQ5/Q6	±0.10	±0.10	0.013	0.013	9	9	±30	—	0.300	—	0.5 typ	300
	DAC-100CCQ5/Q6	±0.20	±0.20	0.013	0.013	8	8	±60	—	0.225	—	0.5 typ	300
	DAC-10BX	0.05	0.05	0.013	0.013	10	10	±25	—	0.135	−5.5V to +10V	—	460
	DAC-10CX	0.1	0.1	0.013	0.013	10	10	±50	—	0.150	−5V to +10V	—	460
12-Bit Linear	DAC-312BR	±0.025	±0.25	±0.003	±0.003	12	12	—	±40	0.25	−10V to +8V	>10	375

6-BIT VOLTAGE-OUTPUT D/A CONVERTER

DAC-01

FEATURES

- **Fast .... 3μs Settling Time Max**
- **Complete .... Includes Reference, Ladder, Op Amp**
- **Low Power Consumption .... 250mW Max**
- **6-Bit Resolution .... 7-Bit Accuracy**
- **3 Output Options .... +10V, ±5V, ±10V**
- **Standard Power Supplies .... ±12V to ±18V**
- **TTL — Compatible Logic Levels**
- **MIL-STD-883 Class B Processing Available From Stock**

GENERAL DESCRIPTION

The DAC-01 is a complete monolithic 6-bit digital-to-analog converter. The device contains current steering logic, current sources, a diffused resistor ladder network, precision voltage reference and fast summing op amp on one chip. Monolithic construction provides low power consumption and high reliability. Wide power supply range, three output voltage options, and three input code options assure flexibility for a wide variety of applications. A seventh bit may also be added for greater resolution. Introduced in 1970, the DAC-01 is still the fastest, lowest power, most accurate 6-bit complete monolithic DAC available. The DAC-01 is ideal for CRT deflection circuits, servo positioning controls, digitally programmed power supplies and pulse generators, modem and telephone system digitizing and demodulation circuits, digital filters, and 6-bit A/D converters.

ORDERING INFORMATION††

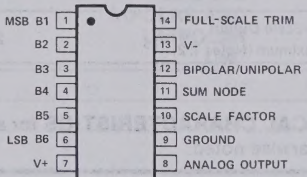
	14-PIN HERMETIC DIP	
FULL TEMP. N.L. LSB	MILITARY TEMP.	COMMERCIAL TEMP.
±1/8	DAC01AY*	
	DAC01Y*	—
±1/4	DAC01BY*	DAC01CY
	DAC01FY*†	DAC01HY†
±1/2	—	DAC01DY

*Available with MIL-STD-883B processing. To order add suffix/883.

†Unipolar only — all others unipolar or bipolar.

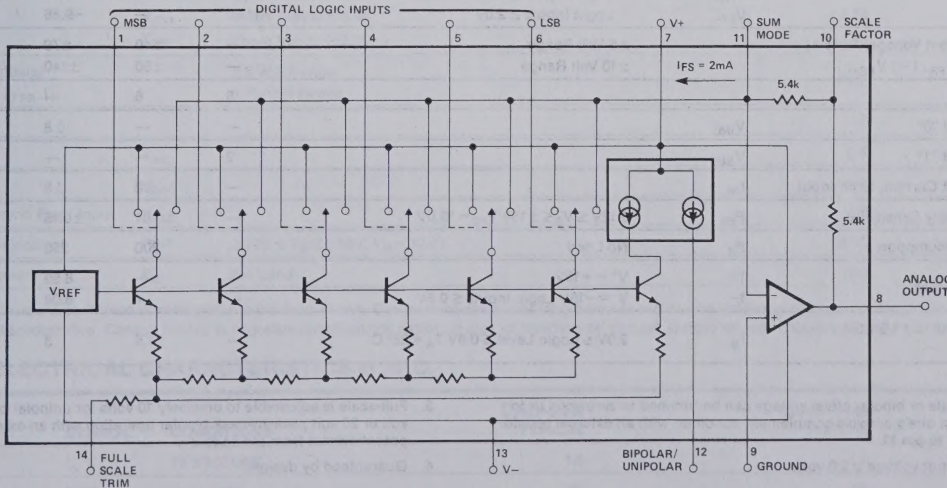
††All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

PIN CONNECTIONS


MSB B1 1
B2 2
B3 3
B4 4
B5 5
LSB B6 6
V+ 7
14 FULL-SCALE TRIM
13 V-
12 BIPOLAR/UNIPOLAR
11 SUM NODE
10 SCALE FACTOR
9 GROUND
8 ANALOG OUTPUT

14-PIN HERMETIC DIP (Y-Suffix)

SIMPLIFIED SCHEMATIC


DIGITAL LOGIC INPUTS
MSB 1
2
3
4
5
LSB 6
V+ 7
SUM MODE 11
SCALE FACTOR 10
I_{FS} = 2mA
5.4k
5.4k
VREF
ANALOG OUTPUT 8
14 FULL SCALE TRIM
13 V−
BIPOLAR/UNIPOLAR 12
9 GROUND

ABSOLUTE MAXIMUM RATINGS (See Note 3)

Operating Temperature
DAC-01A, DAC-01, DAC-01B,
DAC-01F .... −55° C to +125° C
DAC-01C, DAC-01H, DAC-01D .... 0° C to +70° C
DICE Junction Temperature (T_j) .... −65° C to +150° C
V+ Supply Voltage to Ground .... 0 to +18V
V− Supply Voltage to Ground .... 0 to −18V
Logic Input to Ground .... −0.7 to +6V
Internal Power Dissipation (Note 1) 500mW
Storage Temperature .... −65° C to +150° C
Lead Temperature (Soldering, 60 sec) .... 300° C
Output Short-Circuit Duration (Note 2) .... Indefinite

NOTES:

1. Rating applies to ambient temperatures of 100° C. For temperatures above 100° C, derate linearly at 10mW/° C.
2. Short circuit may be to ground or either supply. Rating applies to +125° C case temperature or +75° C ambient temperature.
3. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$ and over the rated operating temperature range, unless otherwise noted.

PARAMETER	SYMBOL	DAC-01A	DAC-01	DAC-01B	DAC-01F	DAC-01C	DAC-01H	DAC-01D	UNITS
Output Options		Unipolar Bipolar	Unipolar Bipolar	Unipolar Bipolar	Unipolar	Unipolar Bipolar	Unipolar	Unipolar Bipolar	
Temperature Range	T_A	-55/+125	-55/+125	-55/+125	-55/+125	0/+70	0/+70	0/+70	°C
Nonlinearity 25° C/Maximum	NL	±0.20	±0.40	±0.40	±0.40	±0.40	±0.40	±0.78	%FS
Nonlinearity Over Temperature — Maximum	NL	±0.30	±0.45	±0.45	±0.45	±0.45	±0.45	±0.78	%FS
Full-Scale Tempco — Maximum	T_C	±80	±80	±120	±80	±160	±160	±160	ppm/° C
Unipolar Zero-Scale Output Voltage — Maximum (Notes 1, 2)	V_{ZS}	25	25	25	40	25	40	50	mV

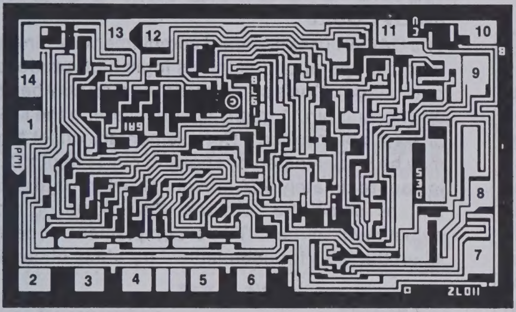
ELECTRICAL CHARACTERISTICS for all DAC-01 grades, $V_S = \pm15V$ and over the rated operating temperature range unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-01 MIN	TYP	MAX	UNITS
Unipolar Full Range Output Voltage (Note 3)	V_{FR}	2kΩ load, logic ≤ 0.8V, short pin 13 to pin 14. Short pin 12 to Ground and pin 10 to pin 11.	+10.0	—	+11.75	V
Bipolar Output Voltage (Note 3) ±5 Volt Range		2kΩ load, short pin 11 to pin 12. Short pin 13 to pin 14, short pin 10 to pin 11.				
	V_{FR+}	Logic Inputs ≤ 0.8V	+4.93	—	+5.94	V
	V_{FR-}	Logic Inputs ≥ 2.0V	−5.94	—	−4.93	
±10 Volt Range		Open pin 10				
	V_{FR+}	Logic Inputs ≤ 0.8V	+9.86	—	+11.89	V
	V_{FR-}	Logic Inputs ≥ 2.0V	−11.89	—	−9.86	
Bipolar Offset Voltage (Note 1) ±1/2 ($\lvert V_{FR+}\rvert - \lvert V_{FS-}\rvert$)		±5 Volt Range	—	±40	±70	mV
		±10 Volt Range	—	±80	±140	
Resolution			6	6	—	Bits
Logic Input "0"	V_{INL}		—	—	0.8	V
Logic Input "1"	V_{INH}		2	—	—	V
Logic Input Current, Each Input	I_{IN}		—	±2	±8	μA
Power Supply Sensitivity	P_{SS}	$\pm12V \le V_S \le \pm18V$ $V_{FS} \approx 10.0V$	—	±0.01	±0.15	%V_{FS}/V
Power Consumption	P_d	No Load	—	200	250	mW
Supply Current	I+	$V^+ = +15V$	—	—	8.58	mA
	I−	$V^- = -15V$ Logic Inputs ≤ 0.8V	—	—	8.08	
Setting Time to ±1/2 LSB (Note 4)	t_S	2.0V ≤ Logic Level ≤ 0.8V $T_A = 25°C$	—	1.5	3	μs

NOTES:

1. Zero-scale or bipolar offset voltage can be trimmed to zero volts or to the exact one's or two's complement condition with an external resistor network to pin 11.
2. Logic input voltage ≥ 2.0 volts.
3. Full-scale is adjustable to precisely 10 volts for unipolar operation and 10 volt or 20 volt peak-to-peak bipolar operation with an external 500 ohm potentiometer from pin 14 to V−.
4. Guaranteed by design.

DICE CHARACTERISTICS



1. B1 (MSB)
2. B2
3. B3
4. B4
5. B5
6. B6 (LSB)
7. V+
8. ANALOG OUTPUT
9. GROUND
10. SCALE FACTOR
11. SUM NODE
12. BIPOLAR/UNIPOLAR
13. V−
14. FULL-SCALE TRIM

DIE SIZE 0.092 × 0.054 inch, 4968 sq. mils (2.34 × 1.37 mm, 3.21 sq. mm)

For additional DICE information refer to Section 2.

WAFER TEST LIMITS at $T_A = 25°C$.

PARAMETER	SYMBOL	CONDITIONS	DAC-01N BIPOLAR AND UNIPOLAR LIMIT	DAC-01G BIPOLAR AND UNIPOLAR LIMIT	UNITS
Nonlinearity	NL	$V_S = \pm 15V$	1/4	1/2	L.S.B. MAX
Zero-Scale Voltage	V_{ZS}	$V_S = \pm 15V$	25	35	mV MAX

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-01 LIMIT	UNITS
Unipolar Full-Scale Output Voltage (All Models)	V_{FR}	2kΩ Load, Logic ≤ 0.8V, Short V− to Full-Scale Trim, Unipolar/Bipolar to Ground, and Scale Factor to Sum Node	10.00 11.75	V MIN V MAX
		2kΩ Load, Short Sum Node to Unipolar/Bipolar. Short V− to Full-Scale Trim and Scale Factor to Sum Node.		
Bipolar Output Voltage	V_{FR+}	Logic Inputs ≤ 0.8V	+4.93	V MIN
±5 Volt Range	V_{FR-}	Logic Inputs ≥ 2.0V	−5.94	V MAX
±10 Volt Range		Open-Scale Factor		
	V_{FR+}	Logic Inputs ≤ 0.8V	+9.78	V MIN
	V_{FR-}	Logic Inputs ≥ 2.0V	−11.89	V MAX
Bipolar Offset Voltage ±1/2 ($\lvert V_{FR+} \rvert - \lvert V_{FR-} \rvert$)		±5 Volt Range ±10 Volt Range	±1/2	LSB MAX
Resolution			6	Bits MAX
Logic Input "0"	V_{INL}		0.8	V MAX
Logic Input "1"	V_{INH}		2	V MIN
Logic Input Current, Each Input	V_{OV}		±8	μA MAX
Power Supply Rejection	PSR	$\pm 12V \leq V_S \leq \pm 18V$, $V_S = 10.0V$	0.15	%FS/V MAX
Power Consumption	P_d	No Load	250	mW MAX

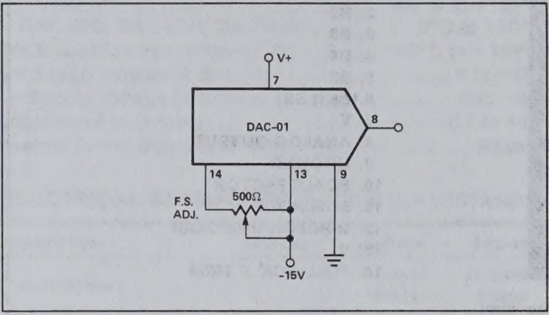
Note: Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at 25° C.

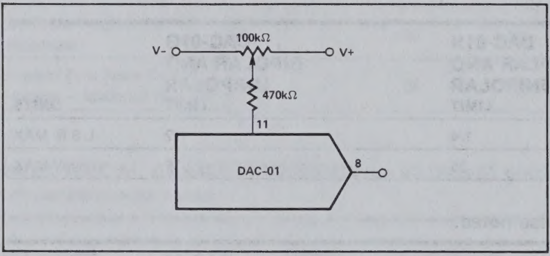
PARAMETER	SYMBOL	CONDITIONS	DAC-01N TYPICAL	DAC-01G TYPICAL	UNITS
Settling Time	t_S	To ±1/2 LSB	1.5	1.5	μs
Full-Scale Tempco	TCV_{FS}	$V_S = \pm 15V$	60	90	ppm/° C

BASIC CIRCUIT CONNECTIONS

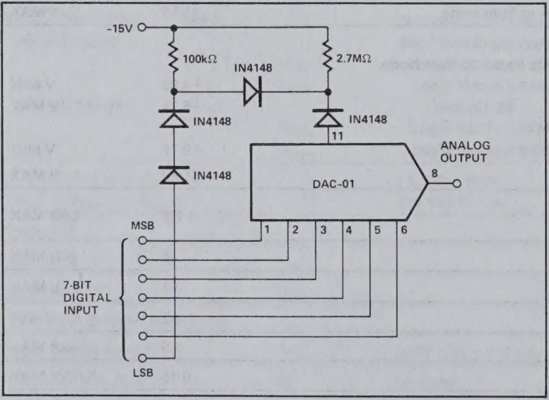
FULL-SCALE ADJUSTMENT TECHNIQUE



OPTIONAL ZERO-SCALE OR BIPOLAR OFFSET ADJUSTMENT



ADDITION OF 7th BIT



APPLICATIONS INFORMATION

INPUT CODES

The DAC-01 uses standard complementary binary coding for unipolar operation (all inputs logic high produces zero output voltage). One's complement coding may be implemented by shorting pin 11 to pin 12 and inverting the MSB (all other bits are not inverted). Complementary offset binary coding may be implemented by shorting pin 11 to pin 12, and injecting approximately 5μA into pin 11 (which is at ground potential) by using the "optional Zero-Scale or bipolar offset adjustment" circuit. Two's complement code is achieved when the MSB for complementary offset binary is inverted.

FULL-SCALE ADJUST

A 500Ω pot from pin 14 to V− can be used to adjust the Full-Scale output voltage to exactly 10 volts in unipolar mode or 10 to 20 volts peak-to-peak in bipolar mode. If no pot is used, connect pin 14 to V−.

SCALE FACTOR

For +10 volts or ±5 volt outputs, short pin 10 to pin 11 (adjusts the feedback resistor around the output amplifier). For ±10 volt output, leave pin 10 open. Intermediate output voltages may be obtained by placing a pot between pin 10 and pin 11. This will, however, seriously degrade the Full-Scale temperature coefficient due to the mismatch between the +1150ppm/°C tempco of the diffused resistors and the pot tempco.

CAPACITIVE LOADS

When driving capacitive loads greater than 50pF in Unipolar mode or 30pF in Bipolar mode a 100pF capacitor may be placed from pin 11 to ground for added stability.

LOWER RESOLUTION APPLICATIONS

When less than 6 bits of resolution is required, connect unused bits to a voltage level greater than +2.0 volts. The +5 volt logic supply is adequate.

10-BIT-PLUS-SIGN VOLTAGE-OUTPUT D/A CONVERTERS
DAC-02/DAC-03/DAC-05

FEATURES

- Complete .... Includes Reference and Op Amp
- Compact .... Single 18-Pin DIP Package
- Bipolar Output .... (±10V) Sign-Magnitude Coding
- DAC-03 — Unipolar Only; .... +5V or +10V
- Monotonicity Guaranteed
- Nonlinearity .... ±1 LSB
- Fast .... 2.0μs Settling Time
- Stable .... Full-Scale Tempco 60ppm/°C
- Low Power Consumption .... 300mW Max
- TTL, CMOS Compatible Inputs
- MIL-STD-883 Class B Processing Available on DAC-05

GENERAL DESCRIPTION

The DAC-02 and DAC-05 are complete 10-bit plus sign D/A converters on a single monolithic chip. All elements of a complete sign-magnitude DAC are included; precision voltage reference, current steering logic, current sources, R-2R resistor network, logic-controlled polarity switch, and high speed internally-compensated output op amp. Monotonicity guaranteed over the entire temperature range is achieved using an untrimmed diffused R-2R resistor network. The buffered reference input is capable of tracking over a wide range of voltages, increasing application flexibility. The wide power supply range, low power consumption, wide logic input compatibility and sign-magnitude coding assures utility in a wide range of applications including CRT displays, data acquisition systems, A/D converters, servo positioning controls, and audio digitizing/reconstruction systems.

The DAC-03 is similar in construction to the DAC-02/DAC-05 except for a unipolar only output. This device is intended for low cost, limited temperature range applications, with the same general specifications as its premium counterparts.

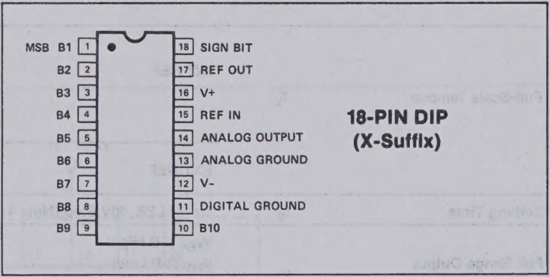
ORDERING INFORMATION †

	PACKAGE: 18-PIN HERMETIC DIP			
MONOTONICITY	MILITARY TEMP*	COMMERCIAL TEMP		
10	DAC05AX	DAC02ACX	DAC03ADX	DAC05EX
9		DAC02BCX	DAC03BDX	
8	DAC05CX	DAC02CCX	DAC03CDX	DAC05GX
7	——	DAC02DDX	DAC03DDX	——

*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

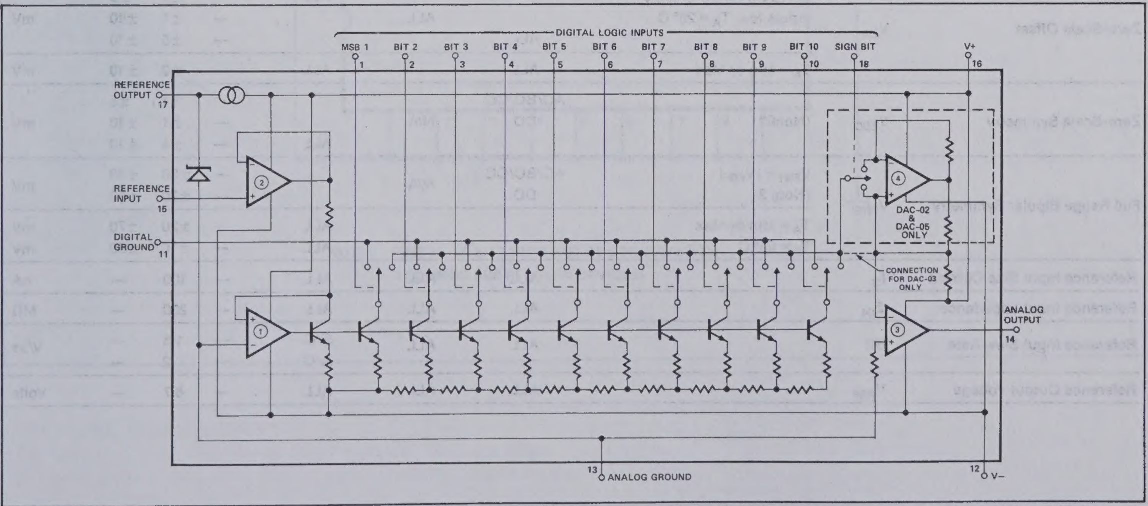
†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

PIN CONNECTIONS


MSB B1 1
B2 2
B3 3
B4 4
B5 5
B6 6
B7 7
B8 8
B9 9
18 SIGN BIT
17 REF OUT
16 V+
15 REF IN
14 ANALOG OUTPUT
13 ANALOG GROUND
12 V-
11 DIGITAL GROUND
10 B10

18-PIN DIP (X-Suffix)

SIMPLIFIED SCHEMATIC


DIGITAL LOGIC INPUTS
MSB 1
BIT 2
BIT 3
BIT 4
BIT 5
BIT 6
BIT 7
BIT 8
BIT 9
BIT 10
SIGN BIT
V+
1
2
3
4
5
6
7
8
9
10
18
16
REFERENCE OUTPUT
17
REFERENCE INPUT
15
DIGITAL GROUND
11
2
1
4
3
DAC-02 & DAC-05 ONLY
CONNECTION FOR DAC-03 ONLY
ANALOG OUTPUT
14
13
ANALOG GROUND
12
V–

ABSOLUTE MAXIMUM RATINGS (Note)

Operating Temperature Range	
DAC-05A, C	−55° C to +125° C
DAC-02 and DAC-03, All DAC-05E, G	0° C to +70° C
Storage Temperature Range	−65° C to +150° C
V+ Supply to Analog Ground	0 to +18V
V− Supply to Analog Ground	0 to −18V
Analog Ground to Digital Ground	0 to ±0.5V
Logic Inputs to Digital Ground	−5V to (V+ −0.7V)
Internal Reference Output Current	300μA
Reference Input Voltage	0 to +10V
Internal Power Dissipation	500mW
Lead Temperature (Soldering, 60 sec)	300° C
Output Short Circuit Duration	Indefinite

(Short circuit may be to ground or either supply.)

NOTE: For ambient temperatures above 100° C derate 100mW/° C.

OUTPUT VOLTAGE RANGE SELECTION TABLE

PRODUCT	OUTPUT VOLTAGE RANGE	ADD AS SUFFIX TO PART NO.
DAC02	±10V	1
DAC03	0 to +10V	1
DAC03	0 to +5V	2
DAC05	±10V	1

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $0 \leq T_A \leq +70°C$ for DAC-02 and DAC-05E & G, $T_A = 25°C$ for DAC-03 and $-55 \leq T_A \leq +125°C$ for DAC-05A & C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-02	DAC-03	DAC-05	MIN	TYP	MAX	UNITS
Monotonicity			AC	AD	A/E	10	—	—	Bits
			BC	BD		9	—	—	
			CC	CD	C/G	8	—	—	
			DD	DD		7	—	—	
Nonlinearity	NL		AC/BC	AD/BD		—	—	±0.1	% FS
			CC	CD	A/E	—	—	±0.2	
			DD	DD		—	—	±0.4	
					C/G	—	—	±0.5	
Full-Scale Tempco	T_C	INT REF	AC/BC/CC		A	—	—	±60	ppm/° C
				ALL		—	±60	—	
					E/G	—	±45	±100	
					C	—	±60	±120	
			DD			—	—	±150	
		EXT REF	ALL		ALL	—	±30	—	ppm/° C
				ALL		—	±40	—	
Settling Time	t_S	To 1/2 LSB, 10V Step (Note 4)	ALL	ALL	ALL	—	2	—	μs
Full Range Output Voltage (Note 1)	V_{FR}	V_{FR+} (SB High)	ALL		ALL	+10	—	+11.5	Volts
		V_{FR-} (SB Low)	ALL		ALL	−11.5	—	−10	
		DAC-03 +10V		ALL		+10	—	+11.5	
		+5V		ALL		+5.00	—	+5.75	
Zero-Scale Offset	V_{ZS}	SB High. All other logic inputs low. $T_A = 25°C$			ALL	—	±1	±5	mV
				ALL		—	±1	±10	
			ALL			—	±5	±10	
		T_A = Min or Max	ALL		ALL	—	±2	±10	mV
Zero-Scale Symmetry	V_{ZSS}	(Note 2)	AC/BC/CC			—	±1	±5	mV
			DD	N/A		—	±1	±10	
					ALL	—	±4	±10	
Full Range Bipolar Symmetry	V_{FRS}	$V_{FR+} - \lvert V_{FR-} \rvert$ (Note 3)	AC/BC/CC	N/A		—	±30	±60	mV
			DD			—	±30	±80	
		T_A = Min or Max			ALL	—	±20	±70	mV
		$T_A = 25°C$			ALL	—	±10	±50	mV
Reference Input Bias Current	I_B		ALL	ALL	ALL	—	100	—	nA
Reference Input Impedance	Z_{IN}		ALL	ALL	ALL	—	200	—	MΩ
Reference Input Slew Rate	SR		ALL	ALL	E/G	—	1.5	—	V/μs
					A/C	—	2	—	
Reference Output Voltage	V_{REF}		ALL	ALL	ALL	—	6.7	—	Volts

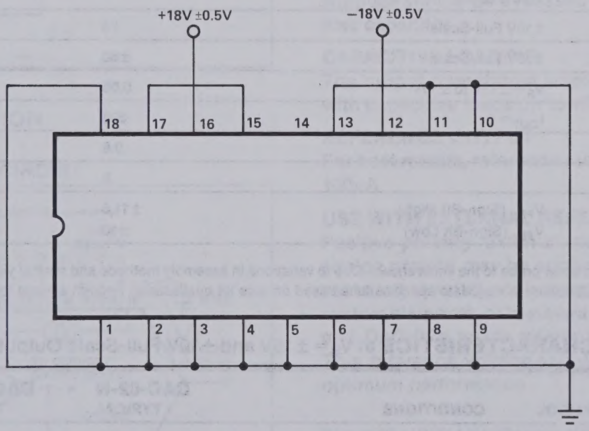
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $0 \le T_A \le +70°C$ for DAC-02 and DAC-05E & G, $T_A = 25°C$ for DAC-03 and $-55 \le T_A \le +125°C$ for DAC-05A & C, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	DAC-02	DAC-03	DAC-05	MIN	TYP	MAX	UNITS
Logic Input Current	I_{IN}	Each input -5V to (V+ − 0.7)V	ALL	ALL	ALL	—	±1	±10	μA
Logic Input 0	V_{INL}		ALL	ALL	ALL	—	—	0.8	Volts
Logic Input 1	V_{INH}		ALL	ALL	ALL	2	—	—	
Positive Supply Current	I+	SB High. All other logic inputs low.	AC/BC/CC		ALL	—	+7	+10	mA
			DD	ALL		—	+7	+11.6	
Negative Supply Current	I−	SB High. All other logic inputs low.	AC/BC/CC		ALL	—	−9	−10	mA
			DD			—	−9	−11.6	
				ALL		—	−10	−11.6	
Power Supply Sensitivity	P_{SS}	$V_S = \pm 12$ to $\pm 18V$	AC/BC/CC			—	±0.015	±0.05	% V_{FS}/V
			DD	ALL		—	±0.015	±0.1	
		T_A = Min to Max			ALL		±0.05	±0.1	
		$T_A = 25°C$			ALL		±.02	±.05	
Power Dissipation	P_d	$I_{OUT} = 0$	AC/BC/CC			—	225	300	mW
			DD	ALL		—	225	350	
		$T_A = 25°C$			ALL	—	200	300	
		T_A = Min to Max			ALL	—	250	350	
Output Drive Current	I_O	Guaranteed by V_{FR} test	ALL	ALL	ALL	—	—	5	mA

NOTES:

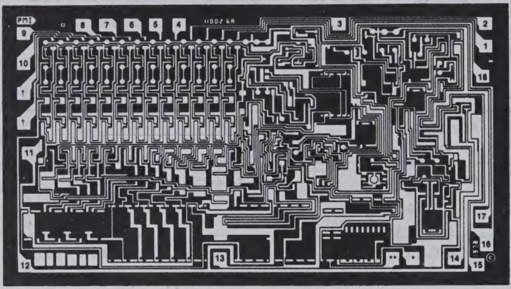
1. Reference output terminal connected directly to reference input terminal, $R_L = 2k\Omega$ for 10V devices, $R_L = 1k\Omega$ for 5V devices, all logic inputs ≥ 2.0V.
2. Zero-scale symmetry is the change in the output voltage produced by switching the sign-bit with all logic bits low ($V_{ZS+} - V_{ZS-}$).
3. Full-scale bipolar symmetry is the magnitude of the difference between V_{FR+} and $|V_{FR-}|$.
4. Guaranteed by design.

BURN-IN TEST CIRCUIT



NOTE : PINS 14, 15, & 17 MUST NOT BE CONNECTED TO A COMMON BUS BETWEEN DEVICES.

DICE CHARACTERISTICS



DIE SIZE 0.163 × 0.090 inch; 14,670 sq. mils
(4.14 × 2.286 mm, 9.464 sq. mm)

1. **BIT 1-MSB**
2. **BIT 2**
3. **BIT 3**
4. **BIT 4**
5. **BIT 5**
6. **BIT 6**
7. **BIT 7**
8. **BIT 8**
9. **BIT 9**
10. **BIT 10**
11. **DIGITAL GROUND**
12. **V−**
13. **ANALOG GROUND**
14. **ANALOG OUTPUT**
15. **REF IN**
16. **V+**
17. **REF OUT**
18. **SIGN BIT**

For additional DICE information refer to Section 2.

†Bits 11 & 12 (not normally used)

NOTE: Voltage output range programmable by connecting *(10V) to analog output for 10 volt range. Jumps from **(5V) to analog output for 5 volt range.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$ and +10V full-scale output, unless otherwise noted.

PARAMETER	CONDITIONS	DAC-02-N LIMIT	DAC-02-G LIMIT	UNITS
Resolution (Bits 11 and 12 Not Normally Used)	Bipolar Output Unipolar Output	13 12	13 12	Bits MAX
Monotonicity		9	8	Bits MIN
Nonlinearity		±0.1	±0.2	% FS MAX
Zero-Scale Offset	Sign Bit High, All Other Inputs Low	±10	±10	mV MAX
Zero-Scale Symmetry	±10V Full-Scale	±5	±5	mV MAX
Full-Scale Bipolar Symmetry	±10V Full-Scale	±60	±60	mV MAX
Power Supply Rejection	$V_S = \pm 12V$ to $\pm 18V$	0.05	0.05	$\%V_{FS}/V$ MAX
Power Dissipation	$I_{OUT} = 0$	300	300	mW MAX
Logic Input "0"		0.8	0.8	V MAX
Logic Input "1"		2	2	V MIN
Output Voltage Analog (All Bits High)	V_{FR+} (Sign-Bit High) V_{FR-} (Sign-Bit Low)	±11.5 ±10	±11.5 V MIN	V MAX

Note: Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ and +10V Full-Scale Output, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-02-N TYPICAL	DAC-02-G TYPICAL	UNITS
Full-Scale Tempco	TCV_{FS}	Internal Reference	60	60	ppm/°C
Settling Time ($T_A = 25°C$)	t_s	To ±1/2 LSB 10 Volt Step	2	2	μs
Logic Input Current	I_{IN}	$T_A = 25°C$	1	1	μA

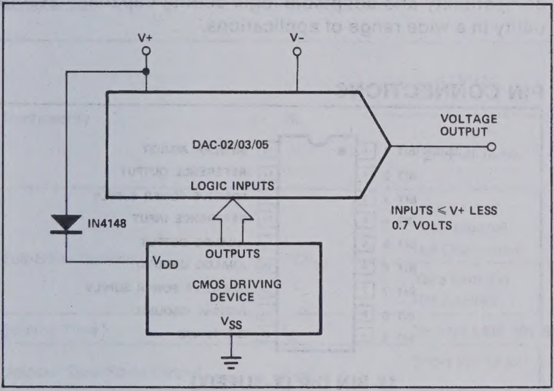
NOTE: When ordering DICE in this series, use DAC-02 numbers and grades above.

TYPICAL APPLICATIONS

The DAC-02's, DAC-03's and DAC-05's logic input stages require about 1μA and are capable of operation with inputs between −5 volts and V+ less 0.7 volt. This wide input voltage range allows direct CMOS interfacing in most applications, the exception being where the CMOS logic and D/A converter must use the same positive power supply.

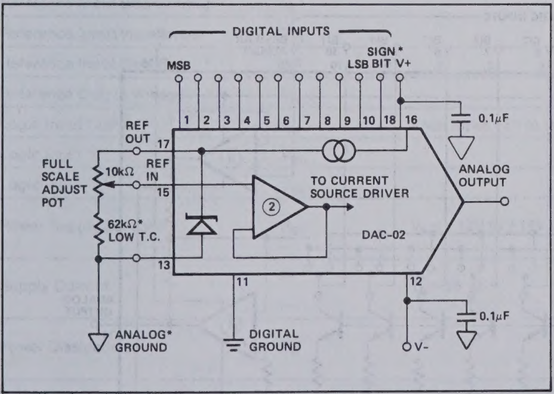
In this special case, a diode should be placed in series with the CMOS driving device's V_{DD} lead as shown in Figure 1. The diode limits V_D to V+ less 0.7 volt — since the output from the CMOS device cannot exceed this value, the DAC's maximum input voltage rule is satisfied. Summarizing: in all applications, the DAC-02, DAC-03 and DAC-05 require either no interfacing components, or at most a single inexpensive diode for full CMOS compatibility.

CMOS LOGIC INTERFACE CIRCUIT



CONNECTION INFORMATION

FULL-SCALE ADJUSTMENT CIRCUIT



FULL-SCALE ADJUSTMENT

Full-scale output voltage may be trimmed by use of a potentiometer and series resistor as shown; however, best results will be obtained if a low tempco resistor is used or if pot and resistor tempcos match. Alternatively, a single pot of ≤72kΩ may be used.

REFERENCE INPUT BYPASS

Lowest noise and fastest settling operation will be obtained by bypassing the reference input to analog ground with a 0.01μF disk capacitor.

GROUNDING

For optimum noise rejection, separate digital and analog grounds have been brought out. Best results will be obtained if these grounds are connected together at one point only, preferably near the DAC-02, DAC-03 and DAC-05 package, so that the large digital currents do not flow through the analog ground path.

APPLICATIONS INFORMATION

LOWER RESOLUTION APPLICATIONS

For applications not requiring full 10-bit resolution, unused logic inputs should be tied to ground.

UNIPOLAR OPERATION

Operation as a 10-bit straight binary converter may be implemented by permanently tying the sign-bit to +5V (for positive full-scale output) or to ground (for negative full-scale output). In the DAC-03 only, Pin 18 unipolar enable is tied to Pin 17.

POWER SUPPLIES

The DAC-02, DAC-03 and DAC-05 will operate within specifications for power supplies ranging from ±12V to ±18V. Power supplies should be bypassed near the package with a 0.1μF disk capacitor.

CAPACITIVE LOADING

The output operational amplifier provides stable operation with capacitive loads up to 100pF.

REFERENCE OUTPUT

For best results, reference output current should not exceed 100μA.

USE WITH EXTERNAL REFERENCES

Positive-polarity external reference voltages referred to analog ground may be applied to the reference input terminal to improve full-scale tempco, to provide tracking to other system elements, or to slave a number of DAC-02's, DAC-03's and DAC-05's to the reference output of any one of them. This reference voltage should be between +5V to +7V for optimum performance.

SIGN PLUS MAGNITUDE CODING TABLE (DAC-02, DAC-03 and DAC-05)

	SIGN-BIT	MSB									LSB
+ FULL SCALE	1	1	1	1	1	1	1	1	1	1	1
+ HALF-SCALE	1	1	0	0	0	0	0	0	0	0	0
ZERO-SCALE (+)	1	0	0	0	0	0	0	0	0	0	0
ZERO-SCALE (−)	0	0	0	0	0	0	0	0	0	0	0
− HALF-SCALE	0	1	0	0	0	0	0	0	0	0	0
− FULL-SCALE	0	1	1	1	1	1	1	1	1	1	1

DAC-06

TWO'S-COMPLEMENT 10-BIT VOLTAGE-OUTPUT D/A CONVERTER

FEATURES

- **Complete .... Includes Reference and Op Amp**
- **Compact.................... Single 18-Pin DIP Package**
- **Bipolar Output .... Two's Complement Coding**
- **Monotonicity Guaranteed**
- **Nonlinearity.......................................±1 LSB**
- **Fast .... 1.5μs Settling Time**
- **Low Power Consumption .... 300mW Max**
- **TTL, CMOS Compatible Inputs**
- **125° C Tested Dice Available**

GENERAL DESCRIPTION

The DAC-06 is a complete 10-bit two's complement D/A converter on a single 90 x 163 mil monolithic chip. All elements of a complete bipolar output two's complement DAC are included — precision voltage reference, current steering logic, current sources, R-2R resistor network, bipolar offset circuit and high speed internally compensated output op amp. Monotonicity guaranteed over the entire operating temperature range is achieved using an untrimmed diffused R-2R resistor network. The buffered reference input is capable of tracking over a wide range of voltages, increasing application flexibility. The user may also easily implement one's complement, straight offset binary, or unipolar operation. The ±12V to ±18V power supply range, low power consumption, TTL and CMOS compatibility, wide logic input compatibility and adaptable logic coding capability assure utility in a wide range of applications.

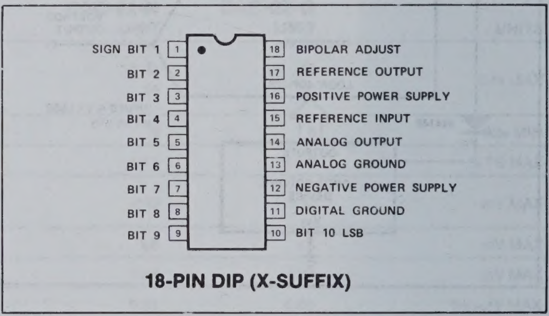
ORDERING INFORMATION†

PACKAGE 18-PIN HERMETIC DIP			
MONOTONICITY	MILITARY TEMP	COMMERCIAL TEMP	
10	—	DAC-06EX	—
9	DAC-06BX*	—	DAC-06FX
8	DAC-06CX*	—	DAC-06GX

*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

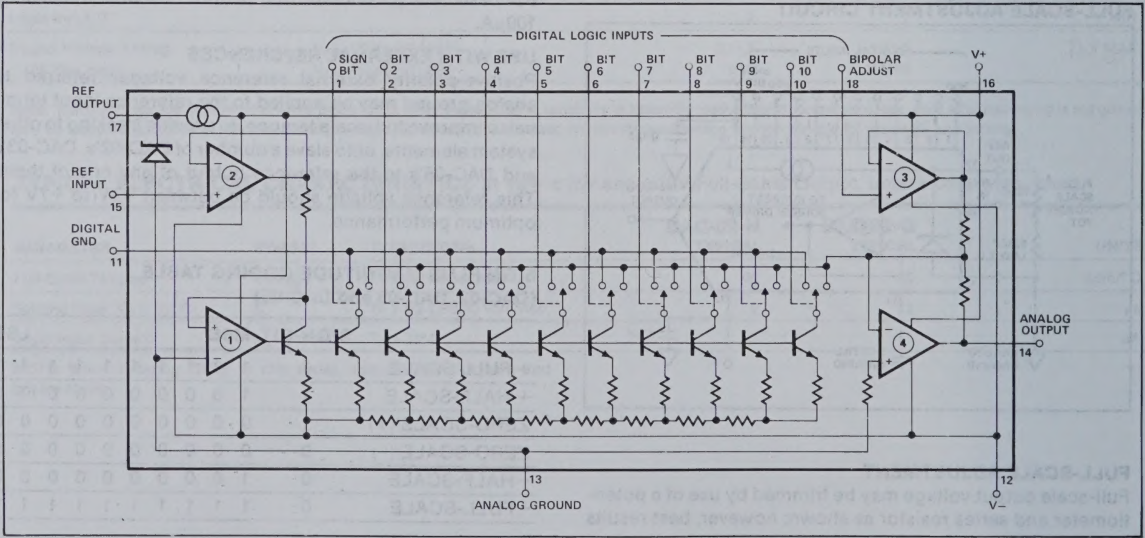
†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

PIN CONNECTIONS


SIGN BIT 1
BIT 2
BIT 3
BIT 4
BIT 5
BIT 6
BIT 7
BIT 8
BIT 9
18 BIPOLAR ADJUST
17 REFERENCE OUTPUT
16 POSITIVE POWER SUPPLY
15 REFERENCE INPUT
14 ANALOG OUTPUT
13 ANALOG GROUND
12 NEGATIVE POWER SUPPLY
11 DIGITAL GROUND
10 BIT 10 LSB

18-PIN DIP (X-SUFFIX)

SIMPLIFIED SCHEMATIC


DIGITAL LOGIC INPUTS
SIGN BIT 1
BIT 2
BIT 3
BIT 4
BIT 5
BIT 6
BIT 7
BIT 8
BIT 9
BIT 10
BIPOLAR ADJUST 18
V+
16
REF OUTPUT
17
REF INPUT
15
DIGITAL GND
11
1
2
3
4
ANALOG OUTPUT
14
13
ANALOG GROUND
12
V–

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	
DAC-06B, C	−55°C to +125°C
DAC-06E, F, G	0°C to +70°C
DICE Junction Temperature (T_j)	−65°C to +150°C
Storage Temperature Range	−65°C to +150°C
V+ Supply to Analog Ground	0 to +18V
V− Supply to Analog Ground	0 to −18V
Analog Ground to Digital Ground	0 to ±0.5V
Logic Inputs to Digital Ground	−5V to (V+ −0.7)V
Internal Reference Output Current	300μA
Reference Input Voltage	0 to +10V
Bipolar Offset Input Voltage	0 to +10V
Internal Power Dissipation	500mW
Lead Temperature (Soldering, 60 sec)	300°C
Output Short-Circuit Duration	Indefinite
(Short circuit may be to ground or either supply)	

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$; $-55°C \le T_A \le +125°C$ for DAC-06B & C; and $0°C \le T_A \le +70°C$ for DAC-06E, F & G, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS		DAC-06	MIN	TYP	MAX	UNITS
Resolution				All	10	—	—	Bits
Monotonicity				E	10	—	—	Bits
				B/F	9	—	—	
				C/G	8	—		
Nonlinearity	NL	$T_A = 25°C$		E	—	—	±0.1	% FS
				B/F	—	—	±0.2	
				C/G	—	—	±0.4	
		T_A = Full Temp.		E	—	—	±0.2	% FS
				B/F	—	—	±0.3	
				C/G	—	—	±0.5	
Full-Scale Tempco	TCV_{FS}	Total Internal Ref Connected		B	—	±45	±90	ppm/°C
				E/F/G	—	±45	±100	
				C	—	±60	±120	
		Zero Drift Ext Ref Applied		All	—	±30	—	ppm/°C
Settling Time	t_S	To ±1/2 LSB, 10V Step		All	—	1.5	—	μs
Unipolar Zero-Scale Output	V_{ZS}	Short Pin 18 to Ground (Note 1)	$T_A = 25°C$	All	—	±1	±5	mV
			T_A = Full Temp.	All	—	±2	±10	mV
Bipolar Offset Voltage	BP Off	Connect Pins 15, 17 & 18 (Note 3)		All	−5	—	+2.5	% Range
Full Range Output Voltage	V_{FR}	Connect Pin 15 to 17 (Note 2) $R_L = 2k\Omega$		All	10	—	11.5	V
Reference Input Bias Current	I_B			All	—	100	—	nA
Reference Input Impedance	Z_{IN}			All	—	200	—	MΩ
Reference Input Slew Rate	SR			All	—	1.5	—	V/μs
Reference Output Voltage	V_{REF}			All	—	6.7	—	V
Logic Input Current	I_{IN}	Each Input −5V to (V+ −0.7)V		All	—	1	10	μA
Logic Input "0"	V_{INL}			All	—	—	0.8	V
Logic Input "1"	V_{INH}			All	2	—	—	V
Power Supply Sensitivity	P_{SS}	$V_S = \pm 12V$ to $\pm 18V$	$T_A = 25°C$	All	—	±0.02	±0.05	% FS/V
			T_A = Full Temp.	All	—	±0.02	±0.1	% FS/V
Supply Current	I+	$T_A = 25°C$		All	—	7	10	mA
	I−			All	—	−9	−10	mA
Power Dissipation	P_D		$T_A = 25°C$	All	—	250	300	mW
			T_A = Full Temp.	All	—	—	350	mW

NOTES:

1. May be operated in the 0 to +10V unipolar mode by shorting Pin 18 to Ground.
2. $V_{FR} = |V_{FR}+| + |V_{FR}-|$ and is trimmable to exactly 10V range with the circuit shown in typical applications.
3. Bipolar offset voltage is trimmable to exact two's or one's complement condition with the circuit shown in typical applications.

TYPICAL APPLICATIONS

ADJUSTING FOR TWO'S COMPLEMENT CODING

1. Connect Full-Scale Adjust and Bipolar Adjust Circuitry as shown in figure.
2. Turn all bits OFF (V_{FS-} −1LSB) = 1000000000
3. Adjust Bipolar Pot for V_{FS} at output .... −5.000V
4. Turn all bits ON (V_{FR+}) = 0111111111
5. Adjust Full-Scale Pot for desired V_{FR+} value .... +4.990V
6. Check Zero-Scale Reading (V_{ZS}) = 0000000000
   If this reading is outside desired V_{ZS} range, readjust Bipolar Pot until the output reads 0.0000V.

TWO'S COMPLEMENT CODING TABLE

	INPUT										IDEAL
	MSB									LSB	OUTPUT
V_{FS+} −1LSB	0	1	1	1	1	1	1	1	1	1	+4.990V
V_{FS+} −2LSB	0	1	1	1	1	1	1	1	1	0	+4.980V
+1LSB	0	0	0	0	0	0	0	0	0	1	+0.010V
Zero	0	0	0	0	0	0	0	0	0	0	0.000V
−1LSB	1	1	1	1	1	1	1	1	1	1	−0.010V
V_{FS-} +1LSB	1	0	0	0	0	0	0	0	0	1	−4.990V
V_{FS-}	1	0	0	0	0	0	0	0	0	0	−5.000V

ADJUSTING FOR ONE'S COMPLEMENT CODING

1. Connect Full-Scale Adjust and Bipolar Adjust Circuitry as shown in above figure.
2. Turn all bits OFF (V_{FR-}) = 1000000000
3. Adjust Bipolar Pot for V_{FR-} at output .... −5.0000V
4. Turn all bits ON (V_{FR+}) = 0111111111
5. Adjust Full-Scale Pot for desired V_{FR+} value .... +5.0000V

ONE'S COMPLEMENT CODING TABLE

	INPUT										IDEAL
	MSB									LSB	OUTPUT
V_{FS+} −1LSB	0	1	1	1	1	1	1	1	1	1	+5.000V
V_{FS+} −2LSB	0	1	1	1	1	1	1	1	1	0	+4.990V
+0	0	0	0	0	0	0	0	0	0	0	+0.005V
−0	1	1	1	1	1	1	1	1	1	1	−0.005V
V_{FS-} +2LSB	1	0	0	0	0	0	0	0	0	1	−4.990V
V_{FS-} +1LSB	1	0	0	0	0	0	0	0	0	0	−5.000V

Note that two zero states will straddle (±1/2 LSB) the true zero. Therefore the DAC will give symmetrical outputs for both positive and negative full-scale.

REFERENCE OUTPUT

For best results, reference output current should not exceed 100μA.

POWER SUPPLIES

The DAC-06 will operate within specifications for power supplies ranging from ±12V to ±18V. Power supplies should be bypassed near the package with a 0.1μF disk capacitor. Chip users should connect the substrate to V−.

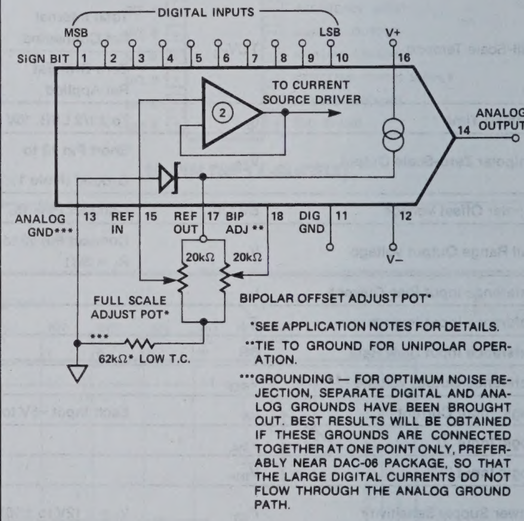
GROUNDING

For optimum noise rejection, separate digital and analog grounds have been brought out. Best results will be obtained if these grounds are connected together at one point only, preferably at the DAC-06 package, so that large digital currents do not flow through the analog ground path.

CAPACITIVE LOADING

The output operational amplifier provides stable operation with capacitive loads up to 100pF.

FULL-SCALE OUTPUT RANGE AND BIPOLAR OFFSET ADJUSTMENT CIRCUIT



*SEE APPLICATION NOTES FOR DETAILS.

**TIE TO GROUND FOR UNIPOLAR OPERATION.

***GROUNDING — FOR OPTIMUM NOISE REJECTION, SEPARATE DIGITAL AND ANALOG GROUNDS HAVE BEEN BROUGHT OUT. BEST RESULTS WILL BE OBTAINED IF THESE GROUNDS ARE CONNECTED TOGETHER AT ONE POINT ONLY, PREFERABLY NEAR DAC-06 PACKAGE, SO THAT THE LARGE DIGITAL CURRENTS DO NOT FLOW THROUGH THE ANALOG GROUND PATH.

EXTERNAL ADJUSTMENT NETWORK

Full-scale output range and bipolar offset may be adjusted by using the circuit shown in the figure above. Best results will be obtained when low tempco pots and resistors are used, or if pot and resistor tempcos match.

CODE CONVERSION TO OFFSET BINARY

Offset binary coding is exactly the same as two's complement coding except that the most significant bit occurs in true, rather than inverted form and the output states are relabeled. To convert the DAC-06 to offset binary code operation, simply place a logic inverter in series with the MSB input (Pin 1) and invert the MSB value shown in steps 2, 4 and 6 of the two's complement adjustment procedure shown above.

OFFSET BINARY CODING TABLE

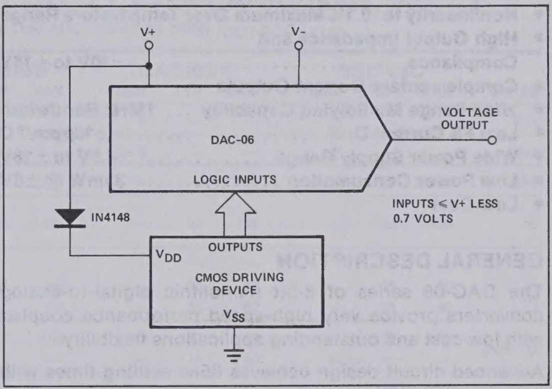
	INPUT										IDEAL
	MSB									LSB	OUTPUT
$V_{FS+}-1LSB$	1	1	1	1	1	1	1	1	1	1	+4.990V
$V_{FS+}-2LSB$	1	1	1	1	1	1	1	1	1	0	+4.980V
ZERO	1	0	0	0	0	0	0	0	0	0	0.00
−1LSB	0	1	1	1	1	1	1	1	1	1	−0.005V
$V_{FS-}+1LSB$	0	0	0	0	0	0	0	0	0	1	−4.990V
V_{FS-}	0	0	0	0	0	0	0	0	0	0	−5.000V

INTERFACING WITH CMOS LOGIC

The DAC-06 logic input stages require about 1μA and are capable of operation with inputs between −5 volts and V+ less 0.7 volt. This wide input voltage range allows direct CMOS interfacing in most applications, the exception being where the CMOS logic and D/A converter must use the same positive power supply.

In this special case, a diode should be placed in series with the CMOS driving device's V_{DD} lead as shown in Figure 1. The diode limits V_D to V+ less 0.7 volt — since the output from the CMOS device cannot exceed this value, the DAC's maximum input voltage rule is satisfied. Summarizing: in all applications, the DAC-06 requires either no interfacing components, or at most a single inexpensive diode for full CMOS compatibility.

CMOS LOGIC INTERFACE CIRCUIT



DAC-08 8-BIT HIGH-SPEED MULTIPLYING D/A CONVERTER (UNIVERSAL DIGITAL LOGIC INTERFACE)

FEATURES

- **Fast Settling Output Current 85ns**
- **Full-Scale Current Prematched to ±1 LSB**
- **Direct Interface to TTL, CMOS, ECL, HTL, PMOS**
- **Nonlinearity to 0.1% Maximum Over Temperature Range**
- **High Output Impedance and Compliance .... −10V to +18V**
- **Complementary Current Outputs**
- **Wide Range Multiplying Capability ... 1MHz Bandwidth**
- **Low FS Current Drift .... ±10ppm/° C**
- **Wide Power Supply Range .... ±4.5V to ±18V**
- **Low Power Consumption .... 33mW @ ±5V**
- **Low Cost**

GENERAL DESCRIPTION

The DAC-08 series of 8-bit monolithic digital-to-analog converters provide very high-speed performance coupled with low cost and outstanding applications flexibility.

Advanced circuit design achieves 85ns settling times with very low "glitch" energy and at low power consumption. Monotonic multiplying performance is attained over a wide 20 to 1 reference current range. Matching to within 1 LSB between reference and full-scale currents eliminates the need for full-scale trimming in most applications. Direct interface to all popular logic families with full noise immunity is provided by the high swing, adjustable threshold logic input.

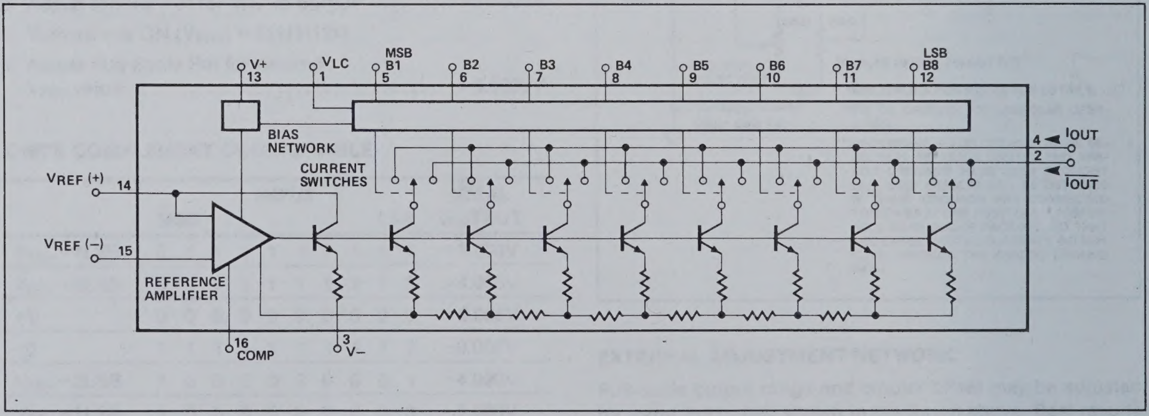
High voltage compliance complementary current outputs are provided, increasing versatility and enabling differential operation to effectively double the peak-to-peak output swing. In many applications, the outputs can be directly converted to voltage without the need for an external op amp.

All DAC-08 series models guarantee full 8-bit monotonicity, and nonlinearities as tight as ±0.1% over the entire operating temperature range are available. Device performance is essentially unchanged over the ±4.5 to ±18V power supply range, with 33mW power consumption attainable at ±5V supplies.

The compact size and low power consumption make the DAC-08 attractive for portable and military/aerospace applications; devices processed to MIL-STD-883, Level B are available.

DAC-08 applications include 8-bit, 1μs A/D converters, servo motor and pen drivers, waveform generators, audio encoders and attenuators, analog meter drivers, programmable power supplies, CRT display drivers, high-speed modems and other applications where low cost, high speed and complete input/output versatility are required.

EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Operating Temperature	
DAC-08AQ, Q	−55°C to +125°C
DAC-08HQ, EQ, CQ, HP, EP, CP	0°C to +70°C
DICE Junction Temperature (T_j)	−65°C to +150°C
Storage Temperature Q Package	−65°C to 150°C
Storage Temperature P Package	−65°C to +125°C
Power Dissipation*	500mW
Derate above 100°C	10mW/°C
Lead Temperature (Soldering, 60 sec)	300°C
V+ Supply to V− Supply	36V
Logic Inputs	V− to V− plus 36V
V_{LC}	V− to V+
Analog Current Outputs (at V_S− = 15V)	4.25mA
Reference Input (V_{14} to V_{15})	V− to V+
Reference Input Differential Voltage (V_{14} to V_{15})	±18V
Reference Input Current (I_{14})	5.0mA

NOTE: Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $I_{REF} = 2.0mA$, $-55°C \le T_A \le +125°C$ for DAC-08/08A, $0°C \le T_A \le +70°C$ for DAC-08C, E & H, unless otherwise noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

			DAC-08A/H			DAC-08/E			DAC-08C			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Resolution			8	—	—	8	—	—	8	—	—	Bits
Monotonicity			8	—	—	8	—	—	8	—	—	Bits
Nonlinearity			—	—	±0.1	—	—	±0.19	—	—	±0.39	%FS
Settling Time	t_S	To ±1/2 LSB, all bits switched ON or OFF, $T_A = 25°C$ (See Note)	—	85	135	—	85	150	—	85	150	ns
Propagation Delay												
Each bit	t_{PLH}	$T_A = 25°C$	—	35	60	—	35	60	—	35	60	ns
All bits switched	t_{PHL}	(See Note)	—	35	60	—	35	60	—	35	60	
Full-Scale Tempco	TCI_{FS}		—	±10	±50	—	±10	±80	—	±10	±80	ppm/°C
		DAC-08E	—	—	—	—	—	±50	—	—	—	
Output Voltage Compliance (True Compliance)	V_{OC}	Full-Scale current change <1/2 LSB, $R_{OUT} > 20M\Omega$ typical	−10	—	+18	−10	—	+18	−10	—	−18	Volts
Full Range Current	I_{FR4}	$V_{REF} = 10.000V$ $R_{14}, R_{15} = 5.000k\Omega$ $T_A = +25°C$	1.984	1.992	2.000	1.94	1.99	2.04	1.94	1.99	2.04	mA
Full Range Symmetry	I_{FRS}	$I_{FR4} - I_{FR2}$	—	±0.5	±4	—	±1	±8	—	±2	±16	μA
Zero-Scale Current	I_{ZS}		—	0.1	1	—	0.2	2	—	0.2	4	μA
Output Current Range	IOR_1	$R_{14}, R_{15} = 5.000k\Omega$ $V_{REF} = +15.0V$, $V- = -10V$	2.1	—	—	2.1	—	—	2.1	—	—	mA
	IOR_2	$V_{REF} = +25.0V$, $V- = -12V$	4.2	—	—	4.2	—	—	4.2	—	—	
Output Current Noise		$I_{REF} = 2mA$	—	25	—	—	25	—	—	25	—	nA
Logic Input Levels												
Logic "0"	V_{IL}	$V_{LC} = 0V$	—	—	0.8	—	—	0.8	—	—	0.8	Volts
Logic Input "1"	V_{IL}		2	—	—	2	—	—	2	—	—	
Logic Input Current		$V_{LC} = 0V$										
Logic "0"	I_{IL}	$V_{IN} = -10V$ to $+0.8V$	—	−2	−10	—	−2	−10	—	−2	−10	μA
Logic Input "1"	I_{IH}	$V_{IN} = 2.0V$ to 18V	—	0.002	10	—	0.002	10	—	0.002	10	
Logic Input Swing	V_{IS}	$V- = -15V$	−10	—	+18	−10	—	+18	−10	—	+18	Volts
Logic Threshold Range	V_{THR}	$V_S = \pm 15V$ (Note)	−10	—	+13.5	−10	—	+13.5	−10	—	+13.5	Volts
Reference Bias Current	I_{15}		—	−1	−3	—	−1	−3	—	−1	−3	μA
Reference Input Slew Rate	dI/dt	$R_{EQ} = 200\Omega$ See fast pulsed $R_L = 100\Omega$ ref. info. $C_C = 0pF$ following.	4	8	—	4	8	—	4	8	—	mA/μs
Power Supply Sensitivity	$PSSI_{FS+}$	$V+ = 4.5V$ to 18V	—	±0.0003	±0.01	—	±0.0003	±0.01	—	±0.0003	±0.01	$\%\Delta I_O/\%\Delta V+$
	$PSSI_{FS-}$	$V- = -4.5V$ to $-18V$ $I_{REF} = 1.0mA$	—	±0.002	±0.01	—	±0.002	±0.01	—	±0.002	±0.01	$\%\Delta I_O/\%\Delta V-$

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $I_{REF} = 2.0mA$, $-55°C \leq T_A \leq +125°C$ for DAC-08/08A, $0°C \leq T_A \leq +70°C$ for DAC-08C, E & H, unless otherwise noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$. (Continued)

			DAC-08A/H			DAC-08/E			DAC-08C			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Power Supply Current	I+	$V_S = \pm5V$, $I_{REF} = 1.0mA$	—	2.3	3.8	—	2.3	3.8	—	2.3	3.8	mA
	I-		—	-4.3	-5.8	—	-4.3	-5.8	—	-4.3	-5.8	
	I+	$V_S = +5V, -15V$, $I_{REF} = 2.0mA$	—	2.4	3.8	—	2.4	3.8	—	2.4	3.8	
	I-		—	-6.4	-7.8	—	-6.4	-7.8	—	-6.4	-7.8	
	I+	$V_S = \pm15V$, $I_{REF} = 2.0mA$	—	2.5	3.8	—	2.5	3.8	—	2.5	3.8	
	I-		—	-6.5	-7.8	—	-6.5	-7.8	—	6.5	7.8	
Power Dissipation	P_d	$\pm5V$, $I_{REF} = 1.0mA$	—	33	48	—	33	48	—	33	48	mW
		$+5V, -5V$, $I_{REF} = 2.0mA$	—	108	136	—	103	136	—	108	136	
		$\pm15V$, $I_{REF} = 2.0mA$	—	135	174	—	135	174	—	135	174	

NOTE: Guaranteed by design.

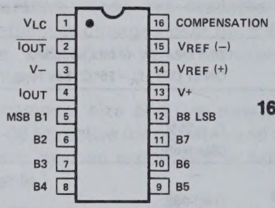
ORDERING INFORMATION†

	16-PIN DUAL-IN-LINE PACKAGE		OPERATING TEMPERATURE RANGE
NL	HERMETIC	PLASTIC	
0.1%	DAC08AQ* DAC08HQ	DAC08HP	MIL COM
0.1%	DAC08Q* DAC08EQ	DAC08EP	MIL COM
0.39%	DAC08CQ	DAC08CP	COM

*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

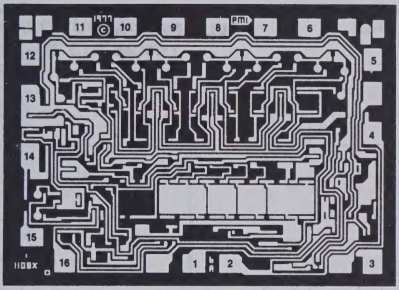
†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

PIN CONNECTIONS



16-PIN DUAL-IN-LINE PACKAGE

DICE CHARACTERISTICS (125°C TESTED DICE AVAILABLE)



DIE SIZE 0.085 × 0.062 inch, 5,270 sq. mils
(2.159 × 1.575 mm, 3.4 sq. mm)

1. **V_{LC}**
2. **$\overline{I_{OUT}}$**
3. **V−**
4. **I_{OUT}**
5. **BIT 1 (MSB)**
6. **BIT 2**
7. **BIT 3**
8. **BIT 4**
9. **BIT 5**
10. **BIT 6**
11. **BIT 7**
12. **BIT 8 (LSB)**
13. **V+**
14. **V_{REF} (+)**
15. **V_{REF} (−)**
16. **COMP**

For additional DICE information refer to Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $I_{REF} = 2.0mA$, $T_A = 125°C$ for DAC-08NT, DAC-08GT devices; $T_A = 25°C$ for DAC-08N, DAC-08G and DAC-08GR devices, unless otherwise noted. Output characteristics apply to both I_{OUT} and $\overline{I_{OUT}}$.

PARAMETER	SYMBOL	CONDITIONS	DAC-08NT LIMIT	DAC-08N LIMIT	DAC-08GT LIMIT	DAC-08G LIMIT	DAC-08GR LIMIT	UNITS
Resolution			8	8	8	8	8	Bits MIN
Monotonicity			8	8	8	8	8	Bits MIN
Nonlinearity			±0.1	±0.1	±0.19	±0.19	±0.39	%FS MAX
Output Voltage Compliance	V_{OC}	Full-Scale Current Change < 1/2 LSB	+18 −10	+18 −10	+18 −10	+18 −10	+18 −10	Volts MAX Volts MIN
Full-Scale Current	I_{FS4} or I_{FS2}	$V_{REF} = 10.000V$ $R_{14}, R_{15} = 5.000k\Omega$	2.04 1.94	2.04 1.94	2.04 1.94	2.04 1.94	2.04 1.94	mA MAX mA MIN
Full-Scale Symmetry	I_{FSS}		±8	±8	±8	±8	±16	nA MAX
Zero-Scale Current	I_{ZS}		2	2	4	4	4	nA MAX
Output Current Range	I_{FS1} or	$V- = -10V$, $V_{REF} = +15V$	2.1	2.1	2.1	2.1	2.1	mA MIN
	I_{FS2}	$V- = -12V$, $V_{REF} = +25V$ $R_{14}, R_{15} = 5.000k\Omega$	4.2	4.2	4.2	4.2	4.2	mA MIN
Logic Input "0"	V_{IL}		0.8	0.8	0.8	0.8	0.8	V MAX
Logic Input "1"	V_{IH}		2	2	2	2	2	V MIN
Logic Input Current		$V_{LC} = 0V$						
Logic "0"	V_{IL}	$V_{IN} = -10V$ to $+0.8V$	±10	±10	±10	±10	±10	µA MAX
Logic "1"	I_{IH}	$V_{IN} = 2.0V$ to $18V$	±10	±10	±10	±10	±10	
Logic Input Swing	V_{IS}	$V- = -15V$	+18 −10	+18 −10	+18 −10	+18 −10	+18 −10	V MAX V MIN
Reference Bias Current	I_{15}		−3	−3	−3	−3	−3	µA MAX
Power Supply Sensitivity	$PSSI_{FS+}$ $PSSI_{FS-}$	$V+ = 4.5V$ to $18V$ $V- = -4.5V$ to $-18V$ $I_{REF} = 1.0mA$	0.01	0.01	0.01	0.01	0.01	%FS/%V MAX
Power Supply Current	I+ I−	$V_S = \pm 15V$ $I_{REF} \leq 2.0mA$	3.8 −7.8	3.8 −7.8	3.8 −7.8	3.8 −7.8	3.8 −7.8	mA MAX
Power Dissipation	P_d	$V_S = \pm 15V$ $I_{REF} \leq 2.0mA$	174	174	174	174	174	mW MAX

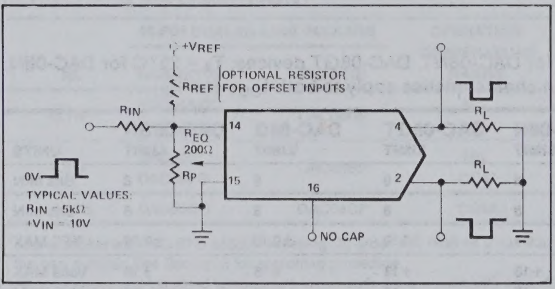
Note: Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, and $I_{REF} = 2.0mA$, unless otherwise noted. Output characteristics apply to both I_{OUT} and $\overline{I_{OUT}}$.

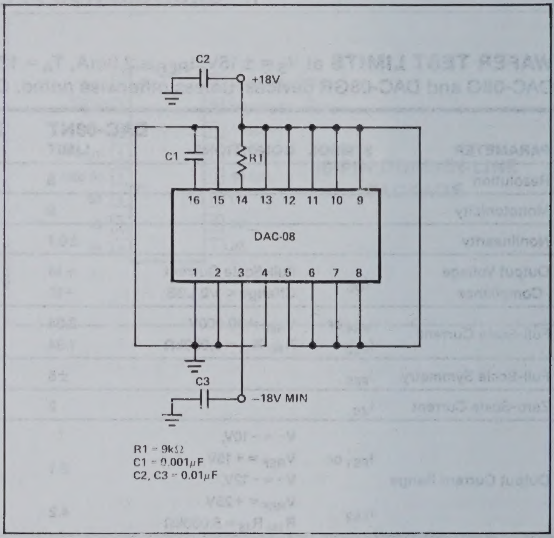
PARAMETER	SYMBOL	CONDITIONS	ALL GRADES TYPICAL	UNITS
Reference Input Slew Rate	dI/dt		8	mA/μs
Propagation Delay	t_{PLH}, t_{PHL}	T_A = 25°C, Any Bit	35	ns
Settling Time	t_S	To ±1/2 LSB, All Bits Switched ON or OFF, T_A = 25°C	85	ns

NOTE:
For DAC08NT & GT 25°C characteristics, see DAC08N & G characteristics respectively.

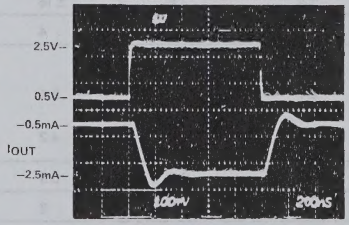
PULSED REFERENCE OPERATION


+VREF
OPTIONAL RESISTOR FOR OFFSET INPUTS
RREF
RIN
REQ 200Ω
RP
14
15
16
4
2
RL
RL
0V
NO CAP
TYPICAL VALUES:
RIN = 5kΩ
+VIN = 10V

BURN-IN CIRCUIT

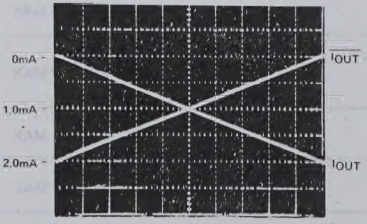

C2
+18V
C1
R1
16 15 14 13 12 11 10 9
DAC-08
1 2 3 4 5 6 7 8
C3
−18V MIN
R1 = 9kΩ
C1 = 0.001μF
C2, C3 = 0.01μF

FAST PULSED REFERENCE OPERATION



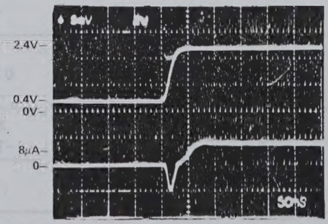
$R_{EQ} \approx 200\Omega$ 200NSEC/DIVISION
$R_L = 100\Omega$
$C_C = 0$

TRUE AND COMPLEMENTARY OUTPUT OPERATION



(0000|0000) I_{REF} = 2mA (1111|1111)

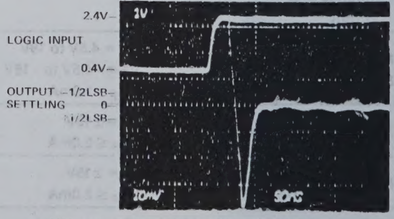
LSB SWITCHING



50NSEC/DIVISION

FULL-SCALE SETTLING TIME

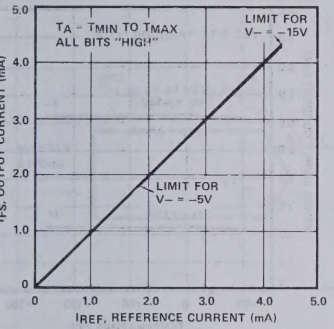
ALL BITS SWITCHED ON



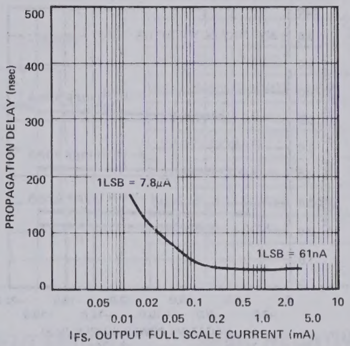
SETTLING TIME FIXTURE 50NSEC/DIVISION
I_{FS} = 2mA, R_L = 1kΩ
1/2LSB = 4μA

TYPICAL PERFORMANCE CHARACTERISTICS

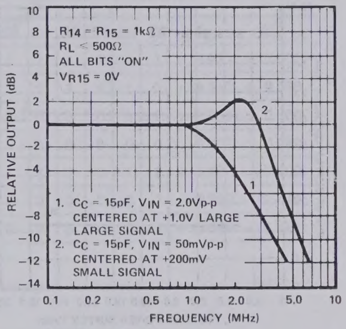
FULL-SCALE CURRENT vs REFERENCE CURRENT



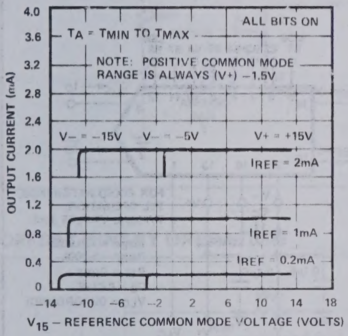
LSB PROPAGATION DELAY vs I_{FS}



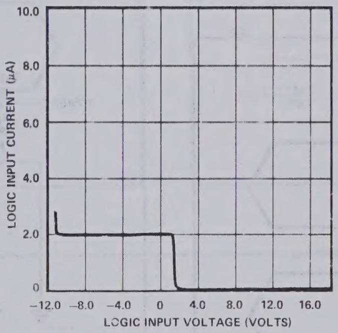
REFERENCE INPUT FREQUENCY RESPONSE



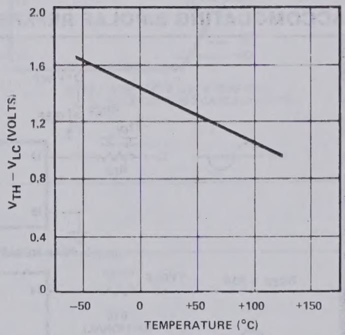
REFERENCE AMP COMMON-MODE RANGE



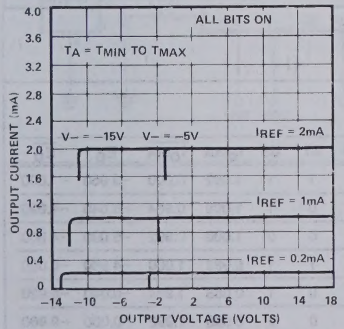
LOGIC INPUT CURRENT vs INPUT VOLTAGE



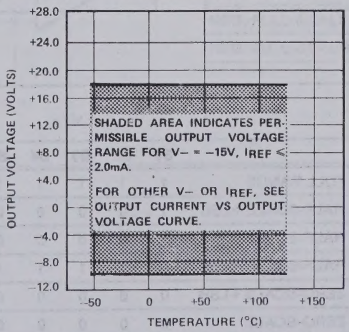
$V_{TH} - V_{LC}$ vs TEMPERATURE



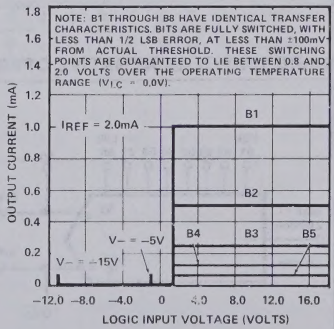
OUTPUT CURRENT vs OUTPUT VOLTAGE (OUTPUT VOLTAGE COMPLIANCE)



OUTPUT VOLTAGE COMPLIANCE vs TEMPERATURE

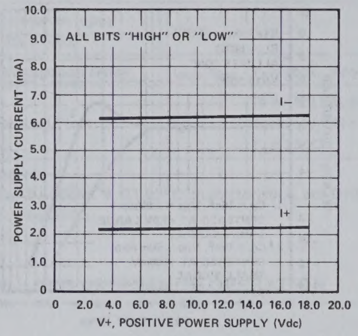


BIT TRANSFER CHARACTERISTICS

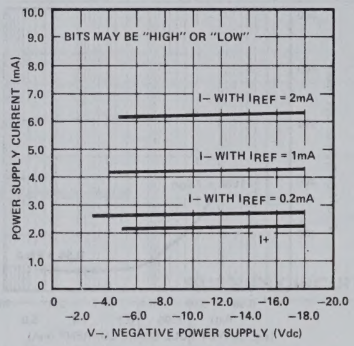


TYPICAL PERFORMANCE CHARACTERISTICS

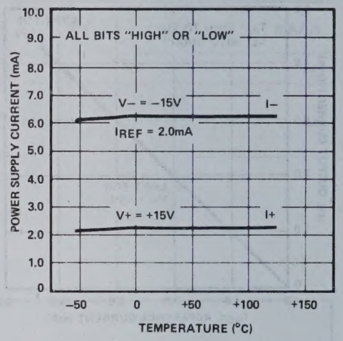
POWER SUPPLY CURRENT vs V+



POWER SUPPLY CURRENT vs V−

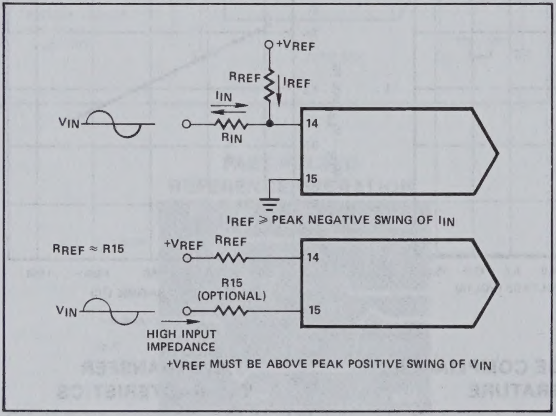


POWER SUPPLY CURRENT vs TEMPERATURE

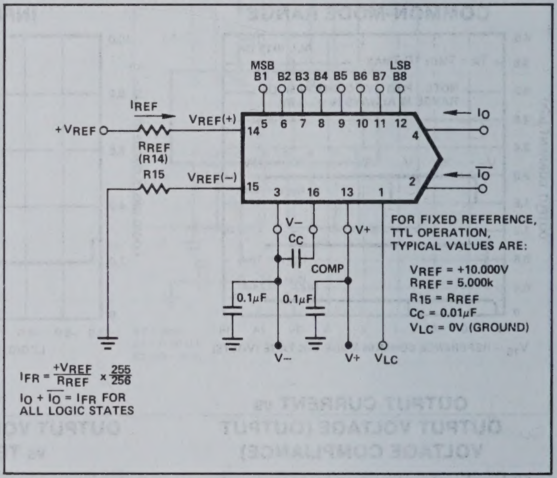


BASIC CONNECTIONS

ACCOMODATING BIPOLAR REFERENCES


+VREF
RREF
IREF
IIN
VIN
RIN
14
15
IREF ≥ PEAK NEGATIVE SWING OF IIN
RREF ≈ R15
+VREF
RREF
14
R15
(OPTIONAL)
VIN
15
HIGH INPUT IMPEDANCE
+VREF MUST BE ABOVE PEAK POSITIVE SWING OF VIN

BASIC POSITIVE REFERENCE OPERATION


MSB
LSB
B1 B2 B3 B4 B5 B6 B7 B8
IREF
+VREF
RREF
(R14)
R15
VREF(+)
VREF(−)
14
5 6 7 8 9 10 11 12
15
3 16 13 1
4
2
IO
IO
V−
CC
V+
COMP
0.1μF
0.1μF
V−
V+
VLC

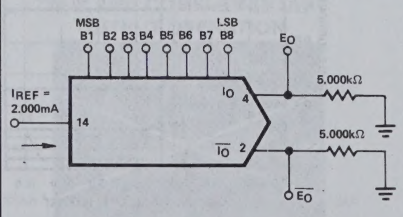
FOR FIXED REFERENCE, TTL OPERATION, TYPICAL VALUES ARE:

$V_{REF} = +10.000V$
$R_{REF} = 5.000k$
$R_{15} = R_{REF}$
$C_C = 0.01\mu F$
$V_{LC} = 0V$ (GROUND)

$$I_{FR} = \frac{+V_{REF}}{R_{REF}} \times \frac{255}{256}$$

$I_O + \overline{I_O} = I_{FR}$ FOR ALL LOGIC STATES

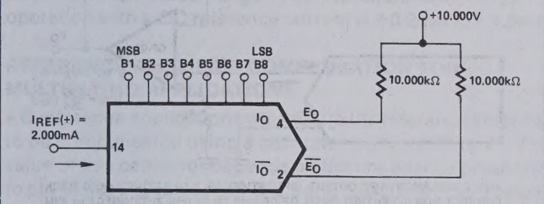
BASIC UNIPOLAR NEGATIVE OPERATION


MSB
LSB
B1 B2 B3 B4 B5 B6 B7 B8
EO
IREF = 2.000mA
14
IO
4
5.000kΩ
5.000kΩ
IO
2
EO

	B1	B2	B3	B4	B5	B6	B7	B8	I_OmA	$\overline{I_O}$mA	E_O	$\overline{E_O}$
FULL RANGE	1	1	1	1	1	1	1	1	1.992	0.000	-9.960	- .000
HALF-SCALE +LSB	1	0	0	0	0	0	0	1	1.008	0.984	-5.040	-4.920
HALF-SCALE	1	0	0	0	0	0	0	0	1.000	0.992	-5.000	-4.960
HALF-SCALE -LSB	0	1	1	1	1	1	1	1	0.992	1.000	-4.960	-5.000
ZERO-SCALE +LSB	0	0	0	0	0	0	0	1	0.008	1.984	-0.040	-9.920
ZERO-SCALE	0	0	0	0	0	0	0	0	0.000	1.992	0.000	-9.960

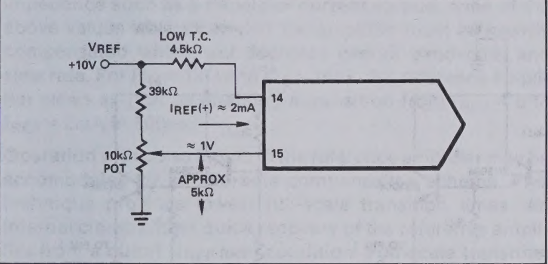
BASIC CONNECTIONS

BASIC BIPOLAR OUTPUT OPERATION

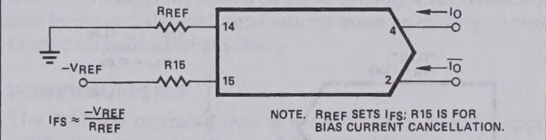

+10.000V
MSB
B1 B2 B3 B4 B5 B6 B7 B8
LSB
10.000kΩ
10.000kΩ
$I_{REF}(+)$ = 2.000mA
14
I_O 4
E_O
$\overline{I_O}$ 2
$\overline{E_O}$

	B1	B2	B3	B4	B5	B6	B7	B8	E_O	$\overline{E_O}$
POS. FULL RANGE	1	1	1	1	1	1	1	1	− 9.920	+10.000
POS. FULL RANGE − LSB	1	1	1	1	1	1	1	0	− 9.840	+ 9.920
ZERO-SCALE + LSB	1	0	0	0	0	0	0	1	− 0.080	+ 0.160
ZERO-SCALE	1	0	0	0	0	0	0	0	0.000	+ 0.080
ZERO-SCALE − LSB	0	1	1	1	1	1	1	1	+ 0.080	0.000
NEG. FULL-SCALE + LSB	0	0	0	0	0	0	0	1	+ 9.920	9.840
NEG. FULL-SCALE	0	0	0	0	0	0	0	0	+10.000	− 9.920

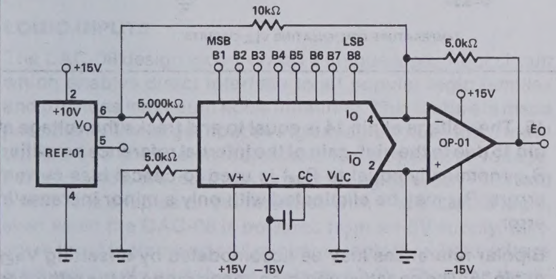
RECOMMENDED FULL-SCALE ADJUSTMENT CIRCUIT


V_{REF}
+10V
LOW T.C.
4.5kΩ
39kΩ
$I_{REF}(+) \approx$ 2mA
14
≈ 1V
10kΩ
POT
15
APPROX
5kΩ

BASIC NEGATIVE REFERENCE OPERATION


R_{REF}
14
4
I_O
$-V_{REF}$
R15
15
2
$\overline{I_O}$
$I_{FS} \approx \frac{-V_{REF}}{R_{REF}}$
NOTE, R_{REF} SETS I_{FS}; R15 IS FOR BIAS CURRENT CANCELLATION.

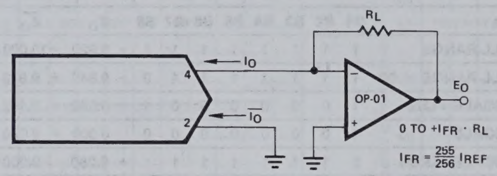
OFFSET BINARY OPERATION


10kΩ
MSB
B1 B2 B3 B4 B5 B6 B7 B8
LSB
5.0kΩ
+15V
2
+10V
V_O
6
5.000kΩ
5
REF-01
4
5.0kΩ
I_O 4
$\overline{I_O}$ 2
+15V
OP-01
E_O
V+ V− C_C V_{LC}
+15V −15V
−15V

	B1	B2	B3	B4	B5	B6	B7	B8	E_O
POS. FULL RANGE	1	1	1	1	1	1	1	1	+4.960
ZERO-SCALE	1	0	0	0	0	0	0	0	0.000
NEG. FULL-SCALE + 1 LSB	0	0	0	0	0	0	0	1	−4.960
NEG. FULL-SCALE	0	0	0	0	0	0	0	0	−5.000

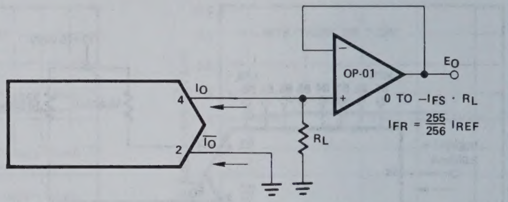
BASIC CONNECTIONS

POSITIVE LOW IMPEDANCE OUTPUT OERATION


RL
IO
4
2
$\overline{I_O}$
OP-01
EO
0 TO +IFR · RL
$I_{FR} = \frac{255}{256} I_{REF}$

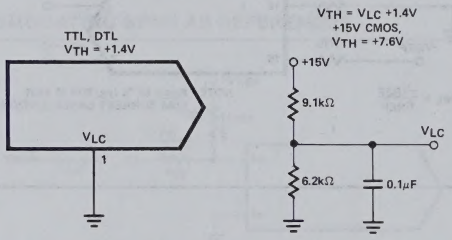
FOR COMPLEMENTARY OUTPUT (OPERATION AS A NEGATIVE LOGIC DAC), CONNECT INVERTING INPUT OF OP-AMP TO $\overline{I_O}$ (PIN 2); CONNECT I_O (PIN 4) TO GROUND.

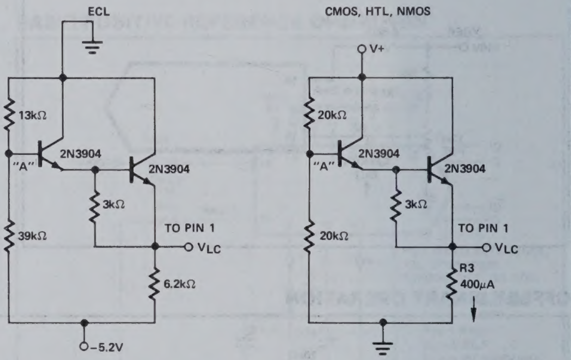
NEGATIVE LOW IMPEDANCE OUTPUT OPERATION


OP-01
EO
IO
4
0 TO $-I_{FS} \cdot R_L$
$I_{FR} = \frac{255}{256} I_{REF}$
RL
2
$\overline{I_O}$

FOR COMPLEMENTARY OUTPUT (OPERATION AS A NEGATIVE LOGIC DAC), CONNECT NON-INVERTING INPUT OF OP-AMP TO I_O (PIN 2); CONNECT I_O (PIN 4) TO GROUND.

INTERFACING WITH VARIOUS LOGIC FAMILIES


TTL, DTL
VTH = +1.4V
VTH = VLC +1.4V
+15V CMOS,
VTH = +7.6V
+15V
9.1kΩ
VLC
VLC
1
6.2kΩ
0.1μF


ECL
13kΩ
"A"
2N3904
2N3904
3kΩ
39kΩ
TO PIN 1
VLC
6.2kΩ
−5.2V
CMOS, HTL, NMOS
V+
20kΩ
"A"
2N3904
2N3904
3kΩ
20kΩ
TO PIN 1
VLC
R3
400μA

TEMPERATURE COMPENSATING V_{LC} CIRCUITS

APPLICATIONS INFORMATION

REFERENCE AMPLIFIER SET-UP

The DAC-08 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to +4.0mA. The full-scale output current is a linear function of the reference current and is given by:

$$I_{FR} = \frac{255}{256} \times I_{REF}, \text{ where } I_{REF} = I_{14}.$$

In positive reference applications, an external positive reference voltage forces current through R_{14} into the $V_{REF(+)}$ terminal (pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to $V_{REF(-)}$ at pin 15; reference current flows from ground through R_{14} into $V_{REF(+)}$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin 15. The voltage at pin 14 is equal to and tracks the voltage at pin 15 due to the high gain of the internal reference amplifier. R_{15} (nominally equal to R_{14}) is used to cancel bias current errors; R_{15} may be eliminated with only a minor increase in error.

Bipolar references may be accomodated by offsetting V_{REF} or pin 15. The negative common-mode range of the reference amplifier is given by: V_{CM-} = V− plus ($I_{REF} \times 1k\Omega$) plus 2.5V. The positive common-mode range is V+ less 1.5V.

When a DC reference is used, a reference bypass capacitor is recommended. A 5.0V TTL logic supply is not recommended as a reference. if a regulated power supply is used as a reference, R_{14} should be split into two resistors with the junction bypassed to ground with a 0.1μF capacitor.

For most applications the tight relationship between I_{REF} and I_{FS} will eliminate the need for trimming I_{REF}. If required, full-scale trimming may be accomplished by adjusting the value of R_{14}, or by using a potentiometer for R_{14}. An improved method of full-scale trimming which eliminates potentiometer T.C. effects is shown in the recommended full-scale adjustment circuit.

Using lower values of reference current reduces negative power supply current and increases reference amplifier negative common-mode range. The recommended range for operation with a DC reference current is +0.2mA to +4.0mA.

REFERENCE AMPLIFIER COMPENSATION FOR MULTIPLYING APPLICATIONS

AC reference applications will require the reference amplifier to be compensated using a capacitor from pin 16 to V−. The value of this capacitor depends on the impedance presented to pin 14: for R_{14} values of 1.0, 2.5 and 5.0kΩ, minimum values of C_C are 15, 37, and 75pF. Larger values of R_{14} require proportionately increased values of C_C for proper phase margin, such that the ratio of C_C(pF) to R_{14} (kΩ) = 15.

For fastest response to a pulse, low values of R_{14} enabling small C_C values should be used. If pin 14 is driven by a high impedance such as a transistor current source, none of the above values will suffice and the amplifier must be heavily compensated which will decrease overall bandwidth and slew rate. For R_{14} = 1kΩ and C_C = 15pF, the reference amplifier slews at 4mA/μs enabling a transition from I_{REF} = 0 to I_{REF} = 2mA in 500ns.

Operation with pulse inputs to the reference amplifier may be accomodated by an alternate compensation scheme. This technique provides lowest full-scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff (I_{REF} = 0) condition. Full-scale transition (0 to 2mA) occurs in 120ns when the equivalent impedance at pin 14 is 200Ω and C_C = 0. This yields a reference slew rate of 16mA/μs which is relatively independent of R_{IN} and V_{IN} values.

LOGIC INPUTS

The DAC-08 design incorporates a unique logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 2μA logic input current and completely adjustable logic threshold voltage. For V− = −15V, the logic inputs may swing between −10V and +18V. This enables direct interface with +15V CMOS logic, even when the DAC-08 is powered from a +5V supply. Minimum input logic swing and minimum logic threshold voltage are given by: V− plus (I_{REF} × 1kΩ) plus 2.5V. The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control pin (pin 1, V_{LC}). The appropriate graph shows the relationship between V_{LC} and V_{TH} over the temperature range, with V_{TH} nominally 1.4 above V_{LC}. For TTL and DTL interface, simply ground pin 1. When interfacing ECL, an I_{REF} = 1mA is recommended. For interfacing other logic families, see preceding page. For general set-up of the logic control circuit, it should be noted that pin 1 will source 100μA typical; external circuitry should be designed to accommodate this current.

Fastest settling times are obtained when pin 1 sees a low impedance. If pin 1 is connected to a 1kΩ divider, for example, it should be bypassed to ground by a 0.01μF capacitor.

ANALOG OUTPUT CURRENTS

Both true and complemented output sink currents are provided where $I_O + \overline{I_O} = I_{FS}$. Current appears at the "true" (I_O) output when a "1" (logic high) is applied to each logic input. As the binary count increases, the sink current at pin 4 increases proportionally, in the fashion of a "positive logic" D/A converter. When a "0" is applied to any input bit, that current is turned off at pin 4 and turned on at pin 2. A decreasing logic count increases $\overline{I_O}$ as in a negative or inverted logic D/A converter. Both outputs may be used simultaneously. If one of the outputs is not required it must be connected to ground or to a point capable of sourcing I_{FS}; do not leave an unused output pin open.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 36V above V− and is independent of the positive supply. Negative compliance is given by V− plus (I_{REF} × 1kΩ) plus 2.5V.

The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection and in other balanced applications such as driving center-tapped coils and transformers.

POWER SUPPLIES

The DAC-08 operates over a wide range of power supply voltages from a total supply of 9V to 36V. When operating at supplies of ±5V or less, $I_{REF} \leq$ 1mA is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common-mode range, negative logic input range, and negative logic threshold range; consult the various figures for guidance. For example, operation at −4.5V with I_{REF} = 2mA is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible, however at least 8V total must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the DAC-08 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required: however, an artificial ground may be used to insure logic swings, etc. remain between acceptable limits.

Power consumption may be calculated as follows:

P_d = (I+) (V+) + (I−) (V−). A useful feature of the DAC-08 design is that supply current is constant and independent of input logic states; this is useful in cryptographic applications and further serves to reduce the size of the power supply bypass capacitors.

TEMPERATURE PERFORMANCE

The nonlinearity and monotonicity specifications of the DAC-08 are guaranteed to apply over the entire rated operating temperature range. Full-scale output current drift is low, typically ±10ppm/°C, with zero-scale output current and drift essentially negligible compared to 1/2 LSB.

The temperature coefficient of the reference resistor R_{14} should match and track that of the output resistor for minimum overall full-scale drift. Settling times of the DAC-08 decrease approximately 10% at −55° C; at +125° C an increase of about 15% is typical.

The reference amplifier must be compensated by using a capacitor from pin 16 to V−. For fixed reference operation, a 0.01μF capacitor is recommended. For variable reference applications, see previous section entitled "Reference Amplifier Compensation for Multiplying Applications".

MULTIPLYING OPERATION

The DAC-08 provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 4mA to 4μA. Monotonic operation is maintained over a typical range of I_{REF} from 100μA to 4.0mA.

SETTLING TIME

The DAC-08 is capable of extremely fast settling times, typically 85ns at $I_{REF} = 2.0$mA. Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The logic switch design enables propagation delays of only 35ns for each of the 8 bits. Settling time to within 1/2 LSB of the LSB is therefore 35ns, with each progressively larger bit taking successively longer. The MSB settles in 85ns, thus determining the overall settling time of 85ns. Settling to 6-bit accuracy requires about 65 to 70ns. The output capacitance of the DAC-08 including the package is approximately 15pF, therefore the output RC time constant dominates settling time if $R_L > 500\Omega$.

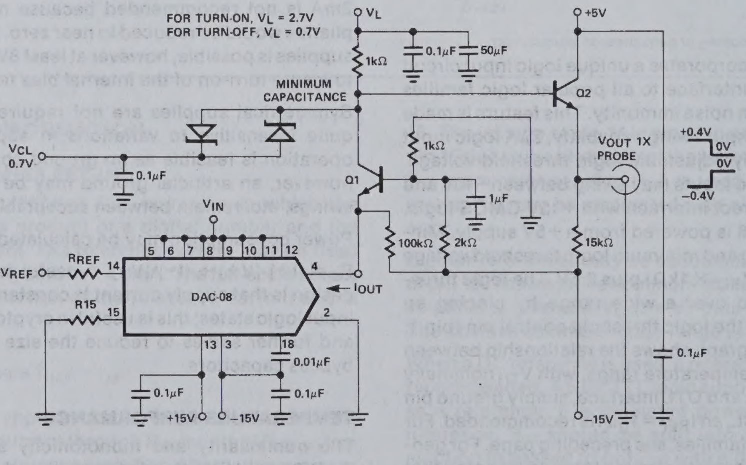
Settling time and propagation delay are relatively insensitive to logic input amplitude and rise and fall times, due to the high gain of the logic switches. Settling time also remains essentially constant for I_{REF} values. The principal advantage of higher I_{REF} values lies in the ability to attain a given output level with lower load resistors, thus reducing the output RC time constant.

Measurement of settling time requires the ability to accurately resolve ±4μA, therefore a 1kΩ load is needed to provide adequate drive for most oscilloscopes. The settling time fixture shown in schematic labelled "Settling Time Measurement" uses a cascode design to permit driving a 1kΩ load with less than 5pF of parasitic capacitance at the measurement node. At I_{REF} values of less than 1.0mA, excessive RC damping of the output is difficult to prevent while maintaining adequate sensitivity. However, the major carry from 01111111 to 10000000 provides an accurate indicator of settling time. This code change does not require the normal 6.2 time constants to settle to within ±0.2% of the final value, and thus settling times may be observed at lower values of I_{REF}.

DAC-08 switching transients or "glitches" are very low and may be further reduced by small capacitive loads at the output at a minor sacrifice in settling time.

Fastest operation can be obtained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is independent of input logic states; 0.1μF capacitors at the supply pins provide full transient protection.

SETTLING TIME MEASUREMENT



10-BIT HIGH-SPEED MULTIPLYING D/A CONVERTER (UNIVERSAL DIGITAL LOGIC INTERFACE)

DAC-10

FEATURES

- **Fast Settling 85ns**
- **Low Full-Scale Drift .... 10ppm/° C**
- **Nonlinearity to 0.05% Max Over Temp Range**
- **Complementary Current Outputs .... 0 to 4mA**
- **Wide Range Multiplying Capability ... 1MHz Bandwidth**
- **Wide Power Supply Range .. +5, −7.5 Min to ±18V Max**
- **Direct Interface to TTL, CMOS, ECL, PMOS, NMOS**

GENERAL DESCRIPTION

The DAC-10 series of 10-bit monolithic multiplying digital-to-analog converters provide high-speed performance and full-scale accuracy.

Advanced circuit design achieves 85ns settling times with very low 'glitch' energy and low power consumption. Direct interface to all-popular logic families with full noise immunity is provided by the high-swing, adjustable-threshold logic inputs.

All DAC-10 series models guarantee full 10-bit monotonicity, and nonlinearities as tight as ±0.05% over the entire operating temperature range are available. Device performance is essentially unchanged over the ±18V power supply range, with 85mW power consumption attainable at lower supplies.

A highly stable, unique trim method is used, which selectively shorts zener diodes, to provide 1/2 LSB full-scale accuracy without the need for laser trimming.

Single-chip reliability coupled with low cost and outstanding flexibility make the DAC-10 device an ideal building block for A/D converters, Data Acquisition systems, CRT display, programmable test equipment, and other applications where low power consumption, input/output versatility, and long-term stability are required.

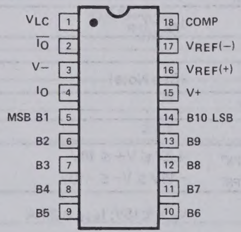
ORDERING INFORMATION†

NL LSB	18-PIN HERMETIC DUAL-IN-LINE PACKAGE MILITARY TEMP.*	COMMERCIAL TEMP.
±1/2	DAC10BX*	DAC10FX
±1	DAC10CX*	DAC10GX

*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

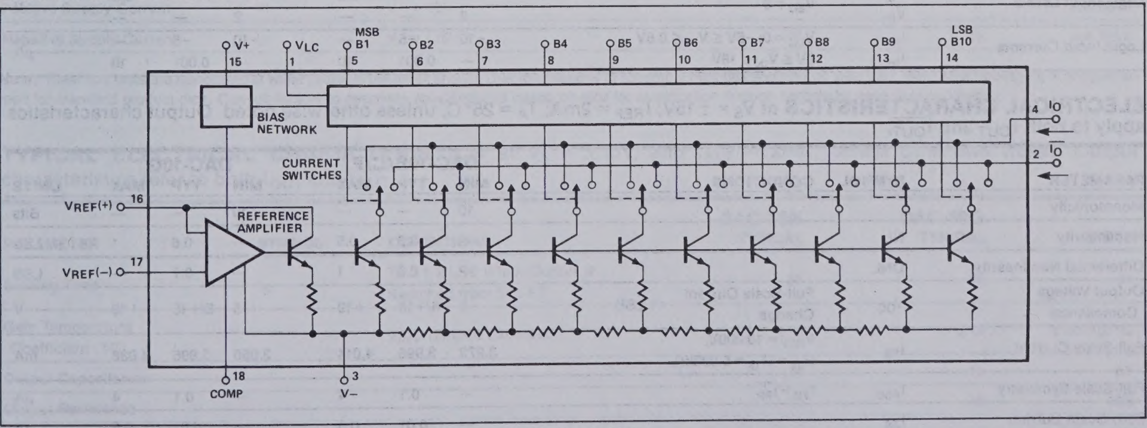
†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

PIN CONNECTIONS


VLC 1
$\overline{I_O}$ 2
V− 3
IO 4
MSB B1 5
B2 6
B3 7
B4 8
B5 9
18 COMP
17 VREF(−)
16 VREF(+)
15 V+
14 B10 LSB
13 B9
12 B8
11 B7
10 B6

18-PIN HERMETIC DUAL-IN-LINE PACKAGE (X-Suffix)

SIMPLIFIED SCHEMATIC


V+ 15
VLC 1
MSB B1 5
B2 6
B3 7
B4 8
B5 9
B6 10
B7 11
B8 12
B9 13
LSB B10 14
BIAS NETWORK
CURRENT SWITCHES
4 IO
2 $\overline{I_O}$
VREF(+) 16
VREF(−) 17
REFERENCE AMPLIFIER
18 COMP
3 V−

Manufactured under one or more of the following patents: 4,055,770; 4,056,740; 4,092,639

ABSOLUTE MAXIMUM RATINGS

Operating Temperature	
DAC-10BX, CX	−55°C to +125°C
DAC-10FX, GX	0°C to +70°C
DICE Junction Temperature (T_j)	−65°C to +150°C
Storage Temperature	−65°C to +150°C
Power Dissipation*	500mW
Derate above 100°C	10mW/°C
Lead Temperature (Soldering, 60 sec)	300°C
V+ Supply to V− Supply	36V
Logic Inputs	V− to V− plus 36V
V_{LC}	V− to V+
Analog Current Outputs	+18V to −18V
Reference Inputs (V_{16} to V_{17})	V− to V+
Reference Input Differential Voltage (V_{16} to V_{17})	±18V
Reference Input Current (I_{16})	2.5mA

NOTE: Ratings apply to both packaged parts and DICE, unless otherwise noted.

*Over full operating range

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$; $I_{REF} = 2mA$; $-55°C \le T_A \le 125°C$ for DAC-10B and DAC-10C, $0°C \le T_A \le 70°C$ for DAC-10F and G, unless otherwise noted. Output characteristics apply to both I_{OUT} and $\overline{I_{OUT}}$.

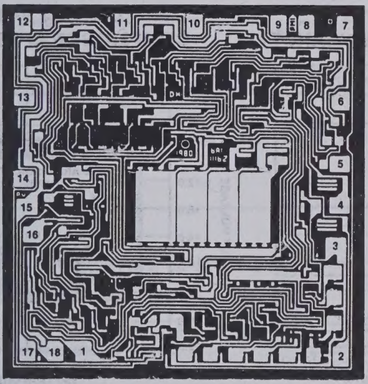
			DAC-10B/F			DAC-10C/G			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Monotonicity			10	—	—	10	—	—	Bits
Nonlinearity	NL		—	0.3	0.5	—	0.6	1	LSB
Differential Nonlinearity	DNL		—	0.3	1	—	0.7	—	LSB
Settling Time	t_S	All Bits Switched ON or OFF Settle to 0.05% of FS (See Note)	—	85	135	—	85	150	ns
Output Capacitance	C_O		—	18	—	—	18	—	pF
Propagation Delay	t_{PLH} t_{PHL}	All Bits Switched $R_L = 5k\Omega$ $R_L = 0$	— —	50 50	— —	— —	50 50	— —	ns
Output Voltage Compliance	V_{OC}	Full-Scale Current Change <1 LSB	— —	−5.5 +10	— —	— —	−5.5 +10	— —	V
Gain Tempco	TCI_{FS}	(See Note)	—	±10	±25	—	±10	±50	ppm/°C
Full-Scale Symmetry	I_{FSS}	$I_{FR} - \overline{I_{FR}}$	—	0.1	4	—	0.1	4	μA
Zero-Scale Current	I_{ZS}		—	0.01	0.5	—	0.01	0.5	μA
Full-Scale Current	I_{FR}	(See Note)	3.960	3.996	4.032	3.920	3.996	4.072	mA
Reference Input Slew Rate	DI/dt		—	6	—	—	6	—	mA/μs
Reference Bias Current	I_B		—	−1	−3	—	−1	−3	μA
Power Supply Sensitivity	$FSSI_{FS}+$ $PSSI_{FS}-$	$4.5V \le V+ \le 18V$ $-18V \le V- \le -10V$	— —	0.001 0.0012	0.01 0.01	— —	0.001 0.0012	0.01 0.01	$\%\Delta I_{FS}/\%\Delta V$
Power Supply Current	I+ I− I+ I−	$V_S = \pm 15V$; $I_{REF} = 2mA$ $V_S = +5V/-7.5V$; $I_{REF} = 1mA$	— — — —	2.3 9 1.8 5.9	4 15 4 9	— — — —	2.3 9 1.8 5.9	4 15 4 9	mA
Power Dissipation	P_d	$V_S = +5V/-7.5V$; $I_{REF} = 1mA$	— —	231 85	276 107	— —	231 85	276 107	mW
Logic Input Levels	V_{IL} V_{IH}	$V_{LC} = 0$	— 2	— —	0.8 —	— 2	— —	0.8 —	V
Logic Input Currents	I_{IL} I_{IH}	$V_{LC} = 0$; $-5V \le V_{IN} \le 0.8V$ $2V \le V_{IN} \le 18V$	−10 —	−5 0.001	— 10	−10 —	−5 0.001	— 10	μA

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$; $I_{REF} = 2mA$; $T_A = 25°C$, unless otherwise noted. Output characteristics apply to both I_{OUT} and $\overline{I_{OUT}}$.

			DAC-10B/C/F			DAC-10G			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Monotonicity			10	—	—	10	—	—	Bits
Nonlinearity	NL		—	0.3	0.5	—	0.6	1	LSB
Differential Nonlinearity	DNL		—	0.3	1	—	0.7	—	LSB
Output Voltage Compliance	V_{OC}	Full-Scale Current Change <1 LSB	−5	−6/+18	+10	−5	−6/+15	+10	V
Full-Scale Current	I_{FS}	$V_{REF} = 10.000V$, $R_{14} = R_{15} = 5.000k\Omega$	3.978	3.996	4.014	3.956	3.996	4.036	mA
Full-Scale Symmetry	I_{FSS}	$I_{FR} - \overline{I_{FR}}$	—	0.1	4	—	0.1	4	μA
Zero-Scale Current	I_{ZS}		—	0.01	0.5	—	0.01	0.5	μA

NOTE: Guaranteed by design.

DICE CHARACTERISTICS



DIE SIZE 0.086 × 0.090 inch, 7740 sq. mils (2.184 × 2.286 mm, 4.993 sq. mm)

1. **V_{LC} (LOGIC) THRESHOLD CONTROL**
2. **$\overline{I_O}$**
3. **V–**
4. **I_O**
5. **B1 (MSB)**
6. **B2**
7. **B3**
8. **B4**
9. **B5**
10. **B6**
11. **B7**
12. **B8**
13. **B9**
14. **B10 (LSB)**
15. **V+**
16. **V_{REF} (+)**
17. **V_{REF} (–)**
18. **COMPENSATION**

For additional DICE information refer to Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $I_{REF} = 2mA$, $T_A = 25°C$, unless otherwise noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

PARAMETER	SYMBOL	CONDITIONS	DAC-10N LIMIT	DAC-10G LIMIT	UNITS
Resolution			10	10	Bits MIN
Monotonicity			10	10	Bits MIN
Nonlinearity	NL		±0.5	±1	LSB MAX
Output Voltage Compliance	V_{OC}	True 1 LSB	+10 –5	+10 –5	V MAX V MIN
Output Current Range		I_{FS} ±3.996 MA	±18	±40	μA MAX
Zero-Scale Current	I_{ZS}	All Bits OFF	0.5	0.5	μA MAX
Logic Input "1"	V_{IH}	$I_{IN} = 100nA$	2	2	V MIN
Logic Input "0"	V_{IL}	V_{LC} @ Ground $I_{IN} = -100\mu A$	0.8	0.8	V MAX
Positive Supply Current	I+	V+ = 15V	4	4	mA MAX
Negative Supply Current	I–	V– = –15V	15	15	mA MAX

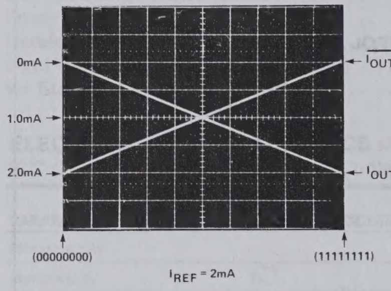
Note: Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, and $I_{REF} = 2mA$, unless otherwise noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

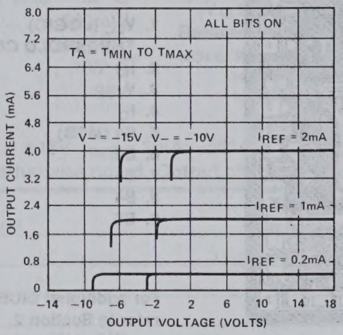
PARAMETER	SYMBOL	CONDITIONS	DAC-10N TYPICAL	DAC-10G TYPICAL	UNITS
Settling Time	t_S	To ±1/2 LSB When Output is Switched from 0 to FS	85	85	ns
Gain Temperature Coefficient (TC)		V_{REF} Tempco Excluded	±10	±10	ppm FS/°C
Output Capacitance			18	18	pF
Output Resistance			10	10	MΩ

TYPICAL PERFORMANCE CHARACTERISTICS

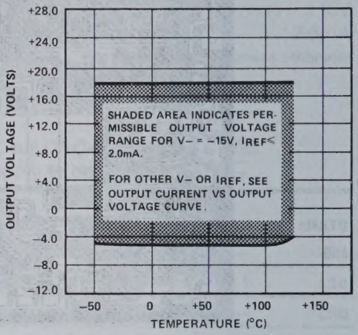
TRUE AND COMPLEMENTARY OUTPUT OPERATIONS



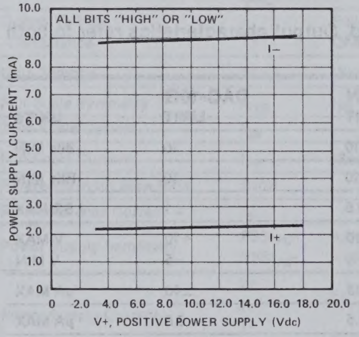
OUTPUT CURRENT vs OUTPUT VOLTAGE (OUTPUT VOLTAGE COMPLIANCE)



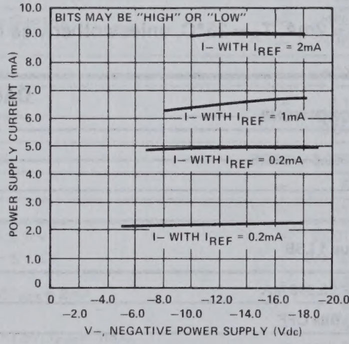
OUTPUT VOLTAGE COMPLAINCE vs TEMPERATURE



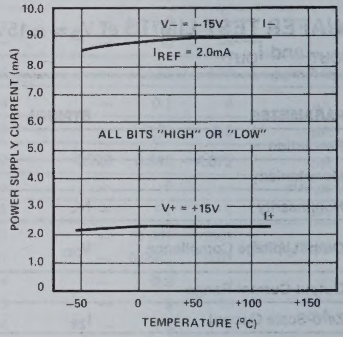
POWER SUPPLY CURRENT vs V+



POWER SUPPLY CURRENT vs V–

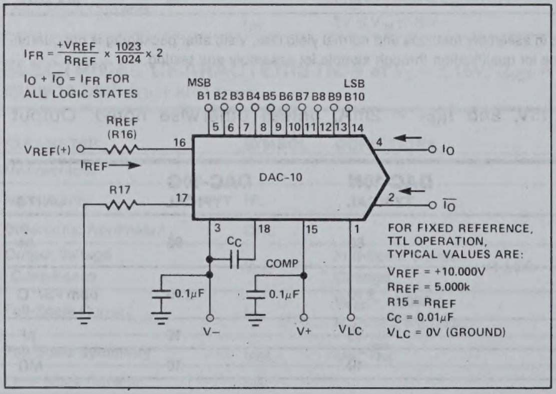


POWER SUPPLY CURRENT vs TEMPERATURE



BASIC CONNECTIONS

BASIC POSITIVE REFERENCE OPERATION



$I_{FR} = \frac{+V_{REF}}{R_{REF}} \times \frac{1023}{1024} \times 2$

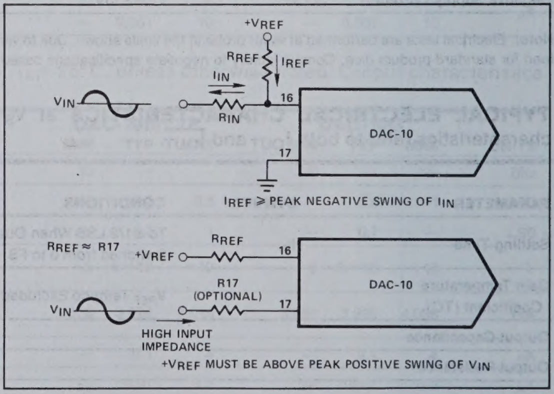
$I_O + \overline{I_O} = I_{FR}$ FOR ALL LOGIC STATES

FOR FIXED REFERENCE, TTL OPERATION, TYPICAL VALUES ARE:

V_{REF} = +10.000V
R_{REF} = 5.000k
R15 = R_{REF}
C_C = 0.01µF
V_{LC} = 0V (GROUND)

MSB
LSB
B1 B2 B3 B4 B5 B6 B7 B8 B9 B10
5 6 7 8 9 10 11 12 13 14
R_{REF} (R16)
V_{REF}(+)
16
I_{REF}
R17
17
DAC-10
4
I_O
2
$\overline{I_O}$
3
18
15
1
C_C
COMP
0.1µF
0.1µF
V–
V+
V_{LC}

ACCOMMODATING BIPOLAR REFERENCES

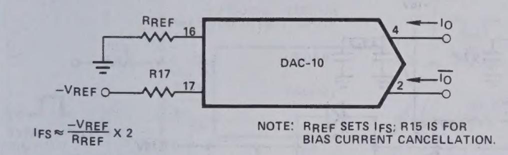


$I_{REF} \geq$ PEAK NEGATIVE SWING OF I_{IN}

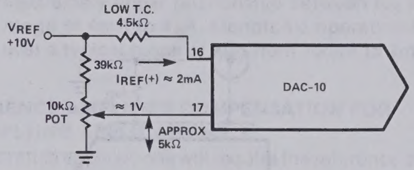
+V_{REF} MUST BE ABOVE PEAK POSITIVE SWING OF V_{IN}

+V_{REF}
R_{REF}
I_{REF}
I_{IN}
V_{IN}
R_{IN}
16
DAC-10
17
$R_{REF} \approx$ R17
+V_{REF}
R_{REF}
16
R17 (OPTIONAL)
V_{IN}
17
DAC-10
HIGH INPUT IMPEDANCE

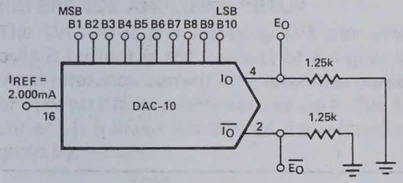
BASIC NEGATIVE REFERENCE OPERATION


RREF
16
R17
17
−VREF
DAC-10
4
I_O
2
$\overline{I_O}$
$I_{FS} \approx \frac{-V_{REF}}{R_{REF}} \times 2$
NOTE: RREF SETS IFS; R15 IS FOR BIAS CURRENT CANCELLATION.

RECOMMENDED FULL-SCALE ADJUSTMENT CIRCUIT

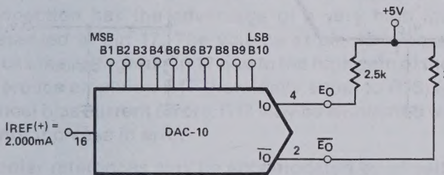

LOW T.C. 4.5kΩ
VREF +10V
39kΩ
IREF(+) ≈ 2mA
16
DAC-10
10kΩ POT
≈ 1V
17
APPROX 5kΩ

BASIC UNIPOLAR NEGATIVE OPERATION


MSB
LSB
B1 B2 B3 B4 B5 B6 B7 B8 B9 B10
E_O
IREF = 2.000mA
16
I_O
4
1.25k
DAC-10
$\overline{I_O}$
2
1.25k
$\overline{E_O}$

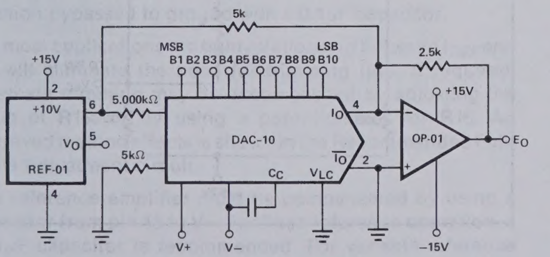
	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	I_OmA	$\overline{I_O}$mA	E_O	$\overline{E_O}$
FULL RANGE	1	1	1	1	1	1	1	1	1	1	3.996	0.000	−4.995	−0.000
HALF-SCALE +LSB	1	0	0	0	0	0	0	0	0	1	2.004	1.992	−2.505	−2.490
HALF-SCALE	1	0	0	0	0	0	0	0	0	0	2.000	1.996	−2.500	−2.495
HALF-SCALE −LSB	0	1	1	1	1	1	1	1	1	1	1.996	2.000	−2.495	2.500
ZERO-SCALE +LSB	0	0	0	0	0	0	0	0	0	1	0.004	3.992	−0.005	−4.990
ZERO-SCALE	0	0	0	0	0	0	0	0	0	0	0.000	3.996	−0.000	−4.995

BASIC BIPOLAR OUTPUT OPERATION


+5V
MSB
LSB
B1 B2 B3 B4 B6 B6 B7 B8 B9 B10
2.5k
2.5k
I_O
4
E_O
IREF(+) = 2.000mA
16
DAC-10
$\overline{I_O}$
2
$\overline{E_O}$

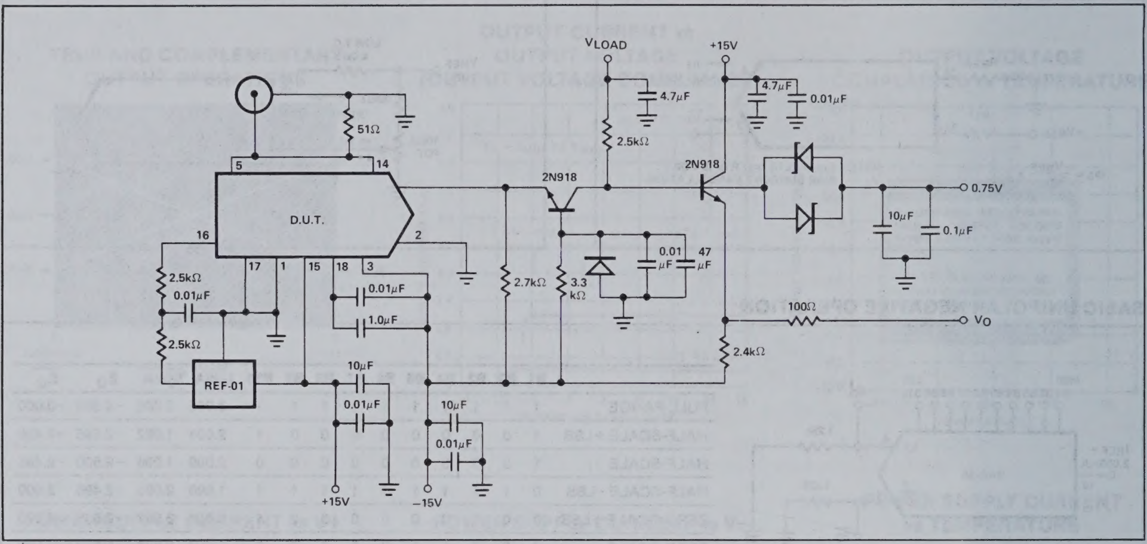
	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	E_O	$\overline{E_O}$
POS FULL RANGE	1	1	1	1	1	1	1	1	1	1	−4.990	+5.000
POS FULL RANGE −LSB	1	1	1	1	1	1	1	1	1	0	−4.980	+4.990
ZERO-SCALE +LSB	1	0	0	0	0	0	0	0	0	1	−0.010	+0.020
ZERO-SCALE	1	0	0	0	0	0	0	0	0	0	0.000	+0.010
ZERO-SCALE −LSB	1	1	1	1	1	1	1	1	1	1	+0.010	0.000
NEG FULL-SCALE +LSB	0	0	0	0	0	0	0	0	0	1	+4.990	−4.980
NEG FULL-SCALE	0	0	0	0	0	0	0	0	0	0	+5.000	−4.990

OFFSET BINARY OPERATION

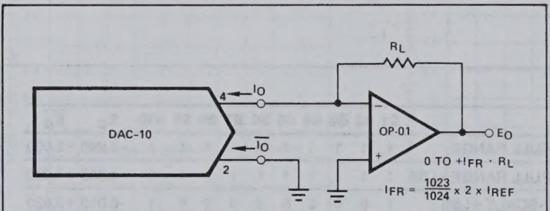

5k
MSB
LSB
B1 B2 B3 B4 B5 B6 B7 B8 B9 B10
2.5k
+15V
2
+10V
6
5.000kΩ
+15V
VO
5
5kΩ
REF-01
4
I_O
4
DAC-10
$\overline{I_O}$
2
OP-01
E_O
CC
VLC
V+
V−
−15V

	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	E_O
POS FULL RANGE	1	1	1	1	1	1	1	1	1	1	+4.990
ZERO-SCALE	1	0	0	0	0	0	0	0	0	0	0.00
NEG FULL-SCALE +LSB	0	0	0	0	0	0	0	0	0	1	−4.990
NEG FULL-SCALE	0	0	0	0	0	0	0	0	0	0	−5.000

SETTLING TIME MEASUREMENT

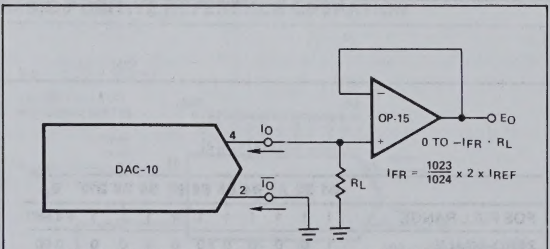

VLOAD
+15V
4.7μF
4.7μF
0.01μF
51Ω
5
14
2.5kΩ
2N918
2N918
0.75V
D.U.T.
16
2
10μF
0.1μF
0.01 μF
47 μF
17
1
15
18
3
2.5kΩ
0.01μF
0.01μF
1.0μF
2.7kΩ
3.3 kΩ
100Ω
VO
2.5kΩ
2.4kΩ
REF-01
10μF
0.01μF
10μF
0.01μF
+15V
−15V

POSITIVE LOW IMPEDANCE OUTPUT OPERATION


RL
4
IO
DAC-10
$\overline{I_O}$
2
OP-01
−
+
EO
0 TO +IFR · RL
$I_{FR} = \frac{1023}{1024} \times 2 \times I_{REF}$

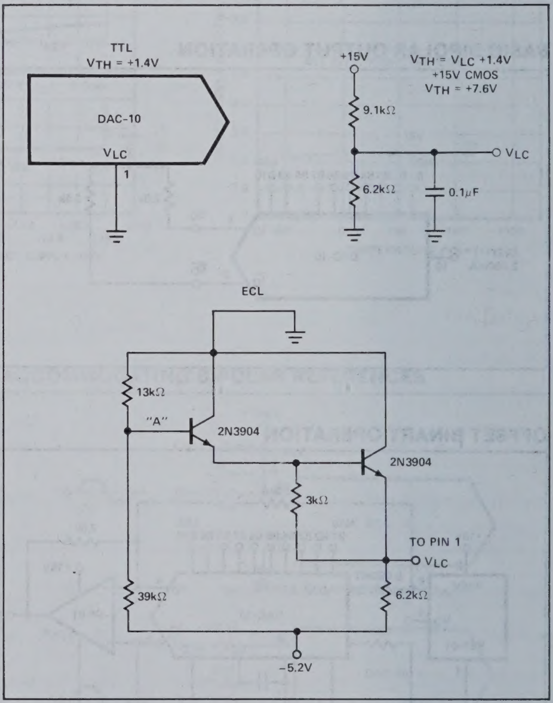
FOR COMPLEMENTARY OUTPUT (OPERATION AS A NEGATIVE LOGIC DAC), CONNECT INVERTING INPUT OF OP-AMP TO $\overline{I_O}$ (PIN 2); CONNECT I_O (PIN 4) TO GROUND.

NEGATIVE LOW IMPEDANCE OUTPUT OPERATION

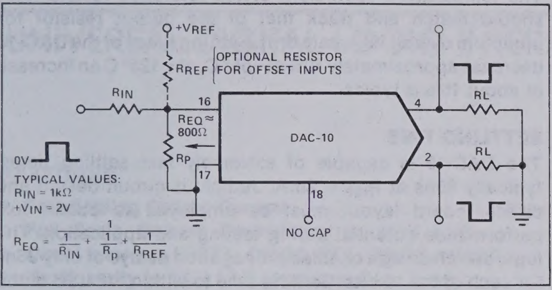

OP-15
−
+
EO
DAC-10
4
IO
2
$\overline{I_O}$
RL
0 TO −IFR · RL
$I_{FR} = \frac{1023}{1024} \times 2 \times I_{REF}$

FOR COMPLEMENTARY OUTPUT (OPERATION AS A NEGATIVE LOGIC DAC), CONNECT NON-INVERTING INPUT OF OP-AMP TO $\overline{I_O}$ (PIN 2); CONNECT I_O (PIN 4) TO GROUND.

INTERFACING WITH VARIOUS LOGIC FAMILIES


TTL
VTH = +1.4V
DAC-10
VLC
1
+15V
VTH = VLC +1.4V
+15V CMOS
VTH = +7.6V
9.1kΩ
VLC
6.2kΩ
0.1μF
ECL
13kΩ
"A"
2N3904
2N3904
3kΩ
TO PIN 1
VLC
39kΩ
6.2kΩ
−5.2V

PULSED REFERENCE OPERATION



APPLICATIONS INFORMATION

REFERENCE AMPLIFIER SETUP

The DAC-10 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to 2mA. The full-scale output current is a linear function of the reference current and is given by:

$$I_{FR} = \frac{1023}{1024} \times 2 \times (I_{REF}) \text{ where } I_{REF} = I_{16}$$

In positive reference applications, an external positive reference voltage forces current through R16 into the $V_{REF(+)}$ terminal (pin 16) of the reference amplifier. Alternatively, a negative reference may be applied to $V_{REF(-)}$ at pin 17; reference current flows from ground through R16 into $V_{(+)}$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin 17. The voltage at pin 18 is equal to and tracks the voltage at pin 17 due to the high gain of the internal reference amplifier. R17 (nominally equal to R16) is used to cancel bias current errors; R17 may be eliminated with only a minor increase in error.

Bipolar references may be accomodated by offsetting V_{REF} or pin 17. The negative common-mode range of the reference amplifier is given by: $V_{CM}- = V-$ plus $(I_{REF} \times 2k\Omega)$ plus 2V. The positive common-mode range is V+ less 1.8V.

When a DC reference is used, a reference bypass capacitor is recommended. A 5V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R16 should be split into two resistors with the junction bypassed to ground with a 0.1μF capacitor.

For most applications the tight relationship between I_{REF} and I_{FS} will eliminate the need for trimming I_{REF}. If required, full-scale trimming may be accomplished by adjusting the value of R16, or by using a potentiometer for R16. An improved method effects is shown in the Recommended Full-Scale Adjustment circuit.

The reference amplifier must be compensated by using a capacitor from pin 18 to V−. For fixed reference operation, a 0.01μF capacitor is recommended. For variable reference applications, see section entitled "Reference Amplifier Compensation for Multiplying Applications."

MULTIPLYING OPERATION

The DAC-10 provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 4mA to 4μA. Monotonic operation is maintained over a typical range of I_{REF} from 100μA to 2mA.

REFERENCE AMPLIFIER COMPENSATION FOR MULTIPLYING APPLICATIONS

AC reference applications will require the reference amplifier to be compensated using a capacitor from pin 18 to V−. The value of this capacitor depends on the impedance presented to pin 16 for R16 values of 1.0, 2.5 and 5.0kΩ, minimum values of C_C are 15, 37, and 75pF. Larger values of R16 require proportionately increased values of C_C for proper phase margin.

For fastest response to a pulse, low values of R16 enabling small C_C values should be used. If pin 16 is driven by a high impedance such as a transistor current source, none of the above values will suffice and the amplifier must be heavily compensated which will decrease overall bandwidth and slew rate. For R16 = 1kΩ and C_C = 15pF, the reference amplifier slews at 4mA/μs enabling a transition from $I_{REF} = 0$ to $I_{REF} = 2$mA in 500ns.

Operation with pulse inputs to the reference amplifier may be accommodated by an alternate compensation scheme. This technique provides lowest full-scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff (I_{REF} = 0) condition. Full-scale transition (0 to 2mA) occurs in 120ns when the equivalent impedance at pin 16 is 200Ω and C_C = 0. This yields a reference slew rate of 16mA/μs which is relatively independent of R_{IN} and V_{IN} values.

LOGIC INPUTS

The DAC-10 design incorporates a unique logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 2μA logic input current and completely adjustable logic threshold voltage. For V− = −15V, the logic inputs may swing between −5 and +18V. This enables direct interface with +15V CMOS logic, even when the DAC-10 is powered from a +5V supply. Minimum input logic swing and minimum logic threshold voltage are given by: V− plus $(I_{REF} \times 2k\Omega)$ plus 3V. The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control pin (pin 1, V_{LC}). The appropriate graph shows the relationship between V_{LC} and V_{TH} over the temperature range, with V_{TH} nominally 1.4V above V_{LC}. For TTL interface, simply ground pin 1. When interfacing ECL, an I_{REF} = 1mA is recommended. For interfacing other logic families, see previous page. For general setup of the logic control circuit, it should be noted that pin 1 will sink 1. 1mA typical; external circuitry should be designed to accommodate this current.

Fastest settling times are obtained when pin 1 sees a low impedance. If pin 1 is connected to a 1kΩ divider, for example, it should be bypassed to ground by a 0.01μF capacitor.

ANALOG OUTPUT CURRENTS

Both true and complemented output sink currents are provided where $I_O + \overline{I_O} = I_{FS}$. Current appears at the "true" output when a "1" is applied to each logic input. As the binary count increases, the sink current at pin 4 increases proportionally, in the fashion of a "positive logic" D/A converter. When a "0" is applied to any input bit, that current is turned off at pin 4 and turned on at pin 2. A decreasing logic count increases $\overline{I_O}$ as in a negative or inverted logic D/A converter. Both outputs may be used simultaneously. If one of the outputs is not required it must still be connected to ground or to a point capable of sourcing I_{FS}; DO NOT LEAVE AN UNUSED OUTPUT PIN OPEN.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 36V above V− and is independent of the positive supply. Negative compliance is +10V above V−.

The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection and in other balanced applications such as driving center-tapped coils and transformers.

POWER SUPPLIES

The DAC-10 operates over a wide range of power supply voltages from a total supply of 9V to 36V. When operating with V− supplies of −10V or less, $I_{REF} \leq 1mA$ is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common-mode range, negative logic input range, and negative logic threshold range; consult the various figures for guidance. For example, operation at −9V with $I_{REF} = 2mA$ is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible, however at least 8V total must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the DAC-10 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required; however, an artificial ground may be used to insure logic swings, etc. remain within acceptable limits.

TEMPERATURE PERFORMANCE

The nonlinearity and monotonicity specifications of the DAC-10 are guaranteed to apply over the entire rated operating temperature range. Full-scale output current drift is tight, typically ±10ppm/°C, with zero-scale output current and drift essentially negligible compared to 1/2 LSB.

The temperature coefficient of the reference resistor R14 should match and track that of the output resistor for minimum overall full-scale drift. Settling times of the DAC-10 decrease approximately 10% at −55°C; at +125°C an increase of about 15% is typical.

SETTLING TIME

The DAC-10 is capable of extremely fast settling times; typically 85ns at $I_{REF} = 2mA$. Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The logic switch design enables propagation delays of only 35ns for each of the 10 bits. Settling time to within 1/2 LSB of the LSB is therefore 35ns, with each progressively larger bit taking successively longer. The MSB settles in 130ns, thus determining the overall settling time of 85ns. Settling to 8-bit accuracy requires about 60 to 78ns. The output capacitance of the DAC-10 including the package is approximately 18pF; therefore the output RC time constant dominates settling time if $R_L > 500\Omega$.

Settling time and propagation delay are relatively insensitive to logic input amplitude and rise and fall times, due to the high gain of the logic switches. Settling time also remains essentially constant for I_{REF} values down to 1mA, with gradual increases for lower I_{REF} values lies in the ability to attain a given output level with lower load resistors, thus reducing the output RC time constant.

Measurement of settling time requires the ability to accurately resolve $\pm 2\mu A$, therefore a $2.5k\Omega$ load is needed to provide adequate drive for most oscilloscopes. The settling time fixture of schematic titled "Settling Time Measurement" uses a cascode design to permit driving a $2.5k\Omega$ load with less than 5pF of parasitic capacitance at the measurement node. At I_{REF} values of less than 1mA, excessive RC damping of the output is difficult to prevent while maintaining adequate sensitivity. However, the major carry from 0111111111 to 1000000000 provides an accurate indicator of settling time. This code change does not require the normal 6.2 time constants to settle to within ±0.2% of the final value, and thus settling times may be observed at lower values of I_{REF}.

DAC-10 switching transients or "glitches" are very low and may be further reduced by small capacitive loads at the output at a minor sacrifice in settling time.

Fastest operation can be obtained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is independent of input logic states; $0.1\mu F$ capacitors at the supply pins provide full transient protection.

2-DIGIT BCD HIGH-SPEED MULTIPLYING D/A CONVERTER (UNIVERSAL DIGITAL LOGIC INTERFACE)

DAC-20

FEATURES

- **Fast Settling Output Current 85ns**
- **Full Scale Current Prematched to ±1/4 LSB**
- **Direct Interface to TTL, CMOS, ECL, PMOS, NMOS**
- **Nonlinearity to ±1/4 LSB Maximum Over Temp.**
- **High Output Impedance and Compliance −10V to +18V**
- **Complementary Current Outputs**
- **Wide Range Multiplying Capability ... 1MHz Bandwidth**
- **Low FS Current Drift .... ±10ppm/ΔC**
- **Wide Power Supply Range .... ±4.5V to ±18V**
- **Low Power Consumption .... 37mW @ 5V**
- **Low Cost**

GENERAL DESCRIPTION

The DAC-20 series of 2-digit BCD monolithic multiplying digital to analog converters provide very high-speed performance coupled with low cost and outstanding applications flexibility.

Advanced circuit design achieves 85ns settling times with very low "glitch" energy and at low power consumption. Monotonic multiplying performace is attained over a wide 20 to 1 reference current range. Matching to within 1 LSB between reference and full-scale currents eliminates the need for full scale trimming in most applications. Direct interface to all popular logic families with full noise immunity is provided by the high swing, adjustable threshold logic inputs.

Complementary current outputs with −10V to +18V voltage compliance enable resistive termination, a voltage output without an external op amp.

Both DAC-20 models guarantee full 2-digit monotonicity, some have nonlinearity as tight as ±1/2 LSB over the entire operating temperature range. Nonlinearity is unchanged over the ±4.5V to ±18V power supply range, with 37mW power consumption attainable at ±5V supplies.

The compact size and low power consumption make the DAC-20 attractive for portable applications.

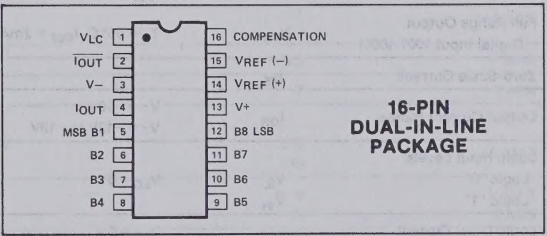
DAC-20 applications include A/D converters, audio attenuators, analog meter drivers, programmable power supplies, high-speed modems and other applications where low cost, high speed and complete input/output versatility are required.

ORDERING INFORMATION†

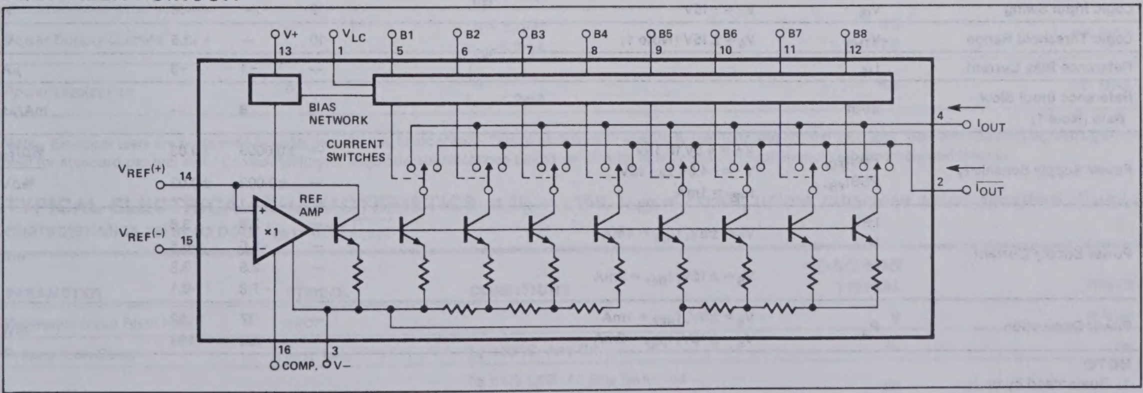
NL LSB	16-PIN DUAL-IN-LINE PACKAGE COMMERCIAL TEMPERATURE RANGE HERMETIC	 PLASTIC
±1/2	DAC20CQ	DAC20CP

†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

PIN CONNECTIONS



EQUIVALENT CIRCUIT



Manufactured under one or more of the following patents: 4,055,773; 4,056,740; 4,092,639

ABSOLUTE MAXIMUM RATINGS ($T_A = 25°C$, unless otherwise noted)

Operating Temperature Range
DAC-20 CQ, CP .... 0°C to +70°C
DICE Junction Temperature (T_j) .... −65°C to +150°C
Storage Temperature Range
Q Package .... −65°C to +150°C
P Package .... −65°C to +125°C
Power Dissipation 500mW
Derate above 100°C .... 10mW/°C
Lead Temperature (Soldering, 60 sec) .... 300°C
V+ Supply to V− Supply 36V
Logic Inputs .... V− to V− plus 36V
V_{LC} .... V− to V+
Reference Inputs (V_{14}, V_{15}) .... V− to V+
Reference Input Differential Voltage (V_{14} to V_{15}) .... ±18V
Reference Input Current (I_{14}) 5.0mA

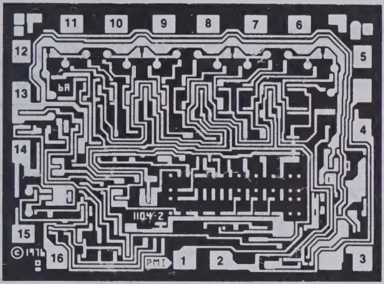
NOTE: Absolute ratings apply to both DICE and packaged parts unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $I_{REF} = 2.0mA$, $0°C \le T_A \le 70°C$, unless otherwise noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

			DAC-20C			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Resolution		BCD 0 to 99 steps	2	—	—	Digits
Monotonicity		BCD 99 steps	2	—	—	Digits
Nonlinearity	NL	0000 0000 to 1001 1001	—	—	±1/2	LSB
Settling Time (Note 1)	t_S	To ±1/2 LSB (±0.5% FS) all bits switched ON or OFF, $T_A = 25°C$	—	85	150	ns
Propagation Delay Each Bit All bits switched (Note 1)	t_{PLH}, t_{PHL}	$T_A = 25°C$	—	35	60	ns
Full Tempco	TCI_{FS}	(Note 1)	—	±10	±80	ppm/°C
Output Voltage Compliance (True Compliance)	V_{OC}	Full-scale current change < 1/2 LSB (< 0.5% FS) $R_{OUT} > 20M\Omega$ typical $I_{REF} = 1mA$	−10	—	+18	V
Full Range Output (Digital Input 1001 1001)	I_{FR4}	$T_A = 25°C$, $I_{REF} = 2mA$	1.92	1.98	2.04	mA
Zero-Scale Current	I_{ZS}		—	0.2	5	μA
Output Current Range	I_{OR}	V− = −10V V− = −12V to −18V	2.2 4.2	2 2	— —	mA
Logic Input Levels Logic "0" Logic "1"	 V_{IL} V_{IH}	$V_{LC} = 0V$	 — 2	 — —	 0.8 —	V
Logic Input Current Logic "0" Logic "1"	 I_{IL} I_{IH}	$V_{LC} = 0V$ $V_{IN} = -10V$ to $+0.8V$ $V_{IN} = 2V$ to $18V$	 — —	 −2 0.002	 ±10 ±10	μA
Logic Input Swing	V_{IS}	V− = −15V	−10	—	+18	V
Logic Threshold Range	V_{THR}	$V_S = \pm15V$ (Note 1)	−10	—	+13.5	V
Reference Bias Current	I_{15}		—	−1	−3	μA
Reference Input Slew Rate (Note 1)	dI/dt		4	8	—	mA/μs
Power Supply Sensitivity	$PSSI_{FS+}$ $PSSI_{FS-}$	V+ = 4.5V to 18V V− = −4.5V to −18V $I_{REF} = 1mA$	— —	±0.0003 ±0.002	±0.03 ±0.03	$\%\Delta I_{FS}$ / $\%\Delta V$
Power Supply Current	I+ I− I+ I−	$V_S = \pm5V$, $I_{REF} = 1mA$ $V_S = \pm15V$, $I_{REF} = 2mA$	— — — —	2.3 −5.0 2.5 −7.8	3.8 −6.5 3.8 −9.1	mA
Power Dissipation	P_d	$V_S = \pm5V$, $I_{REF} = 1mA$ $V_S = \pm15V$, $I_{REF} = 2mA$	— —	37 152	52 194	mW

NOTE:
1. Guaranteed by design.

DICE CHARACTERISTICS



DIE SIZE 0.085 × 0.065 inch, 5,525 sq. mils
(2.159 × 1.651 mm, 3.56 sq. mm)

1. V_{LC}
2. $\overline{I_{OUT}}$
3. V−
4. I_{OUT}
5. BIT 1 (MSB)
6. BIT 2
7. BIT 3
8. BIT 4
9. BIT 5
10. BIT 6
11. BIT 7
12. BIT 8 (LSB)
13. V+
14. V_{REF} (+)
15. V_{REF} (−)
16. COMP

For additional DICE information refer to Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $I_{REF} = 2.0mA$, $T_A = 25°C$, unless otherwise noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

PARAMETER	SYMBOL	CONDITIONS	DAC-20G LIMIT	UNITS
Resolution		BCD 0 to 99 steps	2	Digits MIN
Monotonicity		BCD 99 steps	2	Digits MIN
Nonlinearity	NL	FS = 1001 1001	±1/2	LSB MAX
Output Voltage Compliance	V_{OC}	Full-Scale Current Change <1/2 LSB	+18 −10	V MAX V MIN
Full-Scale Current	I_{FS4}	$V_{REF} = 10V$ $R_{14}, R_{15} = 5k\Omega$	2.04 1.92	mA MAX mA MIN
Zero-Scale Current	I_{ZS}		5	μA MAX
Output Current Range	I_{OR}	$V- = -10V$ $V- = -12V$ to $-18V$	2.1 4.2	mA MIN
Logic "0" Input Level	V_{IL}		0.8	V MAX
Logic "1" Input Level	V_{IH}		2	V MIN
Logic Input Current Logic "0" Logic "1"	 I_{IL} I_{IH}	 $V_{IN} = -10V$ to $+0.8V$ $V_{IN} = 2V$ to $18V$	 ±10 ±10	μA MAX
Logic Input Swing	V_{IS}	$V- = -15V$	+18 −10	V MAX V MIN
Power Supply Sensitivity	$PSSI_{FS+}$ $PSSI_{FS-}$	$V- = -4.5V$ to $-18V$ $V- = -4.5V$ to $-18V$ $I_{REF} = 1mA$	±0.03 ±0.03	$\%\Delta I_{FS}$ / $\%\Delta V$ MAX
Power Supply Current	I+ I−	$V_S = \pm 18V$ $I_{REF} \leq 2mA$	3.8 −7.8	mA MAX
Power Dissipation	P_d	$V_S = \pm 18V$ $I_{REF} \leq 2mA$	194	mW MAX

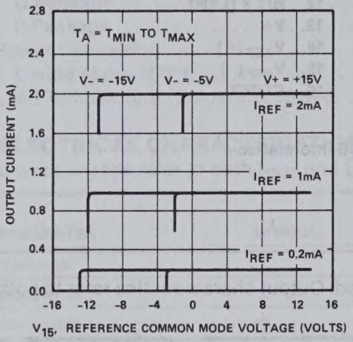
Note: Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $I_{REF} = 2.0mA$, unless otherwise noted specified. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

PARAMETER	SYMBOL	CONDITIONS	DAC-20G TYPICAL	UNITS
Reference Input Slew Rate	dI/dt		8	mA/μs
Propagation Delay	t_{PLH}, t_{PHL}	$T_A = 25°C$, Any Bit	35	ns
Settling Time	t_S	To ±1/2 LSB, All Bits Switched ON or OFF, $T_A = 25°C$	85	ns

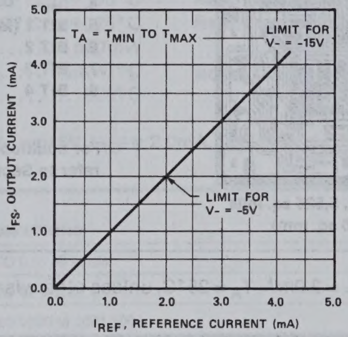
TYPICAL REFERENCE PERFORMACE CHARACTERISTICS

REFERENCE AMP COMMON-MODE RANGE (DIGITAL INPUT 1001 1001)



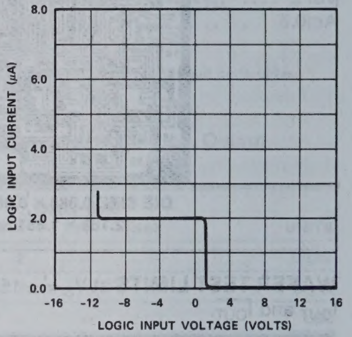
NOTE: POSITIVE COMMON MODE IS ALWAYS (V+) -1.5V; NEGATIVE COMMON MODE RANGE IS V- PLUS (I_{REF} × 800Ω) PLUS 2.5V.

FULL-SCALE CURRENT vs REFERENCE CURRENT (DIGITAL INPUT 1001 1001)

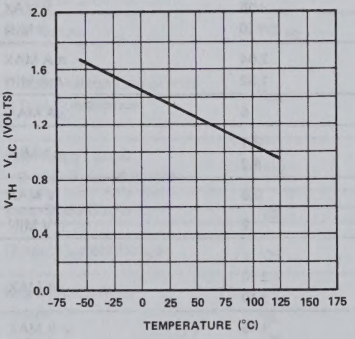


NOTE: THE RECOMMENDED RANGE FOR OPERATION WITH WITH A DC REFERENCE CURRENT IS +0.2mA TO +4.0mA.

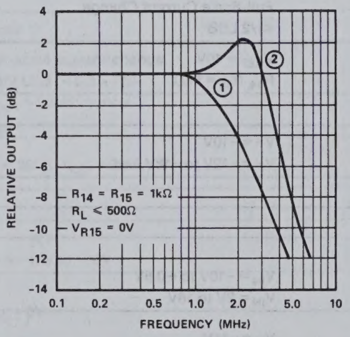
LOGIC INPUT CURRENT vs INPUT VOLTAGE



V_{TH} — V_{LC} vs TEMPERATURE

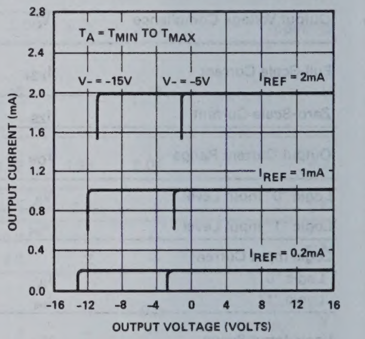


REFERENCE INPUT FREQUENCY RESPONSE (DIGITAL INPUT 1001 1001)

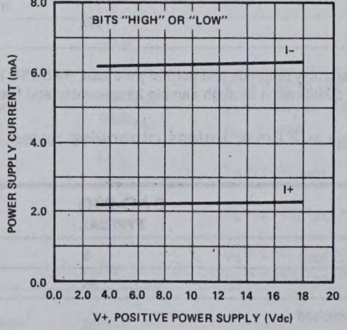


CURVE 1: C_C = 15pF, $V_{IN} = 2.0V_{P-P}$ CENTERED AT +1.0V, LARGE SIGNAL.
CURVE 2: C_C = 15pF, $V_{IN} = 50mV_{P-P}$ CENTERED AT +200mV, SMALL SIGNAL.

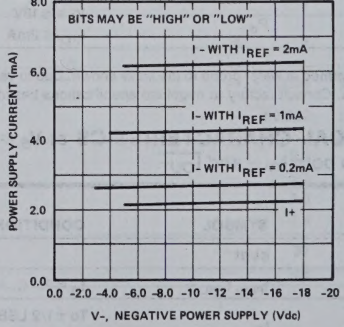
OUTPUT CURRENT vs OUTPUT VOLTAGE (OUTPUT VOLTAGE COMPLIANCE) (DIGITAL INPUT 1001 1001)



POWER SUPPLY CURRENT vs V+

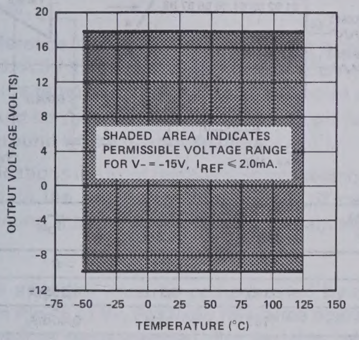


POWER SUPPLY CURRENT vs V−

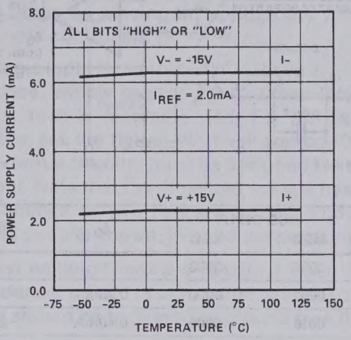


TYPICAL REFERENCE PERFORMACE CHARACTERISTICS

OUTPUT VOLTAGE COMPLIANCE vs TEMPERATURE



POWER SUPPLY CURRENT vs TEMPERATURE



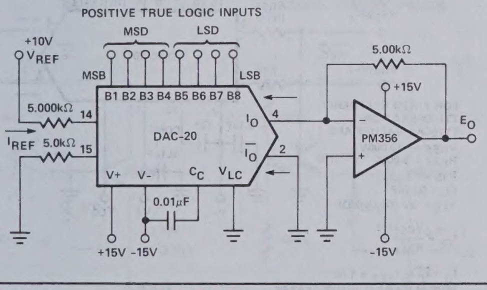
BASIC OUTPUT CONNECTIONS

With complementary current outputs, the DAC-20 may be used with either positive true or negative true (complementary) logic. Current appears at the "true" output (I_O) when a "1" is applied to a logic input. As the BCD-coded input increases, the sink current at Pin 4 increases proportionately, in the fashion of a "positive logic" D/A converter. When a "0" is applied to a logic input, that current is turned OFF at Pin 4 and ON at Pin 2 ($\overline{I_O}$) which is used for negative true or "negative logic" D/A converters.

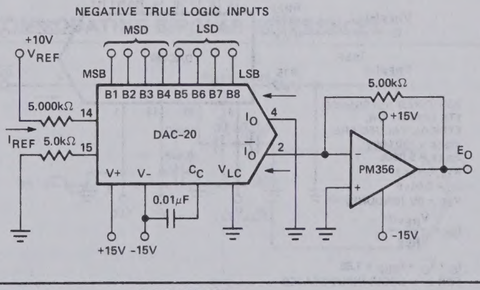
The unused output must be connected to ground or some voltage source capable of sourcing 1.65 times I_{REF}. A detailed discussion of reference input operation begins on the next page.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 36V above V– and is independent of the positive supply. Negative compliance is given by V– plus (I_{REF} × 800Ω) plus 2.5V.

POSITIVE VOLTAGE OUTPUT

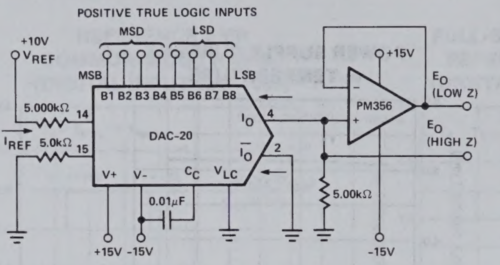

POSITIVE TRUE LOGIC INPUTS
MSD
LSD
+10V
V_{REF}
MSB
LSB
B1 B2 B3 B4 B5 B6 B7 B8
5.000kΩ
14
I_{REF}
5.0kΩ
15
DAC-20
I_O
4
$\overline{I_O}$
2
V+ V- C_C V_{LC}
0.01μF
+15V -15V
5.00kΩ
+15V
PM356
-
+
E_O
-15V

DECIMAL INPUT	BCD INPUT MSD	LSD	I_O	E_O
0	0000	0000	0	0
10	0001	0000	0.20mA	+1.0V
20	0010	0000	0.40mA	+2.0V
30	0011	0000	0.60mA	+3.0V
40	0100	0000	0.80mA	+4.0V
80	1000	0000	1.60mA	+8.0V
99	1001	1001	1.98mA	+9.9V

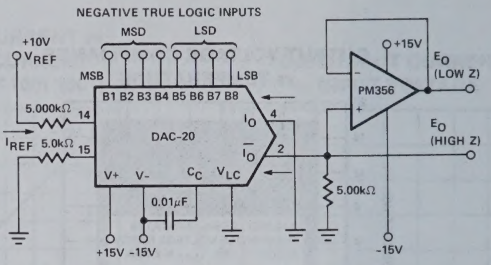

NEGATIVE TRUE LOGIC INPUTS
MSD
LSD
+10V
V_{REF}
MSB
LSB
B1 B2 B3 B4 B5 B6 B7 B8
5.000kΩ
14
I_{REF}
5.0kΩ
15
DAC-20
I_O
4
$\overline{I_O}$
2
V+ V- C_C V_{LC}
0.01μF
+15V -15V
5.00kΩ
+15V
PM356
-
+
E_O
-15V

DECIMAL INPUT	BCD INPUT MSD	LSD	$\overline{I_O}$	E_O
0	1111	1111	0	0
10	1110	1111	0.20mA	+1.0V
20	1101	1111	0.40mA	+2.0V
30	1100	1111	0.60mA	+3.0V
40	1011	1111	0.80mA	+4.0V
80	0111	1111	1.60mA	+8.0V
99	0110	0110	1.98mA	+9.9V

NEGATIVE VOLTAGE OUTPUT


POSITIVE TRUE LOGIC INPUTS
MSD
LSD
+10V
VREF
MSB
LSB
B1 B2 B3 B4 B5 B6 B7 B8
5.000kΩ
14
IREF
5.0kΩ
15
DAC-20
IO
4
IO
2
V+ V- CC VLC
0.01µF
+15V -15V
+15V
PM356
EO (LOW Z)
EO (HIGH Z)
5.00kΩ
-15V

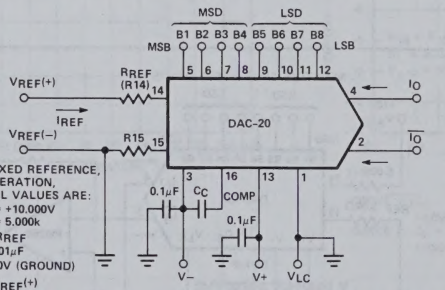
DECIMAL INPUT	BCD INPUT MSD	LSD	I_O	E_O
0	0000	0000	0	0
10	0001	0000	0.20mA	−1.0V
20	0010	0000	0.40mA	−2.0V
30	0011	0000	0.60mA	−3.0V
40	0100	0000	0.80mA	−4.0V
80	1000	0000	1.60mA	−8.0V
99	1001	1001	1.98mA	−9.9V


NEGATIVE TRUE LOGIC INPUTS
MSD
LSD
+10V
VREF
MSB
LSB
B1 B2 B3 B4 B5 B6 B7 B8
5.000kΩ
14
IREF
5.0kΩ
15
DAC-20
IO
4
IO
2
V+ V- CC VLC
0.01µF
+15V -15V
+15V
PM356
EO (LOW Z)
EO (HIGH Z)
5.00kΩ
-15V

DECIMAL INPUT	BCD INPUT MSD	LSD	$\overline{I_O}$	E_O
0	1111	1111	0	0
10	1110	1111	0.20mA	−1.0V
20	1101	1111	0.40mA	−2.0V
30	1100	1111	0.60mA	−3.0V
40	1011	1111	0.80mA	−4.0V
80	0111	1111	1.60mA	−8.0V
99	0110	0110	1.98mA	−9.9V

REFERENCE OPERATION

POSITIVE

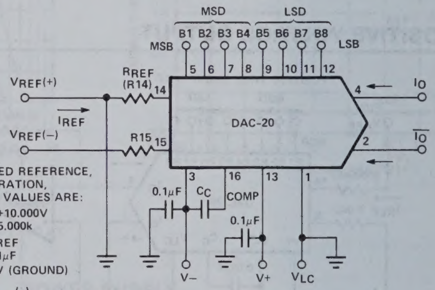

MSD
LSD
B1 B2 B3 B4 B5 B6 B7 B8
MSB
LSB
5 6 7 8 9 10 11 12
VREF(+)
RREF (R14)
14
IREF
VREF(−)
R15
15
DAC-20
4
IO
2
IO
3
16
13
1
0.1µF
CC
COMP
0.1µF
V−
V+
VLC

FOR FIXED REFERENCE,
TTL OPERATION,
TYPICAL VALUES ARE:
V_{REF} = +10.000V
R_{REF} = 5.000k
$R_{15} \approx R_{REF}$
C_C = 0.01µF
V_{LC} = 0V (GROUND)

$$I_{FS} = \frac{V_{REF}(+)}{R_{REF}}$$

$I_O + \overline{I_O} \approx I_{REF} \times 1.65$
FOR ALL LOGIC INPUT STATES

NEGATIVE


MSD
LSD
B1 B2 B3 B4 B5 B6 B7 B8
MSB
LSB
5 6 7 8 9 10 11 12
VREF(+)
RREF (R14)
14
IREF
VREF(−)
R15
15
DAC-20
4
IO
2
IO
3
16
13
1
0.1µF
CC
COMP
0.1µF
V−
V+
VLC

FOR FIXED REFERENCE,
TTL OPERATION,
TYPICAL VALUES ARE:
V_{REF} = +10.000V
R_{REF} = 5.000k
$R_{15} \approx R_{REF}$
C_C = 0.01µF
V_{LC} = 0V (GROUND)

$$I_{FS} = \frac{V_{REF}(-)}{R_{REF}}$$

$I_O + \overline{I_O} \approx I_{REF} \times 1.65$
FOR ALL LOGIC INPUT STATES

REFERENCE AMPLIFIER SETUP

The DAC-20 is a multiplying converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to +4.0mA. The full range output current is a linear function of the reference current and is given by:

$$I_{FR} = 99/100 \times I_{REF}, \text{ where } I_{REF} = I_{14}.$$

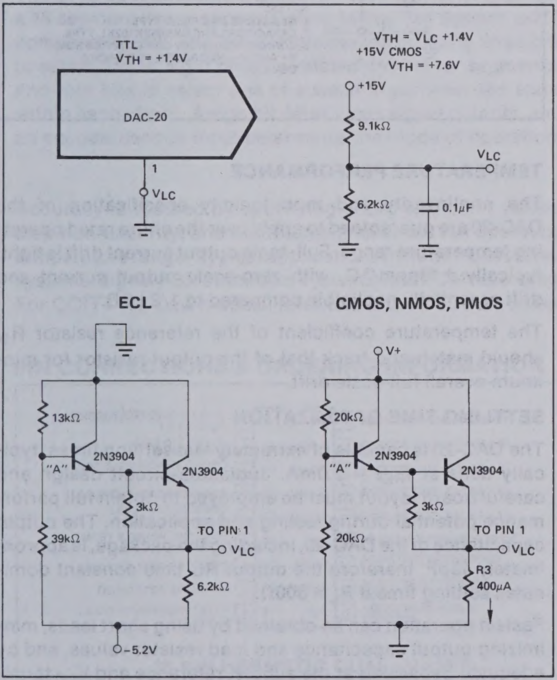
In positive reference applications an external positive reference voltage forces current through R_{14} into the $V_{REF}(+)$ terminal (Pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to $V_{REF}(-)$ at Pin 15; reference current flows from ground through R_{14} into $V_{REF}(+)$, as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at Pin 15. The voltage at Pin 14 is equal to and tracks the voltage at Pin 15 due to the high gain of the internal reference amplifier. R_{15}(nominally equal to R_{14}) is used to cancel bias current errors and may be eliminated with only a minor increase in error.

When a DC reference in used, a reference bypass capacitor is recommended. A 5V TTL logic supply is not recommended as reference. If a regulated power supply is used as a reference, R_{14} should be split into two resistors with the junction bypassed to ground with a 0.1µF capacitor.

For most applications the tight relationship between I_{REF} and I_{FR} will eliminate the need for trimming I_{REF}. If required, full-scale trimming may be accomplished by adjusting the value of R_{14}.

The reference amplifier must be compensated by using a capacitor form Pin 16 to V–. For fixed reference operation, a 0.01µF capacitor is recommended. For variable reference applications, see section entitled "Multiplying Operation."

LOGIC INPUT OPERATION AND INTERFACING



LOGIC THRESHOLD CONTROL

The DAC-20 design incorporates a unique logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 2µA logic input current and completely adjustable logic threshold voltage. For V– = –15V, the logic inputs may swing between –10V and +18V. This enables direct interface with a +15V CMOS logic, even when the DAC-20 is powered from a +5V supply. Minimum logic threshold voltage are given by: V– plus ($I_{REF} \times 800\Omega$) plus 2.5V. The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control pin (Pin 1, V_{LC}).

The logic input threshold is 1.4V above V_{LC}. For TTL and DTL interface, simply ground Pin 1. When interfacing ECL, an I_{REF} = 1mA is recommended. For interfacing other logic families, see the figure. Pin 1 will source 100µA typically, so the external circuitry must be designed to accommodate this current. Note that the threshold voltage has the temperature dependence of two forward biased diodes. The two V_{LC} setting circuits shown, include temperature compensation.

Fastest settling times are obtained when Pin 1 sees a low impedance. If Pin 1 is connected to a 1kΩ divider, for example, it should be bypassed to ground by a 0.01µF capacitor.

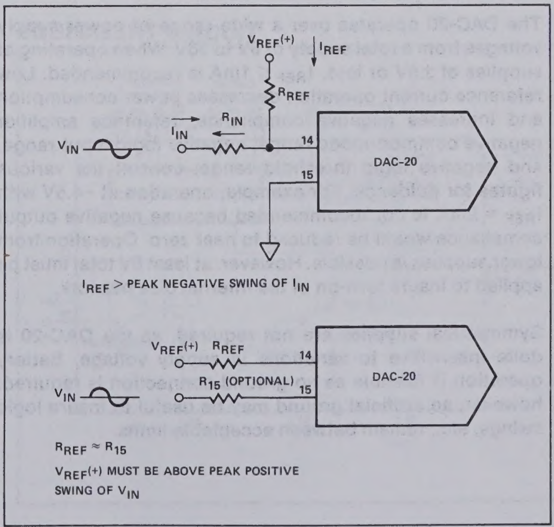
MULTIPLYING OPERATION

The DAC-20 provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 2mA to 4µA. Monotonic operation is maintained over a typical range of I_{REF} from 100µA to 2mA.

Bipolar references may be accommodated by offsetting V_{REF} or Pin 15. The negative common-mode range of the reference amplifier is given by: V_{CM-} = V– plus ($I_{REF} \times 800\Omega$) plus 2.5V. The positive common mode range is V+ less 1.5V.

AC reference applications will require the reference amplifier to be compensated using a capacitor from Pin 16 to V–. The value of this capacitor depends on the impedance presented to Pin 14: for R_{14} values of 1.0, 2.5 and 5.0kΩ, minimum value of C_C are 15, 37, and 75pF. Larger values of R_{14} require

ACCOMMODATING BIPOLAR REFERENCES

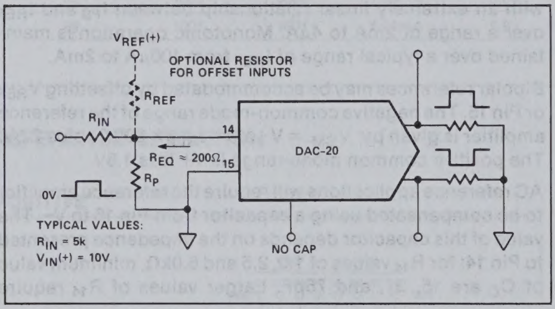


proportionately increased values of C_C for proper phase margin.

For fastest response to a pulse, low values of R_{14} enabling small C_C values should be used. If Pin 14 is driven by a high impedance such as a transistor current source, none of the above values will suffice and the amplifier must be heavily compensated, which will decrease overall bandwidth and slew rate. For $R_{14} = 1k\Omega$ and $C_C = 15pF$, the reference amplifier slews at 4mA/µs enabling a transition from $I_{REF} = 0$ to $I_{REF} = 2mA$ in 500ns.

Operation with pulse inputs to the reference amplifier may be accommodated by the alternate compensation scheme shown above. This technique provides lowest full-scale transition times. An internal clamp allows quick recovery of the reference amplifier for a cutoff ($I_{REF} = 0$) condition. Full-scale transition (0 to 2mA) occurs in 120ns when the equivalent impedance at Pin 14 is 200Ω and $C_C = 0$. This yields a reference slew rate of 16mV/µs, which is relatively independent of R_{IN} and V_{IN} values.

PULSED REFERENCE OPERATION



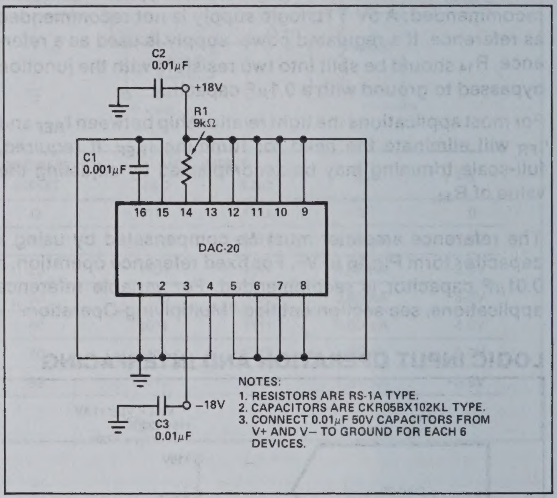
POWER SUPPLY CONSIDERATIONS

The DAC-20 operates over a wide range of power supply voltages from a total supply of 9V to 36V. When operating at supplies of ±5V or less, $I_{REF} \leq 1mA$ is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common-mode range, negative logic input range, and negative logic threshold range; consult the various figures for guidance. For example, operation at −4.5V with $I_{REF} = 2mA$ is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible. However, at least 8V total must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the DAC-20 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required: however, an artificial ground may be useful to insure logic swings, etc., remain between acceptable limits.

Power Consumption may be calculated as follows: $P_d = (1+)(V+) + (1-)(V-)$. A useful feature of the DAC-20 design is that supply current is constant and independent of input logic states; this reduces the size of the power supply bypass capacitors.

BURN-IN CIRCUIT



NOTES:
1. RESISTORS ARE RS-1A TYPE.
2. CAPACITORS ARE CKR05BX102KL TYPE.
3. CONNECT 0.01µF 50V CAPACITORS FROM V+ AND V− TO GROUND FOR EACH 6 DEVICES.

TEMPERATURE PERFORMANCE

The nonlinearity and monotonicity specification of the DAC-20 are guaranteed to apply over the entire rated operating temperature range. Full-scale output current drift is tight, typically ±10ppm/°C, with zero-scale output current and drift essentially negligible compared to 1/2 LSB.

The temperature coefficient of the reference resistor R_{14} should match and track that of the output resistor for minimum overall full-scale drift.

SETTLING TIME OPTIMIZATION

The DAC-20 is capable of extremely fast settling times, typically 85ns at $I_{REF} = 2.0mA$. Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The output capacitance of the DAC-20, including the package, is approximately 15pF; therefore the output RC time constant dominates settling time if $R_L > 500\Omega$.

Fastest operation can be obtained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is independent of input logic states; 0.1µF capacitors at the supply pins provide full transient protection.

COMDAC®
COMPANDING D/A CONVERTER
(μ-255 LAW)

DAC-86

FEATURES

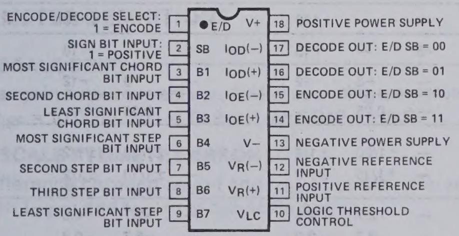
- **Conforms With Bell System μ-255 Companding Law**
- **Meets D3 Compandor Tracking Specifications**
- **Both Encode and Decode Capability**
- **Tight Full-Scale Tolerance Eliminates Calibration**
- **Low Full-Scale Drift Over Temperature**
- **Extremely Low Noise Contribution**
- **Multiplying Reference Inputs**
- **Simplifies PCM System Design**
- **High Reliability**
- **Low Power Consumption and Low Cost**
- **Two Grades Available**

GENERAL DESCRIPTION

The DAC-86 monolithic COMDAC® D/A Converter provides a 15 segment linear approximation to the Bell System μ-255 companding law. The law is implemented by using three bits to select one of eight binarily-related chords (or segments) and four bits to select one of sixteen linearly-related steps within each chord. A sign bit determines signal polarity, and an encode/decode input determines the mode of operation.

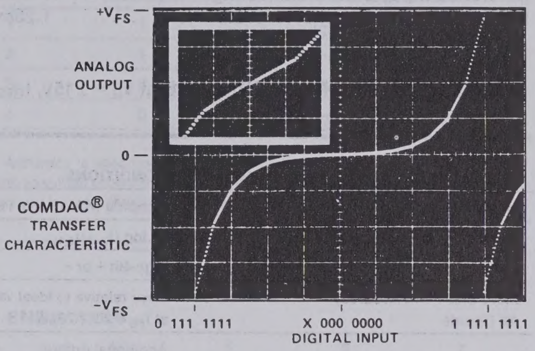
Accuracy is assured by specifying chord end point values, step non-linearity, and monotonicity over the full operating temperature range. Typical applications include PCM carrier systems, digital PBX's intercom systems, and PCM recording. For CCITT "A" Law models, refer to the DAC-89 data sheet.

PIN CONNECTIONS & ORDERING INFORMATION


ENCODE/DECODE SELECT: 1 = ENCODE
1
E/D
SIGN BIT INPUT: 1 = POSITIVE
2
SB
MOST SIGNIFICANT CHORD BIT INPUT
3
B1
SECOND CHORD BIT INPUT
4
B2
LEAST SIGNIFICANT CHORD BIT INPUT
5
B3
MOST SIGNIFICANT STEP BIT INPUT
6
B4
SECOND STEP BIT INPUT
7
B5
THIRD STEP BIT INPUT
8
B6
LEAST SIGNIFICANT STEP BIT INPUT
9
B7
V+
18
POSITIVE POWER SUPPLY
IOD(−)
17
DECODE OUT: E/D SB = 00
IOD(+)
16
DECODE OUT: E/D SB = 01
IOE(−)
15
ENCODE OUT: E/D SB = 10
IOE(+)
14
ENCODE OUT: E/D SB = 11
V−
13
NEGATIVE POWER SUPPLY
VR(−)
12
NEGATIVE REFERENCE INPUT
VR(+)
11
POSITIVE REFERENCE INPUT
VLC
10
LOGIC THRESHOLD CONTROL

18-PIN HERMETIC DUAL-IN-LINE
(X-Suffix)

GRADE	TEMP. RANGE	ACCURACY
DAC-86EX	−25°C/+85°C	±1/2 Step
DAC-86CX	−25°C/+85°C	±1 Step



BELL μ-255 LAW TRANSFER CHARACTERISTIC

The DAC-86 transfer characteristic is a piecewise linear approximation to the Bell System μ-255 law expressed by:

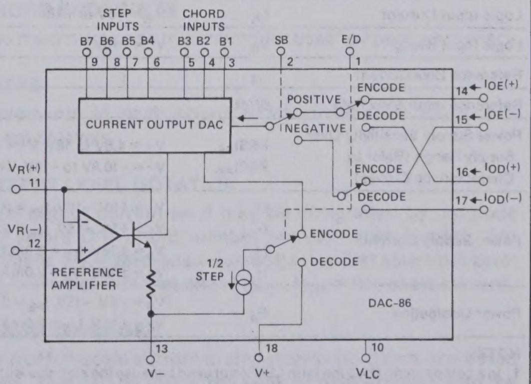
$$Y(\chi) = \operatorname{sgn}(\chi)\,\frac{\ln(1+\mu|\chi|)}{\ln(1+\mu)} \quad -1 \le \chi \le 1$$

for a normalized coding range of ±1

where: χ = input signal level
Y = output compressed signal level
$\mu = 255$

This law is implemented with a eight chord (or segment) piecewise linear approximation with 16 linear steps in each chord. Dynamic range of 72dB in both polarities is achieved with eight-bit coding.

EQUIVALENT CIRCUIT


STEP INPUTS
CHORD INPUTS
B7 B6 B5 B4
9 8 7 6
B3 B2 B1
5 4 3
SB
2
E/D
1
CURRENT OUTPUT DAC
POSITIVE
NEGATIVE
ENCODE
DECODE
ENCODE
DECODE
14 ← IOE(+)
15 ← IOE(−)
16 ← IOD(+)
17 ← IOD(−)
VR(+)
11
VR(−)
12
REFERENCE AMPLIFIER
1/2 STEP
ENCODE
DECODE
DAC-86
13
V−
18
V+
10
VLC

ABSOLUTE MAXIMUM RATINGS

V+ Supply to V− Supply	36V
V_{LC} Swing	V− plus 8V to V+
Analog Current Outputs	V− plus 8V to V− plus 36V
Reference Inputs	V− to V+
Reference Input Differential Voltage	±18V
Reference Input Current	1.25mA
Logic Inputs	V− plus 8V to V− plus 36V
Operating Temperature	−25°C to +85°C
Storage Temperature	−65°C to +150°C
Power Dissipation	500mW
Derate Above 100°C	10mW/°C
Lead Temperature (Soldering, 60 sec)	300°C

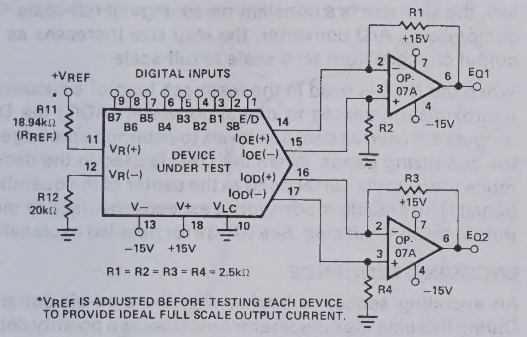
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $I_{REF} = 528\mu A$, $-25°C \le T_A \le +85°C$, for all 4 outputs, unless otherwise noted.

			DAC-86E			DAC-86C			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Resolution		8 chords with 16 steps each	±128	±128	±128	±128	±128	±128	Steps
Dynamic Range		20 log ($I_{7,15}/I_{0,1}$)	72	72	72	72	72	72	dB
Monotonicity		Sign-Bit + or −	128	—	—	128	—	—	Steps
Chord End-Point Accuracy All Chords		Error relative to ideal values at $I_{FS} = 2007.75\mu A$	—	—	±1/2	—	—	±1	Step
Encode Decision Level Current		Additional output encode/decode = 1	3/8	1/2	5/8	1/4	1/2	3/4	Step
Settling Time (Note 1)	t_S	To within ±1/2 step	—	1	—	—	1	—	μsec
Full-Scale Drift (C_7) (Note 2)	ΔI_{FS}	Full temperature range	—	±1/16	±1/10	—	±1/10	±1/4	Step
Output Voltage Compliance	V_{OC}	Full-scale current change ≤ 1/2 step	−5	—	+18	−5	—	+18	Volts
Full-Scale Symmetry Error	$I_O(+) - I_O(-)$	Decode or encode pair Input Code 111 1111	—	±1/40	±1/8	—	±1/40	±1/4	Step
Zero-Scale Current (C_0)	I_{ZS}	Measured at selected output with 000 0000 input	—	1/40	1/8	—	1/40	1/4	Step
Disable Current (All bits high)	I_{DIS}	Leakage of output disabled by E/D and SB	—	5	75	—	5	75	nA
Step Accuracy All Chords		Error relative to ideal values at $I_{FS} = 2007.75\mu A$	—	—	±1/2	—	—	±1	Step
Output Current Range	I_{FSR}		4.2	2.0	—	4.2	2.0	—	mA
Logic Input Levels, Logic "0"	V_{IL}	$V_{LC} = 0V$	—	—	0.8	—	—	0.8	Volts
Logic Input Levels, Logic "1"	V_{IH}	$V_{LC} = 0V$	2	—	—	2	—	—	Volts
Logic Input Current	I_{IN}	$V_{IN} = -5V$ to $+18V$	—	—	120	—	—	120	μA
Logic Input Swing	V_{IS}	$V- = -15V$	−5	—	+18	−5	—	+18	Volts
Reference Bias Current	I_{12}		—	−3	−12	—	−3	−12	μA
Reference Input Slew Rate	dI/dt		—	0.25	—	—	0.25	—	mA/μs
Power Supply Sensitivity Over Supply Range (Refer to Characteristic Curves)	$PSSI_{FS+}$ $PSSI_{FS-}$	$V+ = 4.5V$ to $18V$, $V- = -15V$ $V- = -10.8V$ to $-18V$, $V+ = 15V$	— —	±1/20 ±1/10	±1/2 ±1/2	— —	±1/20 ±1/10	±1/2 ±1/2	Step
Power Supply Current	I+ I− I+ I−	$V_S = +5V, -15V$, $I_{FS} = 2.0mA$ $V_S = +5V, -15V$, $I_{FS} = 2.0mA$ $V_S = \pm 15V$, $I_{FS} = 2.0mA$ $V_S = \pm 15V$, $I_{FS} = 2.0mA$	— — — —	2.7 −6.7 2.7 −6.7	4.5 −9.3 4.5 −9.3	— — — —	2.7 −6.7 2.7 −6.7	4.5 −9.3 4.5 −9.3	mA
Power Dissipation	P_d	$V_S = +5V, -15V$, $I_{FS} = 2.0mA$ $V_S = \pm 15V$, $I_{FS} = 2.0mA$	— —	114 141	167 207	— —	114 141	167 207	mW

NOTE:

1. In a companding DAC the term LSB is not used because the step size within each chord is different. For example, in the first chord around zero (C_O) step size is 0.5μA, while in the last chord near full-scale (C_7) step size is 64μA. Settling time varies for each of the chord bits and step bits and a maximum specification is misleading. In decode operation, the DAC-86 and OP-16 combination will decode eight channels. In the encode mode, the DAC-86 and CMP-01 combination will encode eight channels. Both encode and decode statements assume a 5.2μsec channel time.
2. Guaranteed by design.

OUTPUT CURRENT DC TEST CIRCUIT



R1 = R2 = R3 = R4 = 2.5kΩ

*VREF IS ADJUSTED BEFORE TESTING EACH DEVICE TO PROVIDE IDEAL FULL SCALE OUTPUT CURRENT.

LINE SELECTION TABLE

TEST GROUP	ENCODE/ DECODE	SIGN BIT	OUTPUT MEASUREMENT	
1	1	1	$I_{OE}(+)$	$(E_{01}/R1)$
2	1	0	$I_{OE}(-)$	$(E_{01}/R2)$
3	0	1	$I_{OD}(+)$	$(E_{02}/R3)$
4	0	0	$I_{OD}(-)$	$(E_{02}/R4)$

NOTE: Accuracy is specified in the test circuit using the tables below to be within the specified proportion of a step at the maximum value in each chord. Monotonicity is guaranteed for all input codes.

CONDENSED CURRENT OUTPUT TABLES ($I_{REF} = 528\mu A$)

IDEAL DECODE OUTPUT CURRENT IN MICROAMPS AT CHORD ENDPOINTS

	CHORD	0	1	2	3	4	5	6	7
STEP		000	001	010	011	100	101	110	111
0	0000	0.0	8.25	24.75	57.75	123.75	255.75	519.75	1047.75
15	1111	7.5	23.25	54.75	117.75	243.75	495.75	999.75	2007.75
STEP SIZE		0.5	1	2	4	8	16	32	64

IDEAL ENCODE OUTPUT CURRENT IN MICROAMPS AT CHORD ENDPOINTS

	CHORD	0	1	2	3	4	5	6	7
STEP		000	001	010	011	100	101	110	111
0	0000	0.25	8.75	25.75	59.75	127.75	263.75	535.75	1079.75
15	1111	7.75	23.25	55.75	119.75	247.75	503.75	1015.75	2039.75
STEP SIZE		0.50	1	2	4	8	16	32	64

These tables may be extended to include all of the encode/decode currents (ideal with $SI_{REF} = 528\mu A$) by multiplying any of the numbers in the normalized tables by $0.5\mu A$.

PARAMETER DEFINITIONS

FULL-SCALE DRIFT

The change in output current over the full operating temperature with $V_{REF} = 10.000V$, R11 = 18.94kΩ, and R12 = 20kΩ.

FULL-SCALE SYMMETRY ERROR

The difference between $I_{OD}(-)$ and $I_{OD}(+)$ or the difference between $I_{OE}(-)$ and $I_{OE}(+)$ at full-scale output.

OUTPUT VOLTAGE COMPLIANCE

The maximum output voltage swing at any current level which causes <1/2 step change in output current.

CHORDS

Groups of linearly-related steps in the transfer function. Also known as segments.

CHORD ENDPOINTS

The maximum code in each chord; used to specify accuracy.

STEPS

Increments in each chord which divides the chord into 16 equal levels.

OUTPUT LEVEL NOTATION

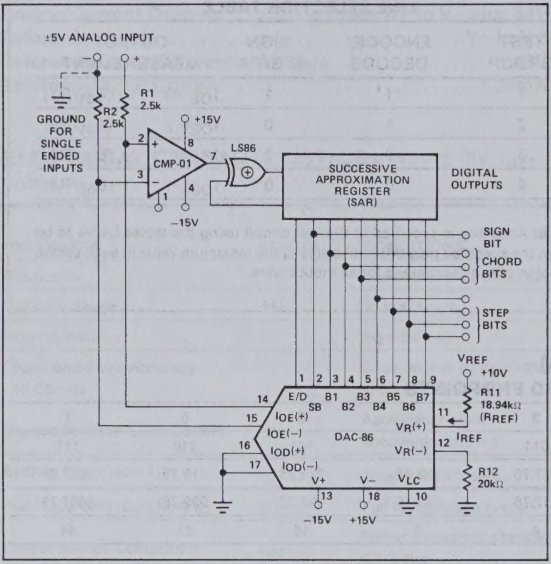
Each output current level may be designated by the code $I_{C,S}$ where C = chord number and S = step number. For example, $I_{0,0}$ = zero-scale current; $I_{0,1}$ = first step from zero; $I_{0,15}$ = endpoint of first chord (C_0); $I_{7,15}$ = full-scale current.

DYNAMIC RANGE

Ratio of full-scale current to step size in chord zero expressed in dB. This can be measured peak or peak-to-peak with the same result.

BASIC ENCODE OPERATION (COMPRESSING A/D CONVERSION)

BASIC ENCODE CONNECTIONS



ENCODE DECISION LEVELS

Compressing A/D conversion with the DAC-86 requires a comparator, an EXCLUSIVE-OR gate, and a successive approximation register — the usual elements in any sign magnitude A/D converter. However, a compressing A/D has one significant difference. In a conventional (linear converter), the step size is a constant percentage of full-scale. In a compressing A/D converter, the step size increases as the output changes from zero-scale to full-scale.

When the DAC is used in the feedback loop of a successive approximation analog to digital converter (ADC) the DAC outputs are used as decision levels to determine the edges of the quantizing bands. When the DAC is used in the decode mode the outputs correspond to the center of the quantizing bands. The encode mode output exceeds the decode mode output by one-half step. See AN-39 for detailed explanation.

ENCODING SEQUENCE

An encoding sequence begins with the sign-bit decision. During this time the comparator functions as a polarity detector. The encode/decode (E/D) input is held at a logic "0". In this mode, current flows into the decode outputs, and the comparator is effectively disconnected from the DAC. Once the input polarity has been determined, the E/D input toggles to a logic "1" allowing current to flow into $I_{OE}(+)$ or $I_{OE}(-)$.

For positive inputs, current flows into $I_{OE}(+)$ through R1, and the comparator's output is entered as the answer for each successive decision. For negative inputs, current flows into $I_{OE}(-)$ through R2 developing a negative voltage which is compared with the analog input. An EXCLUSIVE-OR gate inverts the comparator's output during negative trials to maintain the proper logic coding, all ones for full-scale and all zeros for zero-scale.

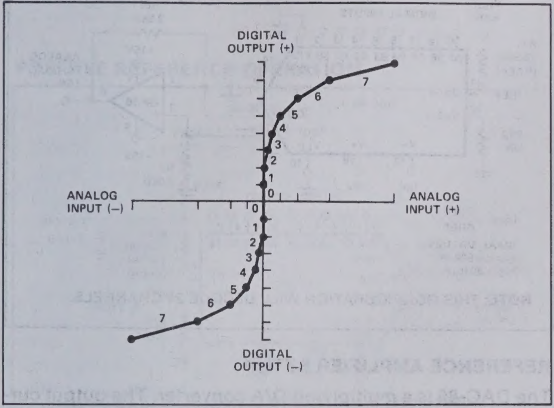
The bits are converted with a successive removal technique, starting with a decision at the code 011 1111 and turning off bits sequentially until all decisions have been made.

NORMALIZED ENCODE LEVEL (SIGN BIT EXCLUDED) $(I_{C,S} = 2[2^{C}(S+17) - 16.5]$

C = chord no. (0 through 7)
S = step no. (0 through 15)

CHORD		0	1	2	3	4	5	6	7
STEP		000	001	010	011	100	101	110	111
0	0000	1	35	103	239	511	1055	2143	4319
1	0001	3	39	111	255	543	1119	2271	4575
2	0010	5	43	119	271	575	1183	2399	4831
3	0011	7	47	127	287	607	1247	2527	5087
4	0100	9	51	135	303	639	1311	2655	5343
5	0101	11	55	143	319	671	1375	2783	5599
6	0110	13	59	151	335	703	1439	2911	5855
7	0111	15	63	159	351	735	1503	3039	6111
8	1000	17	67	167	367	767	1567	3167	6367
9	1001	19	71	175	383	799	1631	3295	6623
10	1010	21	75	183	399	831	1695	3423	6879
11	1011	23	79	191	415	863	1759	3551	7135
12	1100	25	83	199	431	895	1823	3679	7391
13	1101	27	87	207	447	927	1887	3807	7647
14	1110	29	91	215	463	959	1951	3935	7903
15	1111	31	95	223	479	991	2015	4063	8159
STEP SIZE		2	4	8	16	32	64	128	256

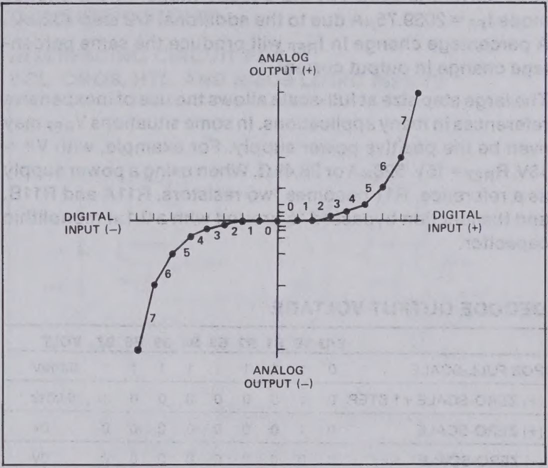
ENCODE TRANSFER CHARACTERISTICS (A/D CONVERSION)



BASIC DECODE OPERATION (EXPANDING D/A CONVERSION)

D/A conversion with the DAC-86 is implemented by using an operational amplifier connected to the decode outputs. The decode mode of operation is selected by applying a logic "0" to the encode/decode input. This enables the $I_{OD}(+)$ or $I_{OD}(-)$ to be selected by the sign-bit input. When the sign-bit input is high, a logic "1", all of the output current flows into $I_{OD}(+)$ forcing a positive voltage at the operational amplifier's output. When the sign-bit input is low, logic "0", all of the output current flows into $I_{OD}(-)$ through R2 forcing a negative voltage output. The sign-bit steers current into $I_{OD}(+)$ or $I_{OD}(-)$, therefore the output will always be symmetrical, limited only by the matching of R1 and R2.

DECODE TRANSFER CHARACTERISTIC (D/A CONVERSION)



NORMALIZED DECODE OUTPUT (SIGN BIT EXCLUDED) $(I_{C,S} = 2[2^C(S+16.5)-16.5]$

C = chord no. (0 through 7)
S = step no. (0 through 15)

STEP	CHORD	0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	0	33	99	231	495	1023	2079	4191
1	0001	2	37	107	247	527	1087	2207	4447
2	0010	4	41	115	263	559	1151	2335	4703
3	0011	6	45	123	279	591	1215	2463	4959
4	0100	8	49	131	295	623	1279	2591	5215
5	0101	10	53	139	311	655	1343	2719	5471
6	0110	12	57	147	327	687	1407	2847	5727
7	0111	14	61	155	343	719	1471	2975	5983
8	1000	16	65	163	359	751	1535	3103	6239
9	1001	18	69	171	375	783	1599	3231	6495
10	1010	20	73	179	391	815	1663	3359	6751
11	1011	22	77	187	407	847	1727	3487	7007
12	1100	24	81	195	423	879	1791	3615	7263
13	1101	26	85	203	439	911	1855	3743	7519
14	1110	28	89	211	455	943	1919	3871	7775
15	1111	30	93	219	471	975	1983	3999	8031
STEP SIZE		2	4	8	16	32	64	128	256

NORMALIZED TABLES

The encode and decode tables are used to calculate the ideal output current at any point. For example, in decode mode at $I_{3,7}$ (011 0111) find 343. 343/8031 × I_{FS} = 85.75μA (I_{FS} = 2007.75μA). Alternatively, use the condensed current tables and add up the number of steps.

BASIC REFERENCE CONSIDERATIONS

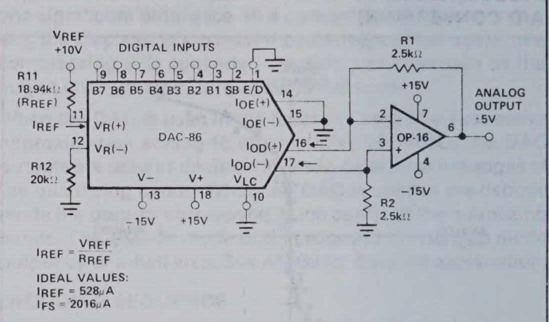
Full-scale output current is ideally 2007.75μA when the reference current is 528μA in the decode mode. In the encode mode I_{FS} = 2039.75μA due to the additional 1/2 step (32μA). A percentage change in I_{REF} will produce the same percentage change in output current.

The large step size at full-scale allows the use of inexpensive references in many applications. In some situations V_{REF} may even be the positive power supply. For example, with V+ = 15V, R_{REF} = 15V/528μA or 28.4kΩ. When using a power supply as a reference, R11 becomes two resistors, R11A and R11B, and the junction bypassed to ground with a 0.1μf monolithic capacitor.

DECODE OUTPUT VOLTAGE

	E/D	SB	B1	B2	B3	B4	B5	B6	B7	VOLT
POS FULL-SCALE	0	1	1	1	1	1	1	1	1	5.019V
(+) ZERO-SCALE +1 STEP	0	1	0	0	0	0	0	0	1	0.0012
(+) ZERO-SCALE	0	1	0	0	0	0	0	0	0	0V
(−) ZERO-SCALE	0	0	0	0	0	0	0	0	0	0V
(−) ZERO-SCALE +1 STEP	0	0	0	0	0	0	0	0	1	−0.0012
NEG FULL-SCALE	0	0	1	1	1	1	1	1	1	−5.019V

BASIC DECODE CONNECTIONS


VREF
+10V
DIGITAL INPUTS
R11
18.94kΩ
(RREF)
IREF
R12
20kΩ
9 8 7 6 5 4 3 2 1
B7 B6 B5 B4 B3 B2 B1 SB E/D
11
VR(+)
12
VR(−)
DAC-86
IOE(+)
14
IOE(−)
15
IOD(+)
16
IOD(−)
17
V−
V+
VLC
13
18
10
−15V
+15V
R1
2.5kΩ
+15V
2
3
7
4
6
OP-16
−15V
R2
2.5kΩ
ANALOG
OUTPUT
±5V
IREF = VREF / RREF
IDEAL VALUES:
IREF = 528μA
IFS = 2016μA

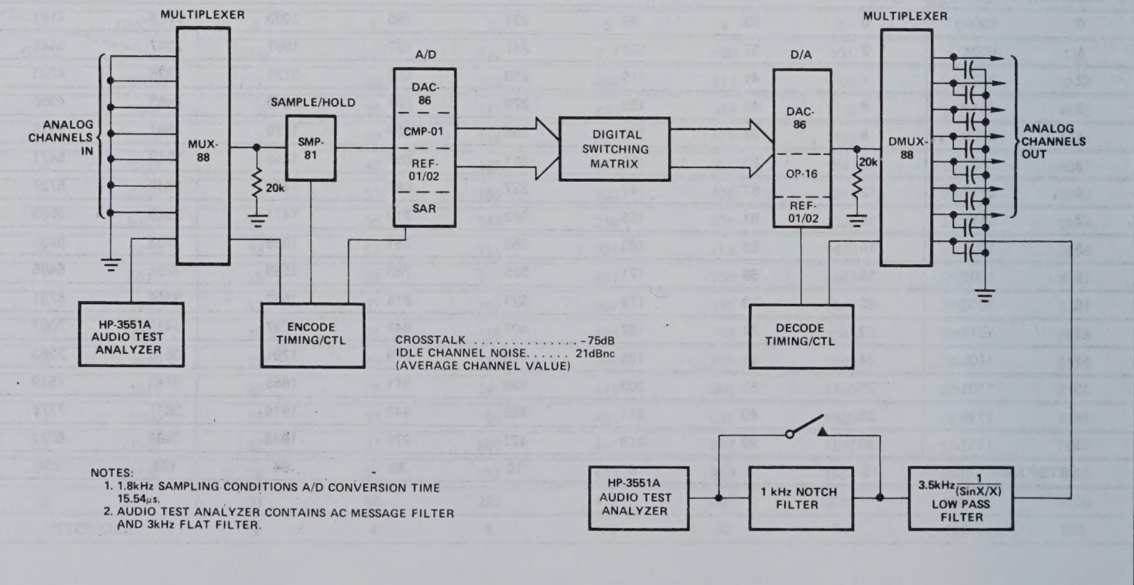
NOTE: THIS CONFIGURATION WILL DECODE 24 CHANNELS.

REFERENCE AMPLIFIER SETUP

The DAC-86 is a multiplying D/A converter. The output current is the product of the normalized digital input and the input reference current. The reference current may be fixed or may vary from nearly zero to +1.0mA. The full-scale output current is a linear function of the reference current.

In external reference applications a positive reference voltage forces current through R11 in the the $V_R(+)$ terminal (pin 11) of the reference amplifier. Alternatively, a negative reference may be applied to $V_R(-)$ at pin 12; reference current flows from ground through R11 into $V_R(+)$. This negative reference connection has the advantage of presenting a very high impedance at pin 12. The voltage at pin 11 is equal to and tracks the voltage at pin 12 due to the high gain of the internal

SYSTEM TEST CIRCUIT

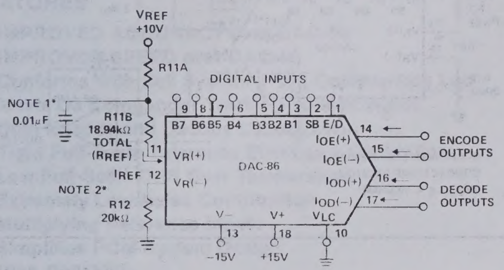

MULTIPLEXER
ANALOG
CHANNELS
IN
MUX-
88
SAMPLE/HOLD
SMP-
81
20k
A/D
DAC-
86
CMP-01
REF-
01/02
SAR
DIGITAL
SWITCHING
MATRIX
D/A
DAC-
86
OP-16
REF-
01/02
20k
MULTIPLEXER
DMUX-
88
ANALOG
CHANNELS
OUT
HP-3551A
AUDIO TEST
ANALYZER
ENCODE
TIMING/CTL
DECODE
TIMING/CTL
HP-3551A
AUDIO TEST
ANALYZER
1 kHz NOTCH
FILTER
3.5kHz 1/(SinX/X)
LOW PASS
FILTER

CROSSTALK . . . . -75dB
IDLE CHANNEL NOISE. 21dBnc
(AVERAGE CHANNEL VALUE)

NOTES:
1. 1.8kHz SAMPLING CONDITIONS A/D CONVERSION TIME 15.54μs.
2. AUDIO TEST ANALYZER CONTAINS AC MESSAGE FILTER AND 3kHz FLAT FILTER.

reference amplifier. R12 (nominally equal to R11) is used to cancel bias current errors and may be eliminated with a minor increase in error.

POSITIVE REFERENCE OPERATION


VREF
+10V
R11A
DIGITAL INPUTS
NOTE 1*
0.01μF
R11B
18.94kΩ
TOTAL
(RREF)
IREF
NOTE 2*
R12
20kΩ
9 8 7 6 5 4 3 2 1
B7 B6 B5 B4 B3 B2 B1 SB E/D
11
12
VR(+)
VR(−)
DAC-86
IOE(+)
IOE(−)
IOD(+)
IOD(−)
14
15
16
17
ENCODE OUTPUTS
DECODE OUTPUTS
V−
V+
VLC
13
18
10
−15V
+15V

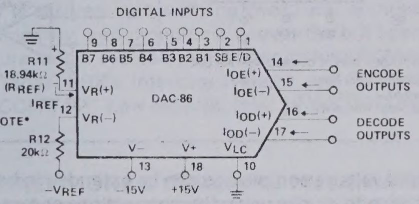
$I_{REF} = \frac{V_{REF}}{R_{REF}}$

DECODE OUTPUTS IDEAL VALUES:	ENCODE OUTPUTS IDEAL VALUES:
$I_{REF} = 528\mu A$	$I_{REF} = 528\mu A$
$I_{FS} = 2016\mu A$	$I_{FS} = 2048\mu A$

NOTES:

1. RECOMMENDED WHEN V_{REF} IS V+ OR THE LOGIC POWER SUPPLY.
2. PINS 11 AND 12 ARE EQUAL IN VOLTAGE. V_{REF} IS IMPRESSED ACROSS R11 (R_{REF}).

NEGATIVE REFERENCE OPERATION


DIGITAL INPUTS
R11
18.94kΩ
(RREF)
IREF
NOTE*
R12
20kΩ
−VREF
9 8 7 6 5 4 3 2 1
B7 B6 B5 B4 B3 B2 B1 SB E/D
11
12
VR(+)
VR(−)
DAC-86
IOE(+)
IOE(−)
IOD(+)
IOD(−)
14
15
16
17
ENCODE OUTPUTS
DECODE OUTPUTS
V−
V+
VLC
13
18
10
−15V
+15V

$I_{REF} = -\frac{-V_{REF}}{R_{REF}}$

DECODE OUTPUTS IDEAL VALUES:	ENCODE OUTPUTS IDEAL VALUES:
$I_{REF} = 528\mu A$	$I_{REF} = 528\mu A$
$I_{FS} = 2016\mu A$	$I_{FS} = 2048\mu A$

NOTE:

PINS 11 AND 12 ARE EQUAL IN VOLTAGE. V_{REF} IS IMPRESSED ACROSS R11 (R_{REF}).

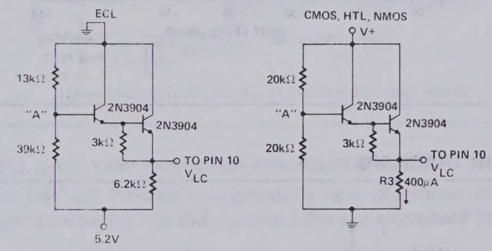
REFERENCE AMPLIFIER OPERATION

For most applications a +10.0V reference, such as the PMI REF-01, is recommended for optimum full-scale temperature performance. (This also minimizes the contributions of reference amplifier V_{OS} and TCV_{OS}). For most applications the tight relationship between I_{REF} and I_{FS} eliminates the need for trimming I_{REF}; but if desired full-scale trimming is accomplished by selecting R11 or by using a potentiometer for R11.

Using lower values of reference current reduces negative power supply current and increases reference amplifier negative common-mode range. While the recommended operating range of DC reference current is 0.1mA to 1.0mA, monotonic operation is maintained over an even wider range.

LOGIC INPUT AND POWER SUPPLY CONSIDERATIONS

INTERFACING CIRCUIT FOR ECL, CMOS, HTL, AND NMOS LOGIC INPUTS


ECL
13kΩ
"A"
39kΩ
2N3904
3kΩ
2N3904
TO PIN 10
VLC
6.2kΩ
5.2V
CMOS, HTL, NMOS
V+
20kΩ
"A"
20kΩ
2N3904
3kΩ
2N3904
TO PIN 10
VLC
R3
400μA

NOTES:

1. SET THE VOLTAGE "A" TO BE AT THE DESIRED LOGIC INPUT SWITCHING THRESHOLD.
2. ALLOWABLE RANGE OF LOGIC THRESHOLD IS TYPICALLY −5V TO +13V WHEN OPERATING THE DAC-86 ON ±15V SUPPLIES.

LOGIC INPUTS

The DAC-86 interfaces with various logic families by referencing V_{LC} (pin 10) at a potential which is 1.4V below the desired logic input switching threshold. However, this voltage source must be capable of sourcing and sinking a changing current at pin 10.

The negative voltage at the logic inputs must be limited to +10V with respect to V− (pin 13).

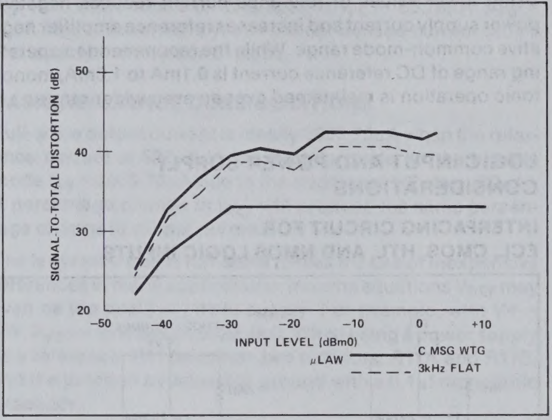
POWER SUPPLIES

Power supply current drain is relatively independent of voltage and temperature and completely independent of the logic input states.

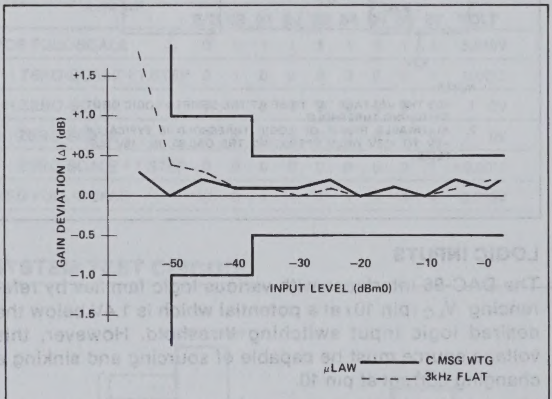
When operating with V− between −15V and −11V, output negative voltage compliance, $V_{OC}(-)$, reference input amplifier common-mode voltage range, and logic input negative voltage range are reduced by an amount equivalent to the difference between −15V and the V− supply in use. Operation with V+ between +5V and +15V affects V_{LC} and the reference amplifier common-mode positive voltage range in the same manner.

SYSTEM PERFORMANCE CHARACTERISITCS

SIGNAL TO QUANTIZING DISTORTION vs INPUT LEVEL



GAIN TRACKING



OUTPUT VOLTAGE COMPLIANCE

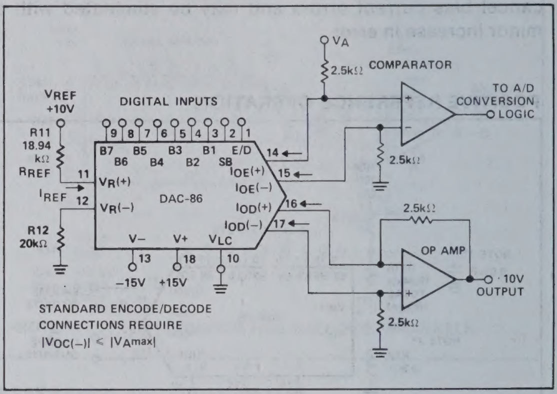
The DAC-86 has true current outputs with wide voltage compliance that enables single ended and balanced load drive capability. Positive voltage compliance is +18V and negative voltage compliance is −5.0V with $I_{REF} = 528\mu A$ and $V = -15V$. Negative voltage compliance $V_{OC}(-)$ for other values of I_{REF} and V− may be obtained from the table, or calculated as follows:

$$V_{OC}(-)\ \min = (V-) + (2\ I_{REF} \times 1.6k\Omega) + 8.4V$$

DICE

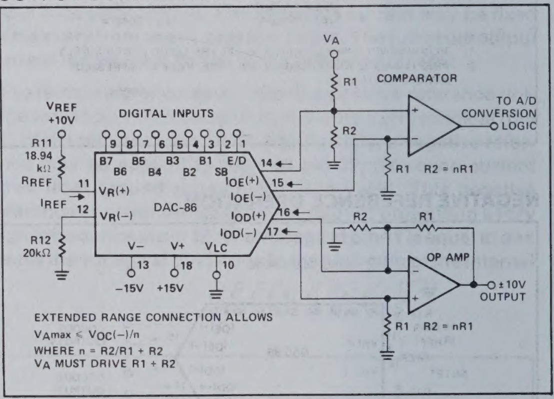
For applicable DICE information, see DAC-88 Data Sheet.

STANDARD OUTPUT CONNECTIONS


VA
2.5kΩ
COMPARATOR
TO A/D CONVERSION LOGIC
VREF +10V
DIGITAL INPUTS
9 8 7 6 5 4 3 2 1
R11 18.94 kΩ
RREF
B7 B5 B3 B1 E/D
B6 B4 B2 SB
11
VR(+)
IREF
12
VR(−)
DAC-86
14
IOE(+)
15
IOE(−)
IOD(+)
16
IOD(−)
17
2.5kΩ
2.5kΩ
R12 20kΩ
V− V+ VLC
13 18 10
−15V +15V
OP AMP
·10V OUTPUT
2.5kΩ

STANDARD ENCODE/DECODE CONNECTIONS REQUIRE $|V_{OC}(-)| \leq |V_{A}max|$

OUTPUT COMPLIANCE EXTENSION CONNECTIONS


VA
R1
COMPARATOR
TO A/D CONVERSION LOGIC
R2
VREF +10V
DIGITAL INPUTS
9 8 7 6 5 4 3 2 1
R11 18.94 kΩ
RREF
B7 B5 B3 B1 E/D
B6 B4 B2 SB
11
VR(+)
IREF
12
VR(−)
DAC-86
14
IOE(+)
15
IOE(−)
IOD(+)
16
IOD(−)
17
R1 R2 = nR1
R2 R1
R12 20kΩ
V− V+ VLC
13 18 10
−15V +15V
OP AMP
±10V OUTPUT
R1 R2 = nR1

EXTENDED RANGE CONNECTION ALLOWS
$V_{A}max \leq V_{OC}(-)/n$
WHERE n = R2/R1 + R2
V_A MUST DRIVE R1 + R2

Output voltage compliance can be extended in both encode and decode modes using the connections shown above.

NEGATIVE OUTPUT VOLTAGE COMPLIANCE $V_{OC}(-)$

V−	I_{FS} 1.0mA	I_{FS} 2.0mA	I_{FS} 4.0mA
−12V	−2.8V	−2.0V	−0.4V
−15V	−5.8V	−5.0V	−3.4V
−18V	−8.8V	−8.0V	−6.4V

MINIMUM NEGATIVE COMPLIANCE

$$V_{OC}(-)\ MIN = (V-) + (2\ I_{REF}\ 1.6k\Omega) + 8.4V$$

COMDAC®
COMPANDING D/A CONVERTER
(μ-255 LAW)

DAC-88

FEATURES

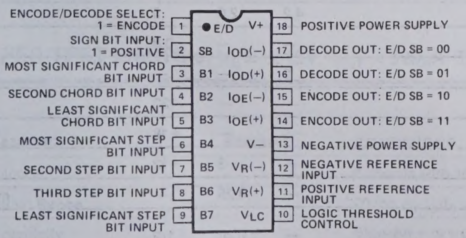
- **IMPROVED ACCURACY over DAC-86**
- **IMPROVED SPEED over DAC-86**
- **Conforms With Bell System μ-255 Companding Law**
- **Meets D3 Compandor Tracking Specifications**
- **Both Encode and Decode Capability**
- **Tight Full-Scale Tolerance Eliminates Calibration**
- **Low Full-Scale Drift Over Temperature**
- **Extremely Low Noise Contribution**
- **Multiplying Reference Inputs**
- **Simplifies PCM System Design**
- **High Reliability**
- **Low Power Consumption and Low Cost**
- **Fully Specified Dice Available**

GENERAL DESCRIPTION

The DAC-88 monolithic COMDAC® D/A Converter provides a 15 segment linear approximation to the Bell System μ-255 companding law. The law is implemented by using three bits to select one of eight binarily-related chords (or segments) and four bits to select one of sixteen linearly-related steps within each chord. A sign bit determines signal polarity, and an encode/decode input determines the mode of operation.

Accuracy is assured by specifying chord end point values, step nonlinearity, and monotonicity over the full operating temperature range. Typical applications include PCM carrier systems, digital PBX's, intercom systems, and PCM recording. For CCITT "A" Law models, refer to the DAC-89 data sheet.

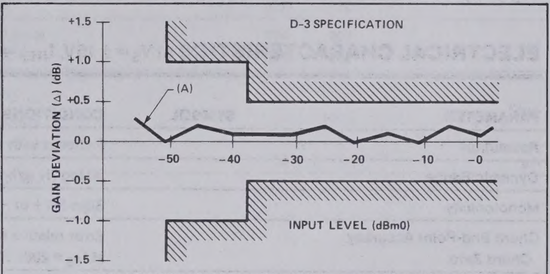
PIN CONNECTIONS & ORDERING INFORMATION


ENCODE/DECODE SELECT: 1 = ENCODE
SIGN BIT INPUT: 1 = POSITIVE
MOST SIGNIFICANT CHORD BIT INPUT
SECOND CHORD BIT INPUT
LEAST SIGNIFICANT CHORD BIT INPUT
MOST SIGNIFICANT STEP BIT INPUT
SECOND STEP BIT INPUT
THIRD STEP BIT INPUT
LEAST SIGNIFICANT STEP BIT INPUT
1 ● E/D
2 SB
3 B1
4 B2
5 B3
6 B4
7 B5
8 B6
9 B7
18 V+
17 IOD(−)
16 IOD(+)
15 IOE(−)
14 IOE(+)
13 V−
12 VR(−)
11 VR(+)
10 VLC
POSITIVE POWER SUPPLY
DECODE OUT: E/D SB = 00
DECODE OUT: E/D SB = 01
ENCODE OUT: E/D SB = 10
ENCODE OUT: E/D SB = 11
NEGATIVE POWER SUPPLY
NEGATIVE REFERENCE INPUT
POSITIVE REFERENCE INPUT
LOGIC THRESHOLD CONTROL

18-PIN HERMETIC DUAL-IN-LINE
(X-Suffix)

Grade	Temp. Range	Accuracy
DAC-88EX	−25° C/+85° C	±1/4 Step

GAIN TRACKING



(A) GAIN TRACKING PERFORMANCE OF DAC-88 IN 8-CHANNEL SYSTEM.

BELL μ-255 LAW TRANSFER CHARACTERISTIC

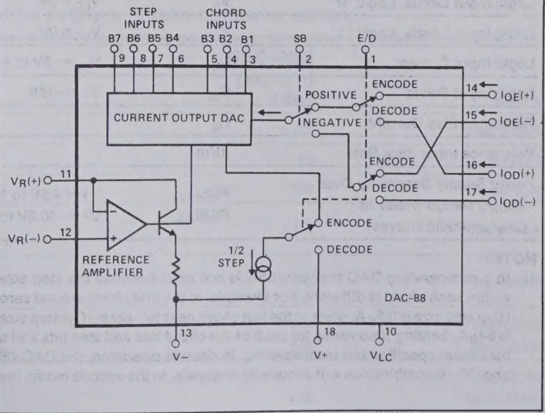
The DAC-88 transfer characteristic is a piecewise linear approximation to the Bell System μ255 law expressed by:

$$Y(\chi) = \operatorname{sgn}(\chi)\ \frac{\ln(1+\mu\,|\chi|)}{\ln(1+\mu)} \quad -1 \leq \chi \leq 1$$

for a normalized coding range of ±1
where: χ = input signal level
Y = output compressed signal level
μ = 255

This law is implemented with an eight chord (or segment) piecewise linear approximation with 16 linear steps in each chord. Dynamic range of 72dB in both polarities is achieved with eight-bit coding.

EQUIVALENT CIRCUIT


STEP INPUTS
CHORD INPUTS
B7 B6 B5 B4
B3 B2 B1
9 8 7 6
5 4 3
SB 2
E/D 1
CURRENT OUTPUT DAC
POSITIVE
NEGATIVE
ENCODE
DECODE
ENCODE
DECODE
14 IOE(+)
15 IOE(−)
16 IOD(+)
17 IOD(−)
VR(+) 11
VR(−) 12
REFERENCE AMPLIFIER
ENCODE
DECODE
1/2 STEP
DAC-88
13 V−
18 V+
10 VLC

ABSOLUTE MAXIMUM RATINGS

V+ Supply to V− Supply	36V
V_{LC} Swing	V− plus 8V to V+
Analog Current Outputs	V− plus 8V to V− plus 36V
Reference Inputs	V− to V+
Reference Input Differential Voltage	±18V
Reference Input Current	1.25mA
Logic Inputs	V− plus 8V to V− plus 36V
Operating Temperature	−25° C to +85° C
Storage Temperature	−65° C to +150° C
Power Dissipation	500mW
Derate Above 100° C	10mW/° C
Lead Temperature (Soldering, 60 sec)	300° C

NOTE: Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $I_{REF} = 528\mu A$, $-25°C \le T_A \le +85°C$, all 4 outputs, unless otherwise noted.

			DAC-88E			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Resolution		8 chords with 16 steps each	±128	±128	±128	Steps
Dynamic Range		20 log ($I_{7,15}/I_{0,1}$)	72	72	72	dB
Monotonicity		Sign-Bit + or −	128	—	—	Steps
Chord End-Point Accuracy Chord Zero		Error relative to ideal values at I_{FS} = 2007.75µA	—	—	±1/4	Step
Chord End-Point Accuracy All Chords Other Than Zero		Error relative to ideal values at I_{FS} = 2007.75µA	—	—	±1/2	Step
Encode Decision Level Current		Additional output encode/decode = 1	3/8	1/2	5/8	Step
Settling Time (Note 1)	t_S	To within ±1/2 step	—	500	—	ns
Settling Time in Chord Zero	T_{SCO}	To within ±1/2 step	—	500	—	ns
Full-scale Drift (C_7) (Note 3)	ΔI_{FS}	Full temperature range	—	±1/16	±1/10	Step
Output Voltage Compliance	V_{OC}	Full-Scale current change ≤ 1/2 step	-5	—	+18	Volts
Full-Scale Symmetry Error (Note 2)	$I_O(+) - I_O(-)$	Decode or encode pair Input Code 111 1111	—	±1/40	±1/8	Step
Zero-Scale Current (C_0) (Note 2)	I_{ZS}	Measured at selected output with 000 0000 input	—	1/40	1/8	Step
Disable Current (All bits high) (Note 2)	I_{DIS}	Leakage of output disabled by E/D and SB	—	5	100	nA
Step Accuracy Chord Zero		Error relative to ideal values at I_{FS} = 2007.75µA	—	—	±1/4	Step
Step Accuracy All Chords Other Than Zero		Error relative to ideal values at I_{FS} = 2016µA	—	—	±1/2	Step
Output Current Range	I_{FSR}		4.2	2.0	0	mA
Logic Input Levels, Logic "0"	V_{IL}	V_{LC} = 0V	—	—	0.8	Volts
Logic Input Levels, Logic "1"	V_{IH}	V_{LC} = 0V	2	—	—	Volts
Logic Input Current	I_{IN}	V_{IN} = −5V to +18V	—	—	120	µA
Logic Input Swing	V_{IS}	V− = −15V	-5	—	+18	Volts
Reference Bias Current	I_{12}		—	-3	-12	µA
Reference Input Slew Rate	dI/dt		—	0.25	—	mA/µs
Power Supply Sensitivity Over Supply Range (Refer to Characteristic Curves)	$PSSI_{FS+}$ $PSSI_{FS-}$	V+ = 4.5V to 18V, V− = −15V V− = −10.8V to −18V, V+ = 15V	— —	±1/20 ±1/10	±1/2 ±1/2	Step

NOTES:

1. In a companding DAC the term LSB is not used because the step size within each chord is different. For example, in the first chord around zero (C_O) step size is 0.5µA, while in the last chord near full-scale (C_7) step size is 64µA. Settling time varies for each of the chord bits and step bits and a maximum specification is misleading. In decode operation, the DAC-88 and OP-16 combination will decode 24 channels. In the encode mode, the DAC-88 and CMP-01 combination will encode eight channels. Both encode and decode statements assume a 5.2µs channel time.
2. Current specifications relate to differential currents between (+) and (−) output leads. At the selected outputs, equal idle currents are present simultaneously on both current output leads.
3. Guaranteed by design.

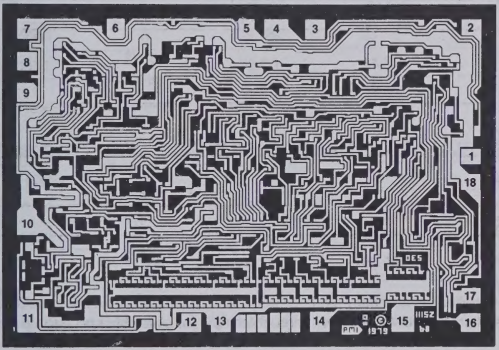
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $I_{REF} = 528\mu A$, $-25°C \leq T_A \leq +85°C$, all 4 outputs, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	DAC-88E MIN	 TYP	 MAX	UNITS
Power Supply Current	I+	$V_S = +5V, -15V, I_{FS} = 2.0mA$	—	2.7	5.5	mA
	I−	$V_S = +5V, -15V, I_{FS} = 2.0mA$	—	−6.7	−12	
	I+	$V_S = \pm 15V, I_{FS} = 2.0mA$	—	2.7	5.5	
	I−	$V_S = \pm 15V, I_{FS} = 2.0mA$	—	−6.7	−12	
Power Dissipation	P_d	$V_S = +5V, -15V, I_{FS} = 2.0mA$	—	114	207	mW
		$V_S = \pm 15V, I_{FS} = 2.0mA$	—	141	262	
Full-Scale Current Deviation From Ideal Deviation (See Tables) (Note 2)	$I_{FS}(D)$	V_{REF} 10.000V, $T_A = 25°C$	—	—	±1/2	Step
	$I_{FS}(E)$	$R11 = 19.53k\Omega$, $R12 = 20k\Omega$	—	—	±1/2	
Idle Current (Note 2)	I_I		—	10	—	μA

NOTE:

2. Current specifications relate to differential currents between (+) and (−) output leads. At the selected outputs, equal idle currents are present simultaneously on both current output leads.

DICE CHARACTERISTICS



1. E/D
2. SIGN-BIT
3. BIT 1 (MSB)
4. BIT 2
5. BIT 3
6. BIT 4
7. BIT 5
8. BIT 6
9. BIT 7 (LSB)
10. V_{LC}
11. V_R (+)
12. V_R (−)
13. V−
14. I_{OE} (+)
15. I_{OE} (−)
16. I_{OD} (+)
17. I_{OD} (−)
18. V+

For additional DICE information refer to Section 2.

DIE SIZE 0.123 × 0.085 inch, 10,455 sq. mils (3.124 × 2.159 mm, 6.745 sq. mm)

WAFER TEST LIMITS at $V_S = \pm 15V$, $I_{REF} = 528\mu A$, $T_A = 25°C$, all 4 outputs, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-88N (NOTE 3) LIMIT	UNITS
Resolution		8 chords with 16 steps each	±128	Steps MIN
Dynamic Range		$20 \log (I_{7,15}/I_{0,1})$	72	dB MIN
Monotonicity		Sign-Bit + or −	128	Steps MIN
Chord End-Point Accuracy Chord Zero		Error relative to ideal values at $I_{FS} = 2007.75\mu A$	±1/4	Step MAX
Chord End-Point Accuracy All Chords Other Than Zero		Error relative to ideal values at $I_{FS} = 2007.75\mu A$	±1/2	Step MAX
Encode Decision Level Current		Additional output encode/decode = 1	3/8 5/8	Step MIN Step MAX
Output Voltage Compliance	V_{OC}	Full-scale current change ≤ 1/2 step	−5 +18	Volts MIN Volts MAX

WAFER TEST LIMITS at $V_S = \pm 15V$, $I_{REF} = 528\mu A$, $T_A = 25°C$, all 4 outputs, unless otherwise noted. (Cont'd)

PARAMETER	SYMBOL	CONDITIONS	DAC-88N (NOTE 3) LIMIT	UNITS
Full-Scale Symmetry Error (Note 2)	$I_O+ - I_O-$	Decode or encode pair Input Code 111 1111	±1/8	Step MAX
Zero-Scale Current (Note 2)	I_{ZS}	Measured at selected output 000 0000 input	1/8	Step Max
Disable Current (All bits high) (Note 2)	I_{DIS}	Leakage of output disabled by E/D and SB	100	nA MAX
Step Accuracy Chord Zero		Error relative to ideal values at $I_{FS} = 2007.75\mu A$	±1/4	Step MAX
Step Accuracy All Chords Other Than Zero		Error relative to ideal values at $I_{FS} = 2016\mu A$	±1/2	Step MAX
Output Current Range	I_{FSR}		4.2	mA MIN
Logic Input Levels, Logic "0"	V_{IL}	$V_{LC} = 0V$	0.8	Volts MAX
Logic Input Levels, Logic "1"	V_{IH}	$V_{LC} = 0V$	2	Volts MIN
Logic Input Current	I_{IN}	$V_{IN} = -5V$ to $+18V$	120	μA MAX
Logic Input Swing	V_{IS}	$V- = -15V$	−5 +18	Volts MIN Volts MAX
Reference Bias Current	I_{12}		−12	μA MAX
Power Supply Sensitivity Over Supply Range (Refer to Characteristic Curves)	$PSSI_{FS-}$ $PSSI_{FS-}$	$V+ = 4.5V$ to $18V$ $V- = 10.8V$ to $-18V$	±1/2 ±1/2	Step MAX Step MAX
Power Supply Current	I+ I−	$V_S = \pm 15V$, $I_{FS} = 2.0mA$	5.75 −12.0	mA MAX
	I+ I−	$V_S = \pm 15V$, $I_{FS} = 2.0mA$	5.75 −12.0	mA MAX
Full-Scale Current Deviation From Ideal Deviation (See Tables) (Note 2)	$I_{FS}D$	V_{REF} 10.000V, $T_A = 25°C$	±1/2	Step MAX
	$I_{FS}E$	R11 = 19.53kΩ R12 = 20kΩ	±1/2	Step MAX

Note: Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

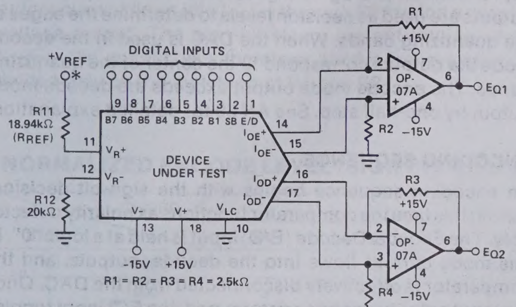
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, and $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-88N TYPICAL	UNITS
Settling Time (Note 1)	t_S	To within ±1/2 step	500	ns
Settling Time in Chord Zero	T_{SCO}	To within ±1/2 step	500	ns
Full-Scale Drift (C_7)	ΔI_{FS}	Full temperature range	±1/16	Step
Reference Input Slew Rate	dI/dt		0.25	mA/μs
Power Dissipation	P_D	V_S +5V, −15V	114	mW
	P_D	$V_S = \pm 15V$	141	mW
Idle Current (Note 2)	I_I		10	μA

NOTES:

1. In a companding DAC the term LSB is not used because the step size within each chord is different. For example, in the first chord around zero (C_0) step size is $0.5\mu A$. While in the last chord near full-scale (C_7) step size is $64\mu A$. Settling time varies for each of the chord bits and step bits and a maximum specification is misleading.
2. Current specifications relate to differential currents between (+) and (−) output leads. At the selected outputs, equal idle currents are present simultaneously on both current output leads.
3. See DAC-88E for typical values.

OUTPUT CURRENT DC TEST CIRCUIT



*V_{REF} IS ADJUSTED BEFORE TESTING EACH DEVICE TO PROVIDE IDEAL FULL-SCALE OUTPUT CURRENT.

LINE SELECTION TABLE

TEST GROUP	ENCODE/ DECODE	SIGN BIT	OUTPUT MEASUREMENT	
1	1	1	$I_{OE}(+)$	$(E_{01}/R1)$
2	1	0	$I_{OE}(-)$	$(E_{01}/R2)$
3	0	1	$I_{OD}(+)$	$(E_{02}/R3)$
4	0	0	$I_{OD}(-)$	$(E_{02}/R4)$

NOTE: Accuracy is specified in the test circuit using the tables below to be within the specified proportion of a step at the maximum value in each chord. Monotonicity is guaranteed for all input codes.

CONDENSED CURRENT OUTPUT TABLES ($I_{REF} = 528\mu A$)

IDEAL DECODE OUTPUT CURRENT IN MICROAMPS AT CHORD ENDPOINTS

STEP	CHORD	0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	0	8.25	24.75	57.75	123.75	255.75	519.75	1047.75
15	1111	7.5	23.25	54.75	117.75	243.75	495.75	999.75	2007.75
STEP SIZE		0.50	1	2	4	8	16	32	64

IDEAL ENCODE OUTPUT CURRENT IN MICROAMPS AT CHORD ENDPOINTS

STEP	CHORD	0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	0.25	8.75	25.75	59.75	127.75	263.75	535.75	1079.75
15	1111	7.75	23.75	55.75	119.75	247.75	503.75	1015.75	2039.75
STEP SIZE		0.50	1	2	4	8	16	32	64

NOTE: These tables may be extended to include all of the encode/ decode currents (ideal with $I_{REF} = 528\mu A$) by multiplying any of the numbers in the normalized tables by 0.25μA.

PARAMETER DEFINITIONS

FULL-SCALE DRIFT

The change in output current over the full operating temperature with V_{REF} = 10.000V, R11 = 18.94kΩ, and R12 = 20kΩ.

ENCODE CURRENT

The difference between $I_{OE}(+)$ and $I_{OD}(+)$ or the difference between $I_{OE}(-)$ and $I_{OD}(-)$ at any code.

FULL-SCALE SYMMETRY ERROR

The difference between $I_{OD}(-)$ and $I_{OD}(+)$ or the difference between $I_{OE}(-)$ and $I_{OE}(+)$ at full-scale output.

OUTPUT VOLTAGE COMPLIANCE

The maximum output voltage swing at any current level which causes <1/2 step change in output current.

IDEAL OUTPUT CURRENT

The difference between the (+) and (−) currents (encode or decode) at any code.

CHORDS

Groups of linearly-related steps in the transfer function. Also known as segments.

CHORD ENDPOINTS

The maximum code in each chord; used to specify accuracy.

STEPS

Increments in each chord which divides the chord into 16 equal levels.

OUTPUT LEVEL NOTATION

Each output current level may be designated by the code $I_{C,S}$ where C = chord number and S = step number. For example, $I_{0,0}$ = zero-scale current: $I_{0,1}$ = first step from zero; $I_{0,15}$ = endpoint of first chord (C_0); $I_{7,15}$ = full-scale current.

DYNAMIC RANGE

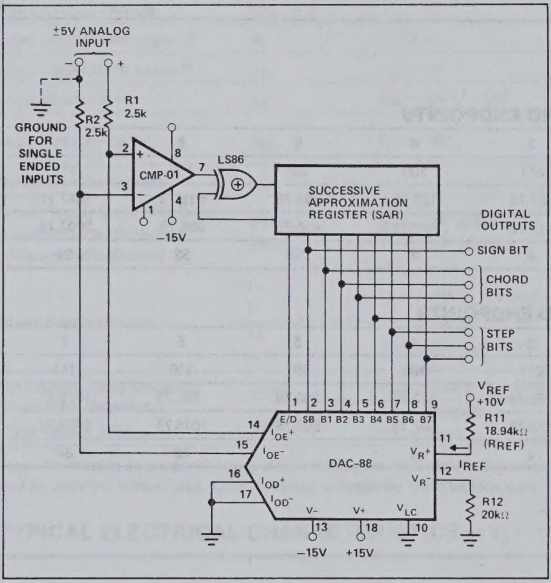
Ratio of full scale current to step size in chord zero, expressed in dB.

BASIC ENCODE OPERATION (COMPRESSING A/D CONVERSION)

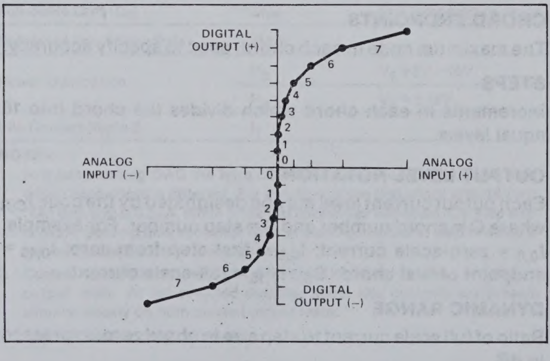
ENCODE DECISION LEVELS

Compressing A/D conversion with the DAC-88 requires a comparator, an EXCLUSIVE-OR gate, and a successive approximation register — the usual elements in any sign magnitude A/D converter. However, a compressing A/D has one significant difference. In a conventional (linear converter), the step size is a constant percentage of full-scale. In a compressing A/D converter, the step size increases as the output changes from zero-scale to full-scale.

BASIC ENCODE CONNECTIONS



ENCODE TRANSFER CHARACTERISTICS (A/D CONVERSION)



When the DAC is used in the feedback loop of a successive approximation analog to digital converter (ADC) the DAC outputs are used as decision levels to determine the edges of the quantizing bands. When the DAC is used in the decode mode the outputs correspond to the center of the quantizing bands. The encode mode output exceeds the decode mode output by one-half step. See AN 39 for detailed explanation.

ENCODING SEQUENCE

An encoding sequence begins with the sign-bit decision. During this time the comparator functions as polarity detector only. The Encode/Decode (E/D) input is held at a logic "0". In this mode current flows into the decode outputs, and the comparator is effectively disconnected from the DAC. Once the input polarity has been determined, the E/D input toggles to a logic "1" allowing current to flow into $I_{OE}(+)$ or $I_{OE}(-)$.

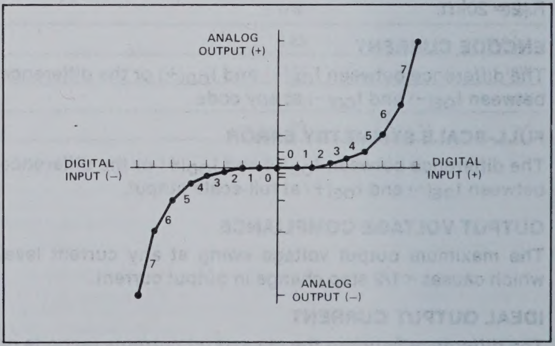
For positive inputs, current flows into $I_{OE}(+)$ through R1, and the comparator's output is entered as the answer for each successive decision. For negative inputs, current flows into $I_{OE}(-)$ through R2 developing a negative voltage which is compared with the analog input. An EXCLUSIVE-OR gate inverts the comparator's output during negative trials to maintain the proper logic coding, all ones for full-scale and all zeros for zero-scale.

The bits are converted with a successive removal technique, starting with a decision at the code 011 1111 and turning off bits sequentially until all decisions have been made.

BASIC DECODE OPERATION (EXPANDING D/A CONVERSION)

D/A conversion with the DAC-88 is implemented by using an operational amplifier connected to the decode outputs. The decode mode of operation is selected by applying a logic "0" to the Encode/Decode input. This mode enables the $I_{OD}(+)$ or $I_{OD}(-)$ to be selected by the sign-bit input. When the sign-bit input is high, a logic "1", all of the output current flows into

DECODE TRANSFER CHARACTERISTIC (D/A CONVERSION)



$I_{OD}(+)$ forcing a positive voltage at the operational amplifier's output. When the sign-bit input is low, logic "0", all of the output current flows into $I_{OD}(-)$ through R2 forcing a negative voltage output. The sign-bit steers current into $I_{OD}(+)$ or $I_{OD}(-)$, the output will therefore always be symmetrical, limited only by the matching of R1 and R2.

NORMALIZED TABLES

The encode and decode tables are used to calculate ideal output current at any point. For example, in decode mode at $I_{3,7}$ (011 0111) find 343. 343/8031 × I_{FS} = 85.75μA (I_{FS} = 2007.75μA). Alternatively, use the condensed current tables and add up the number of steps.

NORMALIZED ENCODE LEVEL (SIGN BIT EXCLUDED) $(I_{C,S} = 2[2^C (S+17) - 16.5]$

C = chord no. (0 through 7)
S = step no. (0 through 15)

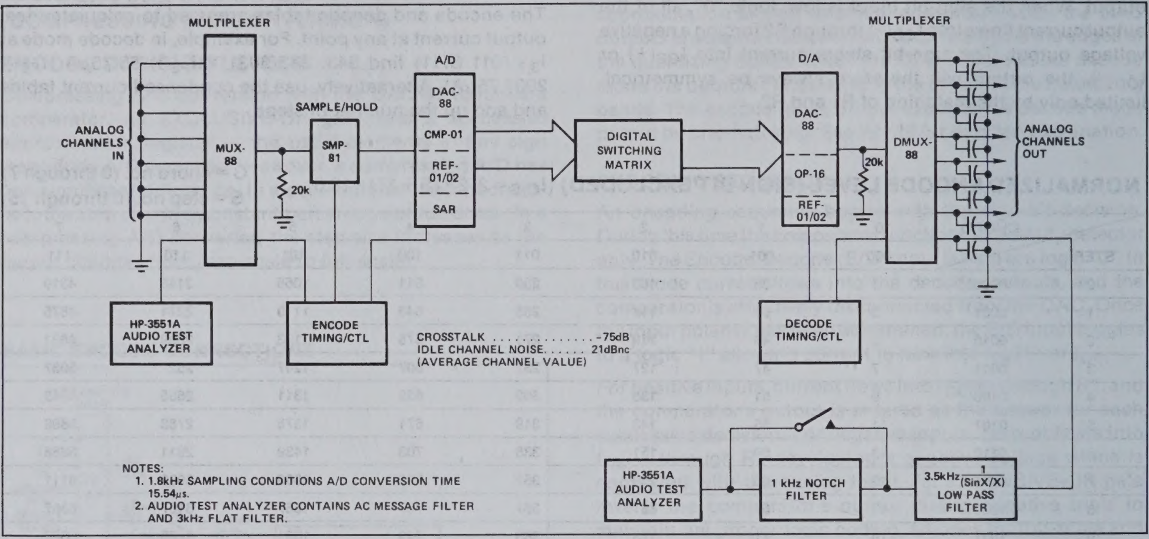
	CHORD	0	1	2	3	4	5	6	7
STEP		000	001	010	011	100	101	110	111
0	0000	1	35	103	239	511	1055	2143	4319
1	0001	3	39	111	255	543	1119	2271	4575
2	0010	5	43	119	271	575	1183	2399	4831
3	0011	7	47	127	287	607	1247	2527	5087
4	0100	9	51	135	303	639	1311	2655	5343
5	0101	11	55	143	319	671	1375	2783	5599
6	0110	13	59	151	335	703	1439	2911	5855
7	0111	15	63	159	351	735	1503	3039	6111
8	1000	17	67	167	367	767	1567	3167	6367
9	1001	19	71	175	383	799	1631	3295	6623
10	1010	21	75	183	399	831	1695	3423	6879
11	1011	23	79	191	415	863	1759	3551	7135
12	1100	25	83	199	431	895	1823	3679	7391
13	1101	27	87	207	447	927	1887	3807	7647
14	1110	29	91	215	463	959	1951	3935	7903
15	1111	31	95	223	479	991	2015	4063	8159
STEP SIZE		2	4	8	16	32	64	128	256

NORMALIZED DECODE OUTPUT (SIGN BIT EXCLUDED) $(I_{C,S} = 2[2^C (S+16.5) - 16.5]$

C = chord no. (0 through 7)
S = step no. (0 through 15)

	CHORD	0	1	2	3	4	5	6	7
STEP		000	001	010	011	100	101	110	111
0	0000	0	33	99	231	495	1023	2079	4291
1	0001	2	37	107	247	527	1087	2207	4447
2	0010	4	41	115	263	559	1151	2335	4703
3	0011	6	45	123	279	591	1215	2463	4959
4	0100	8	49	131	295	623	1279	2591	5215
5	0101	10	53	139	311	655	1343	2719	5471
6	0110	12	57	147	327	687	1407	2847	5727
7	0111	14	61	155	343	719	1471	2975	5983
8	1000	16	65	163	359	751	1535	3103	6239
9	1001	18	69	171	375	783	1599	3231	6495
10	1010	20	73	179	391	815	1663	3359	6751
11	1011	22	77	187	407	847	1727	3487	7007
12	1100	24	81	195	423	879	1791	3615	7263
13	1101	26	85	203	439	911	1855	3743	7519
14	1110	28	89	212	455	943	1919	3871	7775
15	1111	30	93	219	471	975	1983	3999	8031
STEP SIZE		2	4	8	16	32	64	128	256

SYSTEM TEST CIRCUIT


MULTIPLEXER
A/D
SAMPLE/HOLD
ANALOG
CHANNELS
IN
MUX-
88
20k
SMP-
81
DAC-
88
CMP-01
REF-
01/02
SAR
DIGITAL
SWITCHING
MATRIX
D/A
DAC-
88
OP-16
REF-
01/02
20k
MULTIPLEXER
DMUX-
88
ANALOG
CHANNELS
OUT
HP-3551A
AUDIO TEST
ANALYZER
ENCODE
TIMING/CTL
DECODE
TIMING/CTL
HP-3551A
AUDIO TEST
ANALYZER
1 kHz NOTCH
FILTER
3.5kHz $\frac{1}{(\mathrm{SinX/X})}$
LOW PASS
FILTER

CROSSTALK . . . . -75dB
IDLE CHANNEL NOISE. 21dBnc
(AVERAGE CHANNEL VALUE)

NOTES:
1. 1.8kHz SAMPLING CONDITIONS A/D CONVERSION TIME 15.54μs.
2. AUDIO TEST ANALYZER CONTAINS AC MESSAGE FILTER AND 3kHz FLAT FILTER.

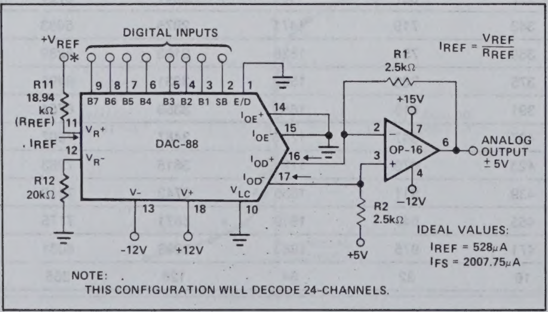
BASIC REFERENCE CONSIDERATIONS

Full-scale output current is ideally 2007.75μA when the reference current is 528μA in the decode mode. In the encode mode I_{FS} = 2039.75μA due to the additional 1/2 step (32μA). A percentage change in I_{REF} will produce the same percentage change in output current.

DECODE OUTPUT VOLTAGE

	E/D	SB	B1	B2	B3	B4	B5	B6	B7	E_0
POS FULL-SCALE	0	1	1	1	1	1	1	1	1	5.019V
(+) ZERO-SCALE +1 STEP	0	1	0	0	0	0	0	0	1	0.0012V
(+) ZERO-SCALE	0	1	0	0	0	0	0	0	0	0V
(−) ZERO-SCALE	0	0	0	0	0	0	0	0	0	0V
(−) ZERO-SCALE +1 STEP	0	0	0	0	0	0	0	0	1	−0.0012V
NEG FULL-SCALE	0	0	1	1	1	1	1	1	1	−5.019V

BASIC DECODE CONNECTIONS


DIGITAL INPUTS
$+V_{REF}$
*
R11
18.94
kΩ
(R_{REF})
I_{REF}
R12
20kΩ
9
8
7
6
5
4
3
2
1
B7 B6 B5 B4 B3 B2 B1 SB E/D
11
V_{R^+}
12
V_{R^-}
DAC-88
I_{OE^+}
I_{OE^-}
I_{OD^+}
I_{OD^-}
14
15
16
17
V-
V+
V_{LC}
13
18
10
-12V
+12V
R1
2.5kΩ
+15V
2
3
7
6
4
OP-16
−12V
R2
2.5kΩ
+5V
ANALOG
OUTPUT
± 5V
$I_{REF} = \frac{V_{REF}}{R_{REF}}$
IDEAL VALUES:
I_{REF} = 528μA
I_{FS} = 2007.75μA

NOTE:
THIS CONFIGURATION WILL DECODE 24-CHANNELS.

The large step size at full-scale allows the use of inexpensive references in many applications. In some applications V_{REF} may even be the positive power supply. For example, with V+ = 15V, R_{REF} = 15V/528μA or 28.4kΩ. When using a power supply as a reference, R11 becomes two resistors, R11A and R11B, and the junction bypassed to ground with a 0.1μf monolithic capacitor.

REFERENCE AMPLIFIER OPERATION

The DAC-88 is a multiplying D/A converter. The output current is the product of the normalized digital input and the input reference current. The reference current may be fixed or may vary from nearly zero to +1.0mA. The full-scale output current is a linear function of the reference current and is given for all four outputs in the figures above.

REFERENCE RECOMMENDATIONS

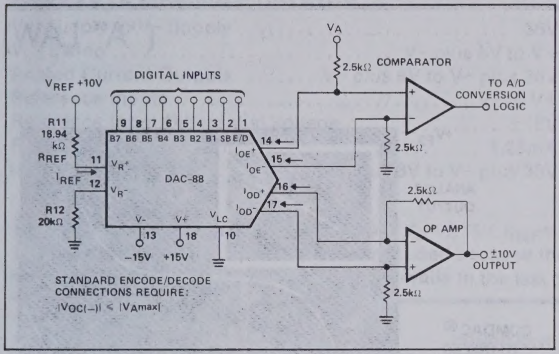
For most applications a +10.0V reference, such as the PMI REF-01, is recommended for optimum full-scale temperature performance.

POWER SUPPLIES

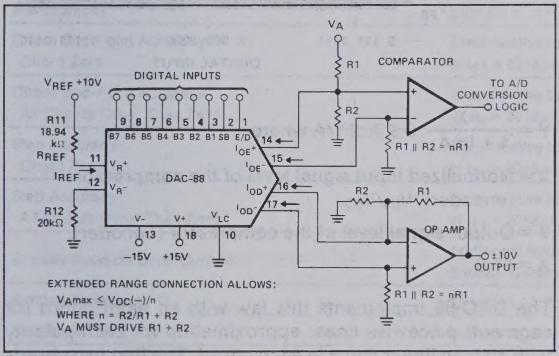
Power supply current drain is relatively independent of voltage and temperature and completely independent of the logic input states.

When operating with V− between −15V and −11V, output negative voltage compliance, $V_{OC}(-)$, reference input amplifier common-mode voltage range, and logic input negative voltage range are reduced by an amount equivalent to the difference between −15V and the V− supply. Operation with V+ between +5V and +15V affects V_{LC} and the reference amplifier common-mode positive voltage range in the same manner.

STANDARD OUTPUT CONNECTIONS


VA
2.5kΩ
COMPARATOR
TO A/D CONVERSION LOGIC
DIGITAL INPUTS
VREF +10V
9 8 7 6 5 4 3 2 1
B7 B6 B5 B4 B3 B2 B1 SB E/D
R11 18.94 kΩ
RREF
IREF
11
12
VR+
VR−
DAC-88
IOE+
IOE−
IOD+
IOD−
14
15
16
17
2.5kΩ
2.5kΩ
OP AMP
±10V OUTPUT
2.5kΩ
R12 20kΩ
V−
V+
VLC
13
18
10
−15V
+15V
STANDARD ENCODE/DECODE CONNECTIONS REQUIRE:
|VOC(−)| ≤ |VAmax|

COMPLIANCE EXTENSION CONNECTIONS


VA
R1
COMPARATOR
R2
TO A/D CONVERSION LOGIC
DIGITAL INPUTS
VREF +10V
9 8 7 6 5 4 3 2 1
B7 B6 B5 B4 B3 B2 B1 SB E/D
R11 18.94 kΩ
RREF
IREF
11
12
VR+
VR−
DAC-88
IOE+
IOE−
IOD+
IOD−
14
15
16
17
R1 ∥ R2 = nR1
R2
R1
OP AMP
±10V OUTPUT
R1 ∥ R2 = nR1
R12 20kΩ
V−
V+
VLC
13
18
10
−15V
+15V
EXTENDED RANGE CONNECTION ALLOWS:
VAmax ≤ VOC(−)/n
WHERE n = R2/R1 + R2
VA MUST DRIVE R1 + R2

OUTPUT VOLTAGE COMPLIANCE

The DAC-88 has true current outputs with wide voltage compliance that enables single ended and balanced load driving capability. Positive voltage compliance is +18V and negative voltage compliance is −5.0V with $I_{REF} = 528\mu A$ and $V = -15V$. Negative voltage compliance $V_{OC}(-)$ for other values of I_{REF} and V− may be obtained from the table, or calculated as follows:

$$V_{OC}(-)\ \text{min} = (V-) + (2\ I_{REF} \times 1.6k\Omega) + 8.4V$$

Output voltage compliance can be extended in both encode and decode modes using the connections shown in the compliance extension diagram.

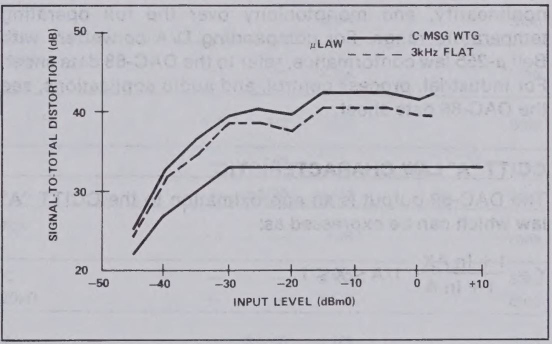
NEGATIVE OUTPUT VOLTAGE COMPLIANCE $V_{OC}(-)$

V−	I_{FS} 1.0mA	2.0mA	4.0mA
−12V	−2.8V	−2.0V	−0.4V
−15V	−5.8V	−5.0V	−3.4V
−18V	−8.8V	−8.0V	−6.4V

MINIMUM NEGATIVE COMPLIANCE

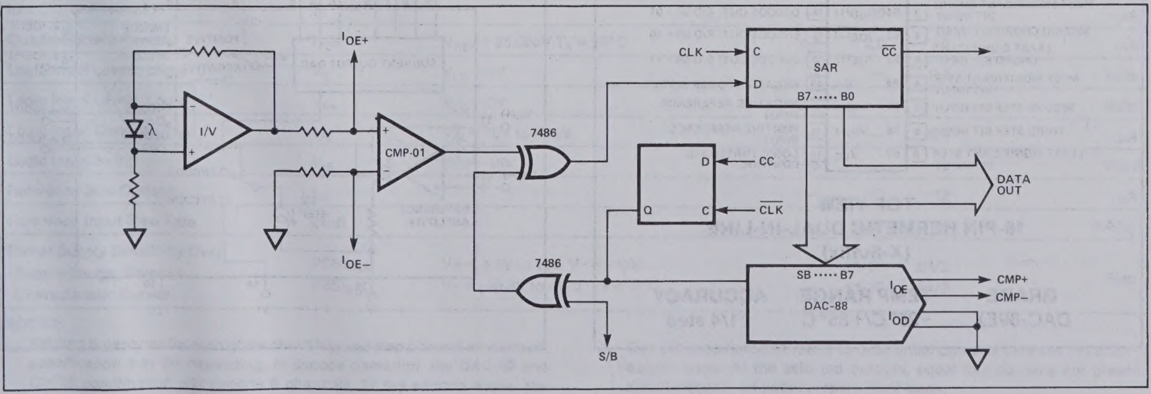
$$V_{OC}(-)\ \text{MIN} = (V-) + (2\ I_{REF}\ 1.6k\Omega) + 8.4V$$

SIGNAL TO QUANTIZING DISTORTION vs INPUT LEVEL



APPLICATIONS

PHOTODIODE LINEARIZING CIRCUIT


λ
I/V
IOE+
IOE−
CMP-01
7486
7486
CLK
C
D
SAR
CC
B7 ····· B0
D
CC
Q
C
CLK
DATA OUT
SB ····· B7
DAC-88
IOE
IOD
CMP+
CMP−
S/B

DAC-89

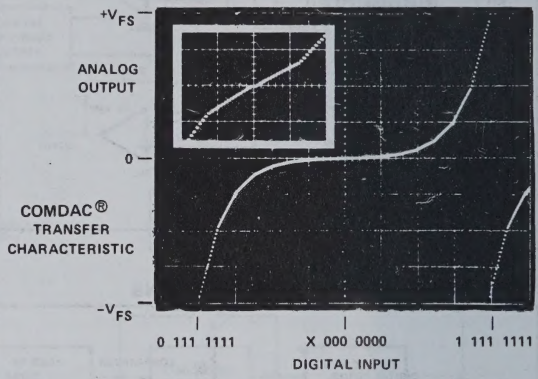
COMDAC®

COMPANDING D/A CONVERTER

("A" LAW)

FEATURES

- **11-Bit Accuracy and Resolution Around Zero**
- **Sign Plus 66dB Dynamic Range**
- **True Current Outputs: −5V to +18V Compliance**
- **Tight Full-Scale Tolerance Eliminates Calibration**
- **Low Full-Scale Drift Over Temperature**
- **Low Power Consumption and Low Cost**
- **Ideal for PCM and 8-Bit μP Applications**
- **Outputs Multiplexed for Time Shared Applications**
- **Fully Specified Dice Available**



GENERAL DESCRIPTION

The DAC-89 monolithic COMDAC® converter provides the complete decode function for "A" Law PCM CODECs. The DAC-89 may be configured in an encoder, decoder, or time-shared between encoding and decoding.

Specifying chord end-point values assures accuracy chord nonlinearity, and monotonicity over the full operating temperature range. For companding D/A converters with Bell μ-255 law conformance, refer to the DAC-88 data sheet. For industrial, process control, and audio applications, see the DAC-86 data sheet.

CCITT "A" LAW CHARACTERISTIC

The DAC-89 output is an approximation to the CCITT "A" law which can be expressed as:

$$Y = \frac{1 + \ln AX}{1 + \ln A} \quad 1/A \leq X \leq 1$$

$$Y = \frac{AX}{1 + \ln A} \quad 0 \leq X \leq 1/A \text{ where:}$$

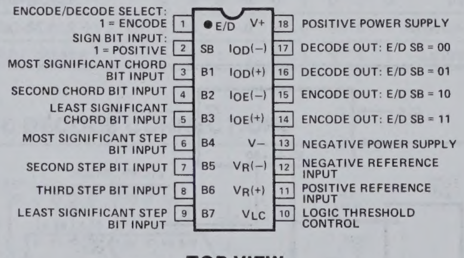
X = Normalized input signal level of the compressor (encoder), V_{IN}/V_{FS}.

Y = Output signal level of the compressor (encoder).

A = 87.6

The DAC-89 implements this law with an eight chord (or segment) piecewise linear approximation for each polarity with sixteen linear steps in each chord. The first two chords are co-linear and of equal step size, and may be considered as one chord of 32 steps. Step sizes of the remaining six chords are binarily related to the first chord.

PIN CONNECTIONS & ORDERING INFORMATION

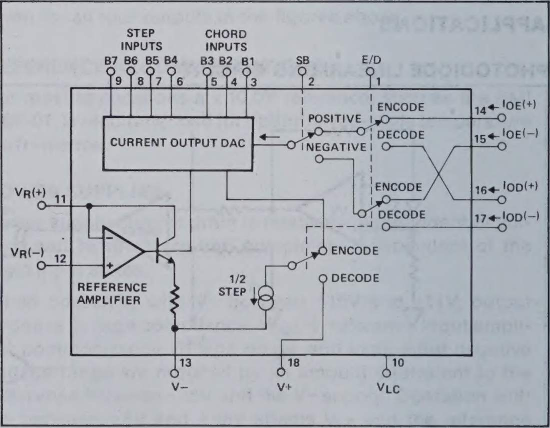


ENCODE/DECODE SELECT: 1 = ENCODE
SIGN BIT INPUT: 1 = POSITIVE
MOST SIGNIFICANT CHORD BIT INPUT
SECOND CHORD BIT INPUT
LEAST SIGNIFICANT CHORD BIT INPUT
MOST SIGNIFICANT STEP BIT INPUT
SECOND STEP BIT INPUT
THIRD STEP BIT INPUT
LEAST SIGNIFICANT STEP BIT INPUT
1 E/D
2 SB
3 B1
4 B2
5 B3
6 B4
7 B5
8 B6
9 B7
18 V+
17 IOD(−)
16 IOD(+)
15 IOE(−)
14 IOE(+)
13 V−
12 VR(−)
11 VR(+)
10 VLC
POSITIVE POWER SUPPLY
DECODE OUT: E/D SB = 00
DECODE OUT: E/D SB = 01
ENCODE OUT: E/D SB = 10
ENCODE OUT: E/D SB = 11
NEGATIVE POWER SUPPLY
NEGATIVE REFERENCE INPUT
POSITIVE REFERENCE INPUT
LOGIC THRESHOLD CONTROL

TOP VIEW
18-PIN HERMETIC DUAL-IN-LINE
(X-Suffix)

GRADE	TEMP RANGE	ACCURACY
DAC-89EX	−25°C/+85°C	±1/4 step

EQUIVALENT CIRCUIT



STEP INPUTS
CHORD INPUTS
B7 B6 B5 B4
B3 B2 B1
9 8 7 6
5 4 3
SB
2
E/D
1
CURRENT OUTPUT DAC
POSITIVE
NEGATIVE
ENCODE
DECODE
ENCODE
DECODE
14 IOE(+)
15 IOE(−)
16 IOD(+)
17 IOD(−)
VR(+) 11
VR(−) 12
REFERENCE AMPLIFIER
1/2 STEP
ENCODE
DECODE
13 V−
18 V+
10 VLC

ABSOLUTE MAXIMUM RATINGS

V+ Supply to V− Supply	36V
V_{LC} Swing	V− plus 8V to V+
Analog Current Outputs	V− plus 8V to V− plus 36V
Reference Inputs	V− to V+
Reference Input Differential Voltage	±18V
Reference Input Current	1.25mA
Logic Inputs	V− plus 8V to V− plus 36V
Operating Temperature Range	−25° C to +85° C
Storage Temperature Range	−65° C to +150° C
Power Dissipation	500mW
Derate Above 100° C	10mW/° C
Lead Temperature (Soldering, 60 sec)	300° C

NOTE: Absolute ratings apply to both DICE and packaged parts unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $I_{REF} = 512\mu A$, $-25° C \leq T_A \leq +85° C$, all 4 outputs, unless otherwise noted. In a companding DAC the term LSB is not used because the step size within each chord is different. For example, in the first chord around zero (C_0) step size is 1.0μA, while in the last chord near full-scale (C_7) step size is 64μA.

			DAC-89E			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Resolution		8 chords with 16 steps each	±128	±128	±128	Steps
Dynamic Range		20 log ($I_{7,15}/I_{0,0}$)	66	—	66	dB
Monotonicity		Sign Bit + or −	128	—	—	Steps
Chord End-Point Accuracy Chord Zero		Error relative to ideal values at $I_{FS} = 2016\mu A$	—	—	±1/4	Step
Chord End-Point Accuracy All Chords Other Than Zero		Error relative to ideal values at $I_{FS} = 2016\mu A$	—	—	±1/2	Step
Step Accuracy Chord Zero		Error relative to ideal values at $I_{FS} = 2016\mu A$	—	—	±1/4	Step
Step Accuracy All Chords Other Than Zero		Error relative to ideal values at $I_{FS} = 2016\mu A$	—	—	±1/2	Step
Encode Decision Level Current		Additional output Encode/Decode = 1	1/4	1/2	3/4	Step
Settling Time (Note 1)	t_S	To within ±1/2 step	—	500	—	ns
Full-Scale Drift (Note 3)	ΔI_{FS}	Full temperature range	—	±1/20	±1/4	Step
Output Voltage Compliance	V_{OC}	Full-scale current change ≤ 1/2 step	−5	—	+18	Volts
Full-Scale Current Deviation from Ideal (See Tables) (Note 2)	$I_{FS}(D)$ $I_{FS}(E)$	V_{REF} 10.000V $T_A = 25° C$ R11 = 19.53kΩ, R12 = 20kΩ	— —	— —	±1/2 ±1/2	Step Step
Full-Scale Symmetry Error (Note 2)	$I_O(+) - I_O(-)$	Decode or Encode pair	—	±1/40	±1/8	Step
Zero-Scale Current (Note 2)	I_{ZS}	Measured at selected output with 000 0000 input	1/4	1/2	3/4	Step
Disable Current (Note 2)	I_{DIS}	Disabled by E/D and SB	—	5.0	100	nA
Idle Current (Note 2)	I_I		—	10	—	μA
Output Current Range	I_{FSR}	$V_{REF} = 25.000V$ $T_A = 25° C$	4.2	2.0	0	mA
Logic Input Levels, Logic "0"	V_{IL}	$V_{LC} = 0V$	—	—	0.8	Volts
Logic Input Levels, Logic "1"	V_{IH}	$V_{LC} = 0V$	2.0	—	—	Volts
Logic Input Current	I_{IN}	$V_{IN} = -5V$ to $+18V$	—	—	120	μA
Logic Input Swing	V_{IS}	$V- = -15V$	−5	—	+18	Volts
Reference Bias Current	I_{12}		—	−3	−12	μA
Reference Input Slew Rate	dI/dt		—	0.25	—	mA/μs
Power Supply Sensitivity Over Supply Range (Refer to Characteristic Curves)	$PSSI_{FS+}$ $PSSI_{FS-}$	$V+ = 4.5V$ to $18V$, $V- = -15V$ $V- = -10.8V$ to $-18V$, $V+ = 15V$	— —	±1/20 ±1/10	±1/2 ±1/2	Step

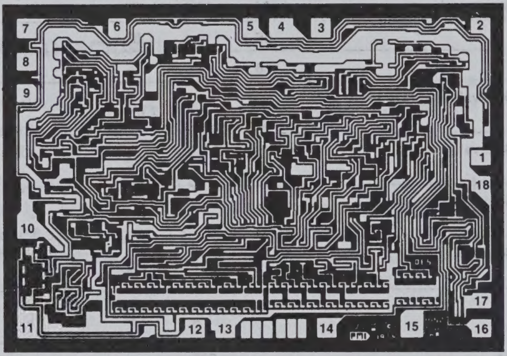
NOTES:

1. Settling time varies for each of the chord bits and step bits and a maximum specification may be misleading. In decode operation, the DAC-89 and OP-16 combination will decode 8 channels. In the encode mode, the DAC-89 and CMP-01 combination will encode 8 channels. Both encode and decode statements assume a 3.9μs channel time.
2. Current specifications relate to differential currents between (+) and (−) output leads. At the selected outputs, equal idle currents are present simultaneously on both current output leads.
3. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $I_{REF} = 512\mu A$, $-25°C \leq T_A \leq +85°C$, all 4 outputs, unless otherwise noted. In a companding DAC the term LSB is not used because the step size within each chord is different. For example, in the first chord around zero (C_0) step size is $1.0\mu A$, while in the last chord near full-scale (C_7) step size is $64\mu A$. (Continued)

PARAMETER	SYMBOL	CONDITIONS	DAC-89E MIN	TYP	MAX	UNITS
Power Supply Current	I+	$V_S = +5V, -15V, I_{FS} = 2.0mA$	—	2.7	5.5	mA
	I−	$V_S = +5V, -15V, I_{FS} = 2.0mA$	—	6.7	−12	
	I+	$V_S = \pm 15V, I_{FS} = 2.0mA$	—	2.7	5.5	
	I−	$V_S = \pm 15V, I_{FS} = 2.0mA$	—	−6.7	−12	
Power Dissipation	P_d	$V_S = +5V, -15V, I_{FS} = 2.0mA$	—	114	207	mW
		$V_S = \pm 15V, I_{FS} = 2.0mA$	—	141	262	

DICE CHARACTERISTICS



1. E/D
2. SIGN-BIT
3. BIT 1 (MSB)
4. BIT 2
5. BIT 3
6. BIT 4
7. BIT 5
8. BIT 6
9. BIT 7 (LSB)
10. V_{LC}
11. V_R (+)
12. V_R (−)
13. V−
14. I_{OE} (+)
15. I_{OE} (−)
16. I_{OD} (+)
17. I_{OD} (−)
18. V+

For additional DICE information refer to Section 2.

DIE SIZE 0.123 × 0.085 inch, 10.455 sq. mils
(3.124 × 2.159 mm, 6.745 sq. mm)

WAFER TEST LIMITS at $V_S = \pm 15V$, $I_{REF} = 528\mu A$, $T_A = 25°C$, all 4 outputs, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-89N (NOTE 3) LIMIT	UNITS
Resolution		8 chords with 16 steps each	±128	Steps MIN
Dynamic Range		20 log $(I_{7,15}/I_{0,1})$	66	dB MIN
Monotonicity		Sign-Bit + or −	128	Steps MIN
Chord End-point Accuracy Chord Zero		Error relative to ideal values at $I_{FS} = 2007.75\mu A$	±1/4	Step MAX
Chord End-point Accuracy All Chords Other Than Zero		Error relative to ideal values at $I_{FS} = 2007.75\mu A$	±1/2	Step MAX
Encode Decision Level Current		Additional output encode/decode = 1	1/4 3/4	Step MIN Step MAX
Output Voltage Compliance	V_{OC}	Full-scale current change ≤ 1/2 step	−5 +18	Volts MIN Volts MAX
Full-Scale Symmetry Error (Note 2)	$I_O+ - I_O-$	Decode or encode pair Input Code 111 1111	±1/8	Step MAX
Zero-Scale Current (Note 2)	I_{ZS}	Measured at selected output 000 0000 input	1/4	Step Max
Disable Current (All bits high) (Note 2)	I_{DIS}	Leakage of output disabled by E/D and SB	100	nA MAX

WAFER TEST LIMITS at $V_S = \pm15V$, $I_{REF} = 528\mu A$, $T_A = 25°C$, all 4 outputs, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	DAC-89N (NOTE 3) LIMIT	UNITS
Step Accuracy Chord Zero		Error relative to ideal values at $I_{FS} = 2007.75\mu A$	±1/4	Step MAX
Step Accuracy All Chords Other Than Zero		Error relative to ideal values at $I_{FS} = 2016\mu A$	±1/2	Step MAX
Output Current Range	I_{FSR}	$V_{REF} = 25.000V$, $T_A = 25°C$	4.2	mA MIN
Logic Input Levels, Logic "0"	V_{IL}	$V_{LC} = 0V$	0.8	Volts MAX
Logic Input Levels, Logic "1"	V_{IH}	$V_{LC} = 0V$	2	Volts MIN
Logic Input Current	I_{IN}	$V_{IN} = -5V$ to $+18V$	120	μA MAX
Logic Input Swing	V_{IS}	$V- = -15V$	−5 +18	Volts MIN Volts MAX
Reference Bias Current	I_{12}		−12	μA MAX
Power Supply Sensitivity Over Supply Range (Refer to Characteristic Curves)	$PSSI_{FS-}$ $PSSI_{FS-}$	$V+ = 4.5V$ to $18V$ $V- = 10.8V$ to $-18V$	±1/2 ±1/2	Step MAX Step MAX
Power Supply Current	I+ I−	$V_S = \pm15V$, $I_{FS} = 2.0mA$	5.5 −12.0	mA MAX
	I+ I−	$V_S = \pm15V$, $I_{FS} = 2.0mA$	5.75 −12.0	mA MAX
Full-Scale Current Deviation From Ideal Deviation (See Tables) (Note 2)	$I_{FS}D$	V_{REF} 10.000V, $T_A = 25°C$	±1/2	Step MAX
	$I_{FS}E$	R11 = 19.53kΩ R12 = 20kΩ	±1/2	Step MAX

Note: Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

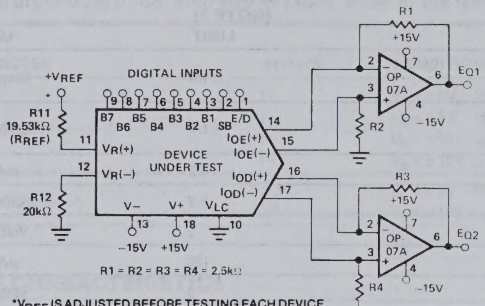
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, and $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-89N TYPICAL	UNITS
Settling Time (Note 1)	t_S	To within ±1/2 step	500	ns
Settling Time in Chord Zero	T_{SCO}	To within ±1/2 step	500	ns
Full-Scale Drift (C_7)	ΔI_{FS}	Full temperature range	±1/20	Step
Reference Input Slew Rate	dI/dt		0.25	mA/μs
Power Dissipation	P_D	V_S +5V, −15V	114	mW
	P_D	$V_S = \pm15V$	141	mW
Idle Current (Note 2)	I_I		10	μA

NOTES:

1. In a companding DAC the term LSB is not used because the step size within each chord is different. For example, in the first chord around zero (C_0) step size is 0.5μA. While in the last chord near full-scale (C_7) step size is 64μA. Settling time varies for each of the chord bits and step bits and a maximum specification is misleading.
2. Current specifications relate to differential currents between (+) and (−) output leads. At the selected outputs, equal idle currents are present simultaneously on both current output leads.
3. See DAC-89E for typical values.

OUTPUT CURRENT DC TEST CIRCUIT



*V_{REF} IS ADJUSTED BEFORE TESTING EACH DEVICE TO PROVIDE IDEAL FULL-SCALE OUTPUT CURRENT.

LINE SELECTION TABLE

TEST GROUP	ENCODE/ DECODE	SIGN BIT	OUTPUT MEASUREMENT	
1	1	1	$I_{OE}(+)$	$(E_{01}/R1)$
2	1	0	$I_{OE}(-)$	$(E_{01}/R2)$
3	0	1	$I_{OD}(+)$	$(E_{02}/R3)$
4	0	0	$I_{OD}(-)$	$(E_{02}/R4)$

NOTE: Accuracy is specified in the test circuit using the tables below to be within the specified proportion of a step at the maximum value in each chord. Monotonicity is guaranteed for all input codes.

CONDENSED CURRENT OUTPUT TABLES

IDEAL DECODE OUTPUT CURRENT IN MICROAMPS AT CHORD ENDPOINTS

	CHORD	0	1	2	3	4	5	6	7
STEP		000	001	010	011	100	101	110	111
0	0000	0.5	16.5	33	66	132	264	528	1056
15	1111	15.5	31.5	63	126	252	504	1008	2016
STEP SIZE		1	1	2	4	8	16	32	64

IDEAL ENCODE OUTPUT CURRENT IN MICROAMPS AT CHORD ENDPOINTS

	CHORD	0	1	2	3	4	5	6	7
STEP		000	001	010	011	100	101	110	111
0	0000	1	17	34	68	136	272	544	1088
15	1111	16	32	64	128	256	512	1024	2048
STEP SIZE		1	1	2	4	8	16	32	64

These tables may be extended to include all of the encode/decode currents (ideal with $I_{REF} = 512\mu A$) by multiplying any of the numbers in the normalized tables by $0.5\mu A$.

PARAMETER DEFINITIONS

STEP NONLINEARITY

Step size deviation from ideal within a chord.

ENCODE CURRENT

The difference between $I_{OE}(+)$ and $I_{OD}(+)$ or the difference between $I_{OE}(-)$ and $I_{OD}(-)$ at any code.

FULL-SCALE DRIFT

The change in output current over the full operating temperature with $V_{REF} = 10.000V$, $R11 = 19.53k\Omega$, and $R12 = 20k\Omega$.

FULL-SCALE SYMMETRY ERROR

The difference between $I_{OD}(-)$ and $I_{OD}(+)$ or the difference between $I_{OE}(-)$ and $I_{OE}(+)$ at full-scale output.

IDEAL OUTPUT CURRENT

The difference between the (+) and (−) currents (encode or decode) at any code.

OUTPUT VOLTAGE COMPLIANCE

The maximum output voltage swing at any current level which causes <1/2 step change in output current.

CHORDS

Groups of linearly-related steps in the transfer function. Also known as segments.

CHORD ENDPOINTS

The maximum code in each chord; used to specify accuracy.

STEPS

Increments in each chord which divides the chord into 16 equal levels.

OUTPUT LEVEL NOTATION

Each output current level may be designated by the code $I_{C,S}$ where C = chord number and S = step number. For example, $I_{0,0}$ = zero-scale current: $I_{0,1}$ = first step from zero; $I_{0,15}$ = endpoint of first chord (C_0); $I_{7,15}$ = full-scale current.

DYNAMIC RANGE

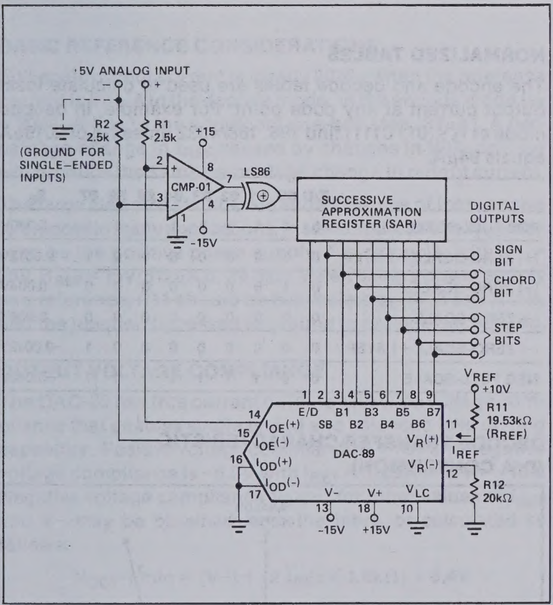
Ratio of full-scale current to step size in chord zero expressed in dB.

BASIC ENCODE OPERATION (COMPRESSING A/D CONVERSION)

ENCODING SEQUENCE

An encoding sequence begins with the sign-bit decision. During this time the comparator functions as a polarity detector only. The Encode/Decode (E/D) input is held at logic "0". In this mode current flows into the decode outputs, and the comparator is effectively disconnected from the DAC. Once the input polarity has been determined, the E/D input toggles "1" allowing current to flow into $I_{OE}(+)$ or $I_{OE}(-)$.

BASIC DECODE CONNECTIONS


±5V ANALOG INPUT
–
+
R2
2.5k
R1
2.5k
+15
(GROUND FOR
SINGLE-ENDED
INPUTS)
2
8
7
3
CMP-01
4
1
-15V
LS86
SUCCESSIVE
APPROXIMATION
REGISTER (SAR)
DIGITAL
OUTPUTS
SIGN
BIT
CHORD
BIT
STEP
BITS
VREF
+10V
R11
19.53kΩ
(RREF)
1 2 3 4 5 6 7 8 9
E/D B1 B3 B5 B7
SB B2 B4 B6
14
IOE(+)
15
IOE(-)
16
IOD(+)
17
IOD(-)
DAC-89
11
VR(+)
IREF
VR(-)
12
R12
20kΩ
V- V+ VLC
13 18 10
-15V +15V

For positive inputs, current flows into $I_{OE}(+)$ through R1, and the comparator's output is entered as the answer for each successive decision. For negative inputs, current flows into $I_{OE}(-)$ through R2 developing a negative voltage which is compared with the analog input. An EXCLUSIVE-OR gate inverts the comparator's output during negative trials to maintain the proper logic coding, all ones for full-scale and all zeros for zero-scale.

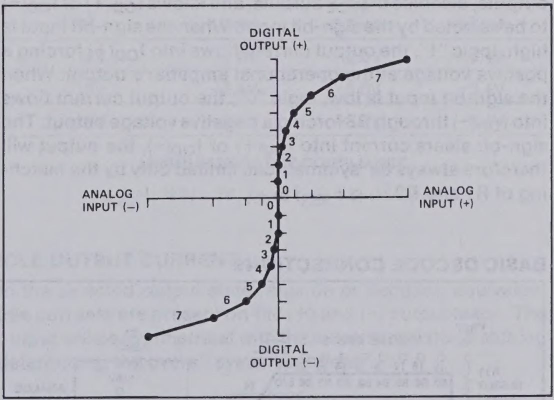
The bits are converted with a successive removal technique starting with a decision at the code 011 1111 and sequentially turning off bits until all decisions have been made.

ENCODE DECISION LEVELS

Compressing A/D conversion with the DAC-89 requires a comparator, an EXCLUSIVE-OR gate, and a successive approximation register — the usual elements in any sign-magnitude A/D converter. However, a compressing A/D has one significant difference. In a conventional (linear) converter, the step size is a constant percentage of full scale, but in a compressing A/D converter, the step size increases as the output changes from zero-scale to full-scale.

When the DAC is used in the feedback loop of a successive approximation analog to digital converter (ADC), the DAC outputs are used as decision levels to determine the edges of the quantizing bands. When the DAC is used in the decode mode the outputs correspond to the center of the quantizing bands. The encode mode output exceeds the decode mode output by one-half step. See AN 39 for detailed explanation.

ENCODE TRANSFER CHARACTERISTIC (A/D CONVERSION)



NORMALIZED ENCODE DECISION LEVELS (SIGN-BIT EXCLUDED)

NORMALIZED ENCODE DECISION

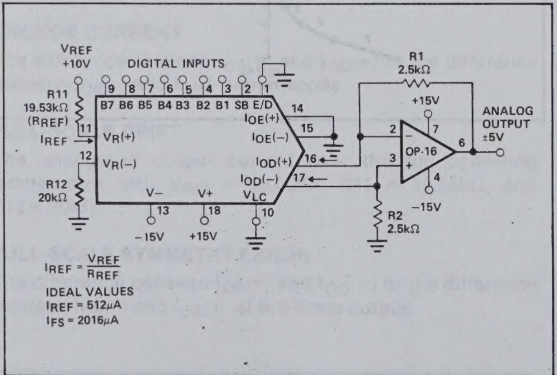
CHORD		0	1	2	3	4	5	6	7
STEP		000	001	010	011	100	101	110	111
0	0000	2	34	68	136	272	544	1088	2176
1	0001	4	36	72	144	288	576	1152	2304
2	0010	6	38	76	152	304	608	1216	2432
3	0011	8	40	80	160	320	640	1280	2560
4	0100	10	42	84	168	336	672	1344	2688
5	0101	12	44	88	176	352	704	1408	2816
6	0110	14	46	92	184	368	736	1472	2944
7	0111	16	48	96	192	384	768	1536	3072
8	1000	18	50	100	200	400	800	1600	3200
9	1001	20	52	104	208	416	832	1664	3328
10	1010	22	54	108	216	432	864	1728	3456
11	1011	24	56	112	224	448	896	1792	3584
12	1100	26	58	116	232	464	928	1856	3712
13	1101	28	60	120	240	480	960	1920	3840
14	1110	30	62	124	248	496	992	1984	3968
15	1111	32	64	128	256	512	1024	2048	*4096
STEP SIZE		2	2	4	8	16	32	64	128

*Virtual Decision Level

BASIC DECODE OPERATION (EXPANDING D/A CONVERSION)

D/A conversion with the DAC-89 is implemented by using an operational amplifier connected to the decode outputs. The decode mode of operation is selected by applying a logic "0" to the Encode/Decode input. This mode enables the I_{OD} outputs, disables the I_{OE} outputs, and allows $I_{OD}(+)$ or $I_{OD}(-)$ to be selected by the sign-bit input. When the sign-bit input is high, logic "1", the output current flows into $I_{OD}(+)$ forcing a positive voltage at the operational amplifier's output. When the sign-bit input is low, logic "0", the output current flows into $I_{OD}(-)$ through R2 forcing a negative voltage output. The sign-bit steers current into $I_{OD}(+)$ or $I_{OD}(-)$, the output will therefore always be symmetrical, limited only by the matching of R1 and R2.

BASIC DECODE CONNECTIONS



$$I_{REF} = \frac{V_{REF}}{R_{REF}}$$

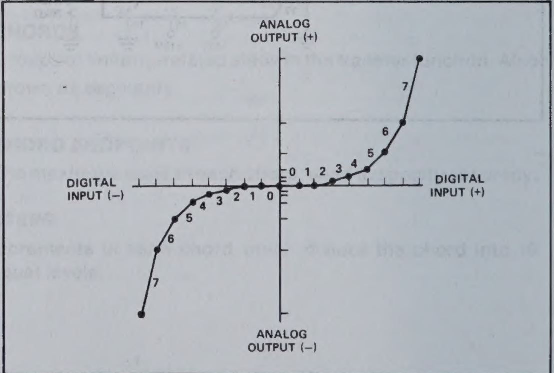
IDEAL VALUES
$I_{REF} = 512\mu A$
$I_{FS} = 2016\mu A$

NORMALIZED TABLES

The encode and decode tables are used to calculate ideal output current at any code point. For example, in decode mode at $I_{3,7}$ (011 0111) find 188. 188/4032 times I_{FS} of 2016μA equals 94μA.

	E/D	SB	B1	B2	B3	B4	B5	B6	B7	E_0
POS FULL-SCALE	0	1	1	1	1	1	1	1	1	5.040V
(+) ZERO-SCALE +1 STEP	0	1	0	0	0	0	0	0	1	0.0012V
(+) ZERO-SCALE	0	1	0	0	0	0	0	0	0	0.004V
(−) ZERO-SCALE	0	0	0	0	0	0	0	0	0	0.004V
(−) ZERO-SCALE +1 STEP	0	0	0	0	0	0	0	0	1	−0.0012V
NEG FULL-SCALE	0	0	1	1	1	1	1	1	1	−5.040V

DECODE TRANSFER CHARACTERISTIC (D/A CONVERSION)



NORMALIZED DECODE OUTPUT (SIGN-BIT EXCLUDED)

NORMALIZED DECODE OUTPUT

STEP \ CHORD		0 000	1 001	2 010	3 011	4 100	5 101	6 110	7 111
0	0000	1	33	66	132	264	528	1056	2112
1	0001	3	35	70	140	280	560	1120	2240
2	0010	5	37	74	148	296	592	1184	2368
3	0011	7	39	78	156	312	624	1248	2496
4	0100	9	41	82	164	328	656	1312	2624
5	0101	11	43	86	172	344	688	1376	2752
6	0110	13	45	90	180	360	720	1440	2880
7	0111	15	47	94	188	376	752	1504	3008
8	1000	17	49	98	196	392	784	1568	3136
9	1001	19	51	102	204	408	816	1632	3264
10	1010	21	53	106	212	424	848	1696	3392
11	1011	23	55	110	220	440	880	1760	3520
12	1100	25	57	114	228	456	912	1824	3648
13	1101	27	59	118	236	472	944	1888	3776
14	1110	29	61	122	244	488	976	1952	3904
15	1111	31	63	126	252	504	1008	2016	4032
STEP SIZE		2	2	4	8	16	32	64	128

BASIC REFERENCE CONSIDERATIONS

Full-scale output current is ideally 2016μ when the reference current is 512μA in the decode mode. In the encode mode I_{FS} = 2048μA due to the additional one-half step (32μA). A percentage change in I_{REF} caused by changes in V_{REF} or R_{REF} will produce the same percentage change in output current.

The large step size at full scale allows the use of inexpensive references in many applications. In some applications V_{REF} may even be the positive power supply. For example, with V+ = 15V, R_{REF} = 15V/512μA or 29.3kΩ. When using a power supply as a reference, R11 should be two resistors, R11A and R11B, and the junction bypassed to ground to provide decoupling.

OUTPUT VOLTAGE COMPLIANCE

The DAC-89 has true current outputs with wide voltage compliance that enables single ended and balanced load driving capability. Positive voltage compliance is +18V and negative voltage compliance is −5.0V with I_{REF} = 512μA and V = −15V. Negative voltage compliance $V_{OC}(-)$ for other values of I_{REF} and V− may be obtained from the table, or calculated as follows:

$$V_{OC}(-) \text{ min} = (V-) + (2\, I_{REF} \times 1.6k\Omega) + 8.4V$$

Output voltage compliance can be extended in both encode and decode modes using the output compliance extension connections. (Figures 1 and 2).

NEGATIVE OUTPUT VOLTAGE COMPLIANCE $V_{OC}(-)$

	I_{FS}		
V−	1.0mA	2.0mA	4.0mA
−12V	−2.8V	−2.0V	−0.4V
−15V	−5.8V	−5.0V	−3.4V
−18V	−8.8V	−8.0V	−6.4V

MINIMUM NEGATIVE COMPLIANCE

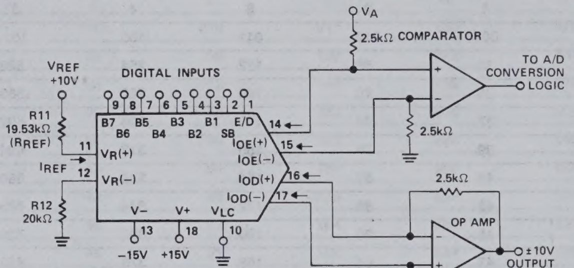
$$V_{OC}(-) \text{ MIN} = (V-) + (2\, I_{REF}\, 1.6k\Omega) + 8.4V$$

IDLE OUTPUT CURRENT

In the selected output state (encode or decode), equivalent idle currents are present on the (+) and (−) output leads. The output will be symmetrical with the external resistor matching determining the overall system accuracy.

OUTPUT COMPLIANCE EXTENSION CONNECTIONS

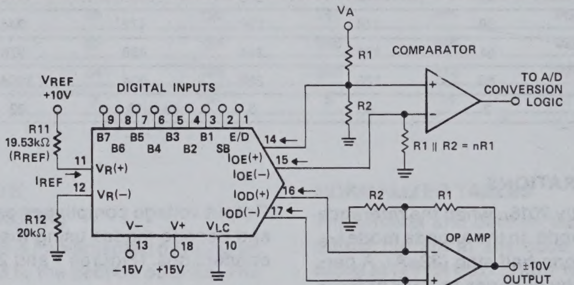
STANDARD ENCODE/DECODE CONNECTIONS


VA
2.5kΩ
COMPARATOR
TO A/D CONVERSION LOGIC
VREF +10V
DIGITAL INPUTS
R11 19.53kΩ (RREF)
IREF
R12 20kΩ
9 8 7 6 5 4 3 2 1
B7 B5 B3 B1 E/D
B6 B4 B2 SB
11 VR(+)
12 VR(−)
IOE(+) 14
IOE(−) 15
IOD(+) 16
IOD(−) 17
V− V+ VLC
13 18 10
−15V +15V
2.5kΩ
2.5kΩ
OP AMP
±10V OUTPUT
2.5kΩ

STANDARD ENCODE/DECODE CONNECTIONS REQUIRE $|V_{OC(-)}| \leq |V_{Amax}|$

Figure 1

EXTENDED RANGE CONNECTIONS


VA
R1
COMPARATOR
R2
TO A/D CONVERSION LOGIC
R1 ∥ R2 = nR1
VREF +10V
DIGITAL INPUTS
R11 19.53kΩ (RREF)
IREF
R12 20kΩ
9 8 7 6 5 4 3 2 1
B7 B5 B3 B1 E/D
B6 B4 B2 SB
11 VR(+)
12 VR(−)
IOE(+) 14
IOE(−) 15
IOD(+) 16
IOD(−) 17
V− V+ VLC
13 18 10
−15V +15V
R2
R1
OP AMP
±10V OUTPUT
R1 ∥ R2 = nR1

EXTENDED RANGE CONNECTION ALLOWS
$V_{Amax} \leq V_{OC(-)}/n$
WHERE $n = R2/R1 + R2$
V_A MUST DRIVE R1 + R2

Figure 2

IDEAL DECODE OUTPUT CURRENT IN MICROAMPS (SIGN-BIT EXCLUDED)

IDEAL DECODE OUTPUT

CHORD		0	1	2	3	4	5	6	7
STEP		000	001	010	011	100	101	110	111
0	0000	0.5	16.5	33	66	132	264	528	1056
1	0001	1.5	17.5	35	70	140	280	560	1120
2	0010	2.5	18.5	37	74	148	296	592	1184
3	0011	3.5	19.5	39	78	156	312	624	1248
4	0100	4.5	20.5	41	82	164	328	656	1312
5	0101	5.5	21.5	43	86	172	344	688	1376
6	0110	6.5	22.5	45	90	180	360	720	1440
7	0111	7.5	23.5	47	94	188	376	752	1504
8	1000	8.5	24.5	49	98	196	392	784	1568
9	1001	9.5	25.5	51	102	204	408	816	1632
10	1010	10.5	26.5	53	106	212	424	848	1696
11	1011	11.5	27.5	55	100	220	440	880	1760
12	1100	12.5	28.5	57	114	228	456	912	1824
13	1101	13.5	29.5	59	118	236	472	944	1888
14	1110	14.5	30.5	61	122	244	488	976	1952
15	1111	15.5	31.5	63	126	252	504	1008	2016
STEP SIZE		1	1	2	4	8	16	32	64

10-BIT CURRENT-OUTPUT D/A CONVERTER

DAC-100

FEATURES

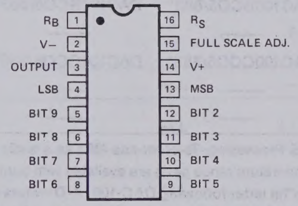
- **Complete .... Internal Reference**
- **Flexible .... 0 to 2mA Output**
- **Fast Settling .... 225nsec (8 Bits), 375nsec (10 Bits)**
- **Stable .... Tempcos to ±15ppm/° C Max**
- **0° C/ +70° C, −25° C/ +85° C, −55° C/ +125° C Models Available**
- **TTL Compatible Logic Inputs**
- **Wide Supply Range .... ±6V to ±18V**
- **8 and 10 Bit Versions Available**
- **MIL-STD-883 Class B Processing Models Available**
- **Low Cost Q3, Q4 Series**

GENERAL DESCRIPTION

The DAC-100 is a complete 10-bit resolution digital-to-analog converter constructed on two monolithic chips in a single 16-pin DIP. Featuring excellent linearity vs. temperature performance, the DAC-100 includes a low tempco voltage reference, ten current source/switches and a high stability thin-film R-2R ladder network. Maximum application flexibility is provided by the fast current output and by matched bipolar offset and feedback resistors which are included for use with an external op amp for voltage output applications. Although all units have 10-bit resolution, a wide choice of linearity and tempco options is provided to allow price/performance optimization.

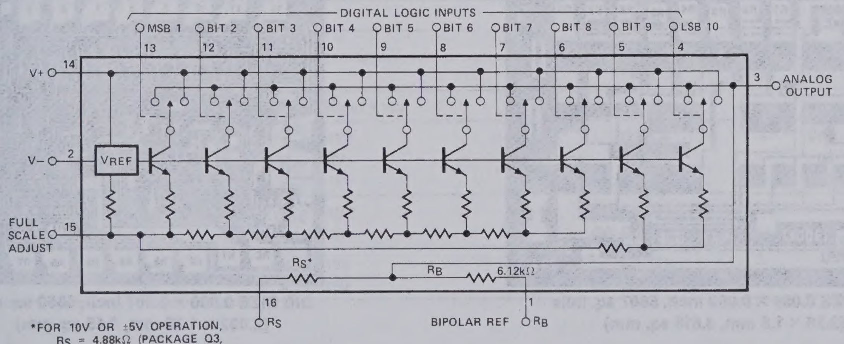
The small size, wide operating temperature range, low power consumption and high reliability construction make the DAC-100 ideal for aerospace applications. Other applications include use in servo-positioning systems, X-Y plotters, CRT displays, programmable power supplies, analog meter movement drivers, waveform generators and high speed analog-to-digital converters.

PIN CONNECTIONS


RB 1
V− 2
OUTPUT 3
LSB 4
BIT 9 5
BIT 8 6
BIT 7 7
BIT 6 8
16 RS
15 FULL SCALE ADJ.
14 V+
13 MSB
12 BIT 2
11 BIT 3
10 BIT 4
9 BIT 5

16-PIN HERMETIC DUAL-IN-LINE PACKAGE (Q-Suffix)

SIMPLIFIED SCHEMATIC


DIGITAL LOGIC INPUTS
MSB 1
BIT 2
BIT 3
BIT 4
BIT 5
BIT 6
BIT 7
BIT 8
BIT 9
LSB 10
13
12
11
10
9
8
7
6
5
4
14
V+
3
ANALOG OUTPUT
2
V−
VREF
FULL SCALE ADJUST
15
RS*
RB
6.12kΩ
16
RS
1
BIPOLAR REF
RB

*FOR 10V OR ±5V OPERATION, RS = 4.88kΩ (PACKAGE Q3, Q5, Q7)
FOR 5V OR ±2.5V OPERATION, RS = 2.44kΩ (PACKAGE Q4, Q6, Q8)

ABSOLUTE MAXIMUM RATINGS (Note 2)

V+ Supply to V− Supply	0 to +36V
V+ Supply to Output	0 to +18V
V− Supply to Output	0 to −18V
Logic Inputs to Output	−1V to +6V
Power Dissipation (Note 1)	500mW
Operating Temperature Range Q3, Q4	0°C to +70°C
Q5, Q6, Q7, Q8	−55°C to +125°C
DICE Junction Temperature	−25°C to +150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	+300°C

NOTES:

1. Rating applies to ambient temperature of 100°C. Above 100°C, derate at 10mW/°C.
2. Ratings apply to DICE and packaged parts, unless otherwise noted.

ORDERING INFORMATION†

N.L.** %FS MAX	TEMPCO** ppm/°C MAX	MILITARY TEMPERATURE $V_O = \pm5V/10V$	MILITARY TEMPERATURE $V_O = \pm2.5V/5V$	INDUSTRIAL TEMPERATURE $V_O = \pm5V/10V$	INDUSTRIAL TEMPERATURE $V_O = \pm2.5V/5V$	COMMERCIAL TEMPERATURE $V_O = \pm5V/10V$	COMMERCIAL TEMPERATURE $V_O = \pm2.5V/5V$
±0.05	±15	—	—	DAC100AAQ7*	DAC100AAQ8*	—	—
±0.05	±30	—	—	DAC100ABQ7*	DAC100ABQ8*	—	—
±0.05	±60	DAC100ACQ5/883*	DAC100ACQ6/883*	DAC100ACQ7*	DAC100ACQ8*	DAC100ACQ3	DAC100ACQ4
±0.10	±30	DAC100BBQ5/883*	DAC100BBQ6/883*	DAC100BBQ7*	DAC100BBQ8*	—	—
±0.10	±60	DAC100BCQ5/883*	DAC100BCQ6/883*	DAC100BCQ7*	DAC100BCQ8*	DAC100BCQ3	DAC100BCQ4
±0.10	±120	—	—	—	—	—	—
±0.20	±60	DAC100CCQ5/883*	DAC100CCQ6/883*	DAC100CCQ7*	DAC100CCQ8*	DAC100CCQ3	DAC100CCQ4
±0.20	±120	—	—	—	—	—	—
±0.30	±120	—	—	DAC100DDQ7*	DAC100DDQ8*	DAC100DDQ3	DAC100DDQ4

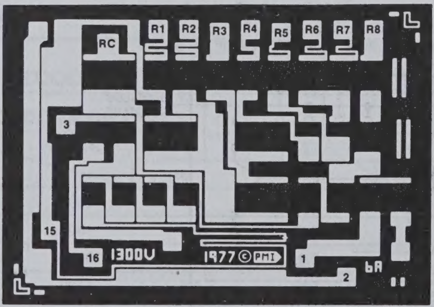
*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

** Part number construction: The 1st letter following DAC-100 (A-D) refers to the non-linearity specification; the 2nd letter (A-D) refers to the full-scale tempco; the letter Q refers to the package; and the end numeral indicates the output voltage and temperature.

DICE CHARACTERISTICS

DAR-01



DIE SIZE 0.089 × 0.063 inch, 5607 sq. mils (2.26 × 1.6 mm, 3.616 sq. mm)

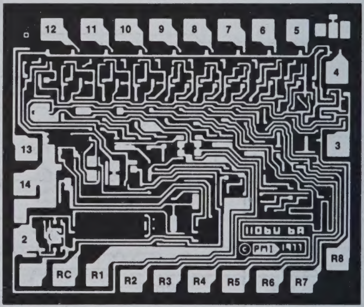
1. R_B
2. V−
3. OUTPUT
15. FULL-SCALE ADJ
16. R_S

R — Pads are connected to similarly marked pads on DAI-01

Note: Pads 4 — 14, See DAI-01

For additional DICE information refer to Section 2.

DAI-01



DIE SIZE 0.080 × 0.067 inch, 5360 sq. mils (2.032 × 1.70 mm, 3.45 sq. mm)

2. V−
3. OUTPUT
4. BIT 10 (LSB)
5. BIT 9
6. BIT 8
7. BIT 7
8. BIT 6
9. BIT 5
10. BIT 4
11. BIT 3
12. BIT 2
13. BIT 1 (MSB)
14. V+

R — Pads are connected to similarly marked pads on DAR-01

Note: Pads 1, 2, 15, 16, See DAR-01

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-25°C \le T_A \le +85°C$ for Q7 and Q8 devices; $0°C \le T_A \le +70°C$ for Q3 and Q4; $-55°C \le T_A \le +125°C$ for Q5 and Q6 devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-100	MIN	TYP	MAX	UNITS
Resolution				10	—	—	Bits
Nonlinearity (For nonlinearity/tempco combinations, see Ordering Information)	NL	(±1/2LSB — 10 bits)	A—	—	—	±0.05	%FS
	NL	(±1/2LSB — 9 bits)	B—	—	—	±0.1	%FS
	NL	(±1/2LSB — 8 bits)	C—	—	—	±0.2	%FS
	NL	(±3/4LSB — 8 bits)	D—	—	—	±0.3	%FS
Full-Scale Tempco (See Full-Scale Test Circuit)	T_C		—A	—	—	±15	ppm/°C
	T_C		—B	—	—	±30	ppm/°C
	T_C		—C	—	—	±60	ppm/°C
	T_C		—D	—	—	±120	ppm/°C
Settling Time $T_A = 25°C$	t_S	to ±0.05% FS	ALL	—	—	375	ns
	t_S	to ±0.1% FS	ALL	—	—	300	ns
	t_S	to ±0.2% FS	ALL	—	—	225	ns
	t_S	to ±0.4% FS	ALL	—	—	150	ns
	t_S	to ±0.8% FS	ALL	—	—	100	ns
Full-Range Output Voltage (Limits guarantee adjustability to exact 10.0 (5.0)V with a 200Ω Trimpot® between Adjust and V−	V_{FR}	Connect FS Adjust to V− 10V Models (Q3, Q5, Q7) (See Full-Scale Test Circuit)		10	—	11.1	V
		5V Models (Q4, Q6, Q8) $V_{IN} = 0.0V$ (See Full-Scale Test Circuit)		5	—	5.55	V
Zero-Scale Output Voltage	V_{ZS}	$V_{IN} = 2.1V$	ALL	—	—	0.013	%FS
Logic Inputs: High	V_{INH}	Measured with respect to output pin	ALL	2.1	—	—	V
Logic Inputs: Low	V_{INL}	Measured with respect to output pin	ALL	—	—	0.7	V
Logic Input Current, Each Input	I_{IN}	$V_{IN} = 0$ to $+6V$	ALL	—	—	5	μA
Logic Input Resistance	R_{IN}	$V_{IN} = 0$ to $+6V$	ALL	—	3	—	mΩ
Logic Input Capacitance	C_{IN}		ALL	—	2	—	pF
Output Resistance	R_O		ALL	—	500	—	kΩ
Output Capacitance	C_O		ALL	—	13	—	pF
Applied Power Supplies: V+			ALL	+6	—	+18	V
Applied Power Supplies: V−			ALL	−6	—	−18	V
Power Supply Sensitivity	P_{SS}	$V_S = \pm 6V$ to $\pm 18V$	ALL	—	—	±0.10	% per Volt
Power Consumption	P_D	$V_S = \pm 15V$	Q3, Q4	—	200	300	mW
	P_D	$V_S = \pm 6V$	Q3, Q4	—	80	100	mW
	P_D	$V_S = \pm 15V$	Q5, Q6, Q7, Q8	—	200	250	mW
Positive Supply Current	I+	$V_S = +15V$	Q3, Q4	—	—	10	mA
	I+	$V_S = +15V$	Q5, Q6, Q7, Q8	—	—	8.33	mA
Negative Supply Current	I−	$V_S = -15V$	Q3, Q4	—	—	−10	mA
	I−	$V_S = -15V$	Q5, Q6, Q7, Q8	—	—	−8.33	mA

WAFER TEST LIMITS at $T_A = 25°C$ for the R2R Ladder Network comprised of R1-R8, R12, R23, R34, R45 and R56 when connected to an ideal DAI-01, unless otherwise noted.

		DAR-01-N			DAR-01-G			DAR-01-GR			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Nonlinearity	VR1 = 3.2V	—	—	±0.035	—	—	±0.05	—	—	±0.1	%

WAFER TEST LIMITS at $T_A = 25°C$, VR1 = 3.2V, unless otherwise noted.

		DAR-01			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Resistance R1	Absolute Measurement	2.56	—	3.84	kΩ
Ratio RC1 to R1	Ideal = 1.00503 to 1	−1	—	+1	%
Ratio R1 to RS1	Ideal = 1.29959 to 1	−1	—	+1	%
Ratio R1 to RS2	Ideal = 1.29959 to 1	−1	—	+1	%
Ratio RB to R1	Ideal = 1.92211 to 1	−1	—	+1	%

Note: Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS in common to all grades.

		DAR-01			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Absolute Temperature Coefficient	All Resistors	—	±120	—	ppm°C
Tracking Temperature Coefficient	All Resistors with Respect to R1	—	3	—	ppm°C

WAFER TEST LIMITS at $T_A = 25°C$ when connected to an ideal DAR-01, unless otherwise noted

			DAI-01-N			DAI-01-G			DAI-01-GR			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Nonlinearity	NL	$V_S = \pm 15V$	—	—	±0.05	—	—	±0.1	—	—	±0.2	%
Internal Reference Voltage	V_{MCR}	$V_S = \pm 15V$	6.600	—	6.825	6.6	—	6.825	6.45	—	6.90	V

WAFER TEST LIMITS at $V_S = +15V$, $T_A = 25°C$ when connected to an ideal DAR-01, unless otherwise noted.

		DAI-01			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Resolution		10	—	10	Bits
Anolog Output Current	All Bits Low, V− Connected to FS Adjust	1840	—	2274	μA
Zero-Scale Output Current	All Bits High, V− Connected to FS Adjust	—	—	±0.25	μA
Logic Input "0"	Measured with Respect to Output	—	—	0.7	V
Logic Input "1"	Measured with Respect to Output	2.1	—	—	V
Supply Current	All Bits High, V− Connected to FS Adjust	—	—	8.33	mA
Power Supply Rejection	$V_S = \pm 6V$ to $\pm 18V$	—	—	0.1	%IFS/V

Note: Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

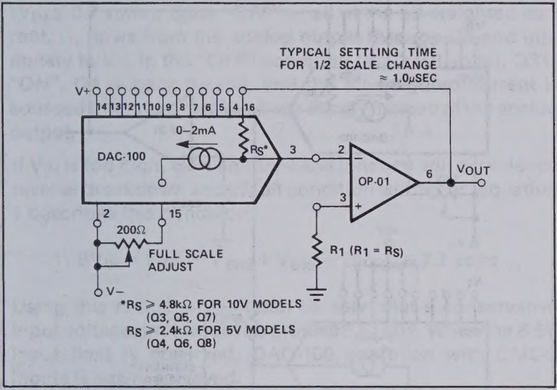
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, and when connected to an ideal DAR-01, unless otherwise noted.

		DAI-01-N			DAI-01-G			DAI-01-GR			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Full-Scale Tempco	(Note)	—	±60	—	—	±60	—	—	±120	—	ppm/°C

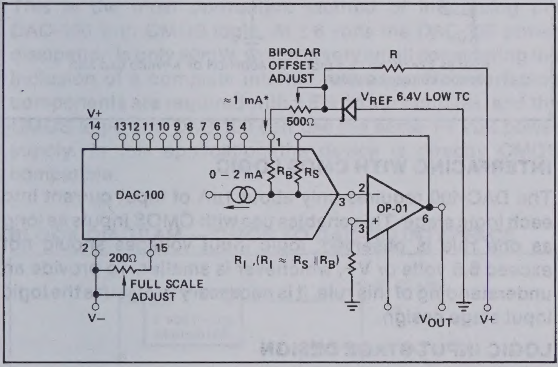
NOTE:
Full-Scale Tempco is defined as the change in output voltage measured in the test circuit shown on the DAC-100 data sheet and is expressed in ppm between 25°C and either temperature extreme divided by the corresponding temperature change.

BASIC CONNECTIONS

BASIC UNIPOLAR VOLTAGE OUTPUT CIRCUIT


TYPICAL SETTLING TIME
FOR 1/2 SCALE CHANGE
≈ 1.0μSEC
V+
14 13 12 11 10 9 8 7 6 5 4 16
0–2mA
DAC-100
RS*
3
2
OP-01
6
VOUT
3
2
15
200Ω
FULL SCALE
ADJUST
R1 (R1 = RS)
V–
*RS ≥ 4.8kΩ FOR 10V MODELS
(Q3, Q5, Q7)
RS ≥ 2.4kΩ FOR 5V MODELS
(Q4, Q6, Q8)

BASIC BIPOLAR VOLTAGE OUTPUT CIRCUIT

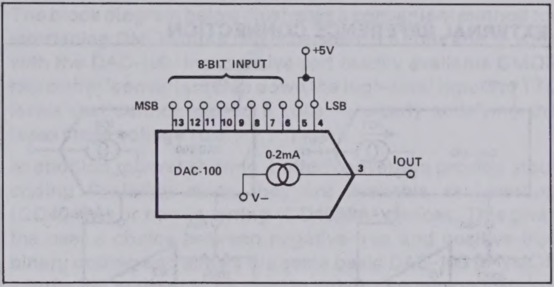

BIPOLAR
OFFSET
ADJUST
R
≈1 mA*
VREF 6.4V LOW TC
500Ω
V+
14
13 12 11 10 9 8 7 6 5 4
1
0 – 2 mA
RB
RS
DAC-100
3
2
OP-01
6
3
2
15
200Ω
RI ,(RI ≈ RS ‖RB)
FULL SCALE
ADJUST
V–
VOUT
V+

APPLICATIONS INFORMATION

FULL RANGE OUTPUT ADJUSTMENT — The output current of the DAC-100 may be reduced to produce an exact 10.000 (5.000) volt output by connecting a 200Ω adjustable resistance between the full-scale adjust pin and V–. Adjustment should be made with an input of all "zeroes."

LOWER RESOLUTION APPLICATIONS — The DAC-100 may be used in applications requiring less than 10 bits of resolution. All unused logic inputs **must** be tied to logic high for proper operation. "Floating" logic inputs can cause improper operation.

REDUCED RESOLUTION APPLICATION


+5V
8-BIT INPUT
MSB
LSB
13 12 11 10 9 8 7 6 5 4
0-2mA
DAC-100
3
IOUT
V–

LOGIC CODING — The DAC-100 uses complementary or inverted binary logic coding, i.e., an all "zeroes" input produces a full range output, while an all "ones" input produces a zero-scale output. Each lesser significant bit's weight is one-half the previous more significant bit's value. High logic input turns the bit "OFF," low logic input level turns the bit "ON".

LOGIC COMPATIBILITY — The input logic levels are directly compatible with TTL logic and may also be used with CMOS logic powered from a single +5 volt supply.

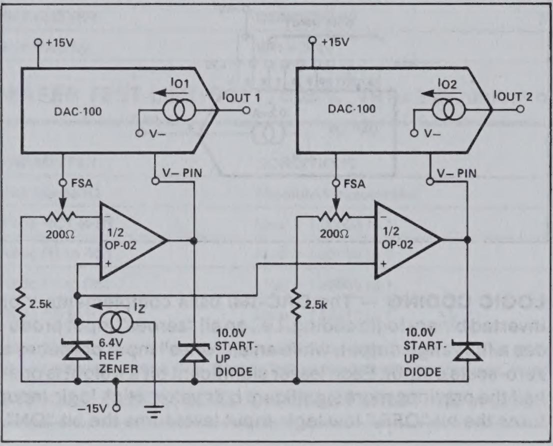
NONLINEARITY (NL) — The maximum deviation from an ideal straight line drawn between the end points, expressed as a percent of full-scale range (FSR) or given in terms of LSB value. The end points are zero-scale output to full-scale output for unipolar operation and minus full-scale to positive full-scale for bipolar operation.

BIPOLAR OPERATION — The DAC-100 may be converted to bipolar operation by injecting a half-scale current into the output; this is accomplished by connecting the internal bipolar resistor to a +6.4 volt reference. Trimming of the zero output may be facilitated by placing a 500Ω adjustable resistance in series with the +6.4 volts.

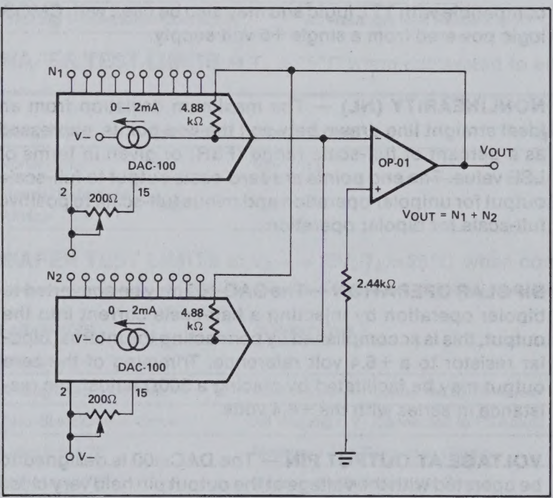
VOLTAGE AT OUTPUT PIN — The DAC-100 is designed to be operated with the voltage at the output pin held very close to zero volts. Input logic threshold levels are directly affected by output pin voltage changes; voltage swings at the output may cause loss of linearity due to improper switching of bits. Large voltage swings may cause permanent damage and should be avoided. Proper ooperation can be obtained with output voltages held within ±0.7 volts; a pair of back-to-back silicon diodes tied from the output ground is a convenient way of clamping the output to this limit.

TYPICAL APPLICATIONS

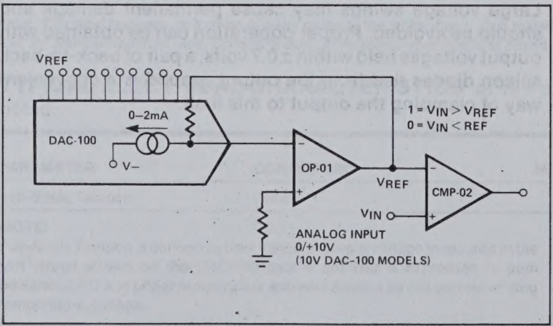
EXTERNAL REFERENCE CONNECTION


+15V
+15V
DAC-100
I_{O1}
$I_{OUT\ 1}$
V−
DAC-100
I_{O2}
$I_{OUT\ 2}$
V−
FSA
V− PIN
FSA
V− PIN
200Ω
1/2 OP-02
200Ω
1/2 OP-02
2.5k
I_Z
2.5k
6.4V REF ZENER
10.0V START-UP DIODE
10.0V START-UP DIODE
−15V

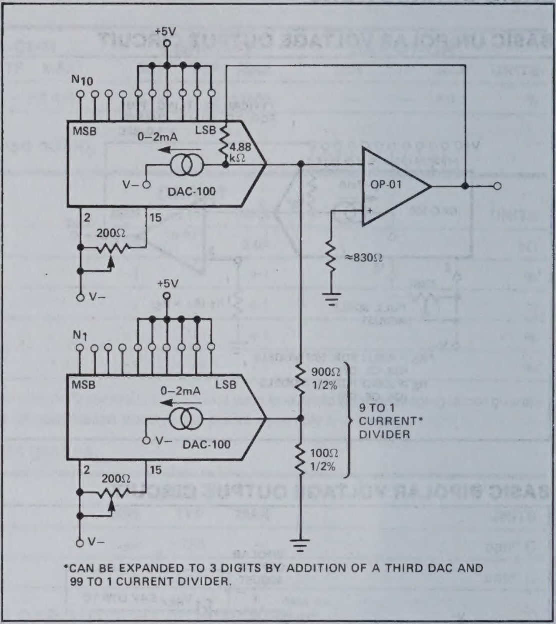
ANALOG SUM OF TWO DIGITAL NUMBERS


N_1
0 – 2mA
4.88 kΩ
V−
DAC-100
2
200Ω
15
V_{OUT}
OP-01
$V_{OUT} = N_1 + N_2$
N_2
2.44kΩ
0 – 2mA
4.88 kΩ
V−
DAC-100
2
200Ω
15
V−

DIGITALLY PROGRAMMED LEVEL DETECTOR


V_{REF}
0–2mA
DAC-100
V−
OP-01
V_{REF}
1 = $V_{IN} > V_{REF}$
0 = $V_{IN} < REF$
CMP-02
V_{IN}
ANALOG INPUT 0/+10V (10V DAC-100 MODELS)

BINARY-CODED-DECIMAL D/A CONVERSION


+5V
N_{10}
MSB
0–2mA
LSB
4.88 kΩ
V−
DAC-100
2
15
200Ω
V−
OP-01
≈830Ω
+5V
N_1
MSB
0–2mA
LSB
V−
DAC-100
900Ω 1/2%
9 TO 1 CURRENT* DIVIDER
100Ω 1/2%
2
200Ω
15
V−

*CAN BE EXPANDED TO 3 DIGITS BY ADDITION OF A THIRD DAC AND 99 TO 1 CURRENT DIVIDER.

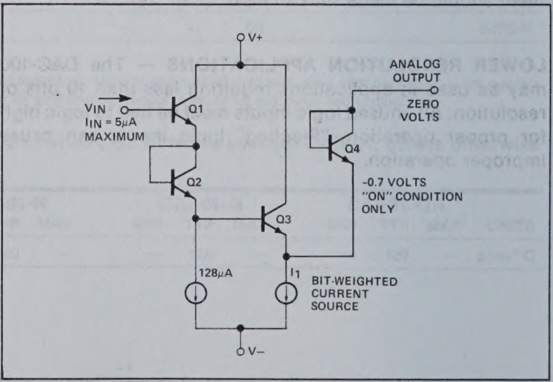
INTERFACING WITH CMOS LOGIC

The DAC-100 requires only about 1μA of input current into each logic stage. This enables use with CMOS inputs as long as one rule is observed; logic input voltages should not exceed 6.5 volts or V+, whichever is smaller. To provide an understanding of this rule, it is necessary to discuss the logic input stage design.

LOGIC INPUT STAGE DESIGN

For simplicity, only one of the ten identical input circuits is shown below. The DAC-100 uses a fast current-steering technique that switches a bit-weighted current between the positive supply (V+) and the analog output, which is usually constrained to be at zero volts (virtual ground) by an external summing amplifier.

DAC-100 — LOGIC INPUT STAGE


V+
ANALOG OUTPUT
ZERO VOLTS
V_{IN}
$I_{IN} = 5\mu A$ MAXIMUM
Q1
Q4
Q2
-0.7 VOLTS "ON" CONDITION ONLY
Q3
128μA
I_1
BIT-WEIGHTED CURRENT SOURCE
V−

Switching is accomplished by forward biasing Q4, diode-connected transistor, for the bit "ON" condition and back biasing Q4 in the "OFF" condition. For the "ON" condition ($V_{IN} \leq 0.7$ volts), Q3 is "OFF" — all of the bit-weighted current, I_1, flows from the analog output through Q4 and ultimately to V−. In the "OFF" condition ($V_{IN} \geq 2.1$ volts), Q3 is "ON", Q4 is back biased, and the bit-weighted current is sourced from the positive power supply instead of the analog output.

If V_{IN} is too high, Q4's emitter-base junction will experience reverse breakdown and a fault condition will occur. Equation 1 describes this condition:

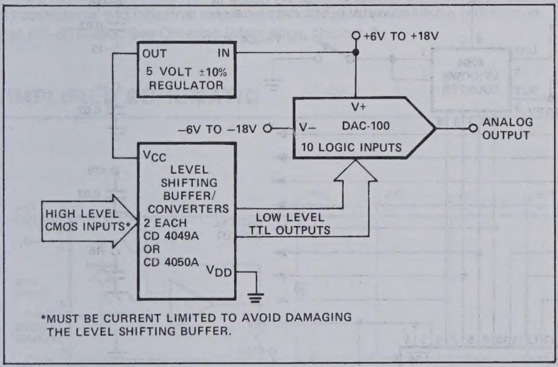
$$1)\ BV_{IH} = V_{BE1} + V_{BE2} + V_{BE3} + BV_{EB4} \cong 7.7 \text{ volts}$$

Using this relationship, it can be seen that a conservative input voltage limit would be around 6.5 volts. When the 6.5V input limit is observed, DAC-100 operation with CMOS inputs is easily achieved.

±6 VOLT POWER SUPPLY OPERATION

This is the most convenient method of interfacing the DAC-100 with CMOS logic. At ±6 volts the DAC-100 power dissipation is only 80mW, which is very small considering the inclusion of a complete internal reference. No interfacing components are required with ±5% power supplies, and the CMOS logic and DAC-100 can use the same +6 volt power supply. In this application the device is directly CMOS compatible.

BLOCK DIAGRAM — CMOS TO DAC-100 INTERFACE



*MUST BE CURRENT LIMITED TO AVOID DAMAGING THE LEVEL SHIFTING BUFFER.

HIGH LEVEL CMOS INTERFACING

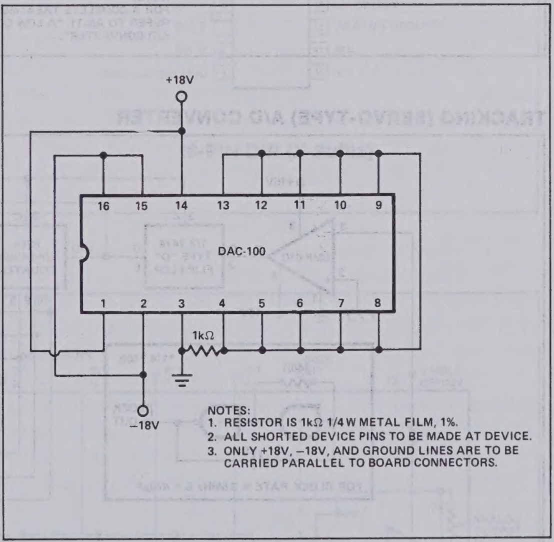
The block diagram below illustrates a convenient method for interfacing CMOS input levels between 6.5 volts and 15 volts with the DAC-100. Inexpensive and readily available CMOS hex buffer/converters step down the high-level inputs to TTL levels that cannot exceed 5 volts — clearly satisfying the input stage voltage rule.

In addition to level shifting, buffer/converters provide input coding flexibility since they are available as inverting (CD4049A) or non-inverting (CD4050A) devices. This gives the user a choice between negative-true and positive-true binary coding and allows the same basic DAC-100 to CMOS interfacing method to be used in either type of application.

Since buffer/converter power consumption is very low, the required +5 volts can be provided by a simple regulator or even a resistive divider in some applications. In a multi-DAC system, one central, inexpensive three-terminal IC regulator can supply several level shifting devices.

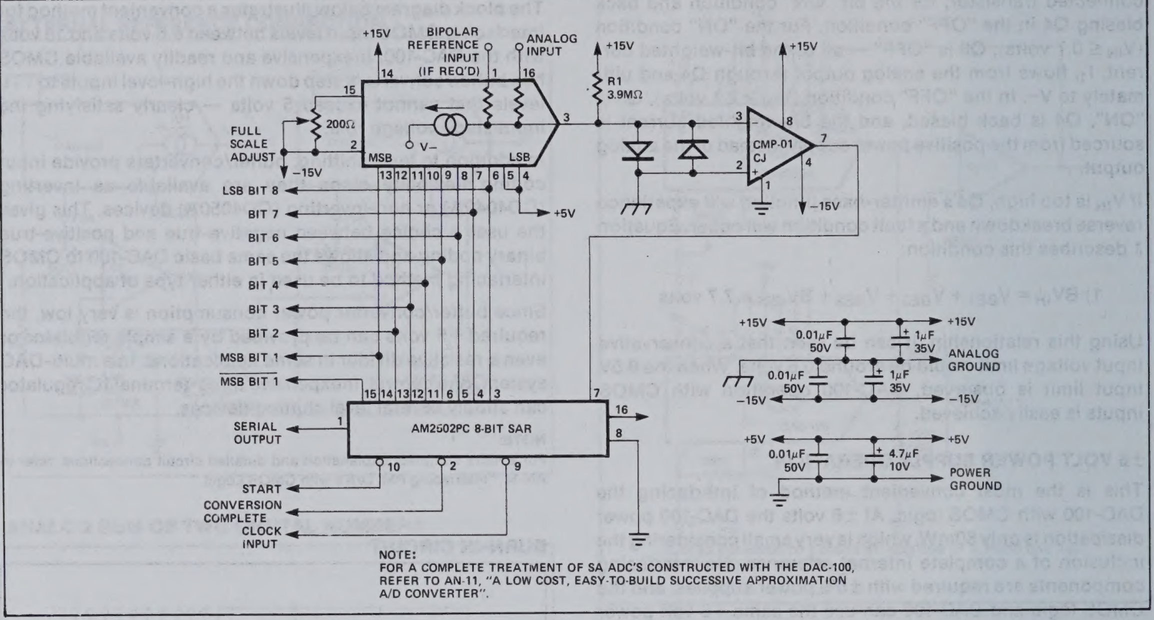
NOTE:
For a more complete explanation and detailed circuit connections, refer to AN-14, "Interfacing PMI D/A's with CMOS Logic."

BURN-IN CIRCUIT



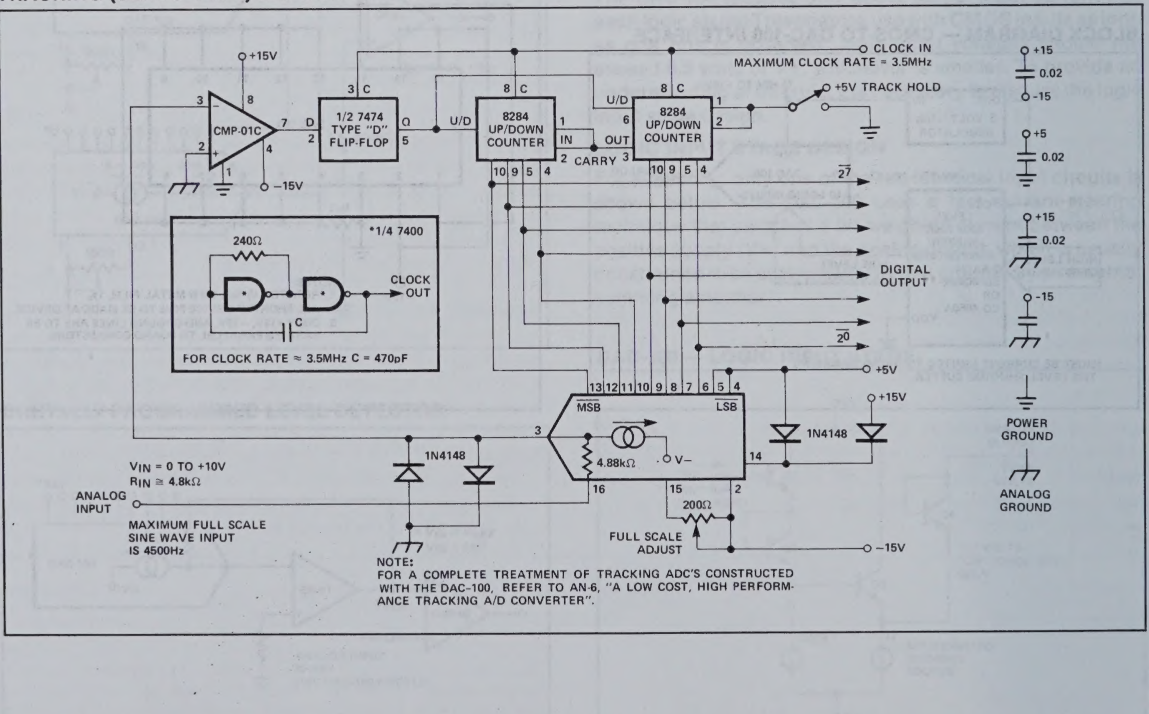
NOTES:
1. RESISTOR IS 1kΩ 1/4 W METAL FILM, 1%.
2. ALL SHORTED DEVICE PINS TO BE MADE AT DEVICE.
3. ONLY +18V, −18V, AND GROUND LINES ARE TO BE CARRIED PARALLEL TO BOARD CONNECTORS.

SUCCESSIVE APPROXIMATION A/D CONVERTER (8-BIT)


+15V
BIPOLAR REFERENCE INPUT (IF REQ'D)
ANALOG INPUT
+15V
+15V
R1
3.9MΩ
15
14
1
16
3
FULL SCALE ADJUST
200Ω
2
V−
MSB
LSB
−15V
3
8
CMP-01 CJ
7
2
4
1
−15V
13 12 11 10 9 8 7 6 5 4
+5V
LSB BIT 8
BIT 7
BIT 6
BIT 5
BIT 4
BIT 3
BIT 2
MSB BIT 1
MSB BIT 1
15 14 13 12 11 6 5 4 3
7
16
8
SERIAL OUTPUT
1
AM2502PC 8-BIT SAR
10
2
9
START
CONVERSION COMPLETE
CLOCK INPUT
+15V
+15V
0.01µF 50V
1µF 35V
ANALOG GROUND
0.01µF 50V
1µF 35V
−15V
−15V
+5V
+5V
0.01µF 50V
4.7µF 10V
POWER GROUND

NOTE:
FOR A COMPLETE TREATMENT OF SA ADC'S CONSTRUCTED WITH THE DAC-100, REFER TO AN-11, "A LOW COST, EASY-TO-BUILD SUCCESSIVE APPROXIMATION A/D CONVERTER".

TRACKING (SERVO-TYPE) A/D CONVERTER


+15V
3
8
CMP-01C
7
2
4
1
−15V
D
2
1/2 7474 TYPE "D" FLIP-FLOP
3 C
Q
5
U/D
8 C
8284 UP/DOWN COUNTER
1
IN
2
CARRY
OUT
3
10 9 5 4
U/D
6
8 C
8284 UP/DOWN COUNTER
1
2
10 9 5 4
CLOCK IN
MAXIMUM CLOCK RATE = 3.5MHz
+5V TRACK HOLD
*1/4 7400
240Ω
C
CLOCK OUT
FOR CLOCK RATE ≈ 3.5MHz C = 470pF
$\overline{2^7}$
DIGITAL OUTPUT
$\overline{2^0}$
+5V
+15V
13 12 11 10 9 8 7 6 5 4
MSB
LSB
3
4.88kΩ
V−
16
15
2
14
1N4148
1N4148
200Ω
FULL SCALE ADJUST
−15V
V_{IN} = 0 TO +10V
R_{IN} ≅ 4.8kΩ
ANALOG INPUT
MAXIMUM FULL SCALE SINE WAVE INPUT IS 4500Hz
+15
0.02
−15
+5
0.02
+15
0.02
−15
POWER GROUND
ANALOG GROUND

NOTE:
FOR A COMPLETE TREATMENT OF TRACKING ADC'S CONSTRUCTED WITH THE DAC-100, REFER TO AN-6, "A LOW COST, HIGH PERFORMANCE TRACKING A/D CONVERTER".

9-BIT VOLTAGE-OUTPUT D/A CONVERTER (8 BITS PLUS SIGN)

DAC-208

FEATURES

- **Complete .... Reference and OP Amp Included**
- **Sign-Magnitude Coding**
- **Unipolar/Bipolar Selectable .... +5V or ±10V**
- **8-Bit Linearity Maintained over Full Temp Range**
- **Fast .... 750ns Settling Time**
- **Multiplying Operation**
- **Guaranteed Monotonicity**
- **MIL-STD-883 Class B Processing Available**

GENERAL DESCRIPTION

The DAC-208 is a complete, voltage output, 8-Bit plus sign D/A converter. A precision voltage reference, logic controlled polarity switch, and high-speed (750 ns settling time) output op amp are included. Nonlinearity, monotonicity, and full-scale temperature coefficient are guaranteed over the full operating range. Enhanced reliability is achieved with monolithic construction and hermetic DIP packaging. Two low-cost 0°C/+70°C and two −55°C/+125°C grades are available in addition to MIL-STD-883 Class B processing. Monotonicity is guaranteed by design.

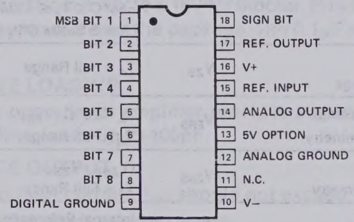
ORDERING INFORMATION†

NL %FS	18-PIN HERMETIC DUAL-IN-LINE MILITARY TEMP	18-PIN HERMETIC DUAL-IN-LINE COMMERCIAL TEMP
0.1	DAC208AX*	DAC208EX
0.2	DAC208BX*	DAC208FX

*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

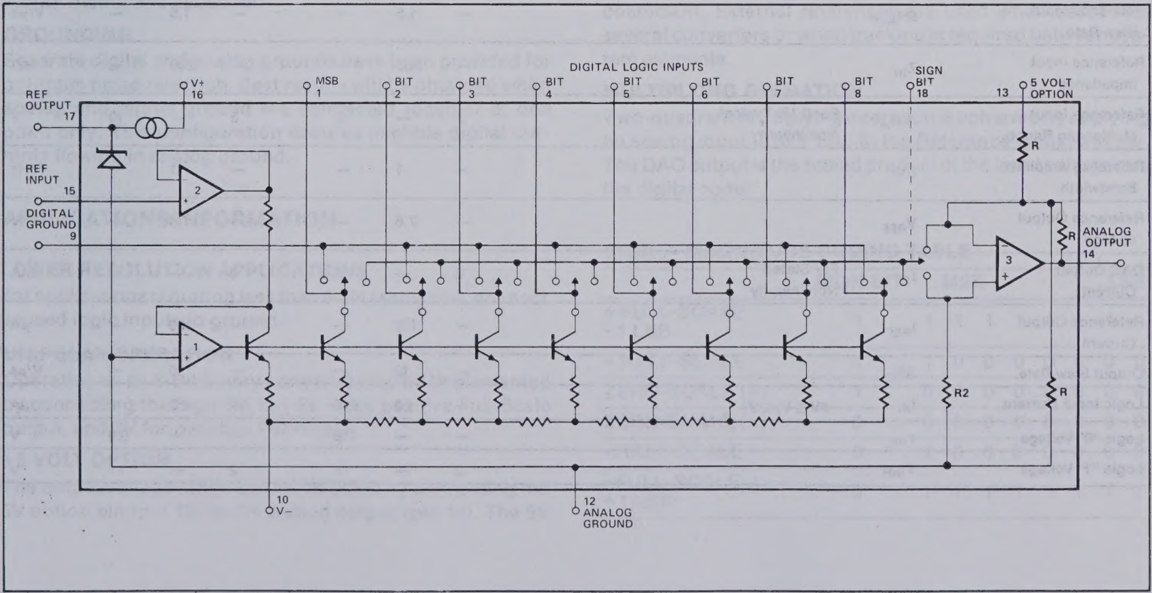
†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

PIN CONNECTIONS


MSB BIT 1 1
BIT 2 2
BIT 3 3
BIT 4 4
BIT 5 5
BIT 6 6
BIT 7 7
BIT 8 8
DIGITAL GROUND 9
18 SIGN BIT
17 REF. OUTPUT
16 V+
15 REF. INPUT
14 ANALOG OUTPUT
13 5V OPTION
12 ANALOG GROUND
11 N.C.
10 V−

18-PIN DIP (X-Suffix)

SIMPLIFIED SCHEMATIC


DIGITAL LOGIC INPUTS
V+ 16
MSB 1
BIT 2
BIT 3
BIT 4
BIT 5
BIT 6
BIT 7
BIT 8
SIGN BIT 18
13
5 VOLT OPTION
REF OUTPUT 17
REF INPUT 15
DIGITAL GROUND 9
2
1
3
R
R
R2
R
ANALOG OUTPUT 14
10 V−
12 ANALOG GROUND

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	
DAC-208A,B	−55° C to +125° C
DAC-208E, F	0° C to +70° C
Storage Temperature Range	−65° C to +150° C
V+ Supply to Analog Ground	0 to +18V
V− Supply to Analog Ground	0 to −18V
Analog Ground to Digital Ground	0 to ±0.5V
Logic Inputs to Digital Ground	−5V to (V+ −0.7V)
Internal Reference Output Current	300μA
Reference Input Voltage	0 to +10V
Internal Power Dissipation	500mW
Lead Soldering Temperature	300° C (60 sec)
Output Short-Circuit Duration	Indefinite
(Short circuit may be to ground or either supply.)	

ELECTRICAL CHARACTERISTICS — MILITARY AND COMMERCIAL GRADES at $V_S = \pm 15V$, $T_A = -55°C$ to $+125°C$ for A and B grades, $T_A = 0°C$ to $+70°C$ for E and F grades, unless otherwise noted.

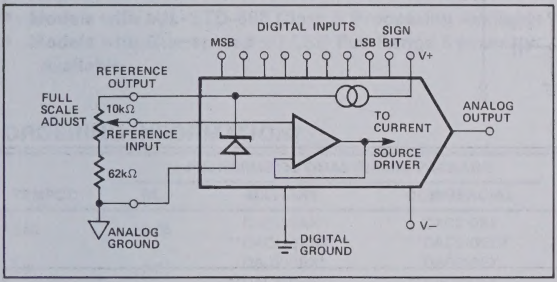
			DAC-208A/E			DAC-208B/F			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Resolution		Including Sign	9	9	9	9	9	9	Bits
Monotonicity			8	—	—	8	—	—	Bits
Nonlinearity	NL	$T_A = 25°C$ $T_A = 0°C - 70°C$ (E and F only) $-55°C \leq T_A \leq +125°C$ (A + B Suffix Only)	— — —	— — —	±0.1 ±0.1 ±0.1	— — —	— — —	±0.2 ±0.2 ±0.2	%FS
Zero-Scale Offset Voltage	V_{ZS}	T_A = Full Range	— —	— —	— ±0.1	— —	— —	— ±0.15	%FS
Bipolar Full Range Voltage Symmetry	V_{FRS}	$T_A = 25°C$ $(V_{FR+} - V_{FR-})$ T_A = Full Range	— —	— —	60 70	— —	— —	70 70	mV
Zero-Scale Voltage Symmetry	V_{ZSS}	$(V_{ZS+} - V_{ZS-})$ T_A = Full Range	—	—	1	—	—	2	mV
Gain Tempco	T_C	Internal Reference External Reference	— —	— 15	40 —	— —	— 30	60 —	ppm/° C
Output Voltage Range	V_{OR+} V_{OR-}		+10.0 +5.0 −11.5	— — —	+11.5 +5.75 −10.0	+10.0 +5.0 −11.5	— — —	+11.5 +5.75 −10.0	V
Differential Nonlinearity	DNL	$T_A = 25°C$	—	—	±1/2	—	—	1	LSB
Settling Time	t_S		—	750	—	—	750	—	ns
Reference Input Slew Rate	SR_{REF}		—	1.5	—	—	1.5	—	V/μs
Reference Input Impedance	Z_{IN}		—	200	—	—	200	—	MΩ
Reference Input Multiplying Range	IVR_m	For 0.1% Typical Nonlinearity	3	—	10	3	—	10	V
Reference Amplifier Bandwidth	BW		—	1	—	—	1	—	MHz
Reference Output Voltage	V_{REF}		—	7.6	—	—	7.6	—	V
DAC Output Current	I_O	For Stated Nonlinearity	0	—	10	0	—	10	mA
Reference Output Current	I_{REF}		—	100	—	—	100	—	μA
Output Slew Rate	SR_O		—	10	—	—	10	—	V/μs
Logic Input Current	I_{IN}	$-5V \leq V_I \leq V+$	—	±2	±10	—	±2	±10	μA
Logic "0" Voltage	V_{INL}		—	—	0.8	—	—	0.8	V
Logic "1" Voltage	V_{INH}		2	—	—	2	—	—	V

ELECTRICAL CHARACTERISTICS — MILITARY AND COMMERCIAL GRADES at $V_S = \pm 15V$, $T_A = -55°C$ to $+125°C$ for A and B grades, $T_A = 0°C$ to $+70°C$ for E and F grades, unless otherwise noted.(Continued)

PARAMETER	SYMBOL	CONDITIONS	DAC-208A/E MIN	DAC-208A/E TYP	DAC-208A/E MAX	DAC-208B/F MIN	DAC-208B/F TYP	DAC-208B/F MAX	UNITS
Power Supply Sensitivity	P_{SS}	T_A = Full Range	0.03	—	0.15	0.03	—	0.15	% V_{FS}/V
Positive Supply Current	I+		—	7	9	—	7	9	mA
Negative Supply Current	I−		—	10	12	—	10	12	mA

CONNECTION INFORMATION

FULL-SCALE ADJUSTMENT CIRCUIT



Full-Scale output voltage is trimmed using the circuit configuration shown above. Low tempco metal-film resistors are recommended. External components should be mounted near the package to ensure good temperature tracking.

REFERENCE INPUT BYPASS

Low noise and fast settling operation can be obtained by bypassing the Reference Input to Analog Ground with a 0.01μF monolithic capacitor.

GROUNDING

Separate digital and analog grounds have been provided for optimum noise rejection. Best results will be obtained when analog and digital ground are connected together at one point only. This configuration ensures neglible digital currents flowing in analog ground.

APPLICATIONS INFORMATION

LOWER RESOLUTION APPLICATIONS

For applications requiring less than 8-Bit resolution, connect unused logic inputs to ground.

UNIPOLAR OPERATION

Operation as an 8-Bit binary converter may be implemented by connecting the Sign-Bit to +5V — for positive Full-Scale output, and 0V for negative Full-Scale.

+5 VOLT OPTION

The output voltage range can be modified by connecting the 5V option pin (pin 13) to the analog output (pin 14). The 5V option is for unipolar operation only. In this configuration the Sign-Bit should be held at logic high (+5V).

POWER SUPPLIES

The DAC-208 will operate within specification for power supplies ranging from ±12V to ±18V for unipolar positive operation; and from ±13V to ±18V for bipolar. Power supplies should be bypassed near the package with 0.1μF monolithic capacitors.

CAPACITIVE LOADING

The output operational amplifier provides stable operation with capacitive loads up to 100pF.

REFERENCE OUTPUT

Reference output current, I_{ref}, should not exceed 100μA.

INTERFACING WITH CMOS LOGIC

The DAC-208 logic input stage requires approximately 1μA, I_{in}, and is capable of operation with inputs between −5V and (V+ −0.7 Volts). The wide input voltage range allows direct CMOS interface with no additional components required.

EXTERNAL REFERENCES

Positive external reference voltages may be applied to the reference input terminal to improve Full-Scale temperature coefficient. External references are used when cascading several converters or when tracking is required between system elements.

MULTIPLYING OPERATION

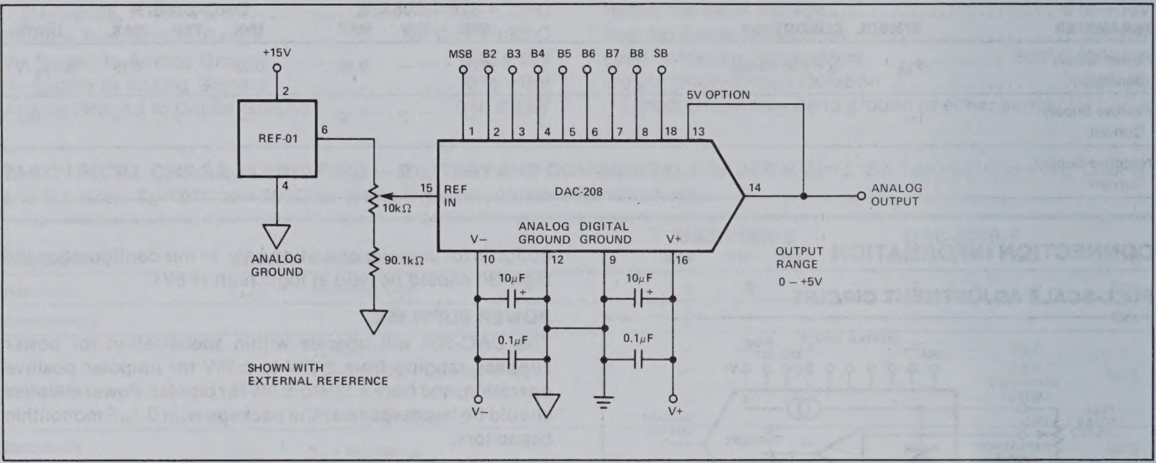
Two-quadrant multiplying operation is achieved by applying an analog input (0 to +10V) to the Reference input terminal. The DAC output is the scaled product of the input voltage and the digital code.

SIGN — MAGNITUDE CODING TABLE

	SIGN BIT	MSB							LSB
+FULL-SCALE −1 LSB	1	1	1	1	1	1	1	1	1
+HALF-SCALE	1	1	0	0	0	0	0	0	0
ZERO-SCALE (+)	1	0	0	0	0	0	0	0	0
ZERO-SCALE (−)	0	0	0	0	0	0	0	0	0
−HALF-SCALE	0	1	0	0	0	0	0	0	0
−FULL-SCALE +1 LSB	0	1	1	1	1	1	1	1	1

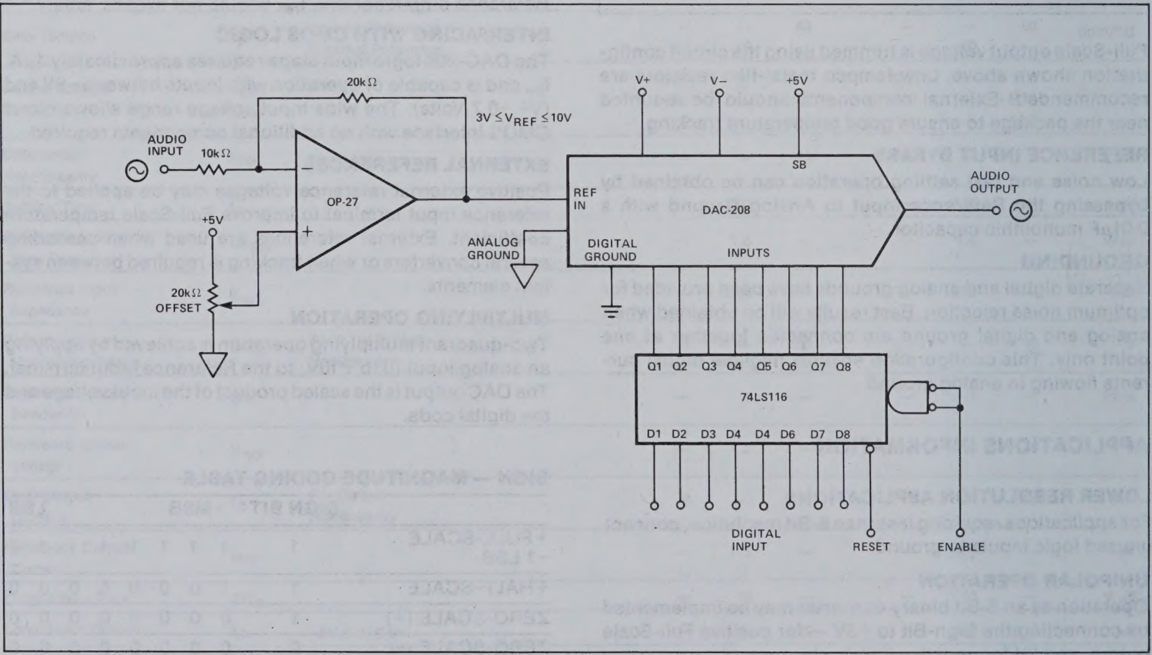
UNIPOLAR OPERATION

5V OPTION


+15V
2
REF-01
6
4
ANALOG GROUND
10kΩ
90.1kΩ
MSB B2 B3 B4 B5 B6 B7 B8 SB
1 2 3 4 5 6 7 8 18 13
5V OPTION
15 REF IN
DAC-208
14
ANALOG OUTPUT
ANALOG GROUND
DIGITAL GROUND
V−
V+
10
12
9
16
10µF
0.1µF
OUTPUT RANGE
0 – +5V
SHOWN WITH EXTERNAL REFERENCE
V−
V+

APPLICATIONS

AUDIO ATTENUATOR


20kΩ
AUDIO INPUT
10kΩ
OP-27
+5V
20kΩ OFFSET
3V ≤ VREF ≤ 10V
V+
V−
+5V
SB
REF IN
DAC-208
AUDIO OUTPUT
ANALOG GROUND
DIGITAL GROUND
INPUTS
Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8
74LS116
D1 D2 D3 D4 D4 D6 D7 D8
DIGITAL INPUT
RESET
ENABLE

11-BIT VOLTAGE-OUTPUT D/A CONVERTER (10 BITS PLUS SIGN)

DAC-210

FEATURES

- **Complete .... Includes Reference and Op Amp**
- **Bipolar Output .... ±10V**
- **Sign-Magnitude Coding**
- **No bipolar Offset Adjustment Required**
- **10-Bit Linearity Maintained over Full Temperature**
- **Multiplying Operation**
- **Fast .... 1.5µs Settling Time**
- **Monotonicity Guaranteed**
- **Reliable .... 100% Burned-In**
- **Models with MIL-STD-883 Class B Processing Available**
- **Models with Guaranteed ±1 LSB Full Range Symmetry Available**

ORDERING INFORMATION†

	18-PIN HERMETIC DUAL IN-LINE PACKAGE		
TEMPCO	**NL**	**MILITARY**	**COMMERCIAL**
±40	±0.05	DAC210AX* **DAC210ASX*	DAC210EX **DAC210ESX
±60	±0.05	DAC210BX* **DAC210BSX*	DAC210FX **DAC210FSX
±30 Typ	±0.10		DAC210GX

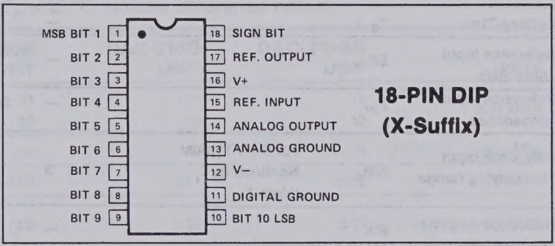
*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

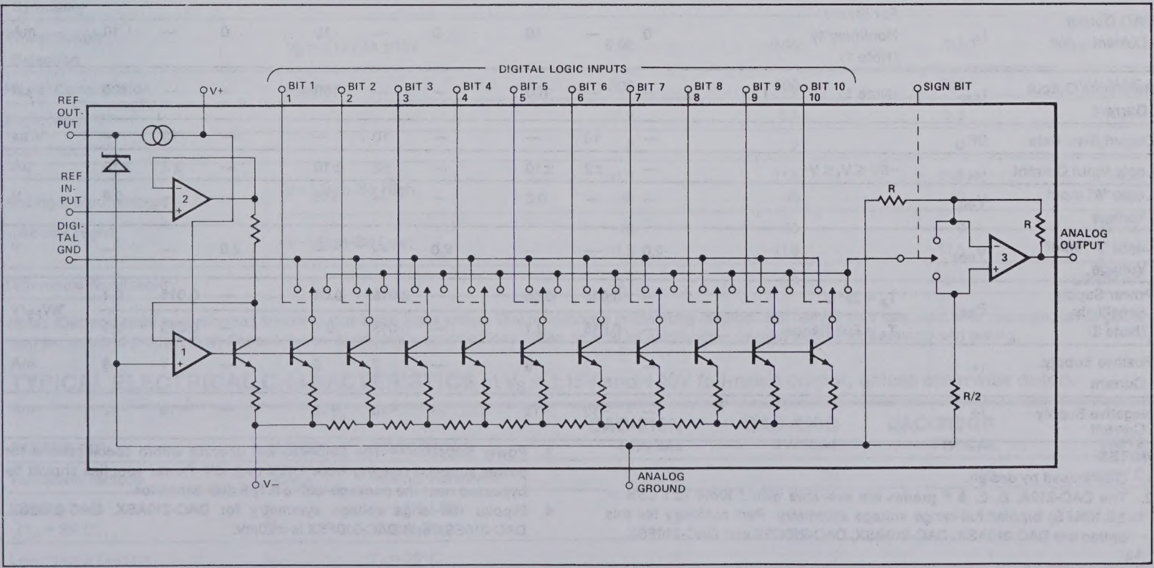
GENERAL DESCRIPTION

The DAC-210 is a complete, monolithic 10-bit plus sign DAC with a ±10V output. A precision voltage reference, a logic controlled polarity switch and output amplifier are included. Linearity, monotonicity, and full-scale temperature coefficient are guaranteed over the full operating temperature range. Ease of application is achieved by the **total** D/A system specs given for nonlinearity and zero-scale offset. System specs eliminate the complex error budget analysis required by less "complete" DACs. Sign-magnitude coding minimizes the "major-carry" zero-code errors inherent in offset coding schemes. Reliability is enhanced by a monolithic design, 100% burn-in, and a hermetic DIP package. MIL-STD-883 Class B processing is available on −55° C to +125° C grades. Also offered are models with a ±1 LSB maximum full-range voltage symmetry error.

PIN CONNECTION


MSB BIT 1 1
BIT 2 2
BIT 3 3
BIT 4 4
BIT 5 5
BIT 6 6
BIT 7 7
BIT 8 8
BIT 9 9
18 SIGN BIT
17 REF. OUTPUT
16 V+
15 REF. INPUT
14 ANALOG OUTPUT
13 ANALOG GROUND
12 V−
11 DIGITAL GROUND
10 BIT 10 LSB
18-PIN DIP
(X-Suffix)

SIMPLIFIED SCHEMATIC


DIGITAL LOGIC INPUTS
BIT 1 1
BIT 2 2
BIT 3 3
BIT 4 4
BIT 5 5
BIT 6 6
BIT 7 7
BIT 8 8
BIT 9 9
BIT 10 10
SIGN BIT
V+
REF OUT-PUT
REF IN-PUT
DIGI-TAL GND
1
2
3
R
R
R/2
ANALOG OUTPUT
V−
ANALOG GROUND

ELECTRICAL CHARACTERISTICS — MILITARY AND COMMERCIAL GRADES at $V_S = \pm 15V$, $-55°C \le T_A \le +125°C$, for A and B grades. $0°C \le T_A \le +70°C$ for E, F and G grades, unless otherwise noted.

			DAC-210A/E			DAC-210B/F			DAC-210G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Resolution		Including Sign	11	—	—	11	—	—	11	—	—	Bits
Monotonicity			10	—	—	10	—	—	9	—	—	Bits
Nonlinearity	NL	$T_A = 25°C$	—	—	±0.05	—	—	±0.05	—	—	±0.10	%FS
		T_A = Full Range	—	—	±0.05	—	—	±0.10	—	—	—	
		T_A = Full Range (A or B only)	—	—	±0.075	—	—	±0.10	—	—	—	
Zero-Scale Offset Voltage	V_{ZS}	$T_A = 25°C$	—	—	±0.05	—	—	±0.1	—	—	—	%FS
		T_A = Full Range	—	—	±0.06	—	—	±.01	—	—	—	
Bipolar Full Range Voltage Symmetry ($V_{FR+} - \mid V_{FR-} \mid$)	V_{FRS}	$T_A = 25°C$ (Note 2)	—	—	40	—	—	60	—	—	80	mV
		T_A = Full Range (Note 4)	—	—	50	—	—	70	—	50	—	
Zero-Scale Voltage Symmetry ($V_{ZS+} - V_{ZS-}$)	V_{ZSS}	T_A = Full Range	—	—	1	—	—	1	—	—	2	mV
Gain Tempco	T_C	Internal Reference	—	—	±40	—	—	±60	—	±30	—	ppm/°C
		External Reference	—	±15	—	—	±30	—	—	±30	—	
Output Voltage Range	$+V_{FR}$		+10.0	—	+11.5	+10.0	—	+11.5	+10.0	—	+11.5	V
	$-V_{FR}$		-11.5	—	-10.0	-11.5	—	-10.0	-11.5	—	-10.0	
Differential Nonlinearity	DNL	$T_A = 25°C$	—	—	±1	—	—	±1	—	±1	—	LSB
Settling Time	T_S		—	1.5	—		1.5	—	—	1.5	—	μs
Reference Input Slew Rate	SR_{REF}		—	1.5	—		1.5	—	—	1.5	—	V/μs
Reference Input Impedance	Z_{IN}		—	200	—	—	200	—	—	200	—	MΩ
Reference Input Multiplying Range	IVR_m	For 0.1% Typical Nonlinearity (Note 1)	3	—	10	3	—	10	3	—	10	V
Reference Amplifier Bandwidth	BW		—	1	—	—	1	—	—	1	—	MHz
Reference Output Voltage	V_{REF}		—	7.6	—	—	7.6	—	—	7.6	—	V
DAC Output Current	I_O	For Stated Nonlinearity (Note 1)	0	—	10	0	—	10	0	—	10	mA
Reference Output Current	I_{REF}	(Note 1)	—	—	100	—	—	100	—	—	100	μA
Output Slew Rate	SR_O		—	10	—	—	10	—	—	10	—	V/μs
Logic Input Current	I_{IN}	$-5V \le V_I \le V+$	—	±2	±10	—	±2	±10	—	±2	±10	μA
Logic "0" Input Voltage	V_{INL}		—	—	0.8	—	—	0.8	—	—	0.8	V
Logic "1" Input Voltage	V_{INH}		2.0	—	—	2.0	—	—	2.0	—	—	V
Power Supply Sensitivity (Note 3)	P_{SS}	$T_A = 25°C$	—	0.015	0.05	—	0.015	0.05	—	0.015	0.1	$\%V_{FS}/V$
		T_A = Full Range	—	0.015	0.1	—	0.015	0.1	—	0.015	0.1	
Positive Supply Current	I+		—	7	9	—	7	9	—	7	9	mA
Negative Supply Current	I+		—	-10	-12	—	-10	-12	—	-10	-12	mA

NOTES:

1. Guaranteed by design.
2. The DAC-210A, B, E, & F grades are available with ±10mV (±1 LSB or ±0.10%FS) bipolar full-range voltage symmetry. Part numbers for this option are DAC-210ASX, DAC-210BSX, DAC-210ESX and DAC-210FSX.
3. Power Supplies — The DAC-210 will operate within specifications for power supplies ranging from ±12V to ±18V. Power supplies should be bypassed near the package with a 0.1μF disk capacitor.
4. Bipolar full-range voltage symmetry for DAC-210ASX, DAC-210BSX, DAC-210ESX and DAC-210FSX is ±20mV.

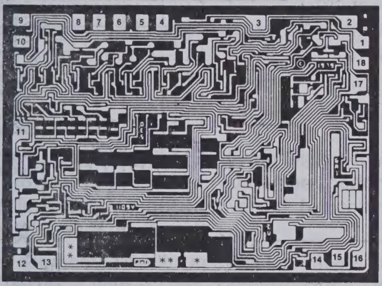
ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	
DAC-210A, B	−55°C to +125°C
DAC-210E, F, G	0°C to +70°C
DICE Junction Temperature (T_j)	−65°C to +150°C
Storage Temperature Range	−65°C to +150°C
V+ Supply to Analog Ground	0 to −18V
Analog Ground to Digital Ground	0 to ±0.5V
Logic Inputs to Digital Ground	−5V to (V+ −0.7V)
Internal Reference Output Current	300μA
Reference Input Voltage	0 to +10V
Internal Power Dissipation	500mW
Derate Above 100°C	10mW/°C
Lead Temperature (Soldering, 60 sec)	300°C
Output Short-Circuit Duration	Indefinite

(Short-circuit may be to ground or either supply.)

NOTE: Absolute ratings apply to both DICE and packaged parts unless otherwise noted.

DICE CHARACTERISTICS



1. B1 (MSB)
2. B2
3. B3
4. B4
5. B5
6. B6
7. B7
8. B8
9. B9
10. B10 (LSB)
11. DIGITAL GROUND
12. V−
13. ANALOG GROUND
14. ANALOG OUTPUT
15. REFERENCE INPUT
16. V+
17. REFERENCE OUTPUT
18. SIGN BIT

NOTE: For 5 volt output option (+5V only) * is connected to analog output. ** is connected to analog ground.

DIE SIZE 0.117 × 0.086 inch, 10,062 sq. mils
(2.972 × 2.18 mm, 5.942 sq. mm)

For additional DICE information refer to Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, +10V full-scale output, $T_A = 25°C$, unless otherwise noted.

PARAMETER	CONDITIONS	DAC-210N LIMIT	DAC-210G LIMIT	DAC-210GR LIMIT	UNITS
Resolution	Bipolar Output	11	11	11	Bits MAX
	Unipolar Output	10	10	10	
Monotonicity		10	9	8	Bits MIN
Nonlinearity		±0.05	±0.1	±0.2	%FS MAX
Zero-Scale Offset	Sign-Bit High, All Other Inputs Low	±5	±10	±10	mV MAX
Zero-Scale Symmetry	±10V Full-Scale	±1	±2	±2	mV MAX
Full-Scale Bipolar Symmetry	±10V Full-Scale	±40	±80	±80	mV MAX
Power Supply Rejection	$V_S = \pm 12V$ to $\pm 18V$	0.05	0.05	0.1	$\%V_{FS}$/V MAX
Power Consumption	$I_{OUT} = 0$	300	300	300	mW MAX
Logic Input "0"		0.8	0.8	0.8	V MAX
Logic Input "1"		2	2	2	V MIN
Analog Output Voltage (All Bits High)	V+ (Sign-Bit High)	11.5	11.5	11.5	V MAX
		10	10	10	V MIN
	V− (Sign-Bit Low)	−10	−10	−10	V MAX
		−11.5	−11.5	−11.5	V MIN
Differential Nonlinearity		±1	±1	±1	LSB MAX

Note: Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

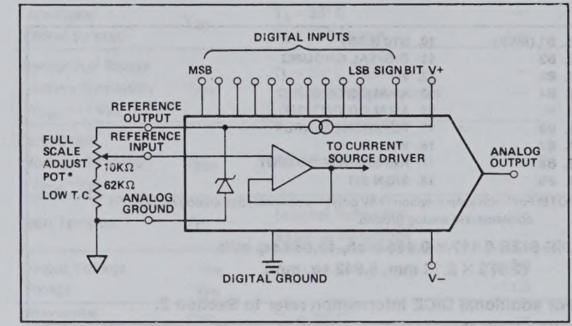
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ and +10V full-scale output, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-210N TYPICAL	DAC-210G TYPICAL	DAC-210GR TYPICAL	UNITS
Full-Scale Tempco	TCV_{FS}	Internal Reference	15	30	30	ppm/°C
Settling Time ($T_A = 25°C$)	t_S	To ±1/2 LSB 10 Volt Step	1.5	1.5	1.5	μs
Logic Input Current	I_{IN}	$T_A = 25°C$	1	1	1	μA

CONNECTION INFORMATION

FULL-SCALE ADJUSTMENT — Full-scale output voltage may be trimmed by use of a potentiometer and series resistor as shown; however, best results will be obtained if a low tempco resistor is used or if pot and resistor tempcos match. Alternatively, a single pot of ≥ 75kΩ may be used.

FULL SCALE ADJUSTMENT CIRCUIT


DIGITAL INPUTS
MSB
LSB
SIGN BIT
V+
REFERENCE OUTPUT
REFERENCE INPUT
FULL SCALE ADJUST POT*
10KΩ
62KΩ
LOW T.C
ANALOG GROUND
TO CURRENT SOURCE DRIVER
ANALOG OUTPUT
DIGITAL GROUND
V−

REFERENCE INPUT BYPASS — Lowest noise and fastest settling operation will be obtained by bypassing the reference input to analog ground with a 0.01μF disk capacitor.

VARIABLE REFERENCES — Operation as a two-quadrant multiplying DAC is achieved by applying an analog input varying between 0 and +10V to the reference input terminal. The DAC output is then the scaled product of this voltage and the digital input.

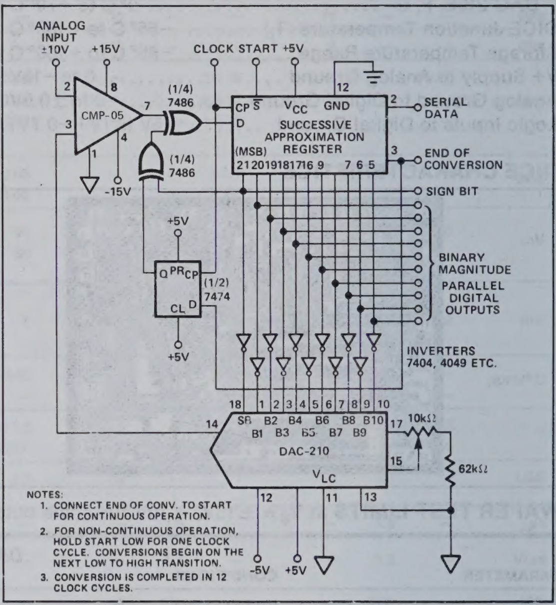
GROUNDING — For optimum noise rejection, separate digital and analog grounds have been brought out. Best results will be obtained if these gounds are connected together at one point only, preferably at the power supply, so that the large digital currents do not flow through the analog ground path.

SIGN — MAGNITUDE CODING TABLE

	SIGN-BIT	MSB LSB
+FULL-SCALE −1 LSB	1	1 1 1 1 1 1 1 1 1 1
+HALF-SCALE	1	1 0 0 0 0 0 0 0 0 0
ZERO-SCALE (+)	1	0 0 0 0 0 0 0 0 0 0
ZERO-SCALE (−)	0	0 0 0 0 0 0 0 0 0 0
−HALF-SCALE	0	1 0 0 0 0 0 0 0 0 0
−FULL-SCALE +1 LSB	0	1 1 1 1 1 1 1 1 1 1

TYPICAL APPLICATIONS

10-BIT SIGN-MAGNITUDE ADC


ANALOG INPUT ±10V
+15V
CLOCK START
+5V
CMP-05
2
8
3
1
4
7
(1/4) 7486
(1/4) 7486
−15V
CP S̄
V_{CC}
GND
12
2
SERIAL DATA
SUCCESSIVE APPROXIMATION REGISTER
(MSB)
21 20 19 18 17 16 9 7 6 5
3
END OF CONVERSION
SIGN BIT
BINARY MAGNITUDE PARALLEL DIGITAL OUTPUTS
+5V
Q PR CP
(1/2) 7474
CL D
+5V
INVERTERS 7404, 4049 ETC.
18 1 2 3 4 5 6 7 8 9 10
14
SB B2 B4 B6 B8 B10
B1 B3 B5 B7 B9
DAC-210
17
10kΩ
15
62kΩ
VLC
12
11
13
−5V
+5V

NOTES:
1. CONNECT END OF CONV. TO START FOR CONTINUOUS OPERATION.
2. FOR NON-CONTINUOUS OPERATION, HOLD START LOW FOR ONE CLOCK CYCLE. CONVERSIONS BEGIN ON THE NEXT LOW TO HIGH TRANSITION.
3. CONVERSION IS COMPLETED IN 12 CLOCK CYCLES.

APPLICATIONS INFORMATION

LOWER RESOLUTION APPLICATION — For applications not requiring full 10-bit resolution, unused logic inputs should be tied to ground.

CAPACITIVE LOADING — The output operational amplifier provides stable operation with capacitive loads up to 100pF.

REFERENCE OUTPUT — For best results, reference output current should not exceed 100μA.

INTERFACING WITH CMOS LOGIC — The DAC-210's logic input stages require about 1μA and are capable of operation with inputs between −5 volts and V+. This wide input voltage range allows direct CMOS Interface with no additional components.

USE WITH EXTERNAL REFERENCES — Positive polarity external reference voltages referred to analog ground may be applied to the reference input terminal to improve full-scale tempco, to provide tracking to other system elements, or to slave a number of DAC-210's to the reference output of any one of them.

12-BIT HIGH-SPEED MULTIPLYING D/A CONVERTER

DAC-312

FEATURES

- **Guaranteed Differential Nonlinearity 0.012%**
- **Nonlinearity 0.025%**
- **Fast Settling Time 250ns**
- **High Compliance .... −5V to +10V**
- **Differential Outputs .... 0 to 4mA**
- **Guaranteed Monotonicity .... 12 Bits**
- **Low Full-Scale Tempco .... 10ppm/°C**
- **Circuit Interface to TTL, CMOS, ECL, PMOS/NMOS**
- **Low Power Consumption 225mW**
- **Industry Standard AM6012 Pinout**

GENERAL DESCRIPTION

The DAC-312 series of 12-bit Multiplying Digital-to-Analog Converters provide high speed with guaranteed performance to 0.012% differential nonlinearity over the full commercial operating temperature range.

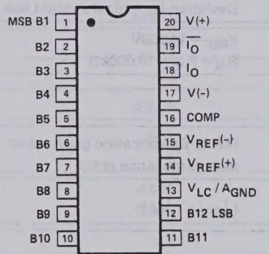
Based on the segmented design approach pioneered by PMI with the COMDAC® line of Data Converters, the DAC-312 combines a 9-bit master D/A Converter with a 3-bit (MSB's) segment generator to form an accurate 12-bit D/A Converter at low cost. This technique guarantees a very uniform step size (up to ±1/2 LSB from the ideal), monotonicity to 12 bits and integral nonlinearity to 0.05% at its differential current outputs. In order to provide the same performance with a 12-bit R-2R ladder design, an integral nonlinearity over temperature of 1/2 LSB (0.012%) would be required.

The 250ns settling time with low glitch energy and low power consumption are achieved by careful attention to the circuit design and stringent process controls. Direct interface with all popular logic families is achieved through the logic threshold terminal.

High compliance and low drift characteristics (as low as 10ppm/°C) are also features of the DAC-312 along with an excellent power supply rejection ratio of ±.001% FS/%ΔV. Operating over a power supply range of +5/−11V to ±18V the device consumes 225mW at the lower supply voltages with an absolute maximum dissipation of 375mW at the higher supply levels.

With their guaranteed specifications, single chip reliability and low cost, the DAC-312 device makes excellent building blocks for A/D Converters, Data Acquisition systems, video display drivers, programmable test equipment and other applications where low power consumption and complete input/output versatility are required.

PIN CONNECTIONS & ORDERING INFORMATION†


MSB B1 1
B2 2
B3 3
B4 4
B5 5
B6 6
B7 7
B8 8
B9 9
B10 10
20 V(+)
19 $\overline{I_O}$
18 I_O
17 V(−)
16 COMP
15 $V_{REF}(-)$
14 $V_{REF}(+)$
13 V_{LC}/A_{GND}
12 B12 LSB
11 B11

20-PIN HERMETIC DUAL-IN-LINE PACKAGE (R-Suffix)

MODEL	TEMP RANGE	DNL
DAC312BR	−55°C/ +125°C	±1 LSB
DAC312FR	0°C/+70°C	±1 LSB
DAC312ER	0°C/+70°C	±1/2 LSB

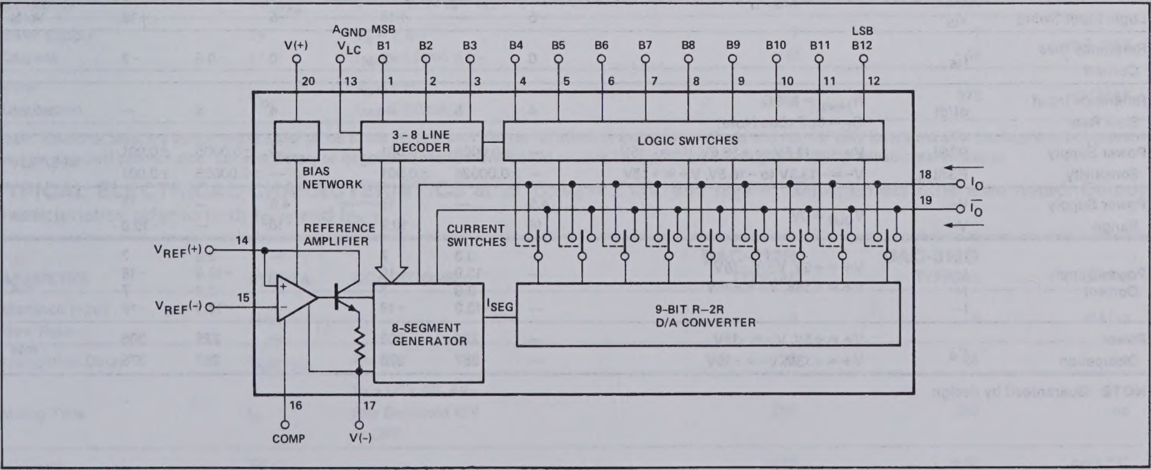
Military Temperature Range Devices
With MIL-STD-883 Class B Processing

MODEL	TEMP	DNL
DAC312BR/883	−55°C/+125°C	±1 LSB

*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

FUNCTIONAL DIAGRAM


V(+)
A_{GND} V_{LC}
MSB B1
B2
B3
B4
B5
B6
B7
B8
B9
B10
B11
LSB B12
20
13
1
2
3
4
5
6
7
8
9
10
11
12
BIAS NETWORK
3 - 8 LINE DECODER
LOGIC SWITCHES
18 I_O
19 $\overline{I_O}$
$V_{REF}(+)$ 14
$V_{REF}(-)$ 15
REFERENCE AMPLIFIER
CURRENT SWITCHES
I_{SEG}
8-SEGMENT GENERATOR
9-BIT R−2R D/A CONVERTER
16 COMP
17 V(−)

Manufactured under one or more of the following patents: 4,055,773; 4,056,740; 4,092,639

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
DAC-312B .... −55°C to +125°C
DAC-312E,DAC312F .... 0°C to +70°C
DICE Junction Temperature .... −65°C to +150°C
Storage Temperature (T_j) .... −65°C to +125°C
Lead Temperature (Soldering, 60 sec) .... 300°C

Power Supply Voltage .... ±18V
Logic Inputs .... −5V to +18V
Analog Current Outputs .... −8V to +12V
Reference Inputs V_{14}, V_{15} .... V− to V+
Reference Input Differential Voltage (V_{14}, to V_{15}) .... ±18V
Reference Input Current (I_{14}) 1.25mA

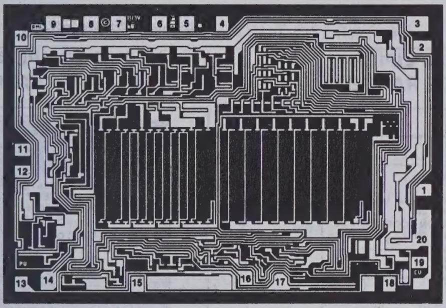
NOTE: Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $I_{REF} = 1.0mA$, $-55°C \le T_A \le 125°C$ for DAC-312B, $0°C \le T_A \le 70°C$ for DAC-312E, DAC-312F, unless otherwise noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

			DAC-312E			DAC-312B/F			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Resolution			12	—	—	12	—	—	Bits
Monotonicity			12	—	—	12	—	—	Bits
Differential Nonlinearity	D.N.L.	Deviation from ideal step size	— —	— —	±0.0125 ±0.5	— —	— —	±0.0250 ±1	%FS LSB
Nonlinearity	N.L.	Deviation from ideal straight line	—	—	±0.05	—	—	±0.05	%FS
Full-Scale Current	I_{FS}	$V_{REF} = 10.000V$ $R_{14} = R_{15} = 10.000k\Omega$	3.967	3.999	4.031	3.935	3.999	4.063	mA
Full-Scale Tempco	TCI_{FS}		— —	±10 ±0.001	±30 ±0.003	— —	±10 ±0.001	±40 ±0.004	ppm/°C %FS/°C
Output Voltage Compliance	V_{OC}	D.N.L. Specification guaranteed over compliance range	−5	—	+10	−5	—	+10	Volts
Full-Scale Symmetry	I_{FSS}	$\lvert I_{FS} \rvert - \lvert \overline{I_{FS}} \rvert$	—	±0.4	±1	—	±0.4	±2	μA
Zero-Scale Current	I_{ZS}		—	—	0.10	—	—	0.10	μA
Settling Time	t_S	To ±1/2 LSB, all bits switched ON or OFF (See Note)	—	250	500	—	250	500	ns
Propagation Delay — all bits	t_{PLH} t_{PHL}	All bits switched 50% point logic swing to 50% point output (See Note)	—	25	50	—	25	50	ns
Output Resistance	R_O		—	>10	—	—	>10	—	MΩ
Output Capacitance	C_{OUT}		—	20	—	—	20	—	pF
Logic Input Levels "0"	V_{IL}	$V_{LC} = GND$	—	—	0.8	—	—	0.8	Volts
Logic Input Levels "1"	V_{IH}	$V_{LC} = GND$	2	—	—	2	—	—	Volts
Logic Input Current	I_{IN}	$V_{IN} = -5$ to $+18V$	—	—	40	—	—	40	μA
Logic Input Swing	V_{IS}		−5	—	+18	−5	—	+18	Volts
Reference Bias Current	I_{15}		0	−0.5	−2	0	−0.5	−2	μA
Reference Input Slew Rate	dI/dt	$R_{14(eq)} = 800\Omega$ $C_C = 0pF$ (See Note)	4	8	—	4	8	—	mA/μs
Power Supply Sensitivity	$PSSI_{FS+}$ $PSSI_{FS-}$	$V+ = +13.5V$ to $+16.5V$, $V- = -15V$ $V- = -13.5V$ to $-16.5V$, $V+ = +15V$	— —	±0.0005 ±0.00025	±0.001 ±0.001	— —	±0.0005 ±0.00025	±0.001 ±0.001	%FS/%ΔV
Power Supply Range	V+ V−	$V_{OUT} = 0V$	4.5 18	— —	18 −10.8	4.5 18	— —	18 −10.8	Volts
Power Supply Current	I+ I− I+ I−	$V+ = +5V$, $V- = -15V$ $V+ = +15V$, $V- = -15V$	— — — —	3.3 −13.9 3.9 −13.9	7 −18 7 −18	— — — —	3.3 −13.9 3.9 −13.9	7 −18 7 −18	mA
Power Dissipation	P_d	$V+ = +5V$, $V- = -15V$ $V+ = +15V$, $V- = -15V$	— —	225 267	305 375	— —	225 267	305 375	mW

NOTE: Guaranteed by design.

DICE CHARACTERISTICS



1. B1 (MSB)
2. B2
3. B3
4. B4
5. B5
6. B6
7. B7
8. B8
9. B9
10. B10
11. B11
12. B12 (LSB)
13. V_{LC}/A_{GND}
14. V_{REF} (+)
15. V_{REF} (–)
16. COMP
17. V–
18. I_O
19. $\overline{I_O}$
20. V+

For additional DICE information refer to Section 2.

DIE SIZE 0.140 × 0.095 inch, 13,300 sq. mils (3.56 × 2.41 mm, 8.58 sq. mm)

WAFER TEST LIMITS at $V_S = \pm 15V$, $I_{REF} = 1.0mA$, $T_A = 25°C$, unless otherwise noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

PARAMETER	SYMBOL	CONDITIONS	DAC-312N LIMIT	DAC-312G LIMIT	UNITS
Resolution			12	12	Bits MIN
Monotonicity			12	12	Bits MIN
Nonlinearity			±0.05	±0.05	%FS MAX
Output Voltage Compliance	V_{OC}	Full-Scale Current Change <1/2 LSB	+10 –5	+10 –5	V MAX V MIN
Full-Scale Current		$V_{REF} = 10.000V$ $R_{14}, R_{15} = 10.000k\Omega$	4.031 3.967	4.063 3.935	mA MAX mA MIN
Full-Scale Symmetry	I_{FSS}		±1	±2	μA MAX
Zero-Scale Current	I_{ZS}		0.1	0.1	μA MAX
Differential Nonlinearity	DNL	Deviation from ideal step size	±0.012 ±1/2	±0.025 ±1	%FS MAX Bits (LSB) MAX
Logic Input Levels "0"	V_{IL}	$V_{LC} = GND$	0.8	0.8	V MAX
Logic Input Levels "1"	V_{IH}	$V_{LC} = GND$	2	2	V MIN
Logic Input Swing	V_{IS}		+18 –5	+18 –5	V MAX V MIN
Reference Bias Current	I_{15}		–2	–2	μA MAX
Power Supply Sensitivity	$PSSI_{FS+}$ $PSSI_{FS-}$	V+ = +13.5V to +16.5V, V– = –15V V– = –13.5V to –16.5V, V+ = +15V	±0.001 ±0.001	±0.001 ±0.001	%/% MAX
Power Supply Current	I+ I–	$V_S = \pm 15V$ $I_{REF} \leq 1.0mA$	7 –18	7 –18	mA MAX
Power Dissipation	P_D	$V_S = +15V$ $I_{REF} \leq 1.0mA$	375	375	mW MAX

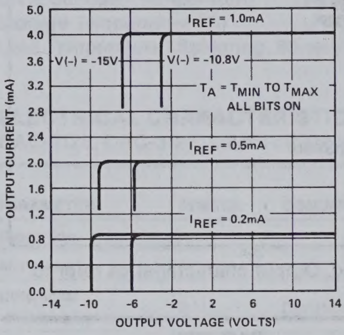
Note: Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at 25°C; $V_S = \pm 15V$, and $I_{REF} = 1.0mA$, unless otherwise noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

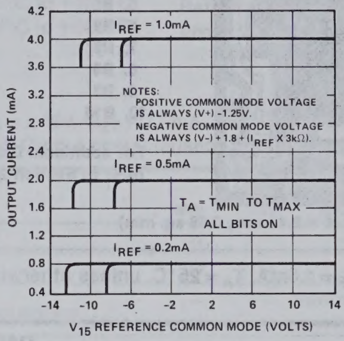
PARAMETER	SYMBOL	CONDITIONS	DAC-312N TYPICAL	DAC-312G TYPICAL	UNITS
Reference Input Slew Rate	dI/dt		8	8	mA/μs
Propagation Delay	t_{PLH}, t_{PHL}	Any Bit	25	25	ns
Settling Time	t_S	To ±1/2 LSB, All Bits Switched ON or OFF.	250	250	ns
Full-Scale	TC_{IFS}		±10	±10	ppm/°C

TYPICAL PERFORMANCE CHARACTERISTICS

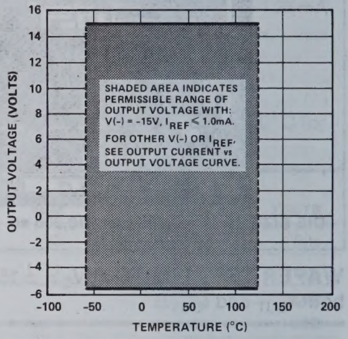
OUTPUT CURRENT vs OUTPUT VOLTAGE (OUTPUT VOLTAGE COMPLIANCE)



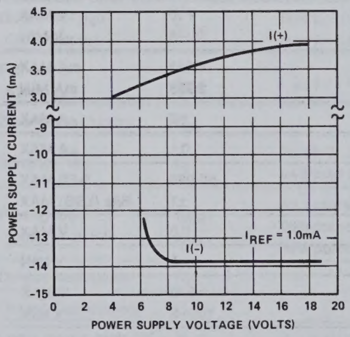
REFERENCE AMPLIFIER COMMON-MODE RANGE



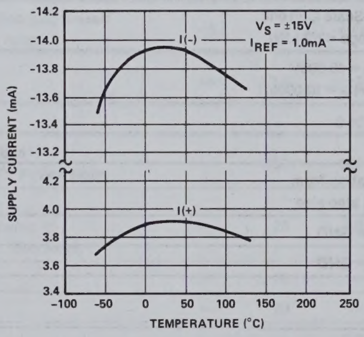
OUTPUT COMPLIANCE vs TEMPERATURE



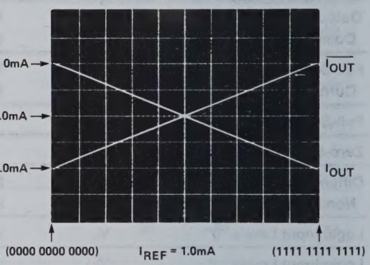
POWER SUPPLY CURRENT vs POWER SUPPLY VOLTAGE



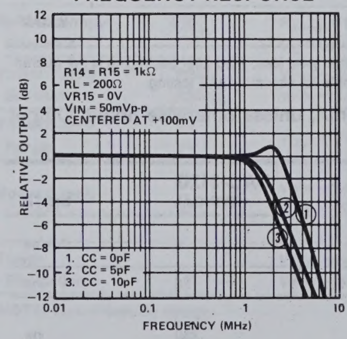
POWER SUPPLY CURRENT vs TEMPERATURE



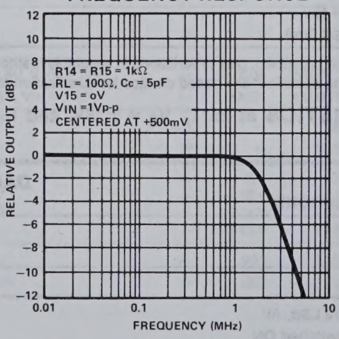
TRUE AND COMPLEMENTARY OUTPUT OPERATION



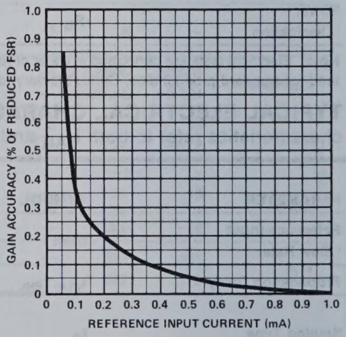
REFERENCE AMPLIFIER SMALL-SIGNAL FREQUENCY RESPONSE



REFERENCE AMPLIFIER LARGE-SIGNAL FREQUENCY RESPONSE

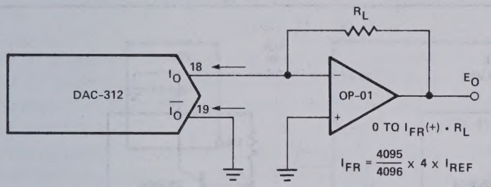


GAIN ACCURACY vs REFERENCE CURRENT



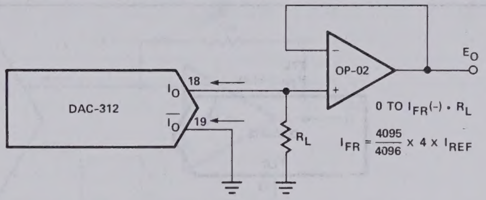
BASIC CONNECTIONS

NEGATIVE LOW IMPEDANCE OUTPUT OPERATION


R_L
DAC-312
I_O
18
$\overline{I_O}$
19
OP-01
E_O
0 TO I_FR(+) • R_L
I_FR = 4095/4096 x 4 x I_REF

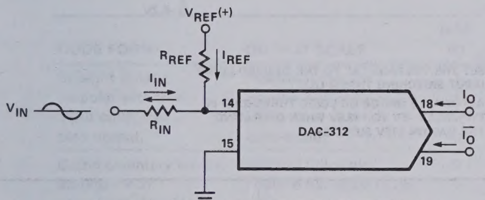
FOR COMPLEMENTARY OUTPUT (OPERATION AS A NEGATIVE LOGIC DAC), CONNECT INVERTING INPUT OF OP-AMP TO $\overline{I_O}$ (PIN 19); CONNECT I_O (PIN 18) TO GROUND.

POSITIVE LOW IMPEDANCE OUTPUT OPERATION

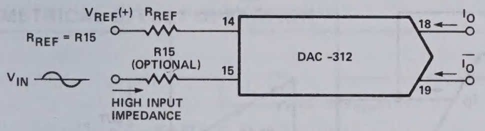

DAC-312
I_O
18
$\overline{I_O}$
19
OP-02
E_O
R_L
0 TO I_FR(-) • R_L
I_FR = 4095/4096 x 4 x I_REF

FOR COMPLEMENTARY OUTPUT (OPERATION AS A NEGATIVE LOGIC DAC), CONNECT NON-INVERTING INPUT OF OP-AMP TO $\overline{I_O}$ (PIN 19); CONNECT I_O (PIN 18) TO GROUND.

ACCOMMODATING BIPOLAR REFERENCES

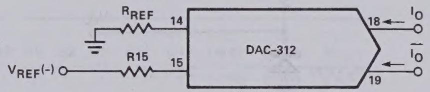

V_REF(+)
R_REF
I_REF
I_IN
V_IN
R_IN
14
15
DAC-312
18
I_O
$\overline{I_O}$
19

$I_{REF} \geq$ PEAK NEGATIVE SWING OF I_{IN}


V_REF(+)
R_REF
R_REF = R15
14
R15 (OPTIONAL)
15
V_IN
HIGH INPUT IMPEDANCE
DAC -312
18
I_O
$\overline{I_O}$
19

$V_{REF}(+)$ MUST BE ABOVE PEAK POSITIVE SWING OF V_{IN}

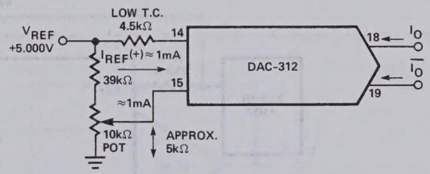
BASIC NEGATIVE REFERENCE OPERATION


R_REF
14
R15
15
V_REF(-)
DAC-312
18
I_O
$\overline{I_O}$
19

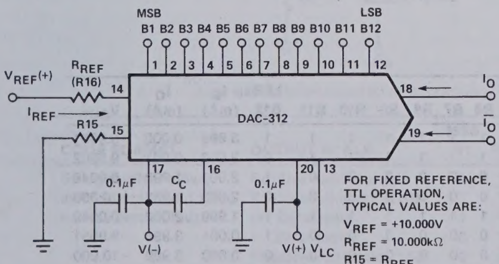
$$I_{FS} \approx \frac{V_{REF}(-)}{R_{REF}} \times 4$$

NOTE: R_{REF} SETS I_{FS}; R15 IS FOR A BIAS CURRENT CANCELLATION.

RECOMMENDED FULL-SCALE ADJUSTMENT CIRCUIT


V_REF +5.000V
LOW T.C. 4.5kΩ
14
I_REF(+) ≈ 1mA
39kΩ
15
≈1mA
10kΩ POT
APPROX. 5kΩ
DAC-312
18
I_O
$\overline{I_O}$
19

BASIC POSITIVE REFERENCE OPERATION


MSB
LSB
B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12
1 2 3 4 5 6 7 8 9 10 11 12
V_REF(+)
R_REF (R16)
14
I_REF
R15
15
DAC-312
18
I_O
$\overline{I_O}$
19
17
16
C_C
0.1μF
0.1μF
V(-)
20
13
V(+)
V_LC

FOR FIXED REFERENCE, TTL OPERATION, TYPICAL VALUES ARE:

V_{REF} = +10.000V

R_{REF} = 10.000kΩ

R15 = R_{REF}

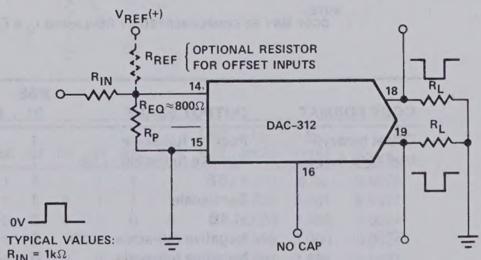
C_C = 0.01μF

V_{LC} = 0V (GROUND)

$$I_{FR} = \frac{V_{REF}(+)}{R_{REF}} \times \frac{4095}{4096} \times 4$$

$I_O + \overline{I_O} = I_{FR}$ FOR ALL LOGIC STATES.

PULSED REFERENCE OPERATION


V_REF(+)
R_REF
OPTIONAL RESISTOR FOR OFFSET INPUTS
R_IN
14
R_EQ ≈ 800Ω
R_P
15
DAC-312
18
19
R_L
R_L
16
NO CAP
0V

TYPICAL VALUES:

R_{IN} = 1kΩ

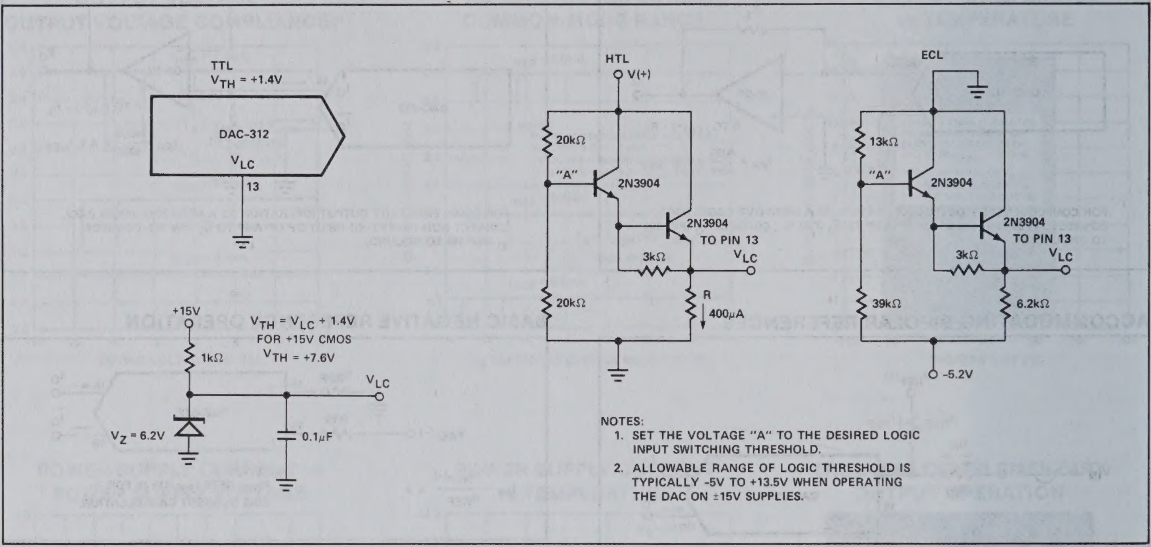
R_P = 4kΩ

$V_{IN}(+)$ = 1V

$$R_{EQ} = \frac{1}{\frac{1}{R_{IN}} + \frac{1}{R_P} + \frac{1}{R_{REF}}}$$

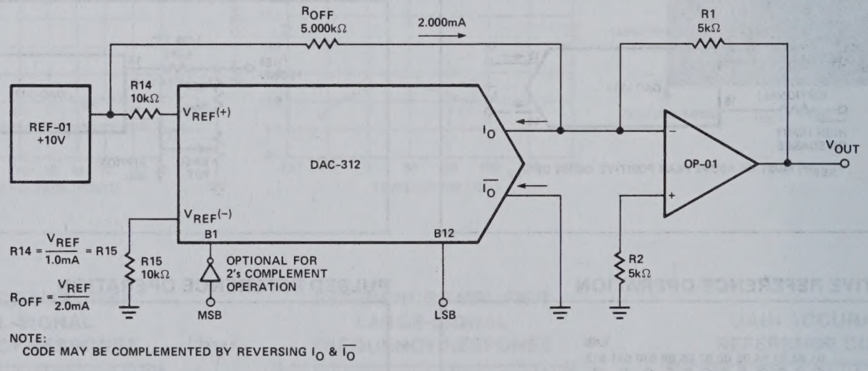
BASIC CONNECTIONS

INTERFACING WITH VARIOUS LOGIC FAMILIES


TTL
V_{TH} = +1.4V
DAC-312
V_{LC}
13
+15V
1kΩ
V_Z = 6.2V
0.1µF
V_{LC}
V_{TH} = V_{LC} + 1.4V
FOR +15V CMOS
V_{TH} = +7.6V
HTL
V(+)
20kΩ
"A"
2N3904
2N3904
TO PIN 13
V_{LC}
3kΩ
20kΩ
R
400µA
ECL
13kΩ
"A"
2N3904
2N3904
TO PIN 13
V_{LC}
3kΩ
39kΩ
6.2kΩ
-5.2V

NOTES:
1. SET THE VOLTAGE "A" TO THE DESIRED LOGIC INPUT SWITCHING THRESHOLD.
2. ALLOWABLE RANGE OF LOGIC THRESHOLD IS TYPICALLY -5V TO +13.5V WHEN OPERATING THE DAC ON ±15V SUPPLIES.

BIPOLAR OFFSET (TRUE ZERO)


R_{OFF}
5.000kΩ
2.000mA
R1
5kΩ
REF-01
+10V
R14
10kΩ
$V_{REF}(+)$
DAC-312
I_O
$\overline{I_O}$
OP-01
V_{OUT}
$V_{REF}(-)$
B1
B12
R15
10kΩ
OPTIONAL FOR
2's COMPLEMENT
OPERATION
MSB
LSB
R2
5kΩ

$R14 = \frac{V_{REF}}{1.0mA} = R15$

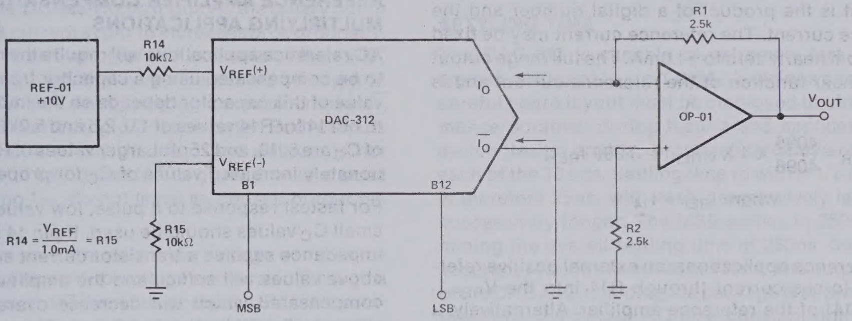
$R_{OFF} = \frac{V_{REF}}{2.0mA}$

NOTE:
CODE MAY BE COMPLEMENTED BY REVERSING I_O & $\overline{I_O}$

CODE FORMAT	OUTPUT SCALE	MSB B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	LSB B12	I_O (mA)	$\overline{I_O}$ (mA)	V_{OUT}
Offset binary; true zero output.	Positive full-scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9951
	Positive full-scale −LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9902
	+LSB	1	0	0	0	0	0	0	0	0	0	0	1	2.001	1.998	0.0049
	Zero-scale	1	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.000
	−LSB	0	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	−0.0049
	Negative full-scale +LSB	0	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	−9.9951
	Negative full-scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	−10.000
2's complement; true zero output MSB complemented (Need inverter at B1).	Positive full-scale	0	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9951
	Positive full-scale −LSB	0	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9902
	+1 LSB	0	0	0	0	0	0	0	0	0	0	0	1	2.001	1.998	0.0049
	Zero-scale	0	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.000
	−1 LSB	1	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	−0.0049
	Negative full-scale +LSB	1	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	−9.9951
	Negative full-scale	1	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	−10.000

BASIC CONNECTIONS

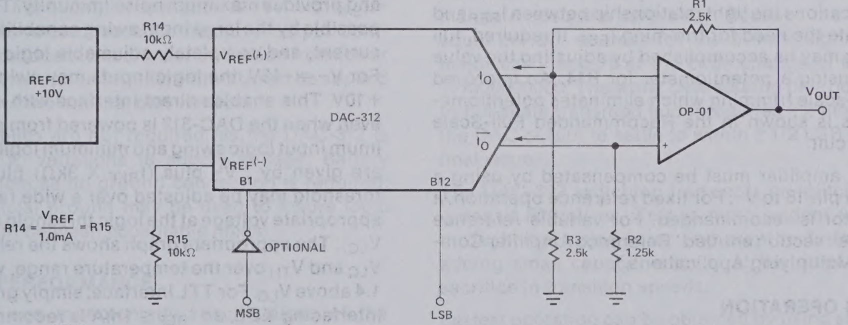
BASIC UNIPOLAR OPERATION


REF-01
+10V
R14
10kΩ
$V_{REF}(+)$
DAC-312
$V_{REF}(-)$
B1
B12
I_O
$\overline{I_O}$
R1
2.5k
OP-01
V_{OUT}
R2
2.5k
$R14 = \frac{V_{REF}}{1.0mA} = R15$
R15
10kΩ
MSB
LSB

NOTE:
CODE MAY BE COMPLEMENTED BY REVERSING I_O & $\overline{I_O}$

CODE FORMAT	OUTPUT SCALE	MSB B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	LSB B12	I_O (mA)	I_O (mA)	V_{OUT}
Straight Binary;	Positive full-scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9976
unipolar with true	Positive full-Scale −LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9951
input code, true	LSB	0	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	0.0024
zero output.	Zero-scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	0.0000
Complementary binary;	Positive full-scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	9.9976
unipolar with	Positive full-scale −LSB	0	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	9.9951
complementary input	LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	0.0024
code, true zero output.	Zero-scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	0.0000

SYMMETRICAL OFFSET OPERATION


REF-01
+10V
R14
10kΩ
$V_{REF}(+)$
DAC-312
$V_{REF}(-)$
B1
B12
I_O
$\overline{I_O}$
R1
2.5k
OP-01
V_{OUT}
$R14 = \frac{V_{REF}}{1.0mA} = R15$
R15
10kΩ
OPTIONAL
R3
2.5k
R2
1.25k
MSB
LSB

NOTE:
CODE MAY BE COMPLEMENTED BY REVERSING I_O & $\overline{I_O}$

CODE FORMAT	OUTPUT SCALE	MSB B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	LSB B12	I_O (mA)	I_O (mA)	V_{OUT}
Straight offset binary;	Positive full-scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.00	9.9976
symmetrical about zero,	Positive full-scale −LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9927
no true zero output.	(+) Zero-scale	1	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.0024
	(−) Zero-scale	0	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	−0.0024
	Negative full-scale −LSB	0	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	−9.9927
	Negative full-scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	−9.9976
1's complement;	Positive full-scale	0	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9976
symmetrical about zero,	Positive full-scale −LSB	0	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9927
no true zero output.	(+) Zero-scale	0	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.0024
MSB complemented	(−) Zero-scale	1	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	−0.0024
(need inverter at B1).	Negative full-scale −LSB	1	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	−9.9927
	Negative full-scale	1	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	−9.9976

APPLICATIONS INFORMATION

REFERENCE AMPLIFIER SETUP

The DAC-312 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to +1.0mA. The full range output current is a linear function of the reference current and is given by:

$$I_{FR} = \frac{4095}{4096} \times 4 \times (I_{REF}) = 3.999\ I_{REF},$$

$$\text{where } I_{REF} = I_{14}$$

In positive reference applications, an external positive reference voltage forces current through R14 into the $V_{REF(+)}$ terminal (pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to $V_{REF(-)}$ at pin 15. Reference current flows from ground through R14 into $V_{REF(+)}$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin 15. The voltage at pin 14 is equal to and tracks the voltage at pin 15 due to the high gain of the internal reference amplifier. R15 (nominally equal to R14) is used to cancel bias current errors.

Bipolar references may be accomodated by offsetting V_{REF} or pin 15. The negative common-mode range of the reference amplifier is given by: $V_{CM}- = V-$ plus (I_{REF} X 3kΩ) plus 1.23V. The positive common-mode range is V+ less 1.8V.

When a DC reference is used, a reference bypass capacitor is recommended. A 5.0V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R14 should be split into two resistors with the junction bypassed to ground with a 0.1μF capacitor.

For most applications the tight relationship between I_{REF} and I_{FS} will eliminate the need for trimming I_{REF}. If required, full scale trimming may be accomplished by adjusting the value of R14, or by using a potentiometer for R14. An improved method of full-scale trimming which eliminates potentiometer T.C. effects is shown in the Recommended Full-Scale Adjustment circuit.

The reference amplifier must be compensated by using a capacitor from pin 16 to V–. For fixed reference operation, a 0.01μF capacitor is recommended. For variable reference applications, see section entitled "Reference Amplifier Compensation for Multiplying Applications."

MULTIPLYING OPERATION

The DAC-312 provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 1mA to 1μA. Monotonic operation is maintained over a typical range of I_{REF} from 100μA to 1.0mA. Although some degradation of gain accuracy will be realized at reduced values of I_{REF}. (See Gain Accuracy vs Reference Current).

REFERENCE AMPLIFIER COMPENSATION FOR MULTIPLYING APPLICATIONS

AC reference applications will require the reference amplifier to be compensated using a capacitor from pin 16 to V–. The value of this capacitor depends on the impedance presented to pin 14 for R14 values of 1.0, 2.5 and 5.0kΩ, minimum values of C_C are 5, 10, and 25pF. Larger values of R14 require proportionately increased values of C_C for proper phase margin.

For fastest response to a pulse, low values of R14 enabling small C_C values should be used. If pin 14 is driven by a high impedance such as a transistor current source, none of the above values will suffice and the amplifier must be heavily compensated which will decrease overall bandwidth and slew rate. For R14 = 1kΩ and C_C = 5pF, the reference amplifier slews at 4mA/μs enabling a transition from $I_{REF} = 0$ to $I_{REF} =$ 1mA in 250ns.

Operation with pulse inputs to the reference amplifier may be accommodated by an alternate compensation scheme. This technique provides lowest full-scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff (I_{REF} = 0) condition. Full-scale transition (0 to 1mA) occurs in 62.5ns when the equivalent impedance at pin 14 is 800Ω and C_C = 0. This yields a reference slew rate of 8mA/μs which is relatively independent of R_{IN} and V_{IN} values.

LOGIC INPUTS

The DAC-312 design incorporates a unique logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 40μA logic input current, and completely adjustable logic threshold voltage. For V– = –15V, the logic inputs may swing between –5 and +10V. This enables direct interface with +15V CMOS logic, even when the DAC-312 is powered from a +5V supply. Minimum input logic swing and minimum logic threshold voltage are given by : V– plus (I_{REF} X 3kΩ) plus 1.8V. The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control pin (pin 13, V_{LC}). The appropriate graph shows the relationship between V_{LC} and V_{TH} over the temperature range, with V_{TH} nominally 1.4 above V_{LC}. For TTL interface, simply ground pin 13. When interfacing ECL, an $I_{REF} \leq$ 1mA is recommended. For interfacing other logic families, see block titled "Interfacing With Various Logic Families". For general setup of the logic control circuit, it should be noted that pin 13 will sink 7mA typical; external circuitry should be designed to accommodate this current.

ANALOG OUTPUT CURRENTS

Both true and complemented output sink currents are provided where $I_O + \overline{I_O} = I_{FR}$. Current appears at the "true" output when a "1" is applied to each logic input. As the binary count increases, the sink current at pin 18 increases proportionally, in the fashion of a "positive logic" D/A converter. When a "0" is applied to any input bit, that current is turned off at pin 18 and turned on at pin 19. A decreasing logic count increases $\overline{I_O}$ as in a negative or inverted logic D/A converter. Both outputs may be used simultaneously. If one of the outputs is not required it must still be connected to ground or to a point capable of sourcing I_{FR}; do not leave an unused output pin open.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 25V above V− and is independent of the positive supply. Negative compliance is +10V above V−.

The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection and in other balanced applications such as driving center-tapped coils and transformers.

POWER SUPPLIES

The DAC-312 operates over a wide range of power supply voltages from a total supply of 20V to 36V. When operating with V− supplies of −10V or less, $I_{REF} \leq 1\text{mA}$ is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common-mode range, negative logic input range, and negative logic threshold range; consult the various figures for guidance. For example, operation at −9V with $I_{REF} = 1\text{mA}$ is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible, however at least 8V total must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the DAC-312 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required; however, an artificial ground may be used to insure logic swings, etc. remain between acceptable limits.

TEMPERATURE PERFORMANCE

The nonlinearity and monotonicity specifications of the DAC-312 are guaranteed to apply over the entire rated operating temperature range. Full-Scale output current drift is tight, typically ±10ppm/°C, with zero-scale output current and drift essentially negligible compared to 1/2 LSB.

The temperature coefficient of the reference resistor R14 should match and track that of the output resistor for minimum overall full-scale drift. Settling times of the DAC-312 decrease approximately 10% at −55°C; at +125°C an increase of about 15% is typical.

SETTLING TIME

The DAC-312 is capable of extremely fast settling times, typically 250ns at $I_{REF} = 1.0\text{mA}$. Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The logic switch design enables propagation delays of only 25ns for each of the 12 bits. Settling time to within 1/2 LSB of the LSB is therefore 25ns, with each progressively larger bit taking successively longer. The MSB settles in 250ns, thus determining the overall settling time of 250ns. Settling to 10-bit accuracy requires about 90 to 130ns. The output capacitance of the DAC-312 including the package is approximately 20pF; therefore, the output RC time constant dominates settling time if $R_L > 500\Omega$

Settling time and propagation delay are relatively insensitive to logic input amplitude and rise and fall times, due to the high gain of the logic switches. Settling time also remains essentially constant for I_{REF} values down to 0.5mA, with gradual increases for lower I_{REF} values lies in the ability to attain a given output level with lower load resistors, thus reducing the output RC time constant.

Measurement of the settling time requires the ability to accurately resolve ±1/2 LSB of current, which is ±500nA for 4mA FSR. In order to assure the measurement is of the actual settling time and not the R.C. time of the output network, the resistive termination on the output of the DAC must be 500 ohms or less. This does, however, place certain limitations on the testing apparatus. At I_{REF} values of less than 0.5mA, it is difficult to prevent RC damping of the output and maintain adequate sensitivity. Because the DAC-312 has 8 equal current sources for the 3 most significant bits, the major carry occurs at the code change of 000111111111 to 111000000000. The worst case settling time occurs at the zero to full-scale transition and it requires 9.2 time constants for the DAC output to settle to within ±1/2 LSB (0.0125%) of its final value.

The DAC-312 switching transients or "glitches" are on the order of 500mV-ns. This is most evident when switching through the major carry and may be further reduced by adding small capacitive loads at the output with a minor sacrifice in transition speeds.

Fastest operation can be obtained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference, and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is independent of input logic states; 0.1µF capacitors at the supply pins provide full transient protection.

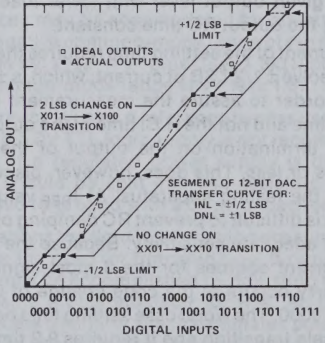
DIFFERENTIAL vs INTEGRAL NONLINEARITY

Integral nonlinearity, for the purposes of the discussion, refers to the "straightness" of the line drawn through the individual response points of a data converter. Differential nonlinearity, on the other hand, refers to the deviation of the spacing of the adjacent points from a 1 LSB ideal spacing. Both may be expressed as either a percentge of full-scale output or as fractional LSBs or both. The following figures define the manner in which these parameters are specified. The left figure shows a portion of the transfer curve of a DAC with 1/2 LSB INL and the (implied) DNL spec of 1 LSB. Below this is a graphic representation of the way this would appear on a CRT, for example, if the D/A Converter output were to be applied to the Y input of a CRT as shown in the application schematic titled "CRT Display Driver". On the right is a portion of the transfer curve of a DAC specified for 2 LSB INL with 1/2 LSB DNL specified and the graphic display below it.

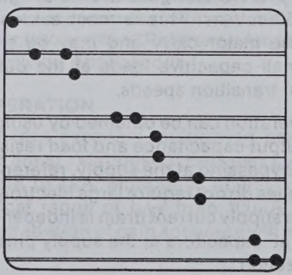
One of the characteristics of an R-2R DAC in standard form is that any transition which causes a zero LSB change (i.e. the same output for two different codes) will exhibit the same output each time that transition occurs. The same holds true for transitions causing a 2 LSB change. These two problem transitions are allowable for the standard definition of monotonicity and also allow the device to be specified very tightly for INL. The major problem arising from this error type is in A/D converter implementations. Inputs producing the same output are now represented by ambiguous output codes for an identical input. Also, 2 LSB gaps can cause large errors at those input levels (assuming 1/2 LSB quantizing levels). It can be seen from the two figures that the DNL specified D/A converter will yield much finer grained data than the INL specified part, thus improving the ability of the A/D to resolve changes in the analog input.

DIFFERENTIAL LINEARITY COMPARISON

D/A CONVERTER WITH ±1/2 LSB INL, ±1 LSB DNL

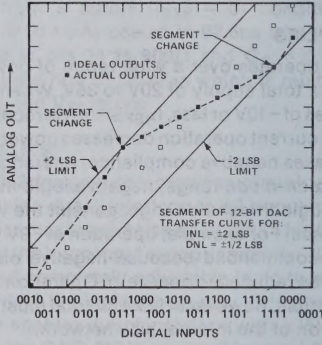


VIDEO DEFLECTION BY DAC's

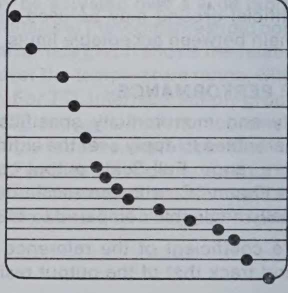


ENLARGED "POSITIONAL" OUTPUTS

D/A CONVERTER WITH ±2 LSB INL, ±1/2 LSB DNL



VIDEO DEFLECTION BY DAC's



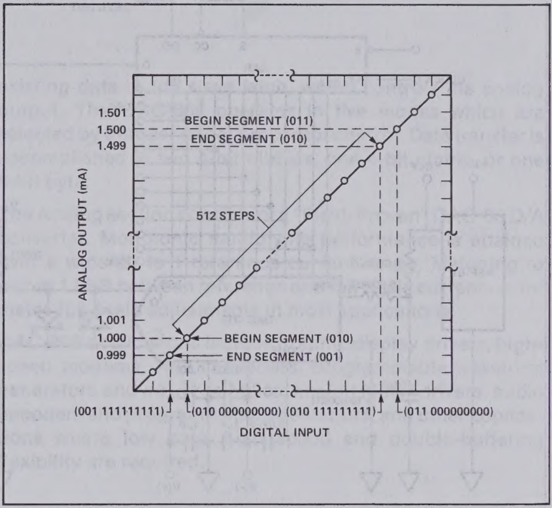
ENLARGED "POSITIONAL" OUTPUTS

DESCRIPTION OF OPERATION

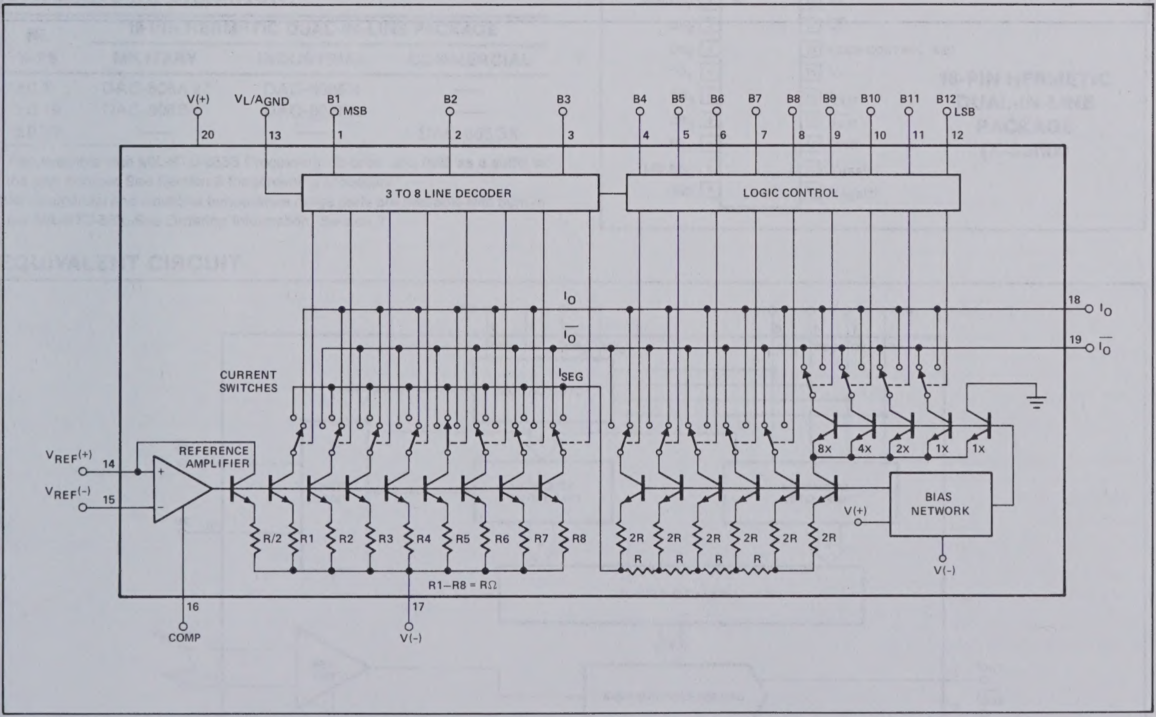
The DAC-312 is divided into two major sections, an 8-segment generator and a 9-bit master/slave D/A Converter. In operation the device performs as follows (See Simplified Schematic):

The three most significant bits (MSB's) are inputs to a 3-to-8 line decoder. The selected resistor (R5 in the figure) is connected to the master/slave 9-bit D/A Converter. All lower order resistors (R1 through R4) are summed into the I_O line, while all higher order resistors (R6 through R8) are summed into the $\overline{I_O}$ line. The R5 current supplies 512 steps of current (0 to 0.499mA for a 1mA reference current) which are also summed into the I_O or $\overline{I_O}$ lines depending on the bits selected. In the figure, the code selected is: 100 110000000. Therefore, 2mA (4 X 0.5mA/segment) + 0.375mA (from master/slave D/A Converter) are summed into I_O giving an I_O of 2.375mA. $\overline{I_O}$ has a current of 1.625mA with this code. As the three MSB's are incremented, each successively higher code adds 0.5mA to I_O and subtracts 0.5mA from $\overline{I_O}$, with the selected resistor feeding its current to the master/slave D/A Converter; thus each increment of the 3 MSB's allows the current in the 9-bit D/A Converter to be added to a pedestal consisting of the sum of all lower order currents from the segment generator. This configuration guarantees monotonicity.

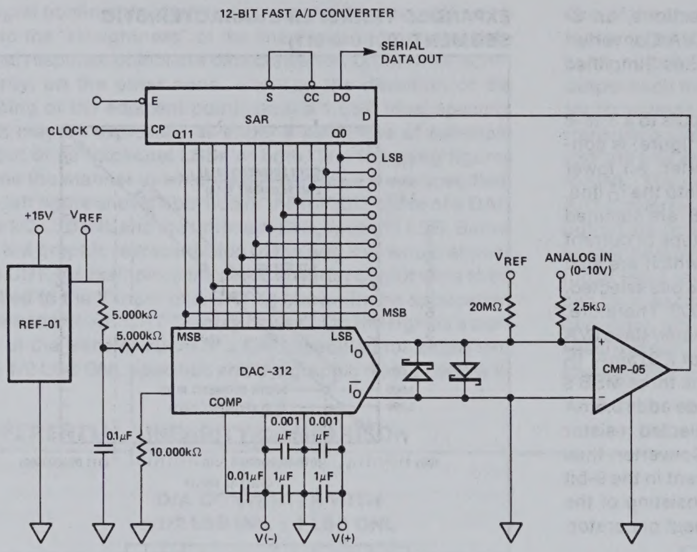
EXPANDED TRANSFER CHARACTERISTIC SEGMENT (001 010 011)



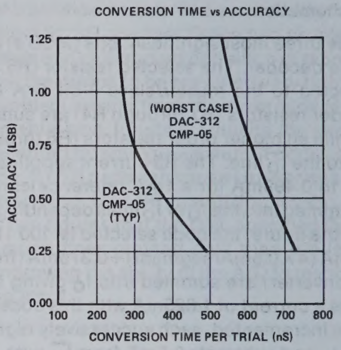
SIMPLIFIED SCHEMATIC


V(+)
20
VL/AGND
13
B1
MSB
1
B2
2
B3
3
B4
4
B5
5
B6
6
B7
7
B8
8
B9
9
B10
10
B11
11
B12
LSB
12
3 TO 8 LINE DECODER
LOGIC CONTROL
IO
IO
18
IO
19
IO
CURRENT SWITCHES
ISEG
8x
4x
2x
1x
1x
VREF(+)
14
VREF(-)
15
REFERENCE AMPLIFIER
+
−
R/2
R1
R2
R3
R4
R5
R6
R7
R8
2R
2R
2R
2R
2R
2R
R
R
R
R
R1−R8 = RΩ
BIAS NETWORK
V(+)
V(-)
16
COMP
17
V(-)

12-BIT FAST A/D CONVERTER


12-BIT FAST A/D CONVERTER
SERIAL DATA OUT
S
CC
DO
E
SAR
D
CLOCK
CP
Q11
Q0
LSB
MSB
+15V
VREF
REF-01
5.000kΩ
5.000kΩ
MSB
LSB
DAC-312
I_O
$\overline{I_O}$
COMP
0.1μF
10.000kΩ
0.001 μF
0.001 μF
0.01μF
1μF
1μF
V(-)
V(+)
VREF
ANALOG IN (0-10V)
20MΩ
2.5kΩ
CMP-05
+
−

NOTE:
DEVICE(S) CONNECTED TO ANALOG INPUT MUST BE CAPABLE OF SOURCING 4.0mA. A BUFFER (eg. BUF-03) MAY BE REQUIRED.



CONVERSION TIME (ns)	TYP	WORST CASE
SAR	33	55
CMP-05	92	125
TOTAL	375ns	680ns
× 13	4.9μs	8.8μs

BYTEDAC® 8-BIT HIGH-SPEED "MICROPROCESSOR COMPATIBLE" MULTIPLYING D/A CONVERTER

DAC-808

FEATURES

- **Dual 4-Bit Input Latch Coupled to 8-Bit Latched DAC**
- **8 and 4-Bit μP Compatible**
- **Easily Interfaced to 8080, and Z-80 Processors**
- **TTL Logic Compatible**
- **Programmable Mode Control**
- **High Output Impedance and Compliance**
- **Proven DAC-08 Analog Flexibility and Reliability**
- **Nonlinearity to ±0.1% Maximum**

GENERAL DESCRIPTION

The BYTEDAC® DAC-808 is a double-buffered latch input digital-to-analog converter designed specifically for 8 and 4-bit microprocessors. The double latch concept allows the processor to load data in the master latch without disturbing existing data in the slave latch, which controls the analog output. The DAC-808 operates in five modes which are selected by the user under processor control. Data transfer is accomplished in two 4-bit nibbles, one 4-bit nibble, or one 8-bit byte.

The Analog section consists of a "Field-Proven" DAC-08 D/A converter. Monotonic multiplying performance is attained over a wide 20 to 1 reference current range. Matching to within 1 LSB between reference and full-scale currents eliminates full-scale adjustments in most applications.

DAC-808 applications include graphic display drivers, high-speed modems, A/D converters, programmable waveform generators and power supplies, analog meter drivers, audio encoders and programmable attenuators, and other applications where low cost, high speed and double-buffering flexibility are required.

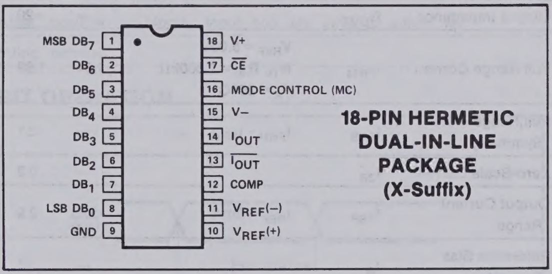
ORDERING INFORMATION†

NL % FS	18 PIN HERMETIC DUAL-IN-LINE PACKAGE MILITARY	 INDUSTRIAL	 COMMERCIAL
±0.1	DAC-808AX*	DAC-808EX	—
±0.19	DAC-808BX*	DAC-808FX	—
±0.39	—	—	DAC-808GX

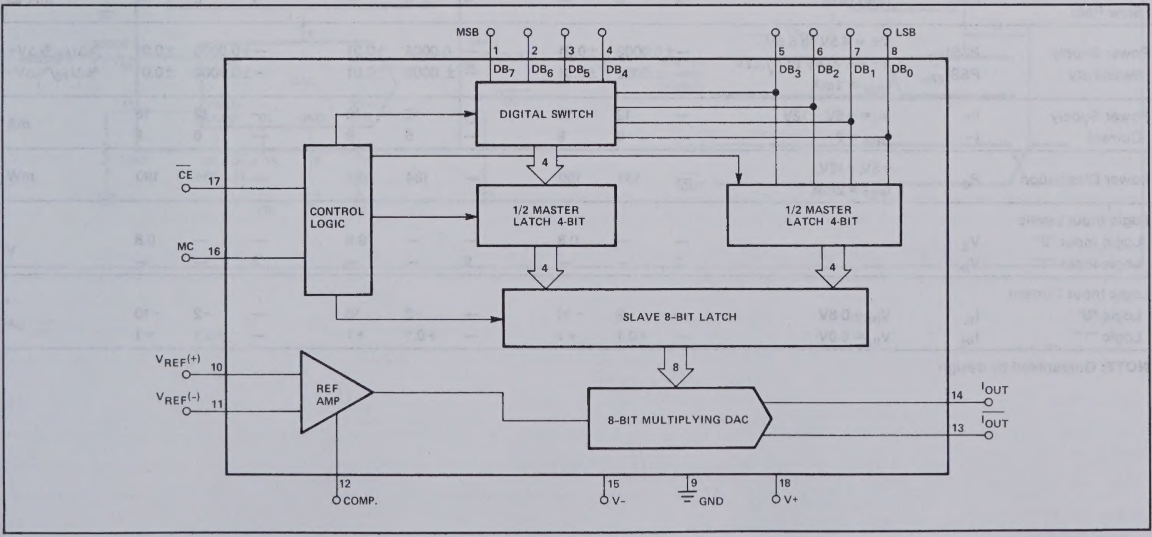
*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

PIN CONNECTIONS


MSB DB$_7$ 1
DB$_6$ 2
DB$_5$ 3
DB$_4$ 4
DB$_3$ 5
DB$_2$ 6
DB$_1$ 7
LSB DB$_0$ 8
GND 9
18 V+
17 $\overline{CE}$
16 MODE CONTROL (MC)
15 V−
14 I$_{OUT}$
13 $\overline{I}_{OUT}$
12 COMP
11 V$_{REF}$(−)
10 V$_{REF}$(+)
18-PIN HERMETIC DUAL-IN-LINE PACKAGE (X-Suffix)

EQUIVALENT CIRCUIT


MSB
1 DB$_7$
2 DB$_6$
3 DB$_5$
4 DB$_4$
5 DB$_3$
6 DB$_2$
7 DB$_1$
8 DB$_0$
LSB
DIGITAL SWITCH
4
$\overline{CE}$ 17
MC 16
CONTROL LOGIC
1/2 MASTER LATCH 4-BIT
1/2 MASTER LATCH 4-BIT
4
4
SLAVE 8-BIT LATCH
8
V$_{REF}$(+) 10
V$_{REF}$(−) 11
REF AMP
8-BIT MULTIPLYING DAC
14 I$_{OUT}$
13 $\overline{I}_{OUT}$
12 COMP.
15 V-
9 GND
18 V+

Manufactured under one or more of the following patents: 4,055,773; 4,056,740; 4,092,639.

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
DAC-808A/B .... −55°C to +125°C
DAC-808E/F .... −25°C to +85°C
DAC-808G .... 0°C to +70°C
DICE Junction Temperature .... −65°C to +150°C
Storage Temperature .... −65°C to +150°C
Power Dissipation 300mW
Derate Above 100°C .... 10mW/°C
Lead Temperature (Soldering, 60 sec) .... 300°C

V+ Supply to V− Supply 18.7V
Logic Inputs .... 0V to 5.5V
Analog Current Outputs .... −5mA
Reference Inputs (V_{10}, V_{11}) .... V− to V+
Reference Input Differential Voltage
(V_{10} to V_{11}) .... ±15V
Reference Input Current 5.0mA

NOTE: Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at V+ = +5V, V− = −12V, I_{REF} = 2.0mA, T_A = −55°C to +125°C for DAC-808A/B, unless otherwise noted. T_A = −25°C to +85°C apply for DAC-808E/F; T = 0°C to +70°C apply for DAC-808G. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

			DAC-808A/E			DAC-808B/F			DAC-808G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Resolution			8	—	—	8	—	—	8	—	—	Bits
Monotonicity			8	—	—	8	—	—	8	—	—	Bits
Nonlinearity			—	—	±0.1	—	—	±0.19	—	—	±0.39	% FS
Full-Scale Tempco	TCI_{FS}	(See Note)	—	±10	±50	—	±10	±80	—	±10	±80	ppm/°C
Output Voltage Compliance	V_{OC}	Full-Scale Current Change < 1/2 LSB	−5	—	+5	−5	—	+5	−5	—	+5	V
Output Impedance	R_{OUT}		—	>20	—	—	>20	—	—	>20	—	MΩ
Full Range Current	I_{FR14}	V_{REF} = 5.00V R_{11}, R_{10} = 2.500kΩ T_A = 25°C	1.94	1.99	2.04	1.94	1.99	2.04	1.94	1.99	2.04	mA
Full Range Symmetry	I_{FRS}	I_{FR14} - I_{FR13}	—	±1	±8	—	±1	±8	—	±1	±8	μA
Zero-Scale Current	I_{ZS}		—	0.2	2	—	0.2	2	—	0.2	2	μA
Output Current Range	I_{FSR}	I_{REF} = 3mA	2.1	2.9	—	2.1	2.9	—	2.1	2.9	—	mA
Reference Bias Current	I_B		—	−1	−3	—	−1	−3	—	−1	−3	μA
Reference Input Slew Rate	dI/dt	(See Note)	4	8	—	4	8	—	4	8	—	mA/μs
Power Supply Sensitivity	$PSSI_{FR+}$ $PSSI_{FR-}$	V+ = 4.5V to 5.5V V− = −10.8V to −13.2V I_{REF} = 1mA	— —	±0.0003 ±.0002	±0.01 ±0.01	— —	0.0003 ±.0002	±0.01 ±0.01	— —	±0.0003 ±0.0002	±0.01 ±0.01	$\%\Delta I_{FS}/\%\Delta V+$ $\%\Delta I_{FS}/\%\Delta V-$
Power Supply Current	I+ I−	V_S = +5V, −12V I_{REF} = 2	— —	12 6	16 9	— —	12 6	16 9	— —	12 6	16 9	mA
Power Dissipation	P_d	+5V, −12V, I_{REF} = 2mA	—	134	190	—	134	190	—	134	190	mW
Logic Input Levels Logic Input "0" Logic Input "1"	 V_{IL} V_{IH}		 — 2	 — —	 0.8 —	 — 2	 — —	 0.8 —	 — 2	 — —	 0.8 —	V
Logic Input Current Logic "0" Logic "1"	 I_{IL} I_{IH}	 V_{IN} = 0.8V V_{IN} = 5.0V	 — —	 −2 +0.1	 −10 +1	 — —	 −2 +0.1	 −10 +1	 — —	 −2 +0.1	 −10 +1	μA

NOTE: Guaranteed by design:

ELECTRICAL CHARACTERISTICS — A.C. PARAMETERS $V_S = +5V, -12V, I_{REF} = 2.0mA, T_A = 25°C$, unless otherwise noted.

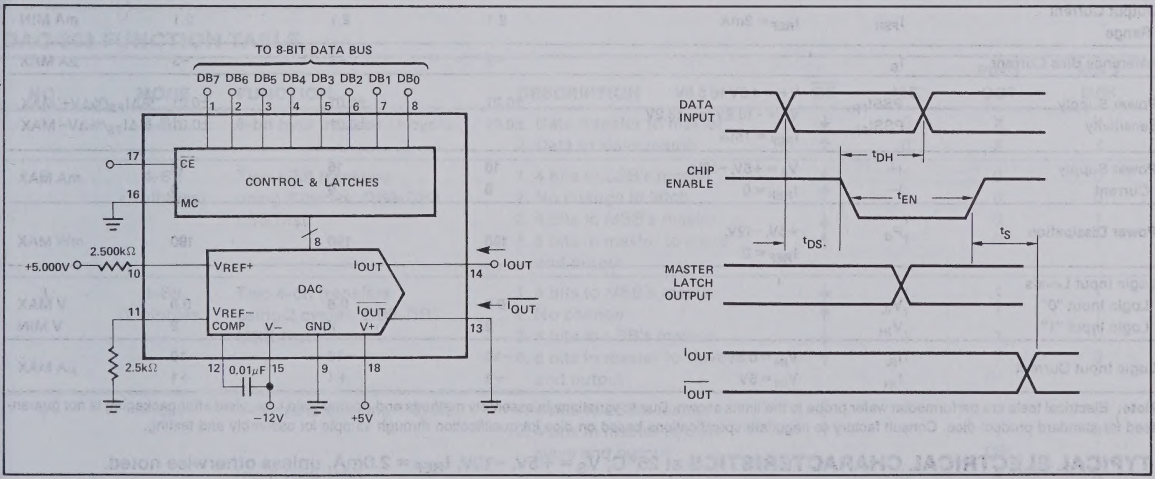
			DAC-808A/E			DAC-808B/F			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Settling Time	t_S	From CE Positive Edge to ±1/2 LSB, All Bits Switched ON or OFF, See Note	—	300	500	—	300	500	ns
Data Input Setup Time	t_{DS}	See Note	50	30	—	50	30	—	ns
Data Input Hold Time	t_{DH}	See Note	100	30	—	100	30	—	ns
Address Input Setup Time (Bits 7 and 6)	t_{AS}	4-Bit Mode, See Note	150	100	—	150	100	—	ns
Address Hold Time	t_{AH}	4-Bit Mode, See Note	—	0	10	—	0	10	ns
Chip Enable Negative Width	t_{EN}	See Note	250	100	—	250	100	—	ns
Chip Enable Positive Width	t_{EP}	See Note	350	200	—	350	200	—	ns

NOTE: Guaranteed by design.

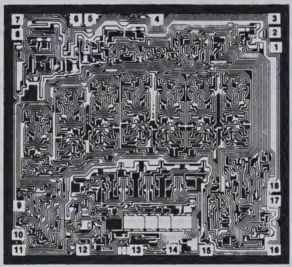
DAC-888 PIN DESCRIPTION

SYMBOL	DESCRIPTION
DB_0 - DB_7	DATA BIT — Bits 0-7 are digital, active-high inputs that have DB_7 assigned the MSB.
$\overline{CE}$	CHIP ENABLE — An active-low input control serving a dual purpose in that it's both the device enable and chip write input terminal.
MC	MODE CONTROL — A control that places the DAC in 8-bit operation when low and 4-bit operation when high.
I_{OUT} - $\overline{I_{OUT}}$	CURRENT OUTPUT — Complementary current outputs when added equal I_{FS}.
V_{REF-}, V_{REF+}	VOLTAGE REFERENCE — Differential inputs that accept a negative, positive, or bipolar input and are used to adjust I_{FS}.
COMP	COMPENSATION — The reference amplifier frequency compensating terminal.

FUNCTIONAL DIAGRAM AND TIMING DIAGRAM FOR 8-BIT OPERATION


TO 8-BIT DATA BUS
DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
1 2 3 4 5 6 7 8
17
CE
CONTROL & LATCHES
16
MC
8
2.500kΩ
+5.000V
10
VREF+
IOUT
DAC
14
IOUT
11
VREF−
COMP
V−
GND
IOUT
V+
IOUT
13
2.5kΩ
12
0.01μF
15
9
18
−12V
+5V
DATA INPUT
tDH
CHIP ENABLE
tEN
tDS
tS
MASTER LATCH OUTPUT
IOUT
IOUT

DICE CHARACTERISTICS



1. DB7 (MSB)
2. DB6
3. DB5
4. DB4
5. DB3
6. DB2
7. DB1
8. DB0 (LSB)
9. GROUND
10. V_{REF} (+)
11. V_{REF} (−)
12. COMP
13. $\overline{I_{OUT}}$
14. I_{OUT}
15. V−
16. MODE CONTROL (MC)
17. $\overline{CE}$
18. V+

DIE SIZE 0.139 × 0.126 inch; 17,514 sq. mils (3.53 × 3.2mm.; 11.296 sq. mm)

For additional DICE information refer to Section 2.

WAFER TEST LIMITS at $V_S = +5V, -12V, I_{REF} = 2.0mA, T_A = 25°C$, unless otherwise noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

PARAMETER	SYMBOL	CONDITIONS	DAC-808N LIMIT	DAC-808G LIMIT	DAC-808GR LIMIT	UNITS
Resolution			8	8	8	Bits MIN
Monotonicity			8	8	8	Bits MIN
Nonlinearity			±0.1	±0.19	±0.39	%FS MAX
Output Voltage Compliance	V_{OC}	Full-Scale Current Change < 1/2 LSB $R_{OUT} > 20 M\Omega$ Typ.	+5 −5	+5 −5	+5 −5	V MAX V MIN
Full Range Current	I_{FR14}	$V_{REF} = 5.00V$ $R_{11}, R_{10} = 2.500k\Omega$ $T_A = 25°C$	2.04 1.94	2.04 1.94	2.04 1.94	mA MAX mA MIN
Full Range Symmetry	I_{FRS}	$I_{FR14} - I_{FR13}$	±8	±8	±8	μA MAX
Zero-Scale Current	I_{ZS}		2	2	2	μA MAX
Output Current Range	I_{FSR}	$I_{REF} = 3mA$	2.1	2.1	2.1	mA MIN
Reference Bias Current	I_B		−3	−3	−3	μA MAX
Power Supply Sensitivity	$PSSI_{FR+}$ $PSSI_{FR-}$	V+ = 4.5V to 5.5V V− = −10.8V to −13.2V $I_{REF} = 1mA$	±0.01 ±0.01	±0.01 ±0.01	±0.01 ±0.01	$\%\Delta I_{FS}/\%\Delta V+$ MAX $\%\Delta I_{FS}/\%\Delta V-$ MAX
Power Supply Current	I+ I−	$V_S = +5V, -12V$ $I_{REF} = 0$	16 9	16 9	16 9	mA MAX
Power Dissipation	P_d	+5V, −12V, $I_{REF} = 0$	190	190	190	mW MAX
Logic Input Levels						
Logic Input "0"	V_{IL}		0.8	0.8	0.8	V MAX
Logic Input "1"	V_{IH}		2	2	2	V MIN
Logic Input Current	I_{IL} I_{IH}	$V_{IN} = 0.8V$ $V_{IN} = 5V$	−10 +1	−10 +1	−10 +1	μA MAX

Note: Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

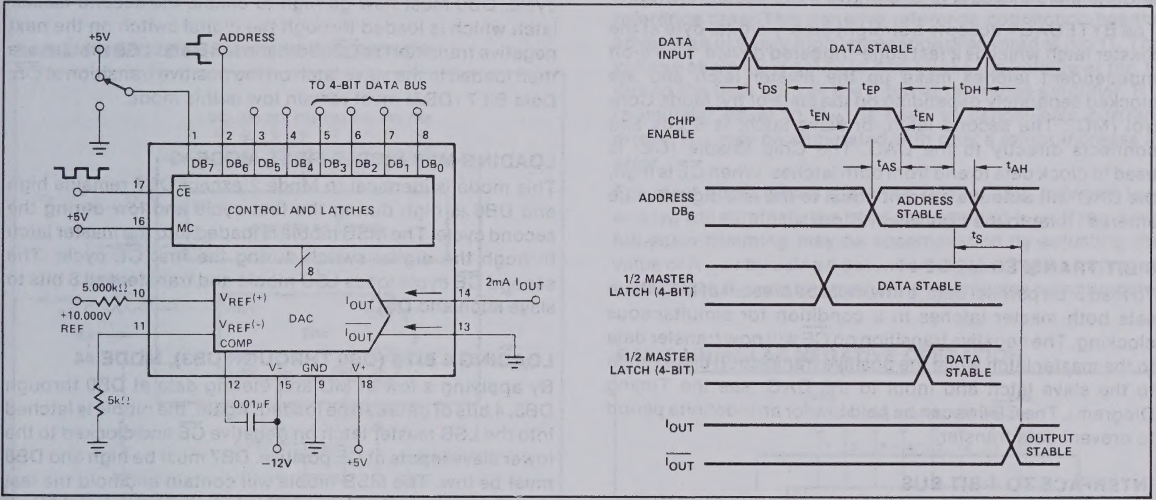
TYPICAL ELECTRICAL CHARACTERISTICS at 25°C; $V_S = +5V, -12V, I_{REF} = 2.0mA$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-808 TYPICAL	UNITS
Reference Input Slew Rate	dI/dt		8	mA/μs
Settling Time	t_S	From CE Positive Edge to ±1/2 LSB, All Bits Switched ON or OFF	300	ns
Data Input Setup Time	t_{DS}		30	ns
Data Input Hold Time	t_{DH}		30	ns
Address Input Setup Time (Bits 7 and 6)	t_{AS}	4-Bit Mode	100	ns

TYPICAL ELECTRICAL CHARACTERISTICS at 25° C; $V_S = +5V, -12V$, $I_{REF} = 2.0mA$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	DAC-808 TYPICAL	UNITS
Address Hold Time	t_{AH}	4-Bit Mode	0	ns
Chip Enable Negative Width	t_{EN}		100	ns
Chip Enable Positive Width	t_{EP}		200	ns

FUNCTIONAL DIAGRAM AND TIMING DIAGRAM FOR 4-BIT OPERATION


+5V
ADDRESS
TO 4-BIT DATA BUS
1 2 3 4 5 6 7 8
DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
17
CE
CONTROL AND LATCHES
+5V
16
MC
8
5.000kΩ
10
+10.000V REF
11
VREF(+)
VREF(−)
COMP
DAC
IOUT
IOUT
14
13
2mA IOUT
V−
GND
V+
12 15 9 18
0.01µF
5kΩ
−12V
+5V
DATA INPUT
DATA STABLE
tDS
tEP
tDH
CHIP ENABLE
tEN
tEN
tAS
tAH
ADDRESS DB6
ADDRESS STABLE
tS
1/2 MASTER LATCH (4-BIT)
DATA STABLE
1/2 MASTER LATCH (4-BIT)
DATA STABLE
IOUT
IOUT
OUTPUT STABLE

DAC-808 FUNCTION TABLE

NO.	MODE	FUNCTION	DESCRIPTION	$\overline{CE}$	MC	PIN 1 DB7	PIN 2 DB6
1	8-Bit	8-bit byte transfer (1 cycle)	1. Data transfer to master	↓	0	X	X
			2. Data to slave match	↑	0	X	X
2	4-Bit (2 nibbles)	Two 4-bit transfers using 2 cycles. DB0-DB3 LSB first.	1. 4 bits to LSB's master	↓	1	0	0
			2. No change in latch	↑	1	0	0
			3. 4 bits to MSB's master	↓	1	0	1
			4. 8 bits in master to slave and output	↑	1	0	1
3	4-Bit (2 nibbles)	Two 4-bit transfers using 2 cycles. DB0-DB3 MSB first.	1. 4 bits to MSB's master	↓	1	1	1
			2. No change	↑	1	1	1
			3. 4 bits to LSB's master	↓	1	1	0
			4. 8 bits in master to slave and output	↑	1	1	0
4	4-Bit	4-bit transfer using 1 cycle.	1. 4 bits to LSB's master	↓	1	1	0
			2. 4 bits in master to LSB slave and output	↑	1	1	0
						OR	
		Input DB0-DB3			0	X	X
		Ground DB4-DB7			0	X	X
5	4-Bit	4-bit transfer using 1 cycle.	1. 4 bits to MSB's master	↓	1	0	1
			2. 4 bits in master to MSB slave and output	↑	1	0	1
						OR	
		Input DB4-DB7			0	X	X
		Ground DB0-DB3			0	X	X
6	None	No operation	Chip disabled — Previous output still present	1	X	X	X

LSB — Least Significant Bit
MSB — Most Significant Bit
X — Insignificant (Don't Care)

↑ — Positive Transition
↓ — Negative Transition
DB — Data Bit

DIGITAL INFORMATION

The DAC-808 is a monolithic microprocessor compatible device consisting of a quad digital switch, two 4-bit master latches, one 8-bit slave latch, control circuitry, and one 8-bit multiplying DAC; all housed in an 18-pin Dual-In-Line Package.

The DAC-808 can be thought of, in the 4-bit mode, as a quad 1 to 2-line digital demultiplexer which selects a 4-bit input and transfers this data to one of two 4-bit master latches.

The BYTEDAC® accepts a straight binary digital byte at the master latch which is a fast edge-triggered device. Two 4-bit independent latches make up the master latch and are clocked separately depending on the state of the Mode Control (MC). The second latch, or slave latch, is 8 bits and connects directly to the DAC. The Chip Enable ($\overline{CE}$) is used to clock data to and from both latches. When $\overline{CE}$ is high, the DAC will output a current equal to the last digital value entered (refer to the Equivalent Circuit).

8-BIT TRANSFER MODE #1

To load 8-bit parallel data, a low must be present at MC which sets both master latches in a condition for simultaneous clocking. The negative transition on $\overline{CE}$ will now transfer data to the master latch while the positive transaction clocks data to the slave latch and input to the DAC (see the Timing Diagram). The $\overline{CE}$ line can be held low for an indefinite period to prevent data transfer.

INTERFACE TO 4-BIT BUS

The DAC-808 is able to handle 4-bit data in four ways, which will be discussed here. Modes 2 and 3 transfer two 4-bit nibbles which are assembled at the slave latch into an 8-bit byte (refer to Function Table). Modes 4 and 5 transfer a single 4-bit nibble only.

LOADING LSB NIBBLE FIRST, MODE #2

For all 4-bit operations the MC pin must be high. A low must be applied to Data Bit 6 (DB6) which now acts as an address pin. Data is brought in at DB0 through DB3 and clocked into the LSB master latch on the negative transition of $\overline{CE}$. Nothing occurs on the positive transition of the $\overline{CE}$'s first cycle. DB6 must now go high to enable the second master latch which is loaded through the digital switch on the next negative transition at $\overline{CE}$. Both the MSB and LSB nibbles are then loaded in the slave latch on the positive transition at $\overline{CE}$. Data Bit 7 (DB7) must remain low in this mode.

LOADING MSB NIBBLE FIRST, MODE #3

This mode is identical to Mode 2 except DB7 remains high and DB6 is high during the first cycle and low during the second cycle. The MSB nibble is loaded into the master latch through the digital switch during the first $\overline{CE}$ cycle. The second $\overline{CE}$ cycle loads LSB nibble and transfers all 8 bits to slave latch and DAC.

LOADING 4 BITS (DB0 THROUGH DB3), MODE #4

By applying a low at MC and etering data at DB0 through DB3, 4 bits of data can be loaded. Again, the nibble is latched into the LSB master latch on negative $\overline{CE}$ and clocked to the lower slave inputs at $\overline{CE}$ positive. DB7 must be high and DB6 must be low. The MSB nibble will contain and hold the last data entered into it. If four LSB's of resolution are all that will be required, the data may be entered in the 8-bit mode with MC low and DB4 through DB7 tied high or low.

DAC-808 EQUIVALENT CIRCUIT

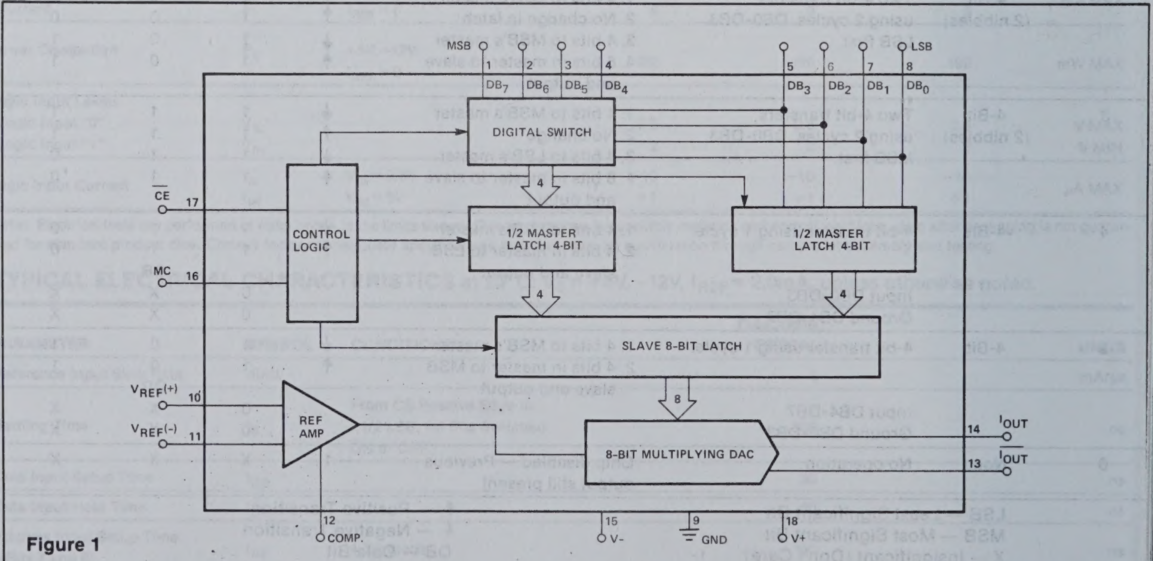


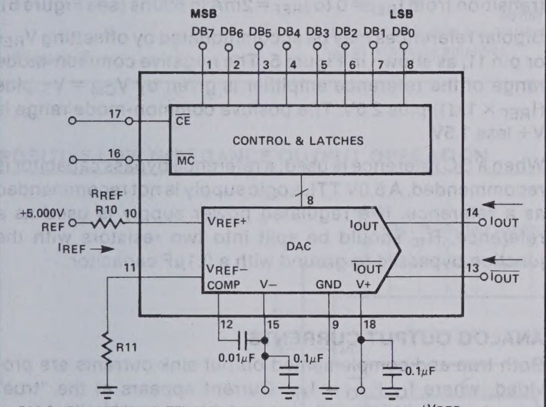
Figure 1

LOADING 4 BITS (DB4 THROUGH DB7), MODE #5

This is the same as Mode 4 except that DB7 is now low and DB6 is now high. The data is still entered into DB0 through DB3, but the data is now loaded into the MSB nibble. The LSB nibble will contain and hold the last data entered into it. If 4 MSB's of resolution are all that will be required, the data may be entered in the 8-bit mode with MC low and DB0 through DB3 tied high or low.

ANALOG INFORMATION

BASIC POSITIVE REFERENCE OPERATION


MSB
LSB
DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
1 2 3 4 5 6 7 8
17
CE
CONTROL & LATCHES
16
MC
8
RREF
+5.000V
REF
R10
10
IREF
VREF+
DAC
IOUT
14
IOUT
11
VREF−
COMP
V−
GND
V+
IOUT
13
IOUT
12
15
9
18
R11
0.01μF
0.1μF
0.1μF

FOR FIXED REFERENCE, TTL OPERATION TYPICAL VALUES ARE:
R_{REF} = 2.5000k
R11 = R_{REF}
V_{LC} = 0V (GROUND)

$I_{FR} \approx \frac{+V_{REF}}{R_{REF}} \times \frac{255}{256}$

$I_{OUT} + \overline{I_{OUT}} = I_{FR}$ FOR ALL LOGIC STATES

Figure 2

REFERENCE AMPLIFIER SET-UP

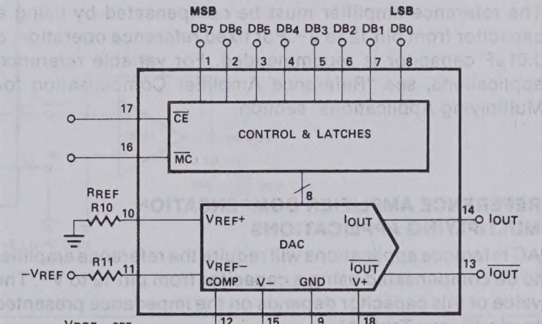
The DAC-808 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly 0 to +4.0mA. The full range output current is a linear function of the reference current and is given by:

$$I_{REF} = \frac{255}{256} \times I_{REF} \text{ where } I_{REF} = I_{10}$$

In positive reference applications, an external positive reference voltage current flows through R_{10} into the $V_{REF(+)}$ terminal of the reference amplifier. Alternatively, a negative reference may be applied to $V_{REF(-)}$; reference current flows from ground through R_{10} into $V_{REF(+)}$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin 11. The voltage at pin 10 is equal to and tracks the voltage at pin 11 due to the high gain of the internal reference amplifier. R_{11} (nominally equal to R_{10}) is used to cancel bias currrent errors; R_{11} may be eliminated with only a minor increase in error.

For most applications the close relationship between I_{REF} and I_{FR} will eliminate the need for trimming I_{REF}. If required, full-scale trimming may be accomplished by adjusting the value of R_{10} or by using a potentiometer for R_{10}. An improved method of full-scale trimming which eliminates potentiometer

BASIC UNIPOLAR NEGATIVE OPERATION

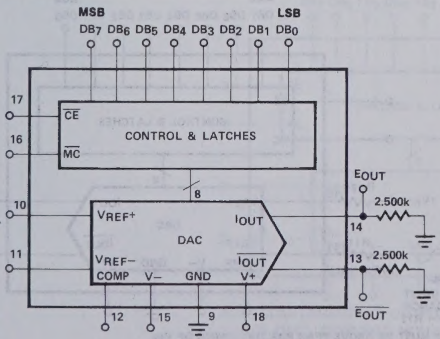

MSB
LSB
DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
1 2 3 4 5 6 7 8
17
CE
CONTROL & LATCHES
16
MC
8
RREF
R10
10
VREF+
IOUT
14
IOUT
DAC
R11
−VREF
11
VREF−
COMP
V−
GND
V+
IOUT
13
IOUT
12
15
9
18

$I_{FR} = \frac{-V_{REF}}{R_{REF}} \times \frac{255}{256}$

NOTE: R_{REF} SETS I_{FS}: R11 IS FOR BIAS CURRENT CANCELLATION.

Figure 3

BASIC NEGATIVE REFERENCE OPERATION


MSB
LSB
DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
17
CE
CONTROL & LATCHES
16
MC
8
IREF = 2.000mA
10
VREF+
IOUT
DAC
11
VREF−
COMP
V−
GND
IOUT
V+
EOUT
2.500k
14
13
2.500k
EOUT
12
15
9
18

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	I_OmA	$\overline{I_O}$mA	E_O	$\overline{E_O}$
FULL-SCALE	1	1	1	1	1	1	1	1	1.992	0.000	−4.980	0.000
FULL-SCALE −1 LSB	1	1	1	1	1	1	1	0	1.984	0.008	−4.960	−0.020
HALF-SCALE +1 LSB	1	0	0	0	0	0	0	1	1.008	0.984	−2.520	−2.460
HALF-SCALE	1	0	0	0	0	0	0	0	1.000	0.992	−2.500	−2.480
HALF-SCALE −1 LSB	0	1	1	1	1	1	1	1	0.992	1.000	−2.480	−2.500
ZERO-SCALE +1 LSB	0	0	0	0	0	0	0	1	0.008	1.984	−0.020	−4.960
ZERO-SCALE	0	0	0	0	0	0	0	0	0.000	1.992	−0.000	−4.980

Figure 4

RECOMMENDED FULL SCALE ADJUSTMENT CIRCUIT

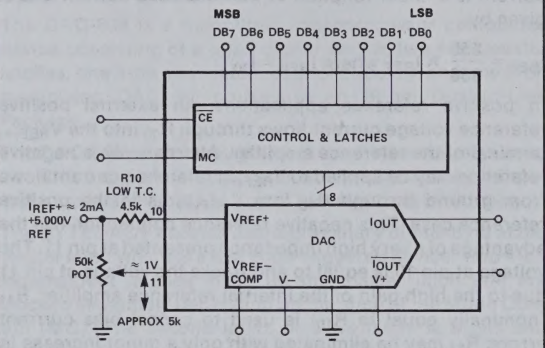

MSB
LSB
DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
CE
CONTROL & LATCHES
MC
R10
LOW T.C.
4.5k
10
IREF+ ≈ 2mA
+5.000V
REF
8
VREF+
IOUT
DAC
50k
POT
≈ 1V
11
VREF−
COMP
V−
GND
IOUT
V+
APPROX 5k

Figure 5

TC effects is shown in the Recommended Full Scale Adjustment Circuit.

Using lower values of reference current reduces negative power supply current and increases reference amplifier negative common-mode range. The recommended range for operation with a DC reference current is +0.2mA to +4.0mA.

The reference amplifier must be compensated by using a capacitor from pin 12 to V−. For fixed reference operation, a 0.01μF capacitor is recommended. For variable reference applications, see "Reference Amplifier Compensation for Multiplying Applications" section.

REFERENCE AMPLIFIER COMPENSATION MULTIPLYING APPLICATIONS

AC reference applications will require the reference amplifier to be compensated using a capacitor from pin 12 to V−. The value of this capacitor depends on the impedance presented to pin 10 (see Table 1).

TABLE 1. REFERENCE AMPLIFIER COMPENSATION

REF. INPUT RESISTANCE	SUGGESTED C_C
1kΩ	15pF
2.5kΩ	37pF
5kΩ	75pF

NOTE: A 0.01μF capacitor is suggested for fixed references.

For fastest response to a pulse, low values of R_{10}, enabling small C_C values, should be used. If pin 10 is driven by a high current source, none of the above values will suffice and the amplifier must be heavily compensated which will decrease overall bandwidth and slew rate. For R_{10} = 1kΩ and C_C = 15pF, the reference amplifier slews at 4mA/μs, enabling a transition from $I_{REF} = 0$ to $I_{REF} = 2$mA in 500ns (see Figure 6).

Bipolar references may be accommodated by offsetting V_{REF} or pin 11, as shown in Figure 5. The negative common-mode range of the reference amplifier is given by V_{CM} = V− plus (I_{REF} × 1kΩ) plus 2.5V. The positive common-mode range is V+ less 1.5V.

When a DC reference is used, a reference bypass capacitor is recommended. A 5.0V TTL Logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R_{10} should be split into two resistors with the junction bypassed to ground with a 0.1μF capacitor.

ANALOG OUTPUT CURRENTS

Both true and complemented output sink currents are provided, where $I_O + \overline{I_O} = I_{FR}$. Current appears at the "true" output when a "1" is applied to each logic input. As the binary count increases, the sink current at pin 14 increases proportionally in the fashion of a "positive logic" D/A converter. When a "0" is applied to any input bit, that current is turned off at pin 14 and turned on at pin 13. A decreasing logic count increases $\overline{I_O}$ as in a negative or inverted logic D/A converter. Both outputs may be used simultaneously. If one of the outputs is not required it must still be connected to ground or to a point capable of sourcing I_{FS}; do not leave an unused output pin open.

ACCOMMODATING BIPOLAR REFERENCES

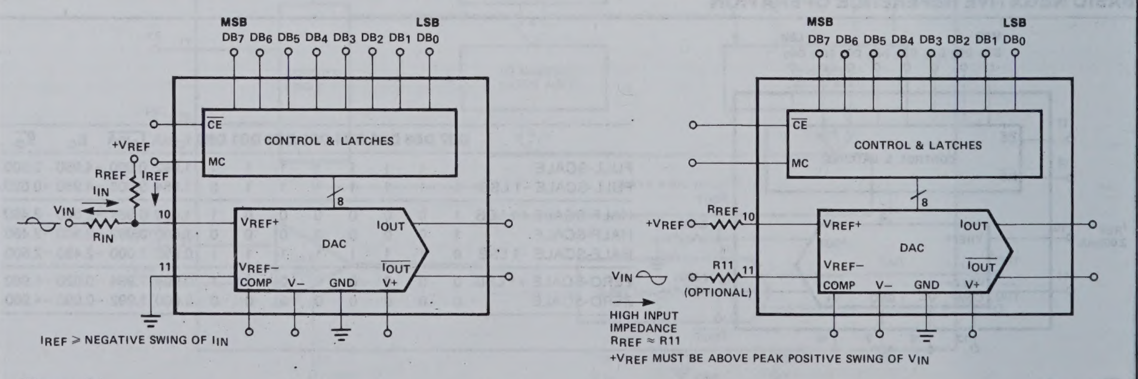
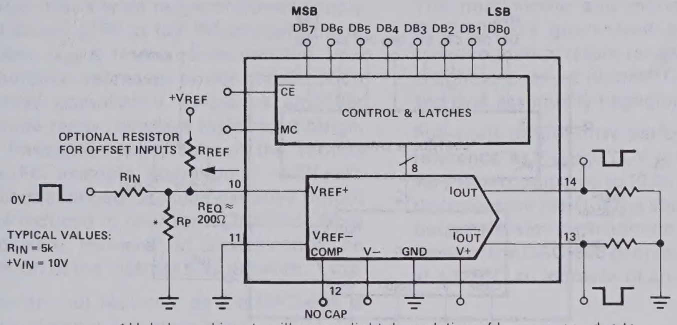

MSB
LSB
DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
CE
CONTROL & LATCHES
+VREF
MC
RREF
IREF
IIN
VIN
10
RIN
8
VREF+
IOUT
DAC
11
VREF−
IOUT
COMP
V−
GND
V+
IREF ≥ NEGATIVE SWING OF IIN
MSB
LSB
DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
CE
CONTROL & LATCHES
MC
RREF
10
+VREF
8
VREF+
IOUT
DAC
VIN
R11
11
(OPTIONAL)
VREF−
IOUT
COMP
V−
GND
V+
HIGH INPUT
IMPEDANCE
RREF ≈ R11
+VREF MUST BE ABOVE PEAK POSITIVE SWING OF VIN

Figure 6

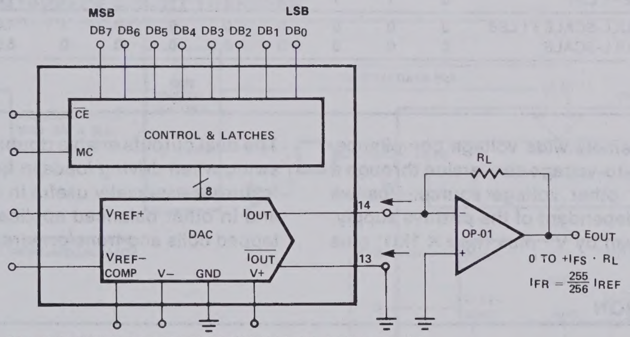
ALTERNATE PULSED REFERENCE OPERATION


MSB
LSB
DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
+VREF
CE
CONTROL & LATCHES
MC
OPTIONAL RESISTOR FOR OFFSET INPUTS
RREF
RIN
0V
10
REQ ≈ 200Ω
* Rp
TYPICAL VALUES:
RIN = 5k
+VIN = 10V
8
VREF+
IOUT
VREF− COMP
V−
GND
IOUT
V+
11
12
NO CAP
14
13

* Unbalanced inputs will cause slight degradation of I_{FS} accuracy due to I_{OS} of reference amplifier.

Figure 7

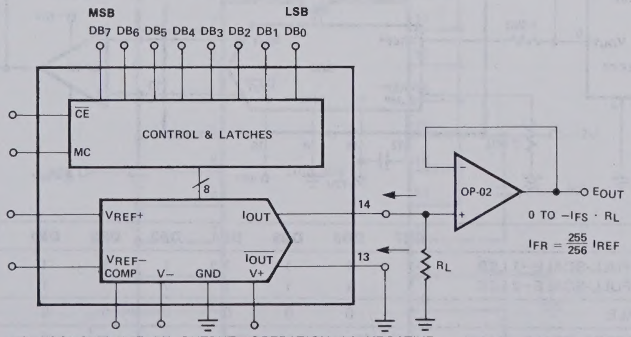
POSITIVE LOW IMPEDANCE OUTPUT OPERATION


MSB
LSB
DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
CE
CONTROL & LATCHES
MC
8
VREF+
DAC
IOUT
VREF− COMP
V−
GND
IOUT
V+
14
13
RL
OP-01
−
+
EOUT
0 TO +IFS · RL
IFR = 255/256 IREF

FOR COMPLEMENTARY OUTPUT (OPERATION AS NEGATIVE LOGIC DAC), CONNECT INVERTING INPUT OF OP-AMP TO $\overline{I_{OUT}}$. CONNECT I_{OUT} TO GROUND.

Figure 8

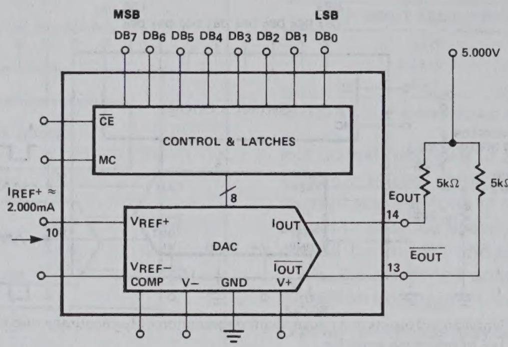
NEGATIVE LOW IMPEDANCE OUTPUT OPERATION


MSB
LSB
DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
CE
CONTROL & LATCHES
MC
8
VREF+
IOUT
VREF− COMP
V−
GND
IOUT
V+
14
13
OP-02
−
+
EOUT
0 TO −IFS · RL
IFR = 255/256 IREF
RL

FOR COMPLEMENTARY OUTPUT (OPERATION AS NEGATIVE LOGIC DAC), CONNECT NON-INVERTING INPUT OF OP-AMP TO $\overline{I_{OUT}}$. CONNECT I_{OUT} TO GROUND.

Figure 9

BASIC BIPOLAR OUTPUT OPERATION


MSB
LSB
DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
5.000V
CE
MC
CONTROL & LATCHES
8
IREF+ ≈ 2.000mA
10
VREF+
VREF−
COMP
V−
GND
V+
DAC
IOUT
IOUT
14
13
EOUT
EOUT
5kΩ
5kΩ

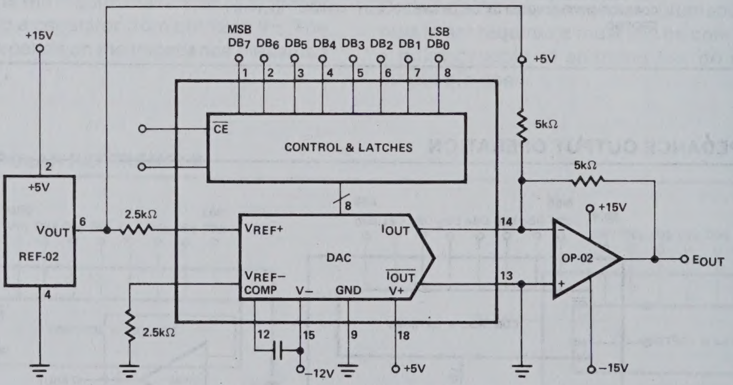
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	E_O	E_O
POSITIVE FULL-SCALE	1	1	1	1	1	1	1	1	−4.960	5.000
POSITIVE FULL-SCALE −1 LSB	1	1	1	1	1	1	1	0	−4.920	4.960
ZERO-SCALE +1 LSB	1	0	0	0	0	0	0	1	−0.040	0.080
ZERO-SCALE	1	0	0	0	0	0	0	0	0.000	0.040
ZERO-SCALE −1 LSB	0	1	1	1	1	1	1	1	0.040	0.000
NEGATIVE FULL-SCALE +1 LSB	0	0	0	0	0	0	0	1	4.900	−4.920
NEGATIVE FULL-SCALE	0	0	0	0	0	0	0	0	5.000	−4.960

Figure 10

Both outputs have an extremely wide voltage compliance, enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 8V and is independent of the positive supply. Negative compliance is given by V− plus ($I_{REF} \times 1k\Omega$) plus 2.5V.

The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection and in other balanced applications such as driving center-tapped coils and transformers.

OFFSET BINARY OPERATION


MSB
LSB
DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
1 2 3 4 5 6 7 8
+15V
+5V
CE
CONTROL & LATCHES
8
2
+5V
VOUT
REF-02
6
4
2.5kΩ
2.5kΩ
VREF+
VREF−
COMP
V−
GND
V+
DAC
IOUT
IOUT
14
13
12
15
9
18
−12V
+5V
5kΩ
5kΩ
+15V
−15V
OP-02
EOUT

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	E_O
POSITIVE FULL-SCALE −1 LSB	1	1	1	1	1	1	1	1	4.960
POSITIVE FULL-SCALE −2 LSB	1	1	1	1	1	1	1	0	4.920
ZERO-SCALE	1	0	0	0	0	0	0	0	0.000
NEGATIVE ZERO-SCALE +2 LSB	0	0	0	0	0	0	0	1	−4.960
NEGATIVE FULL-SCALE +1 LSB	0	0	0	0	0	0	0	0	−5.00

Figure 11

POWER SUPPLIES

The DAC-808 operates over a wide range of power supply voltages from a total supply of 9V to 18V. When operating at supplies of ±5V or less, $I_{REF} \leq 1mA$ is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common-mode range, negative logic input range, and negative logic threshold range; consult the various figures for guidance. For example, operation at −4.5V with $I_{REF} = 2mA$ is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible. However, at least 8V must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the DAC-808 is quite insensitive to variations in supply voltage.

Power consumption may be calculated as follows:

$P_d = (I+)\,(V+) + (I-)\,(V-)$.

TEMPERATURE PERFORMANCE

The nonlinearity and monotonicity specifications of the DAC-808 are guaranteed to apply over the entire rated operating temperature range. Full-scale output current drift is tight, typically ±10ppm/°C, with zero scale output current and drift essentially negligible compared to 1/2 LSB.

Full-scale output drive performance will be best with +5.0V reference, as V_{OS} and TCV_{OS} of the reference amplifier will be very small compared to 10.0V. The temperature coefficient of the reference resistor R_{10} should match and track that of the output resistor for minimum overall full-scale drift. Settling times of the DAC-808 decrease approximately 10% at −55°C; at +125°C an increase of about 15% is typical.

APPLICATIONS

8080 MICROPROCESSOR INTERFACE — 8-BIT TRANSFER

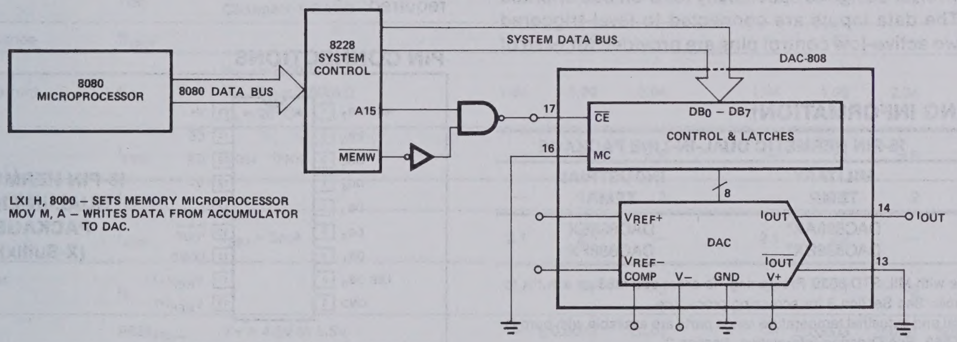
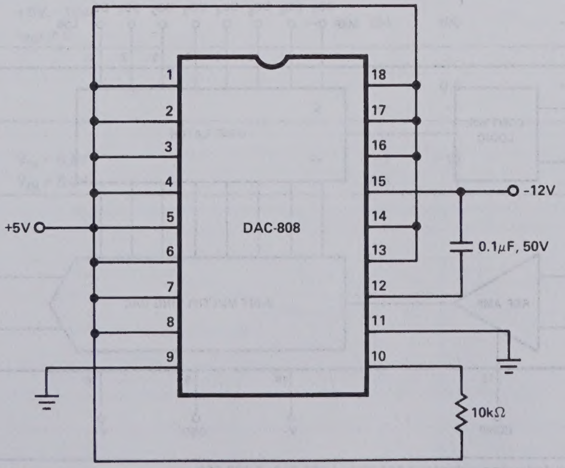

8080 MICROPROCESSOR
8080 DATA BUS
8228 SYSTEM CONTROL
A15
MEMW
LXI H, 8000 – SETS MEMORY MICROPROCESSOR
MOV M, A – WRITES DATA FROM ACCUMULATOR TO DAC.
SYSTEM DATA BUS
DAC-808
17
CE
16
MC
DB0 – DB7
CONTROL & LATCHES
8
VREF+
VREF−
COMP
V−
GND
V+
DAC
IOUT
IOUT
14
IOUT
13

Figure 12

TYPICAL BURN-IN CIRCUIT


1
2
3
4
5
6
7
8
9
18
17
16
15
14
13
12
11
10
+5V
DAC-808
-12V
0.1μF, 50V
10kΩ

DAC-888

BYTEDAC® 8-BIT HIGH-SPEED "MICROPROCESSOR COMPATIBLE" MULTIPLYING D/A CONVERTER

FEATURES

- **8-Bit Level Triggered Latch**
- **8-Bit μP Compatible**
- **Easily Interfaced to All 8-Bit Processors**
- **TTL Logic Compatible**
- **$\overline{CE}$ and $\overline{WR}$ Inputs**
- **High Output Impedance and Compliance**
- **Proven DAC-08 Analog Flexibility and Reliability**
- **Nonlinearity to ±0.1% Max**
- **Low Power Dissipation 134mW**

GENERAL DESCRIPTION

The BYTEDAC® DAC-888 is a buffered 8-bit digital-to-analog converter designed specifically for 8-bit bus oriented systems. The data inputs are connected to level-triggered latches. Two active-low control pins are provided for ease of interface to virtually all available microprocessors. The latches may also be operated in a transparent mode by holding both control pins low. Additionally, the DAC-888 has a data hold time requirement, of zero nanoseconds.

The Analog section consists of a "Field-Proven" DAC-08 D/A Converter. Monotonic multiplying performance is attained over a wide 20 to 1 reference current range. Matching to within 1 LSB between reference and full-scale currents eliminates full-scale adjustment in most applications.

DAC-888 applications include graphic display drivers, high-speed modems, A/D converters, programmable waveform generators and power supplies, analog meter drivers, audio encoders and programmable attenuators; and other applications where low cost, high speed and buffered flexibility are required.

ORDERING INFORMATION†

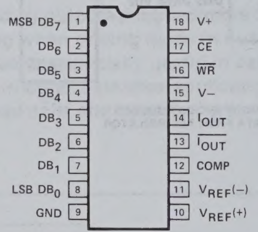
18-PIN HERMETIC DUAL-IN-LINE PACKAGE

NL %FS	MILITARY TEMP.	INDUSTRIAL TEMP.
0.1	DAC888AX*	DAC888EX
0.19	DAC888BX*	DAC888FX

*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

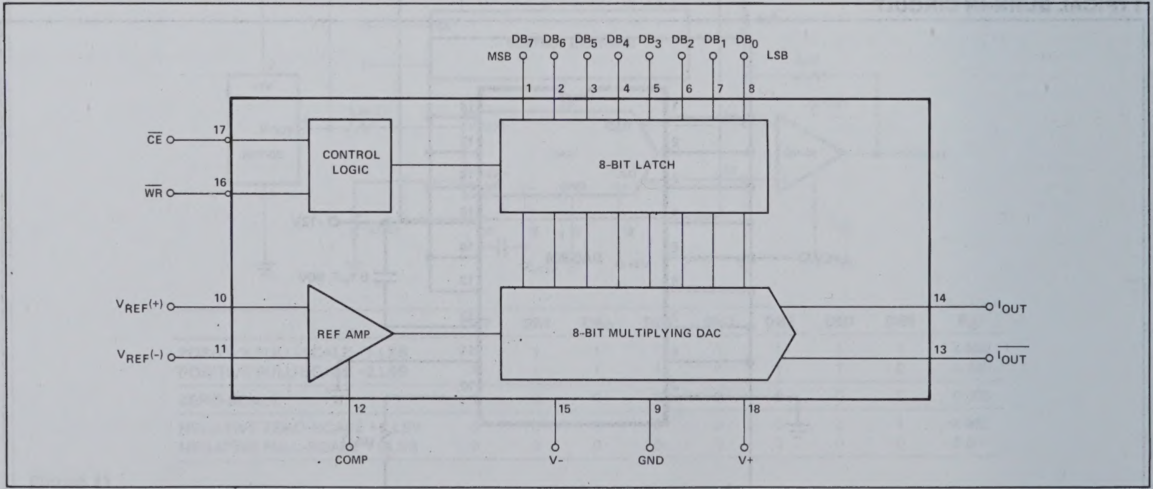
†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

PIN CONNECTIONS


MSB DB7
DB6
DB5
DB4
DB3
DB2
DB1
LSB DB0
GND
1
2
3
4
5
6
7
8
9
18
17
16
15
14
13
12
11
10
V+
CE
WR
V−
IOUT
IOUT
COMP
VREF(−)
VREF(+)

18-PIN HERMETIC DUAL-IN-LINE PACKAGE (X-Suffix)

FUNCTIONAL DIAGRAM


DB7
DB6
DB5
DB4
DB3
DB2
DB1
DB0
MSB
LSB
1
2
3
4
5
6
7
8
CE
17
WR
16
CONTROL LOGIC
8-BIT LATCH
VREF(+)
10
VREF(−)
11
REF AMP
8-BIT MULTIPLYING DAC
14
IOUT
13
IOUT
12
COMP
15
V-
9
GND
18
V+

Manufactured under one or more of the following patents: 4,055,773; 4,056,740; 4,092,639

ABSOLUTE MAXIMUM RATINGS

Operating Temperature	
DAC-888 A/B	−55°C to +125°C
DAC-888 E/F	−25°C to +85°C
DICE Junction Temperature (T_j)	−65°C to +150°C
Storage Temperature	−65°C to +150°C
Power Dissipation	300mW
Derate above 100°C	10mW/°C
Lead Temperature (Soldering, 60 sec)	300°C
V+ Supply to V− Supply	18.1V
Logic Inputs	0V to 5.5V
Analog Current Outputs	−5mA
Reference Inputs (V_{10} to V_{11})	V− to V+
Reference Input Differential Voltage (V_{10} to V_{11})	±15V
Reference Input Current	5mA

NOTE: Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at V+ = +5V, V− = −12V, I_{REF} = 2mA, T_A = −55°C to +125°C for DAC-888A/B, unless otherwise noted. T_A = 25°C to +85°C apply for DAC-888E/F. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

			DAC-888A/E			DAC-888B/F			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Resolution			8	—	—	8	—	—	Bits
Monotonicity			8	—	—	8	—	—	Bits
Nonlinearity			—	—	±0.1	—	—	±0.19	%FS
Full-Scale Tempco	TCI_{FS}	(See note)	—	±10	±50	—	±10	±80	ppm/°C
Output Voltage Compliance	V_{OC}	Full-Scale Current Change < 1/2 LSB	−5	—	+5	−5	—	+5	V
Output Impedance	R_{OUT}		—	>20	—	—	>20	—	MΩ
Full Range Current	I_{FR}	V_{REF} = 5.00V R_{11}, R_{10} = 2.500kΩ T_A = 25°C	1.94	1.99	2.04	1.94	1.99	2.04	mA
Full Range Symmetry	I_{FRS}	$I_{FR14} - I_{FR13}$	—	±1	±8	—	±1	±8	μA
Zero-Scale Current	I_{ZS}		—	0.2	2	—	0.2	2	μA
Output Current Range	I_{FSR}	I_{REF} = 3mA	2.1	2.9	—	2.1	2.9	—	mA
Reference Bias Current	I_B		—	−1	−3	—	−1	−3	μA
Power Supply Sensitivity	$PSSI_{FR+}$ $PSSI_{FR-}$	V+ = 4.5V to 5.5V V− = −10.8V to −13.2V I_{REF} = 1mA	— —	±0.0003 ±0.0002	±0.01 ±0.01	— —	±0.0003 ±0.0002	±0.01 ±0.01	$\%\Delta I_{FS}/\%\Delta V+$ $\%\Delta I_{FS}/\%\Delta V-$
Power Supply Current	I+ I−	V_S = +5V, −12V I_{REF} = 0	— —	12 6	16 9	— —	12 6	16 9	mA
Power Dissipation	P_d	+5V, −12V I_{REF} = 0	—	134	190	—	134	190	mW
Logic Input Levels									
Logic Input "0"	V_{IL}		—	—	0.8	—	—	0.8	V
Logic Input "1"	V_{IH}		2	—	—	2	—	—	V
Logic Input Current									
Logic Input "0"	I_{IL}	V_{IN} = 0.8V	—	−2	−10	—	−2	−10	μA
Logic Input "1"	I_{IH}	V_{IN} = 5.0V	—	0.1	1	—	0.1	1	μA

NOTE: Guaranteed by design.

ELECTRICAL CHARACTERISTICS — A.C. PARAMETERS $V_S = +5V, -12V, I_{REF} = 2mA, T_A = 25°C$.

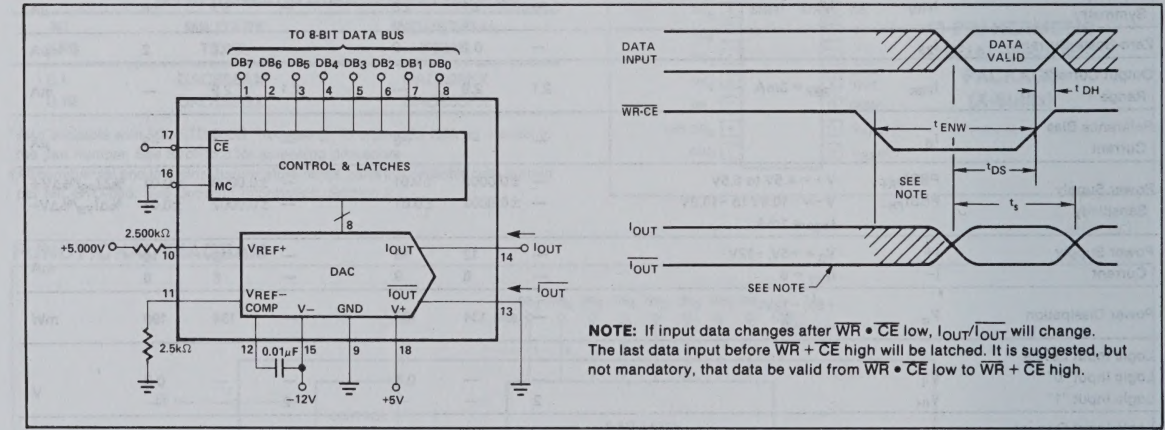
			DAC-888A/E			DAC-888B/F			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Settling Time	t_S	From $\overline{CE}$ & $\overline{WR}$ Negative Level to ±1/2LSB, All Bits Switched ON or OFF, (See note)	—	300	400	—	300	400	ns
Reference Input Slew Rate	dI/dt	(See Note)	4	8	—	4	8	—	mA/μs
Data Input Setup Time	t_{DS}	(See note)	150	—	—	150	—	—	ns
Data Input Hold Time	t_{DH}	(See note)	10	—	—	10	—	—	ns
Chip Enable/Write Pulse Width	t_{ENW}	(See note)	250	—	—	250	—	—	ns

NOTE: Guaranteed by design.

DAC-888 PIN DESCRIPTION

SYMBOL	DESCRIPTION	
DB_0 - DB_7	DATA BIT — Bits 0-7 are digital, active-high inputs. DB_7 is assigned as the MSB.	PINS 1-8
$\overline{CE}$	CHIP ENABLE — An active low input control which is the device enable input terminal.	PIN 17
$\overline{WR}$	WRITE CONTROL — An active low control which enables the microprocessor to write data to the DAC.	PIN 16
$I_{OUT} \bullet \overline{I_{OUT}}$	CURRENT OUTPUT — Complementary current outputs, which when added, equal I_{FS}.	PINS 13-14
V_{REF+}, V_{REF-}	VOLTAGE REFERENCE — Differential inputs that accept a negative, positive, or bipolar input and are used to set I_{FS}.	PINS 10-11
COMP	COMPENSATION — The reference amplifier frequency compensating terminal.	PIN 12

FUNCTIONAL DIAGRAM AND TIMING DIAGRAM FOR 8-BIT OPERATION

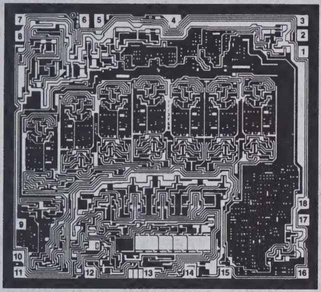

TO 8-BIT DATA BUS
DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
1 2 3 4 5 6 7 8
17
CE
16
MC
CONTROL & LATCHES
8
2.500kΩ
+5.000V
10
VREF+
DAC
IOUT
14
IOUT
11
VREF−
COMP
V−
GND
V+
IOUT
13
IOUT
2.5kΩ
12
0.01μF
15
9
18
−12V
+5V
DATA INPUT
DATA VALID
t DH
WR•CE
t ENW
tDS
SEE NOTE
ts
IOUT
IOUT
SEE NOTE

NOTE: If input data changes after $\overline{WR} \bullet \overline{CE}$ low, $I_{OUT}/\overline{I_{OUT}}$ will change. The last data input before $\overline{WR} + \overline{CE}$ high will be latched. It is suggested, but not mandatory, that data be valid from $\overline{WR} \bullet \overline{CE}$ low to $\overline{WR} + \overline{CE}$ high.

OPERATION TABLE

$\overline{CE}$	$\overline{WR}$	OUTPUT
I	X	NO CHANGE
O	I	NO CHANGE
O	O	UPDATE LATCHES (TRANSPARENT)

DICE CHARACTERISTICS



1. DB7 (MSB)
2. DB6
3. DB5
4. DB4
5. DB3
6. DB2
7. DB1
8. DB0 (LSB)
9. GROUND
10. V_{REF} (+)
11. V_{REF} (−)
12. COMP
13. $\overline{I_{OUT}}$
14. I_{OUT}
15. V−
16. $\overline{WR}$
17. $\overline{CE}$
18. V+

DIE SIZE 0.139 × 0.126 inch; 17, 514 sq. mils (3.53 × 3.2mm.; 11.296 sq. mm.)

For additional DICE information refer to Section 2.

WAFER TEST LIMITS at $V_S = +5, -12V$, $I_{REF} = 2mA$, $T_A = 25°C$, unless otherwise noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

PARAMETER	SYMBOL	CONDITIONS	DAC-888N LIMIT	DAC-888G LIMIT	UNITS
Resolution			8	8	Bits MIN
Monotonicity			8	8	Bits MIN
Nonlinearity			±0.1	±0.19	%FS MAX
Output Voltage Compliance	V_{OC}	Full-Scale Current Change < 1/2 LSB $R_{OUT} > 20 M\Omega$ Typ.	+5 −5	+5 −5	V MAX V MIN
Full Range Current	I_{FR14}	$V_{REF} = 5.00V$ $R_{11}, R_{10} = 2.500k\Omega$ $T_A = 25°C$	2.04 1.94	2.04 1.94	mA MAX mA MIN
Full Range Symmetry	I_{FRS}	I_{FR14}-I_{FR13}	±8	±8	μA MAX
Zero-Scale Current	I_{ZS}		2	2	μA MAX
Output Current Range	I_{FSR}	$I_{REF} = 3mA$	2.1	2.1	mA MIN
Reference Bias Current	I_B		−3	−3	μA MAX
Power Supply Sensitivity	$PSSI_{FR+}$ $PSSI_{FR-}$	V+ = 4.5V to 5.5V V− = −4.5V to −12V $I_{REF} = 1mA$	±0.01 ±0.01	±0.01 ±0.01	$\%\Delta/_{FS}/\%\Delta V+$ MAX $\%\Delta/_{FS}/\%\Delta V-$ MAX
Power Supply Current	I+ I−	$V_S = +5V, -12V$ $I_{REF} = 0$	16 9	16 9	mA MAX
Power Dissipation	P_d	+5V, −12V, $I_{REF} = 0$	190	190	mW MAX
Logic Input Levels Logic Input "0" Logic Input "1"	 V_{IL} V_{IH}		 0.8 2	 0.8 2	 V MAX V MIN
Logic Input Current	I_{IL} I_{IH}	$V_{IN} = 0.8V$ $V_{IN} = 5.0V$	−10 1	−10 1	μA MAX

Note: Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS $V+ = +5V, -12V$, $I_{REF} = 2mA$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-888 TYPICAL	UNITS
Reference Input Slew Rate	dI/dt		8.0	mA/μs
Settling Time	t_S	From $\overline{CE}$ Negative Edge to ±1/2 LSB, All bits Switched ON or OFF	300	ns
Data Input Setup Time	t_{DS}		100	ns
Data Input Hold Time	t_{DH}		0	ns
Chip Enable Write Pulse Width	t_{ENW}		200	ns

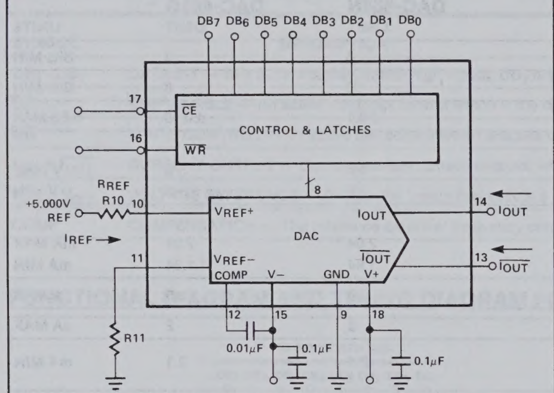
DIGITAL INFORMATION

The BYTEDAC® DAC-888 is a monolithic microprocessor compatible D/A converter consisting of an 8-bit level triggered latch, control circuitry and one 8-bit multiplying D/A converter housed in an 18-pin dual in line package (DIP).

The DAC-888 accepts 8-bit binary bytes at the data inputs. Data access is accomplished when $\overline{WR}$ and $\overline{CE}$ are low. During the low state of $\overline{CE}$ and $\overline{WR}$, the latches are transparent, therefore, data should be valid from 100ns prior to $\overline{WR}$ and $\overline{CE}$ low until $\overline{CE}$ or $\overline{WR}$ high. When $\overline{CE}$ or $\overline{WR}$ goes high, the data stored in the latches will hold the selected output indefinitely.

ANALOG INFORMATION

BASIC POSITIVE REFERENCE OPERATION


DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
17
$\overline{CE}$
CONTROL & LATCHES
16
$\overline{WR}$
8
RREF
R10
+5.000V REF
10
IREF
VREF+
IOUT
DAC
14
IOUT
11
VREF−
COMP
V−
GND
V+
$\overline{IOUT}$
13
$\overline{IOUT}$
12
15
9
18
R11
0.01µF
0.1µF
0.1µF

FOR FIXED REFERENCE, TTL OPERATION TYPICAL VALUES ARE:

$R_{REF} = 2.5000k$
$R11 = R_{REF}$

$$I_{FR} = \frac{+V_{REF}}{R_{REF}} \times \frac{255}{256}$$

$I_{OUT} + \overline{I_{OUT}} = I_{FR}$
FOR ALL LOGIC STATES

REFERENCE AMPLIFIER SET-UP

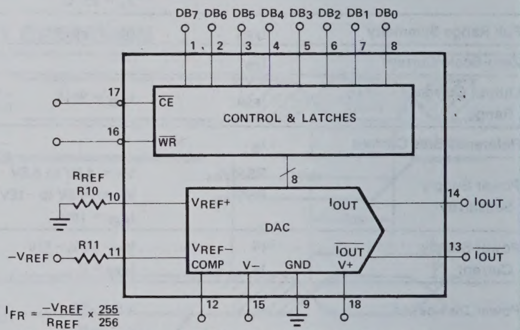
The DAC-888 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly 0 to +4.0mA. The full range output currrent is a linear function of the reference current and is given by:

$$I_{FR} = \frac{255}{256} \times I_{REF} \text{ where } I_{REF} = 1_{10}$$

In positive reference applications, an external positive reference voltage current flows through R_{10} into the $V_{REF(+)}$ terminal of the reference amplifier. Alternatively, a negative reference may be applied to $V_{REF(-)}$; reference current flows from ground through R_{10} into $V_{REF(+)}$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin 11. The voltage at pin 10 is equal to and tracks the voltage at pin 11 due to the high gain of the internal reference amplifier. R_{11} (nominally equal to R_{10}) is used to cancel bias current errors; R_{11} may be eliminated with only a minor increase in error.

For most applications the tight relationship between I_{REF} and I_{FR} will eliminate the need for trimming I_{REF}. If required, full-scale trimming may be accomplished by adjusting the value of R_{10} or by using a potentiometer for R_{10}. An improved method of full-scale trimming which eliminates potentio-

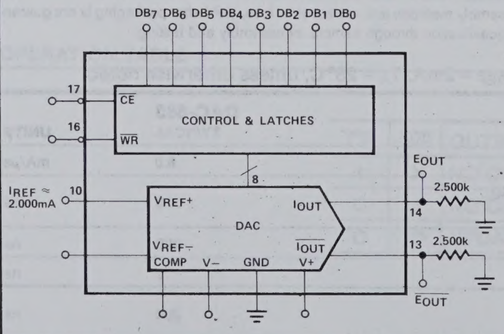
BASIC NEGATIVE REFERENCE OPERATION


DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
1 2 3 4 5 6 7 8
17
$\overline{CE}$
CONTROL & LATCHES
16
$\overline{WR}$
8
RREF
R10
10
VREF+
IOUT
DAC
14
IOUT
R11
−VREF
11
VREF−
COMP
V−
GND
V+
$\overline{IOUT}$
13
$\overline{IOUT}$
12
15
9
18

$$I_{FR} = \frac{-V_{REF}}{R_{REF}} \times \frac{255}{256}$$

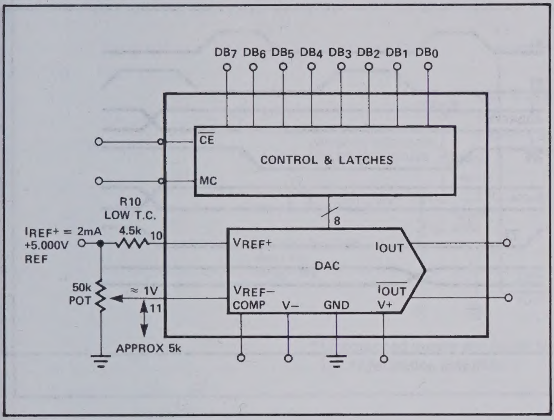
NOTE: R_{REF} SETS I_{FS}: R11 IS FOR BIAS CURRENT CANCELLATION AND IS EQUAL TO R_{REF}.

BASIC UNIPOLAR NEGATIVE OPERATION


DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
17
$\overline{CE}$
CONTROL & LATCHES
16
$\overline{WR}$
8
IREF ≈ 2.000mA
10
VREF+
IOUT
DAC
VREF−
COMP
V−
GND
$\overline{IOUT}$
V+
EOUT
2.500k
14
13
2.500k
$\overline{EOUT}$

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	I_OmA	$\overline{I_O\text{mA}}$	E_O	$\overline{E_O}$
FULL-SCALE	1	1	1	1	1	1	1	1	1.992	0.000	−4.980	0.000
FULL-SCALE −1 LSB	1	1	1	1	1	1	1	0	1.984	0.008	−4.960	−0.020
HALF-SCALE +1 LSB	1	0	0	0	0	0	0	1	1.008	0.984	−2.520	−2.460
HALF-SCALE	1	0	0	0	0	0	0	0	1.000	0.992	−2.500	−2.480
HALF-SCALE −1 LSB	0	1	1	1	1	1	1	1	0.992	1.000	−2.480	−2.500
ZERO-SCALE +1 LSB	0	0	0	0	0	0	0	1	0.008	1.984	−0.020	−4.960
ZERO-SCALE	0	0	0	0	0	0	0	0	0.000	1.992	−0.000	−4.980

RECOMMENDED FULL-SCALE ADJUSTMENT CIRCUIT


DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
CE
MC
CONTROL & LATCHES
8
R10
LOW T.C.
IREF+ = 2mA
+5.000V
REF
4.5k
10
VREF+
IOUT
DAC
VREF−
COMP
V−
GND
IOUT
V+
50k
POT
≈ 1V
11
APPROX 5k

meter TC effects is shown in the Recommended Full Scale Adjustment Circuit.

Using lower values of reference current reduces negative power supply current and increases reference amplifier negative common mode range. The recommended range for operation with a DC reference current is +0.2mA to +4.0mA.

The reference amplifier must be compensated by using a capacitor from pin 12 to V−. For fixed reference operation a 0.01μF capacitor is recommended. For variable reference applications, see "Reference Amplifier Compensation for Multiplying Applications" section.

REFERENCE AMPLIFIER COMPENSATION FOR MULTIPLYING APPLICATIONS

AC reference applications will require the reference amplifier to be compensated using a capacitor from pin 12 to V−. The value of this capacitor depends on the impedance presented to pin 10 (see Table 1).

TABLE 1. REFERENCE AMPLIFIER COMPENSATION

REF. INPUT RESISTANCE	SUGGESTED C_C
1kΩ	15pF
2.5kΩ	37pF
5kΩ	75pF

NOTE: A 0.01μF capacitor is suggested for fixed references.

For fastest response to a pulse, low values of R_{10}, enabling small C_C values, should be used. If pin 10 is driven by a high current source, none of the above values will suffice and the amplifier must be heavily compensated which will decrease overall bandwidth and slew rate. For R_{10} = 1kΩ and C_C = 15pF, the reference amplifier slews at 4mA/μs, enabling a transition from $I_{REF} = 0$ to $I_{REF} = 2mA$ in 500ns (see Figure, pulsed reference operation).

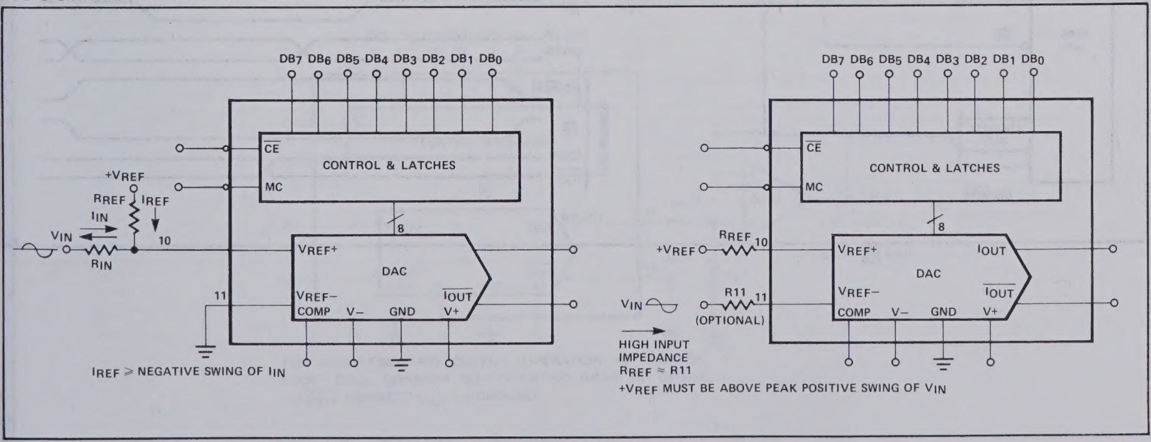
Bipolar references may be accommodated by offsetting V_{REF} or pin 11, as shown in Figure below. The negative common-mode range of the reference amplifier is given by V_{CM} = V− plus (I_{REF} X 1kΩ) plus 2.5V. The positive common-mode range is V+ less 1.5V.

When a DC reference is used, a reference bypass capacitor is recommended. A 5.0V TTL Logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R_{10} should be split into two resistors with the junction bypassed to ground with a 0.1μF capacitor.

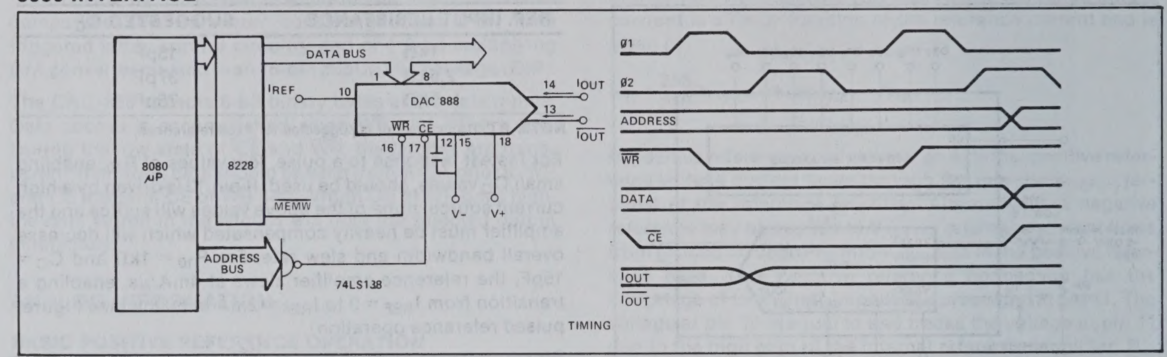
ANALOG OUTPUT CURRENTS

Both true and complemented output sink currents are provided, where $I_O + \overline{I_O} = I_{FR}$. Current appears at the "true" output when a "1" is applied to each logic input. As the binary count increases, the sink current at pin 14 increases proportionally in the fashion of a "positive logic" D/A converter. When a "0" is applied to any input bit, that current is turned off at pin 14 and turned on at pin 13. A decreasing logic count increases $\overline{I_O}$ as in a negative or inverted logic D/A converter. Both outputs may be used simultaneously. If one of the outputs is not required it must still be connected to ground or to a point capable of sourcing I_{FS}; do not leave an unused output pin open.

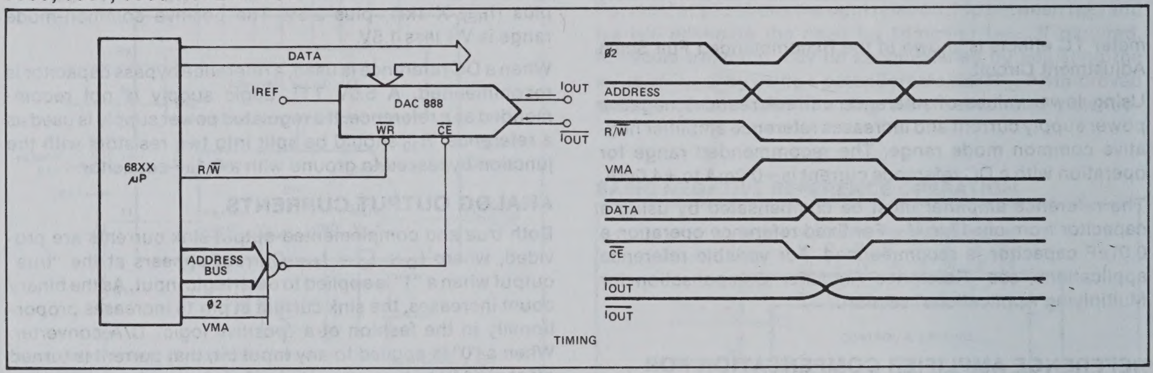
ACCOMMODATING BIPOLAR REFERENCES


DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
CE
MC
CONTROL & LATCHES
8
+VREF
RREF
IREF
IIN
VIN
RIN
10
11
VREF+
DAC
VREF−
COMP
V−
GND
IOUT
V+
IREF ≥ NEGATIVE SWING OF IIN
DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
CE
MC
CONTROL & LATCHES
8
RREF
10
+VREF
R11
11
VIN
(OPTIONAL)
VREF+
IOUT
DAC
VREF−
IOUT
COMP
V−
GND
V+
HIGH INPUT
IMPEDANCE
RREF ≈ R11
+VREF MUST BE ABOVE PEAK POSITIVE SWING OF VIN

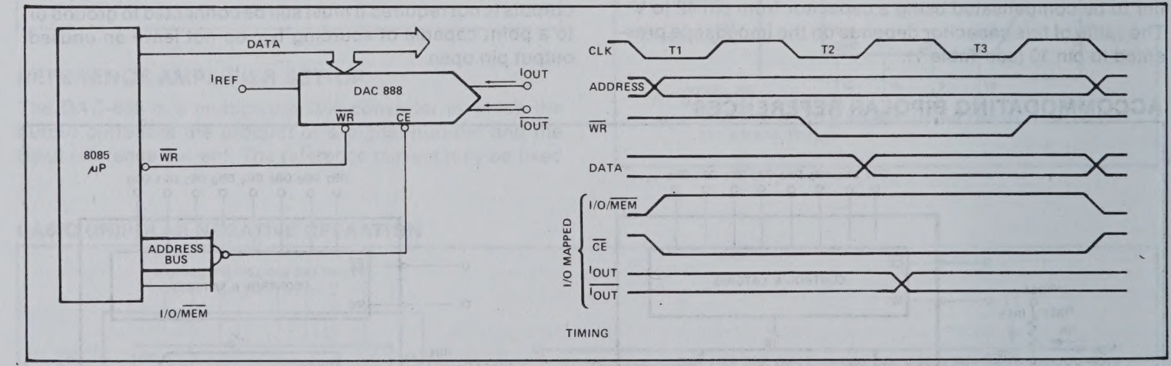
8080 INTERFACE


8080
μP
8228
MEMW
DATA BUS
1
8
IREF
10
DAC 888
14
IOUT
13
IOUT
WR
CE
16
17
12
15
18
V-
V+
ADDRESS BUS
74LS138
Ø1
Ø2
ADDRESS
WR
DATA
CE
IOUT
IOUT
TIMING

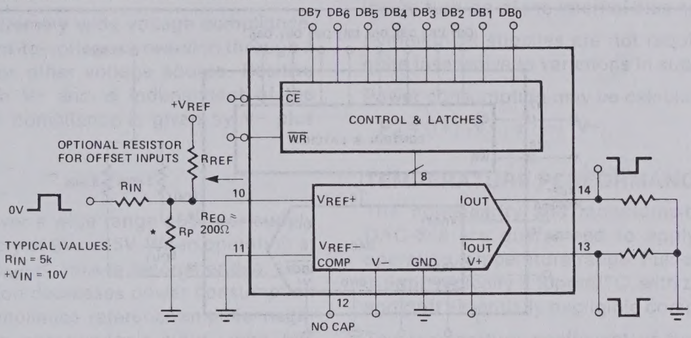
6800, 6801, 6809 INTERFACE


68XX
μP
DATA
IREF
DAC 888
IOUT
IOUT
WR
CE
R/W
ADDRESS BUS
Ø2
VMA
Ø2
ADDRESS
R/W
VMA
DATA
CE
IOUT
IOUT
TIMING

8085 INTERFACE

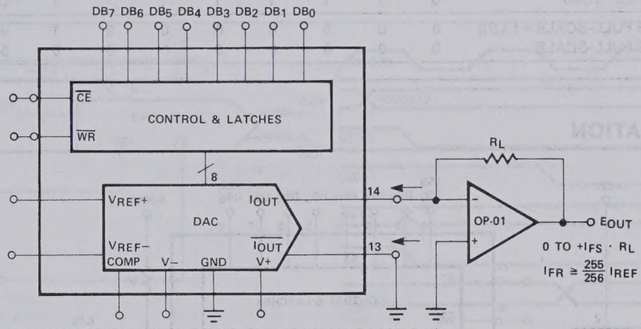

8085
μP
DATA
IREF
DAC 888
IOUT
IOUT
WR
CE
WR
ADDRESS BUS
I/O/MEM
CLK
T1
T2
T3
ADDRESS
WR
DATA
I/O MAPPED
I/O/MEM
CE
IOUT
IOUT
TIMING

PULSED REFERENCE OPERATION


DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
CE
CONTROL & LATCHES
WR
+VREF
OPTIONAL RESISTOR
FOR OFFSET INPUTS
RREF
RIN
0V
10
REQ ≈ 200Ω
*
RP
TYPICAL VALUES:
RIN = 5k
+VIN = 10V
8
VREF+
IOUT
VREF−
COMP
V−
GND
IOUT
V+
11
14
13
12
NO CAP

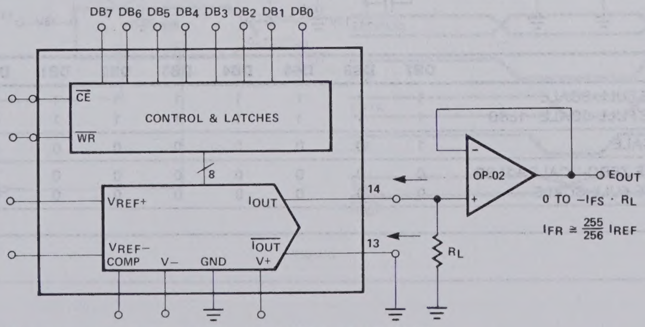
* Unbalanced inputs will cause slight degradation of I_{FS} accuracy due to I_{OS} of reference amplifier.

POSITIVE LOW IMPEDANCE OUTPUT OPERATION


DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
CE
CONTROL & LATCHES
WR
8
VREF+
IOUT
DAC
VREF−
COMP
V−
GND
IOUT
V+
14
13
RL
OP-01
EOUT
0 TO +IFS · RL
IFR ≅ 255/256 IREF

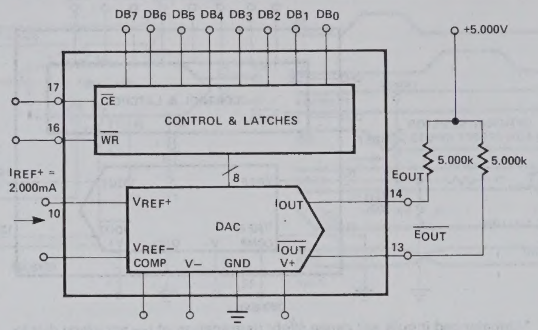
FOR COMPLEMENTARY OUTPUT (OPERATION AS NEGATIVE LOGIC DAC), CONNECT INVERTING INPUT OF OP-AMP TO $\overline{I_{OUT}}$. CONNECT I_{OUT} TO GROUND.

NEGATIVE LOW IMPEDANCE OUTPUT OPERATION


DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
CE
CONTROL & LATCHES
WR
8
VREF+
IOUT
VREF−
COMP
V−
GND
IOUT
V+
14
13
OP-02
EOUT
0 TO −IFS · RL
IFR ≅ 255/256 IREF
RL

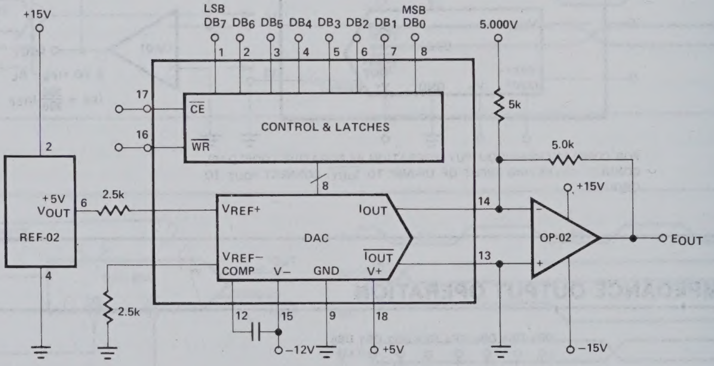
FOR COMPLEMENTARY OUTPUT (OPERATION AS NEGATIVE LOGIC DAC), CONNECT NON-INVERTING INPUT OF OP-AMP TO $\overline{I_{OUT}}$. CONNECT I_{OUT} TO GROUND.

BASIC BIPOLAR OUTPUT OPERATION


DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
+5.000V
17
CE
16
WR
CONTROL & LATCHES
8
IREF+ = 2.000mA
10
VREF+
DAC
IOUT
VREF−
COMP
V−
GND
IOUT
V+
5.000k
5.000k
EOUT
14
EOUT
13

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	E_O	$\overline{E_O}$
POSITIVE FULL-SCALE	1	1	1	1	1	1	1	1	−4.960	5.000
POSITIVE FULL-SCALE −1 LSB	1	1	1	1	1	1	1	0	−4.920	4.960
ZERO-SCALE +1LSB	1	0	0	0	0	0	0	1	−0.040	0.080
ZERO-SCALE	1	0	0	0	0	0	0	0	0.000	0.040
ZERO-SCALE −1LSB	0	1	1	1	1	1	1	1	0.040	0.000
NEGATIVE FULL-SCALE +1 LSB	0	0	0	0	0	0	0	1	4.900	−4.920
NEGATIVE FULL-SCALE	0	0	0	0	0	0	0	0	5.000	−4.960

OFFSET BINARY OPERATION


+15V
LSB
DB7 DB6 DB5 DB4 DB3 DB2 DB1
MSB
DB0
1 2 3 4 5 6 7 8
5.000V
17
CE
16
WR
CONTROL & LATCHES
5k
5.0k
2
+5V
VOUT
REF-02
6
2.5k
4
8
VREF+
IOUT
DAC
14
+15V
OP-02
EOUT
VREF−
COMP
V−
GND
IOUT
V+
13
2.5k
12
15
9
18
−12V
+5V
−15V

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	E_O
POSITIVE FULL-SCALE	1	1	1	1	1	1	1	1	4.960
POSITIVE FULL-SCALE −1LSB	1	1	1	1	1	1	1	0	4.920
ZERO-SCALE	1	0	0	0	0	0	0	0	0.000
NEGATIVE ZERO-SCALE +1LSB	0	0	0	0	0	0	0	1	−4.960
NEGATIVE FULL-SCALE	0	0	0	0	0	0	0	0	−5.000

BASIC BIPOLAR OUTPUT OPERATION

Both outputs have an extremely wide voltage compliance, enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 18V above V− and is independent of the positive supply. Negative compliance is given by V− plus (I_{REF} X 1kΩ) plus 2.5V.

POWER SUPPLIES

The DAC-888 operates over a wide range of power supply voltages from a total supply of 9V to 15V. When operating at supplies of ±5V or less, $I_{REF} \leq$ 1mA is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common-mode range, negative logic input range, and negative logic threshold range; consult the various figures for guidance. For example, operation at −4.5V with I_{REF} = 2mA is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible. However, at least 8V must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the DAC-888 is quite insensitive to variations in supply voltage.

Power consumption may be calculated as follows:

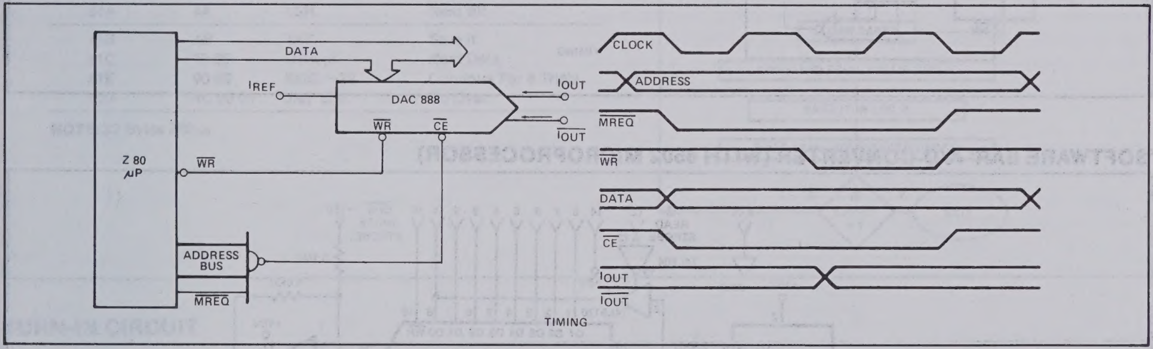
$$P_d = (I+)\,(V+) + (I-)\,(V-).$$

TEMPERATURE PERFORMANCE

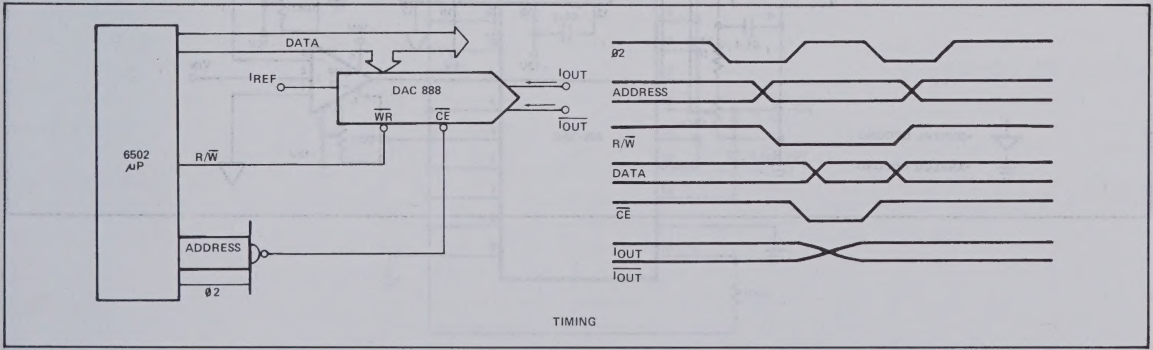
The nonlinearity and monotonicity specifications of the DAC-888 are guaranteed to apply over the entire rated operating temperature range. Full-scale output current drift is tight, typically ±10ppm/°C, with zero scale output current and drift essentially negligible compared to 1/2 LSB.

The temperature coefficient of the reference resistor R_{10} should match and track that of the output resistor for minimum overall full-scale drift. Settling times of the DAC-888 decrease approximately 10% at −55°C; at +125°C an increase of about 15% is typical.

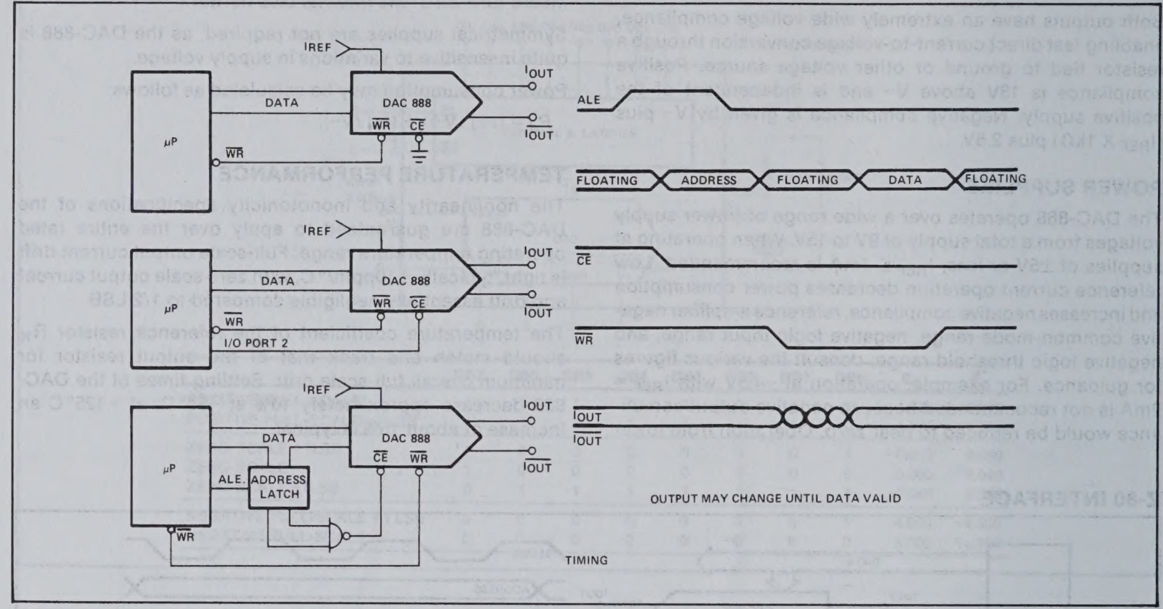
Z-80 INTERFACE


DATA
I_{REF}
DAC 888
$\overline{WR}$
$\overline{CE}$
I_{OUT}
$\overline{I_{OUT}}$
Z 80
µP
$\overline{WR}$
ADDRESS BUS
$\overline{MREQ}$
CLOCK
ADDRESS
$\overline{MREQ}$
$\overline{WR}$
DATA
$\overline{CE}$
I_{OUT}
$\overline{I_{OUT}}$
TIMING

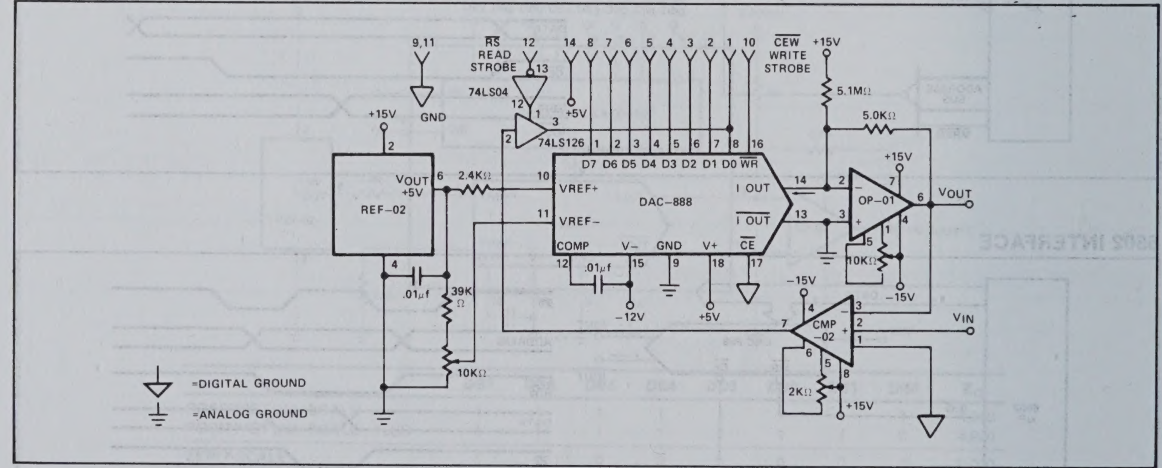
6502 INTERFACE


DATA
I_{REF}
DAC 888
$\overline{WR}$
$\overline{CE}$
I_{OUT}
$\overline{I_{OUT}}$
6502
µP
R/$\overline{W}$
ADDRESS
ø2
ø2
ADDRESS
R/$\overline{W}$
DATA
$\overline{CE}$
I_{OUT}
$\overline{I_{OUT}}$
TIMING

8048 INTERFACE


IREF
IOUT
$\overline{\text{IOUT}}$
DATA
DAC 888
$\overline{\text{WR}}$
$\overline{\text{CE}}$
µP
$\overline{\text{WR}}$
I/O PORT 2
ALE
ADDRESS LATCH
ALE
FLOATING
ADDRESS
FLOATING
DATA
FLOATING
$\overline{\text{CE}}$
$\overline{\text{WR}}$
IOUT
$\overline{\text{IOUT}}$
OUTPUT MAY CHANGE UNTIL DATA VALID
TIMING

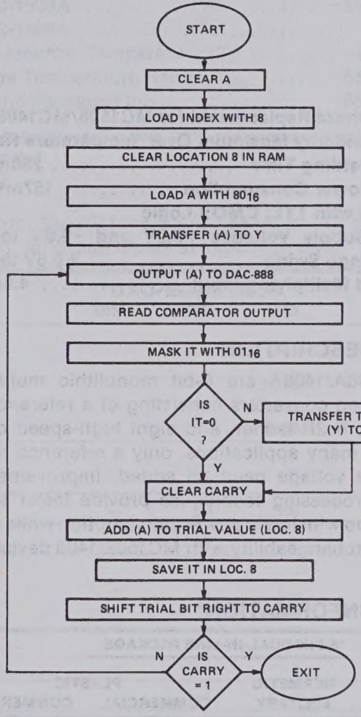
'SOFTWARE SAR' A/D CONVERTER (WITH 6502 MICROPROCESSOR)


9,11
GND
$\overline{\text{RS}}$ READ STROBE
12
13
74LS04
74LS126
14 8 7 6 5 4 3 2 1 10
$\overline{\text{CEW}}$ WRITE STROBE
+15V
+5V
5.1MΩ
5.0KΩ
REF–02
VOUT +5V
2.4KΩ
DAC–888
D7 D6 D5 D4 D3 D2 D1 D0 $\overline{\text{WR}}$
VREF+
VREF–
COMP
V–
GND
V+
$\overline{\text{CE}}$
I OUT
$\overline{\text{I OUT}}$
OP–01
VOUT
10KΩ
–15V
.01µf
39KΩ
10KΩ
–12V
+5V
CMP –02
2KΩ
VIN
=DIGITAL GROUND
=ANALOG GROUND

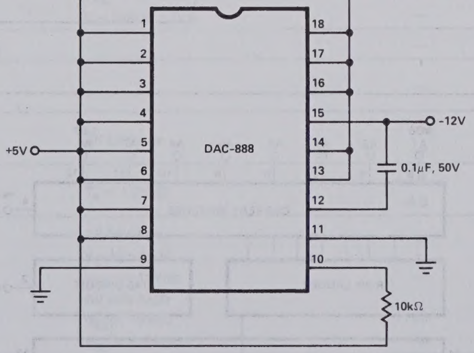
SUCCESSIVE APPROXIMATION ANALOG-TO-DIGITAL CONVERSION PROGRAM LISTING USING DAC-888 AND SYM 1 PCB WITH 6502μP WITH FLOW CHART

```
LOCATION   DATA       MNEMONIC          COMMENTS
500        A9 00      LDA #00           Clear
502        A2 08      LDX #08           Set Index Register
504        95 00      STA ,X            Clear Memory at 08H
506        A9 80      LDA #80           Trial Bit
508        A8         TAY               TO Y
509        8D 00 10   STA 1000 (Cont.)  Output
50C        AD 00 1C   LDA 1C00          Read Comp.
50F        29 01      AND A, #01        Mask it
511        F0 01      BEQ * +1          Branch if CMP = 0
513        98         TYA               Get Trial Bit
514        18         CLC               Clear Carry
515        75 00      ADC ,X            Result Summed With
                                        Previous Test
517        95 00      STA ,X            Save it
519        98         TYA               Get Trial Value
51A        4A         LSR               Next Bit
51B        A8         TAY               Save it
51C        15 00      ORA ,X            Next Data
51E        90 E9      BCC *-23          Continue For 8 Trials
520        4C 00 05   JMP 500           Do Over
```

NOTE: 32 Bytes 260μs


START
CLEAR A
LOAD INDEX WITH 8
CLEAR LOCATION 8 IN RAM
LOAD A WITH 80_{16}
TRANSFER (A) TO Y
OUTPUT (A) TO DAC-888
READ COMPARATOR OUTPUT
MASK IT WITH 01_{16}
IS IT=0 ?
N
TRANSFER TRIAL BIT (Y) TO A
Y
CLEAR CARRY
ADD (A) TO TRIAL VALUE (LOC. 8)
SAVE IT IN LOC. 8
SHIFT TRIAL BIT RIGHT TO CARRY
N
IS CARRY = 1
Y
EXIT

BURN-IN CIRCUIT


1
2
3
4
5
6
7
8
9
18
17
16
15
14
13
12
11
10
DAC-888
+5V
-12V
0.1μF, 50V
10kΩ

DAC-1508A/1408A

8-BIT MULTIPLYING D/A CONVERTERS

FEATURES

- **Improved Direct Replacement for MC1508/MC1408**
- **0.19% Nonlinearity Maximum Over Temperature Range**
- **Improved Settling Time .... 250ns, Typ**
- **Improved Power Consumption .... 157mW, Typ**
- **Compatible with TTL, CMOS Logic**
- **Standard Supply Voltages +5.0V and −5.0V to −15V**
- **Output Voltage Swing .... +0.5V to −5.0V**
- **High-Speed Multiplying Input 4.0mA/μs**

GENERAL DESCRIPTION

The DAC-1508A/1408A are 8-bit monolithic multiplying digital-to-analog converters consisting of a reference current amplifier, R-2R ladder, and eight high-speed current switches. For many applications, only a reference resistor and reference voltage need be added. Improvements in design and processing techniques provide faster settling times combined with lower power consumption while retaining direct interchangeability with MC1508/1408 devices.

The R-2R ladder divides the reference current into eight binarily-related components which are fed to the switches. A remainder current equal to the least significant bit is always shunted to ground, therefore the maximum output current is 255/256 of the reference amplifier input current. For example, a full-scale output current of 1.992mA would result from a reference input current of 2.0mA.

The DAC-1508A/1408A is useful in a wide variety of applications, including waveform synthesizers, digitally programmable gain and attenuation blocks, CRT character generation, audio digitizing and decoding, stepping motor drives, programmable power supplies and in building tracking and successive approximation analog-to-digital converters.

For significantly improved speed and applications flexibility your attention is directed to the DAC-08 8-bit high-speed multiplying D/A converter data sheet. For D/A converters, which include precision voltage references on the chip, please refer to the DAC-210 or the DAC-100 data sheet.

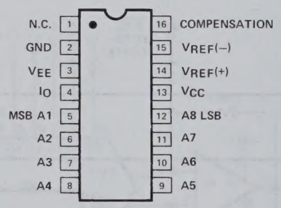
ORDERING INFORMATION†

RELATIVE ACCURACY % FS	16-PIN DUAL-IN-LINE PACKAGE		
	HERMETIC	PLASTIC	
	MILITARY	COMMERCIAL	COMMERCIAL
±0.19%	DAC1508A-8Q*	DAC1408A-8Q	DAC1408A-8P
±0.39%	—	DAC1408A-7Q	DAC1408A-7P
±0.78%	—	DAC1408A-6Q	DAC1408A-6P

*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

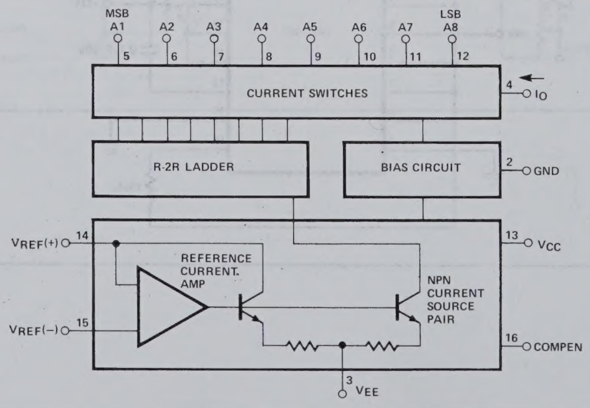
†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

PIN CONNECTIONS



16-PIN DUAL-IN-LINE PACKAGE HERMETIC (Q) EPOXY (P)

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage
V_{CC} .... +5.5Vdc
V_{EE} .... −16.5Vdc
Digital Input Voltage, V_5 through V_{12} .... +5.5, 0Vdc
Applied Output Voltage .... +0.5, −5.2Vdc
Reference Current, I_{14} 5mA
Power Dissipation (Package Limitation), P_d
Ceramic Package (or Epoxy B Package) 100mW
Derate above $T_A = +25°C$ .... 6.7mW/°C
Derate above $T_A = +100°C$ for
Epoxy B Package .... 5.3mW/°C
Operating Temperature Range, T_A
DAC-1508A .... −55°C to +125°C
DAC-1408A .... 0°C to +75°C
DICE Junction Temperature (T_j) .... −65°C to 150°C
Storage Temperature Range, T_{stg} ...... −65°C to +150°C
Plastic Package Only .... −65°C to +125°C

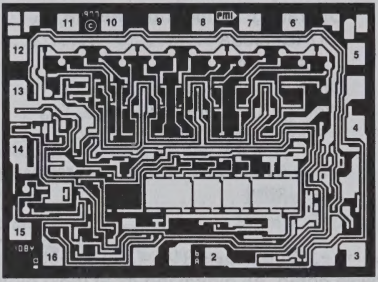
NOTE: Ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_{CC} = +5Vdc$, $V_{EE} = -15Vdc$, $V_{REF}/R14 = 2mA$, $-55°C \leq T_A \leq +125°C$ for DAC-1508A-8, $0°C \leq T_A \leq +75°C$ for DAC-1408A, unless otherwise noted. All digital inputs at logic high level.

PARAMETER	SYMBOL	CONDITIONS	DAC-1508A/1408A MIN	TYP	MAX	UNITS
Relative Accuracy (error relative to Full-Scale I_O)						
DAC-1508A-B, DAC-1408A-8			—	—	±0.19	
DAC-1408A-7	E_r		—	—	±0.39	%IFS
DAC-1408A-6			—	—	±0.78	
Settling Time to within 1/2 LSB (includes t_{PLH})	t_S	$T_A = +25°C$, (Note 1)	—	250	—	ns
Propagation Delay Time	t_{PLH}, t_{PHL}	$T_A = +25°C$, (Note 1)	—	30	100	ns
Output Full-Scale Current Drift	TCI_O		—	±20	—	ppm/°C
Digital Input Logic Levels (MSB)						
High Level, Logic "1"	V_{IH}		2	—	—	Vdc
Low Level, Logic "1"	V_{IL}		—	—	0.8	
Digital Input Current (MSB)	I_{IH}	High Level, $V_{IH} = 5.0V$	—	0	0.04	mA
	I_{IL}	Low Level, $V_{IL} = 0.8V$	—	−0.4	−0.8	
Reference Input Bias Current (Pin 15)	I_{15}		—	−1	−3	μA
Output Current Range	I_{OR}	$V_{EE} = -5V$	0	2.0	2.1	mA
		$V_{EE} = -15V$	0	2.0	4.2	
Output Current	I_O	$V_{REF} = 2.000V$, $R14 = 1000\Omega$	1.9	1.99	2.1	mA
Output Current	$I_{O(min)}$	All bits low	—	0	4	μA
Output Voltage Compliance ($E_r \leq 0.19\%$ at $T_A = +25°C$)	V_O	$I_{REF} = 1mA$				Vdc
		$V_{EE} = -5$	—	—	−0.6, +0.5	
		V_{EE} below −10V	—	—	−5, +0.5	
Reference Current Slew Rate	SRI_{REF}		—	4	—	mA/μs
Output Current Power Supply Sensitivity	$PSSI_{0-}$		—	0.5	2.7	μA/V
Power Supply Current	I_{CC}	All bits low	—	+9	+14	mA
	I_{EE}		—	−7.5	−13	
Power Supply Voltage	V_{CCR}	$T_A = +25°C$	+4.5	+5	+5.5	Vdc
	V_{EER}		−4.5	−15	−16.5	
Power Dissipation	P_d	All bits low				mW
		$V_{EE} = -5Vdc$	—	82	135	
		$V_{EE} = -15Vdc$	—	157	265	
		All bits high				
		$V_{EE} = -5Vdc$	—	70	—	
		$V_{EE} = -15Vdc$	—	132	—	

NOTE:
1. Guaranteed by design.

DICE CHARACTERISTICS



DIE SIZE 0.085 × 0.062 inch, 5270 sq. mils (2.16 × 1.58 mm, 3.39 sq. mm)

1. **N.C.**
2. **GROUND**
3. **V_{EE}**
4. **I_O**
5. **A1 (MSB)**
6. **A2**
7. **A3**
8. **A4**
9. **A5**
10. **A6**
11. **A7**
12. **A8 (LSB)**
13. **V_{CC}**
14. **$V_{REF}(+)$**
15. **$V_{REF}(-)$**
16. **COMP**

For additional DICE information refer to Section 2.

WAFER TEST LIMITS at V+ = 5V, V− = 15V, I_{REF} = 2mA, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-1408A-G LIMIT	UNITS
Resolution			8	Bits MIN
Monotonicity			8	Bits MIN
Nonlinearity			±0.19	%FS MAX
Output Voltage Compliance	V_O	Full-Scale Current Change <1/2 LSB V− = −5V V− below +10V	+0.5 +0.6 0.5	V MAX V MIN V MIN
Full-Scale Current	I_{FS}	V_{REF} = 2.000V, R_{14}, R_{15} = 1.000kΩ	2, ±0.1	mA MAX
Zero-Scale Current	I_{ZS}	(All Bits Low)	4	μA MAX
Output Current Range	I_{OR}	V− = −5V V− = −15V	2.1 4.2	mA MAX
Logic "0" Input Level	V_{IL}		0.8	V MAX
Logic "1" Input Level	V_{IH}		2	V MIN
Logic Input Current Logic "0" Logic "1"	 I_{IL} I_{IH}	 Low Level, V_{IL} = −0.8V High Level, V_{IH} = 5V	 ±10 ±10	μA MAX
Reference Bias Current	I_{15}		-3	μA MAX
Output Current Power Supply Sensitivity	$PSSI_{0-}$		2.7	μA/V MAX
Power Supply Current (All Bits Low)	I+ I−		+14 −13	mA MAX
Power Supply Voltage Range	V_{CCR} V_{EER}		+5, ±0.5 −16.5, −4.5	V MAX/MIN
Power Dissipation (All Bits Low)	P_d	V− = 5V V− = −15V	135 265	mW MAX

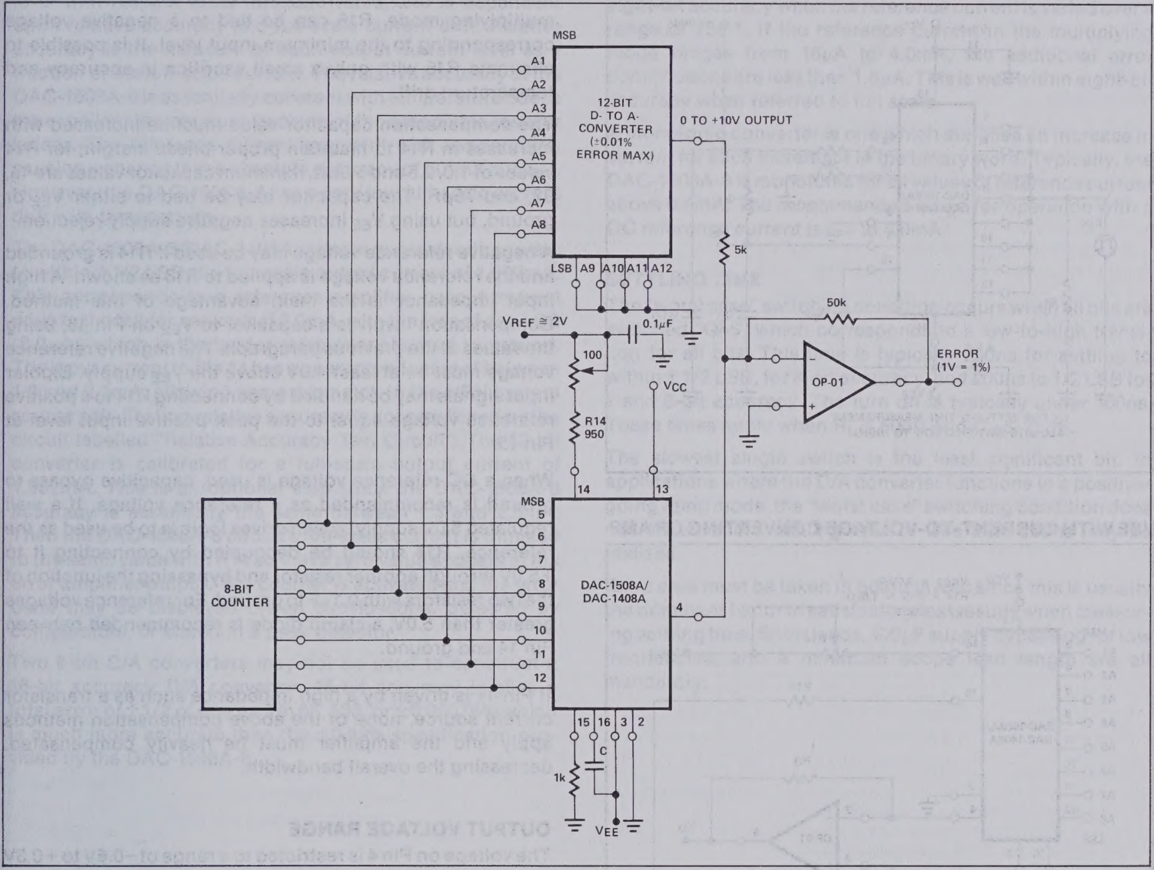
Note: Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at V+ = +5V, V− = −15V, T_A = 25°C, V_{LC} and I_{OUT} connected to ground, and I_{REF} = 2mA, unless otherwise noted. Output characteristics refer to I_{OUT} only.

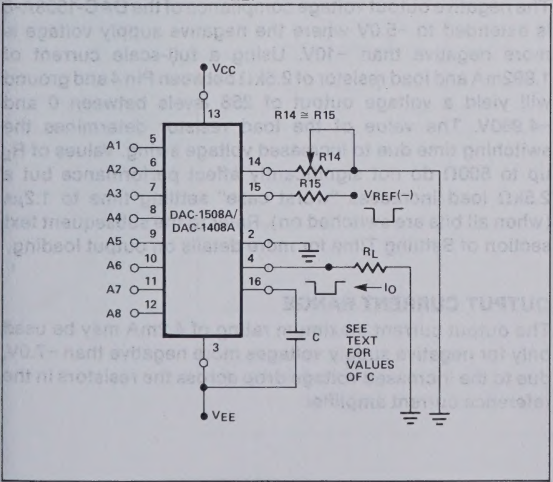
PARAMETER	SYMBOL	CONDITIONS	DAC-1408G TYPICAL	UNITS
Reference Input Slew Rate	dI/dt		4	mA/μs
Propagation Delay	t_{PLH}, t_{PHL}	Any Bit	30	ns
Settling Time	t_S	To ±1/2 LSB, All Bits Switched ON or OFF	250	ns

APPLICATIONS

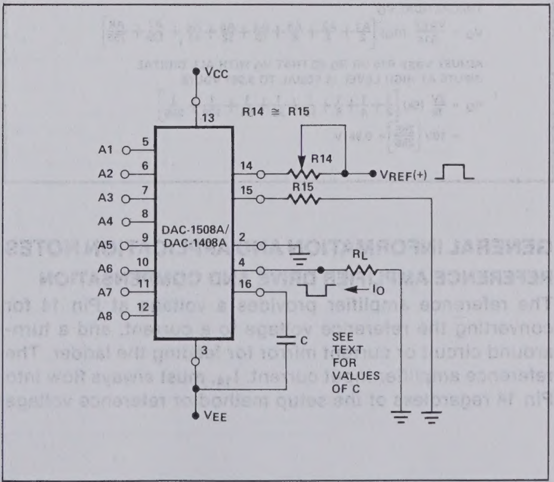
RELATIVE ACCURACY TEST CIRCUIT


MSB
A1
A2
A3
A4
A5
A6
A7
A8
12-BIT
D- TO A-
CONVERTER
(±0.01%
ERROR MAX)
0 TO +10V OUTPUT
LSB
A9
A10
A11
A12
5k
50k
VREF ≅ 2V
0.1μF
100
VCC
OP-01
ERROR
(1V = 1%)
R14
950
14
13
MSB
5
6
7
8
9
10
11
12
8-BIT
COUNTER
DAC-1508A/
DAC-1408A
4
15
16
3
2
C
1k
VEE

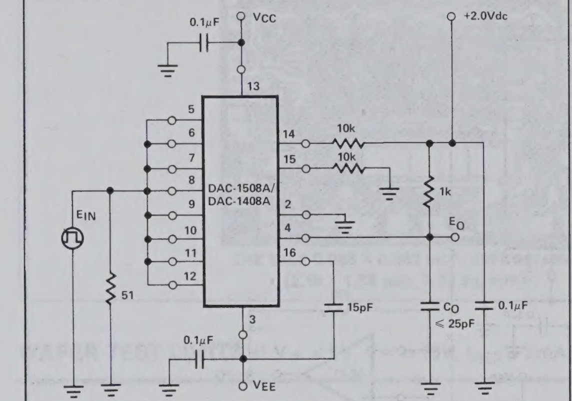
USE WITH NEGATIVE V_{REF}


VCC
13
R14 ≅ R15
A1
A2
A3
A4
A5
A6
A7
A8
5
6
7
8
9
10
11
12
DAC-1508A/
DAC-1408A
14
15
R14
R15
VREF(−)
2
4
16
RL
IO
3
C
SEE
TEXT
FOR
VALUES
OF C
VEE

USE WITH POSITIVE V_{REF}

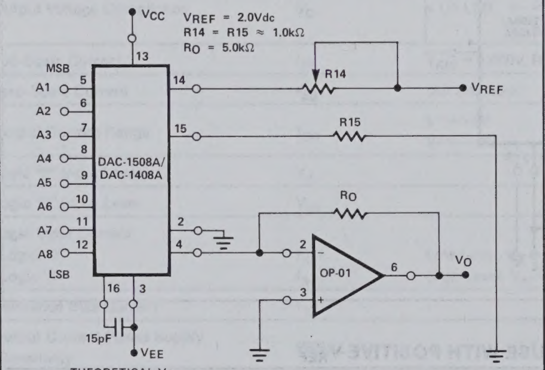

VCC
13
R14 ≅ R15
A1
A2
A3
A4
A5
A6
A7
A8
5
6
7
8
9
10
11
12
DAC-1508A/
DAC-1408A
14
15
R14
R15
VREF(+)
2
4
16
RL
IO
3
C
SEE
TEXT
FOR
VALUES
OF C
VEE

TRANSIENT RESPONSE AND SETTLING TIME TEST CIRCUIT



E_O FOR SETTLING TIME MEASUREMENT
(ALL BITS SWITCHED LOW TO HIGH)

USE WITH CURRENT-TO-VOLTAGE CONVERTING OP AMP



THEORETICAL V_O

$$V_O = \frac{V_{REF}}{R14}(R_O)\left[\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right]$$

ADJUST V_{REF} R15 OR R_O SO THAT V_O WITH ALL DIGITAL INPUTS AT HIGH LEVEL IS EQUAL TO 9.961 VOLTS.

$$V_O = \frac{2V}{1k}(5k)\left[\frac{1}{2}+\frac{1}{4}+\frac{1}{8}+\frac{1}{16}+\frac{1}{32}+\frac{1}{64}+\frac{1}{128}+\frac{1}{256}\right]$$

$$= 10V\left[\frac{255}{256}\right] = 9.961V$$

GENERAL INFORMATION AND APPLICATION NOTES

REFERENCE AMPLIFIER DRIVE AND COMPENSATION

The reference amplifier provides a voltage at Pin 14 for converting the reference voltage to a current, and a turn-around circuit or current mirror for feeding the ladder. The reference amplifier input current, I_{14}, must always flow into Pin 14 regardless of the setup method or reference voltage polarity. Connections for a positive voltage are shown on the preceding page. The reference voltage source supplies the full current I_{14}. For bipolar reference signals, as in the multiplying mode, R15 can be tied to a negative voltage corresponding to the minimum input level. It is possible to eliminate R15 with only a small sacrifice in accuracy and temperature drift.

The compensation capacitor value must be increased with increases in R14 to maintain proper phase margin; for R14 values of 1.0, 2.5 and 5.0kΩ, minimum capacitor values are 15, 37, and 75pF. The capacitor may be tied to either V_{EE} or ground, but using V_{EE} increases negative supply rejection.

A negative reference voltage may be used if R14 is grounded and the reference voltage is applied to R15 as shown. A high input impedance is the main advantage of this method. Compensation involves a capacitor to V_{EE} on Pin 16, using the values of the previous paragraph. The negative reference voltage must be at least 4.0V above the V_{EE} supply. Bipolar input signals may be handled by connecting R14 to a positive reference voltage equal to the peak positive input level at Pin 15.

When a DC reference voltage is used, capacitive bypass to ground is recommended as a reference voltage. If a well regulated 5.0V supply, which drives logic is to be used as the reference, R14 should be decoupled by connecting it to +5.0V through another resistor and bypassing the junction of the two resistors with 0.1μF to ground. For reference voltages greater than 5.0V, a clamp diode is recommended between Pin 14 and ground.

If Pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, decreasing the overall bandwidth.

OUTPUT VOLTAGE RANGE

The voltage on Pin 4 is restricted to a range of −0.6V to +0.5V when $V_{EE} = -5V$ due to the current switching methods employed in the DAC-1508A-8.

The negative output voltage compliance of the DAC-1508A-8 is extended to −5.0V where the negative supply voltage is more negative than −10V. Using a full-scale current of 1.992mA and load resistor of 2.5kΩ between Pin 4 and ground will yield a voltage output of 256 levels between 0 and −4.980V. The value of the load resistor determines the switching time due to increased voltage swing. Values of R_L up to 500Ω do not significantly affect performance but a 2.5kΩ load increases "worst case" settling time to 1.2μs (when all bits are switched on). Refer to the subsequent text section of Settling Time for more details on output loading.

OUTPUT CURRENT RANGE

The output current maximum rating of 4.2mA may be used only for negative supply voltages more negative than −7.0V, due to the increased voltage drop across the resistors in the reference current amplifier.

ACCURACY

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy and full-scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full-scale current. The relative accuracy of the DAC-1508A-8 is essentially constant with temperature due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current. However, the DAC-1508A-8 has a very low full-scale current drift with temperature.

The DAC-1508A-8/DAC-1408A series is guaranteed accurate to within ±1/2 LSB at a full-scale output current of 1.992mA. This corresponds to a reference amplifier output current drive to the ladder network of 2.0mA, with the loss of one LSB (8.0μA), which is the ladder remainder shunted to ground. The input current to Pin 14 has a guaranteed value of between 1.9 and 2.1mA, allowing some mismatch in the NPN current source pair. Testing relative accuracy is accomplished by the circuit labelled "Relative Accuracy Test Circuit". The 12-bit converter is calibrated for a full-scale output current of 1.992mA. This is an optional step since the DAC-1508A-8 accuracy is essentially the same between 1.5 and 2.5mA. Then the DAC-1508A-8 circuit's full-scale current is trimmed to the same value with R14 so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D/A converters may not be used to construct a 16-bit accuracy D/A converter. 16-bit accuracy implies a total error of ±1/2 of one part in 65, 536, or ±0.00076% which is much more accurate than the ±0.19% specification provided by the DAC-1508A-8.

MULTIPLYING ACCURACY

The DAC-1508A-8 may be used in the multiplying mode with eight-bit accuracy when the reference current is varied over a range of 256:1. If the reference current in the multiplying mode ranges from 16μA to 4.0mA, the additional error contributions are less than 1.6μA. This is well within eight-bit accuracy when referred to full scale.

A monotonic converter is one which supplies an increase in current for each increment in the binary word. Typically, the DAC-1508A-8 is monotonic for all values of reference current above 0.5mA. The recommended range for operation with a DC reference current is 0.5 to 4.0mA.

SETTLING TIME

The "worst case" switching condition occurs when all bits are switched "ON", which corresponds to a low-to-high transition for all bits. This time is typically 250ns for settling to within ±1/2 LSB, for 8-bit accuracy, and 200ns to 1/2 LSB for 7 and 6-bit accuracy. The turn off is typically under 100ns. These times apply when $R_L \leq 500\Omega$ and $C_O \leq 25pF$.

The slowest single switch is the least significant bit. In applications where the D/A converter functions in a positive-going ramp mode, the "worst case" switching condition does not occur, and a settling time of less than 250ns may be realized.

Extra care must be taken in board layout since this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, 100μF supply bypassing for low frequencies, and a minimum scope lead length are all mandatory.

PM-562 12-BIT MULTIPLYING D/A CONVERTER

PRELIMINARY

FEATURES

- **Single-Chip Monolithic Construction**
- **Binary Model, Positive Logic**
- **Nonlinearity to ±1/4 LSB (Max)**
- **Settling Time .... 1.5μs (Typ)**
- **Fits AD562 Socket Directly**
- **Guaranteed Monotonicity**
- **High-Speed Multiplying Capability**
- **TTL and CMOS Logic Input Capability**
- **Low Power Consumption**
- **Low Cost**
- **MIL-STD-883 Level B Model Available**

GENERAL DESCRIPTION

The PM-562 is a 12-bit monolithic multiplying digital-to-analog converter consisting of a reference current amplifier, an R-2R ladder network, range and offset scaling resistors, and 12 high-speed current switches. Improvements over the AD562 include lower power dissipation, greater negative power supply range, increased output resistance and lower zero-scale current. The PM-562 is pin equivalent with the AD562.

The PM-562 uses a unique trimming method; selective shorting of zener diodes by avalanche migration, to achieve 13-bit accuracy rather than laser trimming. Reliability of this trimming method has been proven in several other PMI products with over nine years of reliability history. The PM-562 is recommended for 12-bit accuracy D/A applications where single-chip reliability, small size and low cost are primary considerations.

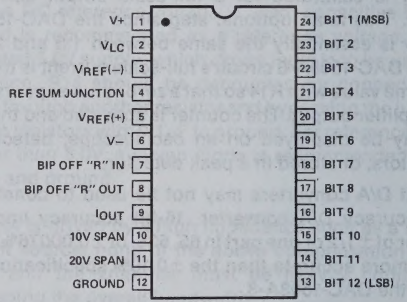
ORDERING INFORMATION†

PMI MODEL NO.	ADI MODEL NO.	TEMP. RANGE
PM562AV*	AD562SD/BIN	−55°/+125°C
PM562AV/883*	AD562SD/BIN/883	−55°/+125°C
PM562EV	AD562AD/BIN	−25°/+85°C
PM562FV	AD562KD/BIN	0°/+70°C

*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

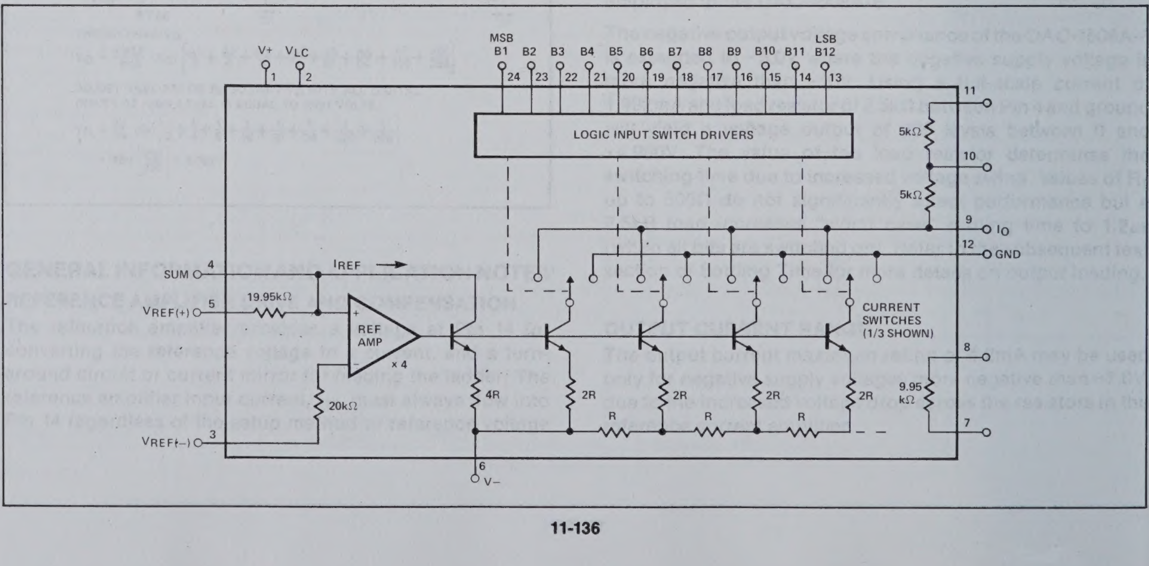
PIN CONNECTIONS



V+ 1
VLC 2
VREF(−) 3
REF SUM JUNCTION 4
VREF(+) 5
V− 6
BIP OFF "R" IN 7
BIP OFF "R" OUT 8
IOUT 9
10V SPAN 10
20V SPAN 11
GROUND 12
24 BIT 1 (MSB)
23 BIT 2
22 BIT 3
21 BIT 4
20 BIT 5
19 BIT 6
18 BIT 7
17 BIT 8
16 BIT 9
15 BIT 10
14 BIT 11
13 BIT 12 (LSB)

TOP VIEW
24-PIN HERMETIC DIP

EQUIVALENT CIRCUIT



V+
VLC
1
2
MSB
B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12
LSB
24 23 22 21 20 19 18 17 16 15 14 13
LOGIC INPUT SWITCH DRIVERS
11
5kΩ
10
5kΩ
9
IO
12
GND
SUM 4
IREF
VREF(+) 5
19.95kΩ
REF AMP
x 4
20kΩ
4R
2R
2R
2R
2R
R
R
R
CURRENT SWITCHES (1/3 SHOWN)
8
9.95 kΩ
7
VREF(−) 3
6
V−

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	
PM-562A	−55°C to +125°C
PM-562E	−25°C to +85°C
PM-562F	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Power Dissipation	500mW
Derate Above 100°C	10mV/°C
Lead Temperature (Soldering, 60 sec)	300°C

Positive Power Supply (V+)	36V minus V−
Negative Power Supply (V−)	−36V plus V+
V+ to V−	36V
Logic Inputs	V− to V− plus +36V
Summing Junction (Pin 4)	V− to V+
CMOS/TTL Threshold (Pin 2)	V− to V+
I_{OUT} (Pin 9)	+18 to −5V
Span Resistors	36V

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $V_{REF} = +10.0000V$, $T_A = +25°C$, unless otherwise noted.

			PM-562A			PM-562E			PM-562F			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Resolution		T_A = Full Range	12	—	—	12	—	—	12	—	—	Bits
Monotonicity		T_A = Full Range	12	—	—	12	—	—	12	—	—	Bits
Nonlinearity	NL		—	—	±1/4	—	—	±1/2	—	—	±1/2	LSB
Differential Nonlinearity	DNL		—	—	±1/2	—	—	±1/2	—	—	±1/2	LSB
Settling Time	t_S	To ±1/2 LSB, all bits ON or OFF, current into short circuit.	—	1.5	—	—	1.5	—	—	1.5	—	μs
Voltage Noise (All bits ON)	E_n	0.1Hz to 10Hz	—	30	—	—	30	—	—	30	—	μV_{p-p}
Output Voltage Compliance	V_{OC}		−1.5	—	+10	−1.5	—	+10	−1.5	—	+10	V
Output Current Range I_{REF} = 0.5mA	I_{OR}	Unipolar Bipolar	−1.6 ±0.8	−2 ±1	−2.4 ±1.2	−1.6 ±0.8	−2 ±1	−2.4 ±1.2	−1.6 ±0.8	−2 ±1	−2.4 ±1.2	mA
Output Resistance	R_O		—	2	—	—	2	—	—	2	—	MΩ
Output Capacitance			—	30	—	—	30	—	—	30	—	pF
Zero-Scale Current	I_{ZS}	All bits OFF	—	0.01	0.05	—	0.01	0.05	—	0.01	0.05	%FS
Logic Inputs — TTL, V+ = 5V, Pin 3 Ground	V_{IH} V_{IL}	I_{IH} = 100nA (Max) I_L = 100μA (Max)	2 —	— —	— 0.8	2 —	— —	— 0.8	2 —	— —	— 0.8	V
Logic Inputs — CMOS, 4.75V ≤ V+ ≤ 15.8V, Pin 2 to Pin 1	V_{IH} V_{IL}	I_{IH} = 100nA (Max) I_{IL} = 100μA (Max)	70 —	— —	— 30	70 —	— —	— 30	70 —	— —	— 30	%V+
Reference Voltage Input	Z_{IN} V_{RR}	 Range (Nominal)	— −5	20 —	— 10	— −5	20 —	— 10	— −5	20 —	— 10	kΩ V
External Adjustment Range		(See last page)	—	±0.25	—	—	±0.25	—	—	±0.25	—	%
Power Supply Requirements	I+ I−	V+, 4.75V to 15.8V V−, −13.5V to −16.5V	— —	7 −5	18 −25	— —	7 −5	18 −25	— —	7 −5	18 −25	mA
Power Supply Sensitivity of Gain		V+ = +5V V+ = +15V V− = −15V	— —	— —	2 6	— —	— —	2 6	— —	— —	2 6	ppmFS/%

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $V_{REF} = +10.0000V$, $-55°C \le T_A \le +125°C$ for PM-562A, $-25°C \le T_A \le +85°C$ for PM-562E, $0°C \le T_A \le +75°C$ for PM-562F, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-562A MIN	PM-562A TYP	PM-562A MAX	PM-562E MIN	PM-562E TYP	PM-562E MAX	PM-562F MIN	PM-562F TYP	PM-562F MAX	UNITS
Zero-Scale Temperature Coefficient	TC_{ZS}	Leakage Current	—	—	2	—	—	2	—	—	2	ppmFS/°C
Bipolar Offset Temperature Coefficient			—	—	4	—	—	4	—	—	4	ppmFS/°C
Gain Temperature Coefficient		Excludes V_{REF}	—	—	5	—	—	5	—	—	5	ppmFS/°C
Differential Nonlinearity Temperature Coefficient			—	2	—	—	2	—	—	2	—	ppmFS/°C

MULTIPLYING ELECTRICAL CHARACTERISTICS at $T_A = +25°C$ (All Models)

Parameter	Description	Typical	Units
Quadrants	Two-quadrant: bipolar operation is achieved using the digital inputs only.	—	—
Reference Voltage	Unipolar: Digital input multiplies reference voltage.	0 to +10	V
Accuracy	10 bits for reduced reference voltage of +1V.	±0.05	%FS
Reference Feedthrough (Unipolar Mode)	All bits OFF, 0 to +10V (p-p) sinewave frequency for 1/2 LSB (p-p) feedthrough.	2	kHz
Output Slew Rate	All bits ON, 10V step change in reference voltage.	1	mA/µsec
Output Settling Time	All bits ON, 10V step change in reference voltage, to ±0.01%FS.	5	µsec
Reference Amplifier Bandwidth	Closed-loop, small-signal	1	MHz

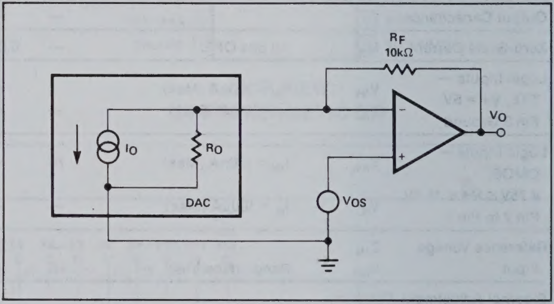
OUTPUT RESISTANCE ERROR

The D/A converter equivalent circuit and output voltage equations show that a low output resistance (R_O) can provide a significant error term due to V_{OS} drift of the output amplifier. Note that the higher R_O (2MΩ) offered by the PM-562 gives an apparent V_{OS} drift that is one-half as large as that resulting from the 8kΩ R_O of the standard AD562 and one-tenth as large as that of the HI563 ($R_O = 1kΩ$) when using a 10kΩ span resistor (R_F).

$$\Delta V_O = \Delta I_O R_F + \Delta V_{OS}$$

$$\text{Since: } \Delta I_O = \Delta V_{OS}/R_O$$

$$\text{Then: } \Delta V_O = \Delta V_{OS}(R_F/R_O + 1)$$



ADJUSTMENT PROCEDURES

BIPOLAR OFFSET

With all bits OFF, adjust R1 until op amp output is −2.5V on ±2.5V range, −5V on ±5V range, or −10V on ±10V range.

UNIPOLAR OFFSET

With all bits OFF, adjust R4 until op amp output is 0V. R1 and the connection from Pin 8 to Pin 9 are not required.

BIPOLAR BINARY GAIN

Turn Bit 1 (MSB) ON. Turn Bits 2 through 12 OFF. Adjust R2 until output is 0V.

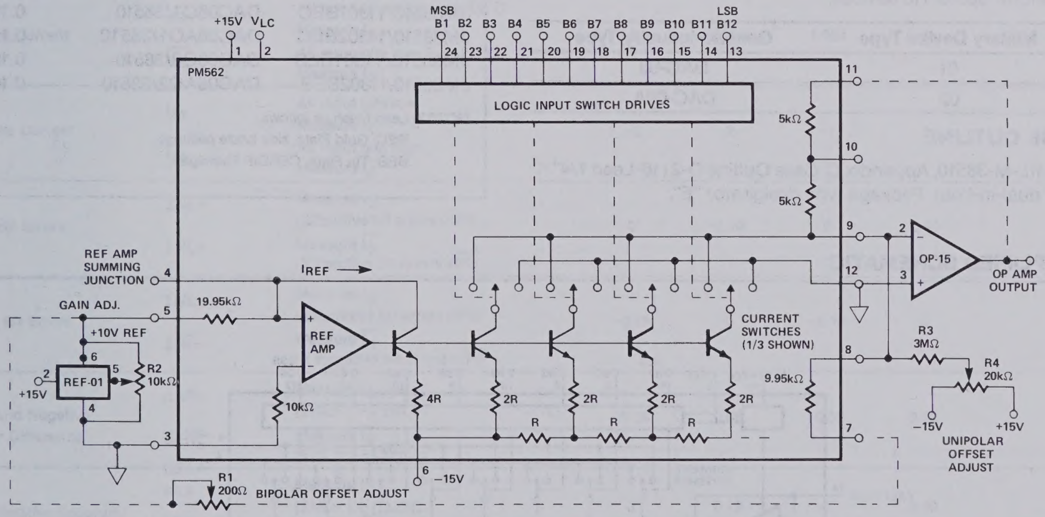
UNIPOLAR BINARY GAIN

Turn all bits ON. Adjust R2 until op amp output is +4.9988V for 0 to +5V range, or +9.9976V for 0 to +10V range.

CONNECTION TABLE FOR VARIOUS VOLTAGE RANGES

RANGE	OP AMP	CONNECTIONS	
−2.5V TO +2.5V	OUT TO PIN 10	PIN 11 TO PIN 9	R1 AS BELOW
−5V TO +5V	OUT TO PIN 10	N.C. TO PIN 11	R1 AS BELOW
−10V TO +10V	OUT TO PIN 11	N.C. TO PIN 10	R1 AS BELOW
0 TO +5V	OUT TO PIN 10	PIN 11 TO PIN 9	R4 AS BELOW
0 TO +10V (NOTE 4)	OUT TO PIN 7, 11	PIN 8 TO PIN 9	R4 AS BELOW

CONNECTION DIAGRAM



+15V
VLC
MSB
B1
B2
B3
B4
B5
B6
B7
B8
B9
B10
B11
LSB
B12
1
2
24
23
22
21
20
19
18
17
16
15
14
13
PM562
LOGIC INPUT SWITCH DRIVES
11
5kΩ
10
5kΩ
9
2
OP-15
3
12
OP AMP OUTPUT
REF AMP SUMMING JUNCTION
4
IREF
GAIN ADJ.
5
19.95kΩ
+10V REF
6
REF AMP
REF-01
+15V
R2 10kΩ
4
10kΩ
4R
2R
2R
2R
2R
R
R
R
CURRENT SWITCHES (1/3 SHOWN)
8
R3 3MΩ
R4 20kΩ
9.95kΩ
7
−15V
+15V
UNIPOLAR OFFSET ADJUST
3
6
−15V
R1 200Ω
BIPOLAR OFFSET ADJUST

NOTES:

1. For TTL and DTL inputs, connect +5V to Pin 1. Pin 2 may be grounded or left open.
2. For low voltage CMOS, connect +5V to Pin 1; short Pin 2 to Pin 1.
3. For high voltage CMOS, connect +15V to Pin 1; short Pin 2 to Pin 1.
4. To minimize thermal effects on nonlinearity, all units are tested in the unipolar mode with span/offset resistors connected in parallel. This connection is recommended for precision 10 volt unipolar applications. The alternative connection using a single 5k resistor may be used but typically will result in linearity degradations up to 0.1 LSB.

JM38510/11301/11302

JAN 8-BIT MULTIPLYING D/A CONVERTER

GENERAL DESCRIPTION

This data sheet covers the electrical requirements of the monolithic 8-bit digital-to-analog converters found in MIL-M-38510/113. Devices supplied to this data sheet are manufactured and tested at PMI's MIL-M-38510 certified facility and are listed in QPL-38510.

Complete device requirements will be found in MIL-M-38510 and MIL-M-38510/113 for Class B processed devices.

Device Types shall be as follows:
01 D/A Converter, 8 bit, 0.19% linearity
02 D/A Converter, 8 bit, 0.10% linearity

GENERIC CROSS-REFERENCE INFORMATION

This cross-reference information is presented for the convenience of the user. The Generic-Industry types listed may not have identical operational performance characteristics across the military temperature range or reliability factors equivalent to the MIL-M-38510/113 devices.

Military Device Type	Generic-Industry Type
01	DAC-08
02	DAC-08A

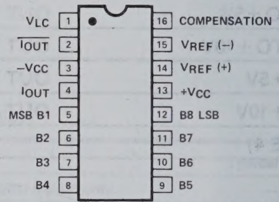
CASE OUTLINE

Per MIL-M-38510, Appendix C, Case Outline D-2 (16-Lead 1/4" × 7/8", dual-in-line). Package type designator "E".

POWER AND THERMAL CHARACTERISTICS

Package	Case outline	Maximum allowable power dissipation	Maximum θJ — C	Maximum θJ — A
Dual-in-line	E	400mW at T_A = 125°C	35°C/W	120°C/W

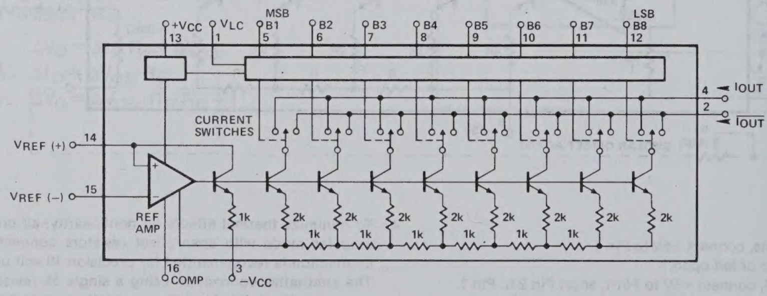
PIN CONNECTIONS & ORDERING INFORMATION


VLC 1
$\overline{\text{IOUT}}$ 2
–VCC 3
IOUT 4
MSB B1 5
B2 6
B3 7
B4 8
16 COMPENSATION
15 VREF (–)
14 VREF (+)
13 +VCC
12 B8 LSB
11 B7
10 B6
9 B5

Jan Device Type	PMI Device Type	Linearity
JM38510/11301BEC	DAC08Q1/38510	0.19%
JM38510/11302BEC	DAC08AQ1/38510	0.10%
JM38510/11301BEB	DAC08Q2/38510	0.19%
JM38510.11302BEB	DAC08AQ2/38510	0.10%

NOTES: Lead finish as follows
BEC: Gold Plate, side braze package
BEB: Tin Plate, CERDIP Package

SIMPLIFIED SCHEMATIC


+VCC 13
VLC 1
MSB B1 5
B2 6
B3 7
B4 8
B5 9
B6 10
B7 11
LSB B8 12
4 IOUT
2 $\overline{\text{IOUT}}$
CURRENT SWITCHES
VREF (+) 14
VREF (–) 15
REF AMP
1k
2k
16 COMP
3 –VCC

ABSOLUTE MAXIMUM RATINGS

Supply Voltage $[+V_{CC}-(-V_{CC})]$ 36Vdc
Voltage, Digital Input to Negative Supply
$[V_{logic}-(-V_{CC})]$ .... 0 to 36Vdc
Voltage, Logic Control (V_{LC}) .... $-V_{CC}$ to $+V_{CC}$
Reference Voltage Input $[(V_{14}, V_{15})]$ .... $-V_{CC}$ to $+V_{CC}$
Reference Input Current (I_{14}) 5mA
Reference Input Differential Voltage
$[(V_{14}-V_{15})]$ .... ±18Vdc
Lead Temperature (Soldering, 60 sec) .... 300° C
Junction Temperature .... 175° C
Storage Temperature .... −65° C to +150° C

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range .... ±5Vdc to ±15Vdc*
Ambient Temperature Range .... −55° C to +125° C

***NOTE:**
A slight degradation in linearity can occur when the supply voltage is near the ±5V end of the recommended operating range.

ELECTRICAL CHARACTERISTICS at $\pm V_{CC}=\pm 15$Vdc; Source resistance = 50 ohms; $I_{REF}=2.$mA; Figure 1; Ambient temperature range = −55° C to +125° C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	01 LIMITS MIN	01 LIMITS MAX	02 LIMITS MIN	02 LIMITS MAX	UNITS
Monotonicity	$\Delta(i)$	Measure I_O, $(\overline{I_{ON}}-I_{ON-1})\geq 0$ at each major carry point	0	16	0	16	µA
	$\Delta(\overline{i})$	Measure $\overline{I_O}$, $(\overline{I_{ON}}-\overline{I_{ON-1}})\geq 0$ at each major carry point	0	16	0	16	
Output Symmetry	ΔI_{FS}	$I_{FS}-\overline{I_{FS}}$	−8	8	−4	4	µA
Full-Scale Current Temperature Coefficient	$T_C(I_{FS})$ $\overline{T_C(I_{FS})}$	All input bits high, Measure I_O All input bits low, Measure $\overline{I_O}$	−50	50	−50	50	ppm/° C
Full-Scale Current	I_{FS} $\overline{I_{FS}}$	All input bits high, $T_A=25°$ C Measure I_O All input bits low, $T_A=25°$ C Measure $\overline{I_O}$	1.94	2.04	1.984	2	mA
Zero-Scale Current	I_{ZS} $\overline{I_{ZS}}$	All input bits low Measure I_O All input bits high, Measure $\overline{I_O}$	−2	2	−1	1	µA
Positive Bit Errors	$\Sigma NL+$ $\Sigma\overline{NL}+$	Measure I_O (ΣPositive bit errors)/IFS Measure $\overline{I_O}$ (Σ Positive bit errors)/$\overline{IFS}$	0	0.19	0	0.10	%
Negative Bit Errors	$\Sigma NL-$ $\Sigma\overline{NL}-$	Measure I_O (ΣNegative bit errors)/IFS Measure $\overline{I_O}$ (Σ Negative bit errors)/$\overline{IFS}$	−0.19	0	−0.10	0	%
Positive and Negative Bit Error Difference	$\Delta\Sigma NL$ $\Delta\Sigma\overline{NL}$	Measure I_O $\lvert\Sigma NL+\rvert-\lvert\Sigma NL-\rvert$ Measure $\overline{I_O}$ $\lvert\Sigma\overline{NL}+\rvert-\lvert\Sigma\overline{NL}-\rvert$	−0.05	0.05	−0.03	0.03	%
Positive Relative Accuracy	$NL+$ $\overline{NL}+$	Measure I_O $\lvert\Sigma NL+\rvert+\lvert\Delta\Sigma NL\rvert$ Measure $\overline{I_O}$ $\lvert\Sigma\overline{NL}+\rvert+\lvert\Delta\Sigma\overline{NL}\rvert$	0	0.19	0	0.10	%
Negative Relative Accuracy	$NL-$ $\overline{NL}-$	Measure I_O $\lvert\Sigma NL-\rvert+\lvert\Delta\Sigma NL\rvert$ Measure $\overline{I_O}$ $\lvert\Sigma\overline{NL}-\rvert+\lvert\Delta\Sigma\overline{NL}\rvert$	0	0.19	0	0.10	%

Bit Error
Bit error is the deviation of the analog output from its ideal value (after zero-scale and full-scale errors have been calibrated out) when turning on an individual bit. This is measured for all n bits.

Bit error (analog value) $= V_n-(FSR/2^n)$
Where V_n = analog output with bit n on only.
FSR = full-scale range
n = number of bits

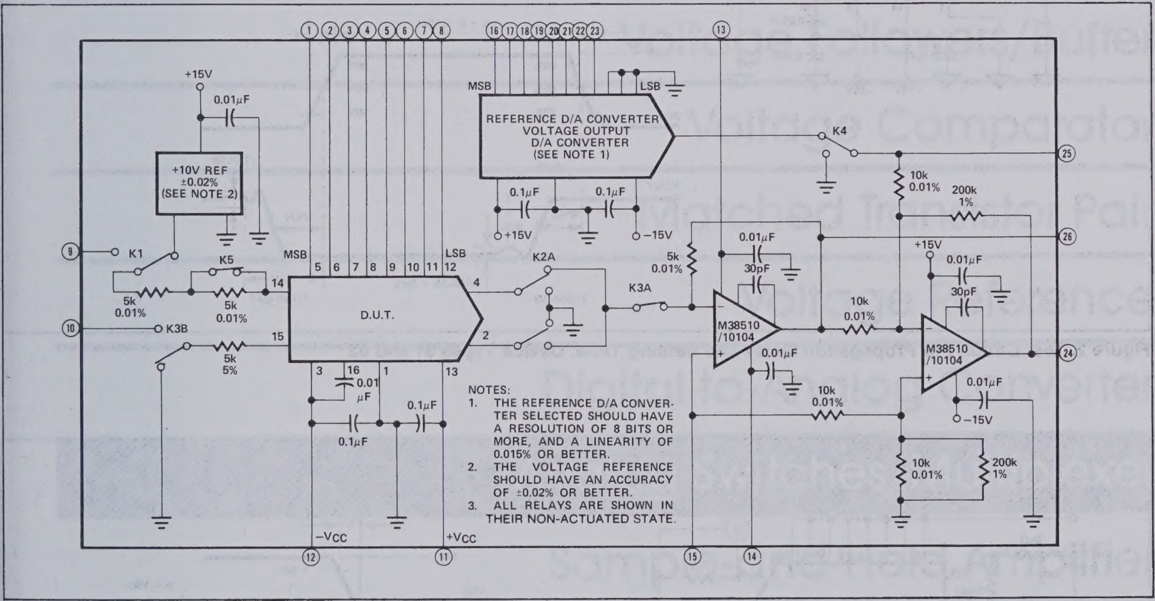
Summation Nonlinearity (ΣNL)
Summation nonlinearity is the sum of all positive bit errors or all negative bit errors, whichever is larger. By summing up all the bit errors in one direction, you obtain the worst possible nonlinearity (i.e. if bit 2 is 1 LSB high and bit 4 is 1/2 LSB high, then bits 2 and 4 together will be 1 1/2 LSBs high. This is essentially the same as integral nonlinearity since the bit errors are superimposed on each other to give the worst case nonlinearity.

ELECTRICAL CHARACTERISTICS at ±V_{CC} = ±15Vdc; Source resistance = 50 ohms; I_{REF} = 2.0mA; Figure 1; Ambient temperature range = −55° C to +125° C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	01 LIMITS MIN	01 LIMITS MAX	02 LIMITS MIN	02 LIMITS MAX	UNITS
Output Current Range	$I_{FS}R_1$	All input bits high, Measure I_O, $-V_{CC} = -10V$, $V_{REF} = 15V$	2.1	—	2.1	—	mA
	$\overline{I_{FS}R_1}$	All input bits low, Measure $\overline{I_O}$, $-V_{CC} = -10V$, $V_{REF} = 15V$					
	$I_{FS}R2$	All input bits high, Measure I_O $-V_{CC} = -12V$, $V_{REF} = 25V$	4.2	—	4.2	—	
	$\overline{I_{FS}R2}$	All input bits low, Measure $\overline{I_O}$ $-V_{CC} = -12V$, $V_{REF} = 25V$					
Reference Bias Current	$I_{REF}-$	All input bits low	−3	0	−3	0	μA
High Level Input Current	I_{IH}	All input bits V_{IN} = 18V, each input measured separately	−0.05	10	−0.05	10	μA
Low Level Input Current	I_{IL}	All input bits V_{IN} = 10V, each input measured separately	−10	—	−10	—	μA
Full-Scale Current At +18V Compliance	$I_{FS}+$	All input bits high, Measure I_O, $V_{IO} = 18V$	1.90	2.08	1.94	2.04	mA
	$\overline{I_{FS}}+$	All Input bits low, Measure $\overline{I_O}$, $V_{IO} = 18V$					
Full-Scale Current At −10V Compliance	$I_{FS}-$	All input bits high, Measure I_O, $V_{IO} = -10V$	1.90	2.08	1.94	2.04	mA
	$\overline{I_{FS}}-$	All input bits low, Measure $\overline{I_O}$, $V_{IO} = -10V$					
Change In Full Scale Current Due to Voltage Compliance	ΔI_{FSC}	All input bits high, Measure I_O, 25° C ≤ T_A ≤ 125° C $T_A = -55°C$ V_{IO} = 18V to −10V	 −4 −8	 4 8	 −4 −8	 4 8	μA
	$\Delta\overline{I_{FSC}}$	All Input bits low, Measure $\overline{I_O}$ 25° C ≤ T_A ≤ 125° C $T_A = -55°C$ V_{IO} = 18V to −10V	 −4 −8	 4 8	 −4 −8	 4 8	
Power Supply Sensitivity From $+V_{CC}$	$P_{SS}I_{FS}+1$	All input bits high, Measure I_O, $+V_{CC}$ = 4.5V to +5.5V, $-V_{CC} = -18V$	−4	4	−4	4	μA
	$\overline{P_{SS}I_{FS}}+1$	All input bits low, Measure $\overline{I_O}$, $+V_{CC}$ = 4.5V to +5.5V, $-V_{CC} = -18V$					
	$P_{SS}I_{FS}+2$	All input bits high, Measure I_O, $+V_{CC}$ = 12V to 18V, $-V_{CC} = -18V$	−8	8	−8	8	
	$\overline{P_{SS}I_{FS}}+2$	All input bits low, Measure $\overline{I_O}$, $+V_{CC}$ = 12V to 18V, $-V_{CC} = -18V$					
Power Supply Sensitivity From $-V_{CC}$	$P_{SS}I_{FS}-1$	All input bits high, Measure I_O, $+V_{CC}$ = 18V, $-V_{CC}$ = −12V to −18V	−8	8	−8	8	μA
	$\overline{P_{SS}I_{FS}}-1$	All input bits low, Measure $\overline{I_O}$, $+V_{CC}$ = 18V, $-V_{CC}$ = −12V to −18V					
	$P_{SS}I_{FS}-2$	All input bits high, Measure I_O, $+V_{CC}$ = 18V, $-V_{CC}$ = −4.5V to −5.5V I_{REF} = 1mA	−2	2	−2	2	
	$\overline{P_{SS}I_{FS}}-2$	All input bits low, Measure $\overline{I_O}$ $+V_{CC}$ = 18V, $-V_{CC}$ = −4.5V to −5.5V I_{REF} = 1mA					

ELECTRICAL CHARACTERISTICS at $\pm V_{CC} = \pm 15$Vdc; Source resistance = 50 ohms; $I_{REF} = 2.0$mA; Figure 1; Ambient temperature range = −55°C to +125°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	01 LIMITS MIN	01 LIMITS MAX	02 LIMITS MIN	02 LIMITS MAX	UNITS
Supply Current From $+V_{CC}$	$I_{CC}+$	All input bits high	0.4	3.8	0.4	3.8	mA
Supply Current From $-V_{CC}$	$I_{CC}-$	All input bits high	−7.8	−0.8	−7.8	−0.8	mA
Propagation Delay Time, High-to-Low Level	t_{PHL}	Figure 2, Measure V_O	6	60	6	60	ns
Propagation Delay Time, Low-to-High Level	t_{PLH}	Figure 2, Measure V_O	6	60	6	60	ns
Reference Amplifier Input Slew Rate	dI_O/dt $T_A = 25°C$	Figure 3, Measure V_O	1.5	—	1.5	—	mA/μs
Settling Time, High-to-Low Level	t_{SHL} $T_A = 25°C$	Figure 2, Output within 1/2 LSB of final value of I_O	10	135	10	135	ns
Settling Time, Low-to-High Level	t_{SLH} $T_A = 25°C$	Figure 2, Output within 1/2 LSB of final value of I_O	10	135	10	135	ns



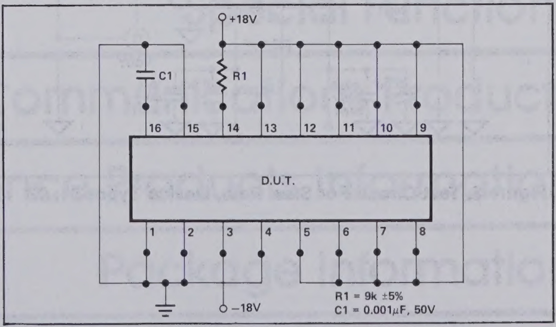
+15V
0.01μF
+10V REF ±0.02% (SEE NOTE 2)
K1
K5
5k 0.01%
5k 0.01%
K3B
5k 5%
MSB
LSB
D.U.T.
REFERENCE D/A CONVERTER VOLTAGE OUTPUT D/A CONVERTER (SEE NOTE 1)
0.1μF
+15V
−15V
K4
K2A
K3A
10k 0.01%
200k 1%
5k 0.01%
0.01μF
30pF
M38510 /10104
−Vcc
+Vcc
−15V

NOTES:
1. THE REFERENCE D/A CONVERTER SELECTED SHOULD HAVE A RESOLUTION OF 8 BITS OR MORE, AND A LINEARITY OF 0.015% OR BETTER.
2. THE VOLTAGE REFERENCE SHOULD HAVE AN ACCURACY OF ±0.02% OR BETTER.
3. ALL RELAYS ARE SHOWN IN THEIR NON-ACTUATED STATE.

Figure 1. Test Circuit For Static Tests

BURN-IN

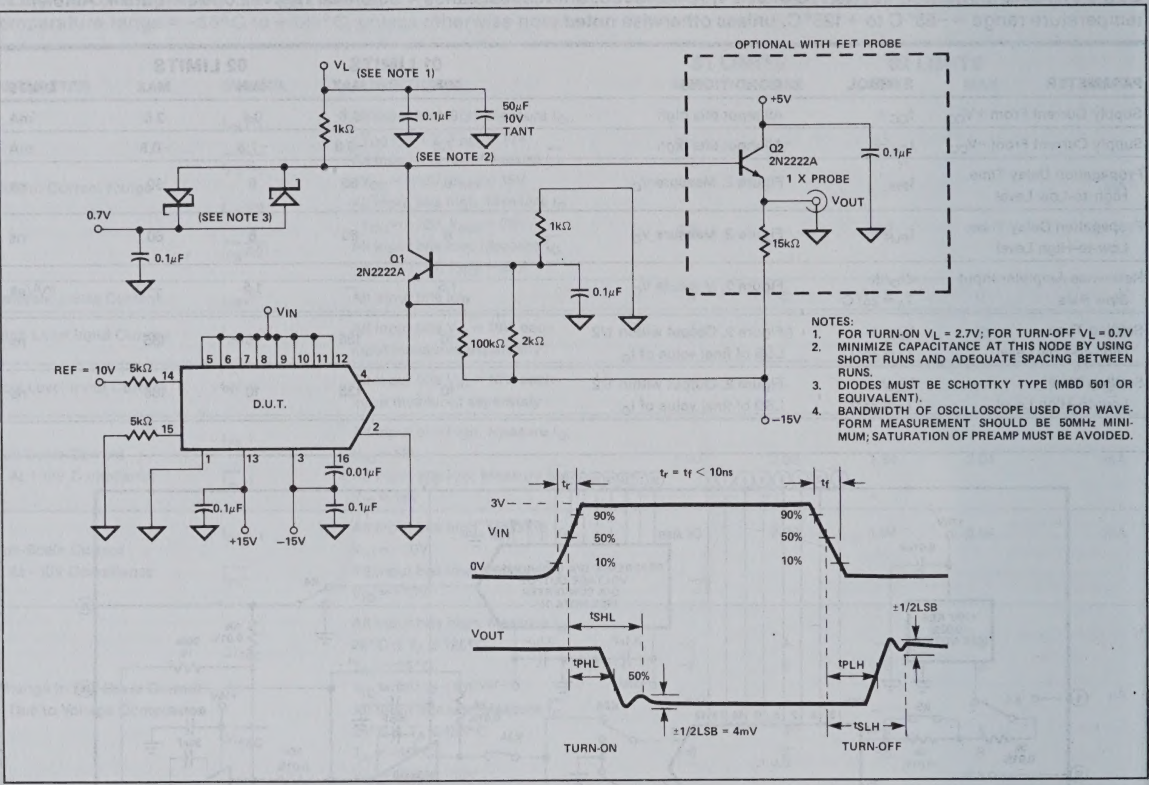
Devices supplied by PMI have been subjected to burn-in per method 1015 of MIL-STD-883 using test condition C or test condition F with the circuit shown in Figure 4.



+18V
C1
R1
D.U.T.
−18V

R1 = 9k ±5%
C1 = 0.001μF, 50V

Figure 4. Test Circuit, Burn-In and Operating Life Test


VL (SEE NOTE 1)
1kΩ
0.1μF
50μF 10V TANT
(SEE NOTE 2)
(SEE NOTE 3)
0.7V
0.1μF
Q1 2N2222A
1kΩ
0.1μF
VIN
100kΩ
2kΩ
REF = 10V
5kΩ
5kΩ
D.U.T.
5 6 7 8 9 10 11 12
14
15
4
2
1
13
3
16
0.01μF
0.1μF
0.1μF
+15V
−15V
OPTIONAL WITH FET PROBE
+5V
Q2 2N2222A
1 X PROBE
VOUT
0.1μF
15kΩ
−15V
tr = tf < 10ns
tr
tf
3V
VIN
0V
90%
50%
10%
tSHL
VOUT
tPHL
50%
±1/2LSB = 4mV
TURN-ON
±1/2LSB
tPLH
tSLH
TURN-OFF

NOTES:
1. FOR TURN-ON V_L = 2.7V; FOR TURN-OFF V_L = 0.7V
2. MINIMIZE CAPACITANCE AT THIS NODE BY USING SHORT RUNS AND ADEQUATE SPACING BETWEEN RUNS.
3. DIODES MUST BE SCHOTTKY TYPE (MBD 501 OR EQUIVALENT).
4. BANDWIDTH OF OSCILLOSCOPE USED FOR WAVEFORM MEASUREMENT SHOULD BE 50MHz MINIMUM; SATURATION OF PREAMP MUST BE AVOIDED.

Figure 2. Test Circuit For Propagation Delay and Settling Time, Device Types 01 and 02

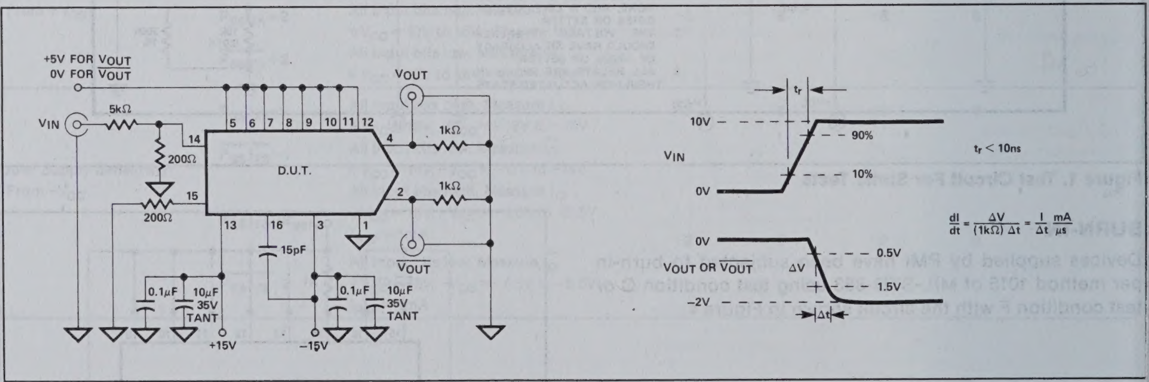

+5V FOR VOUT
0V FOR V̄OUT
VIN
5kΩ
200Ω
200Ω
14
15
D.U.T.
5 6 7 8 9 10 11 12
4
2
13
16
3
1
15pF
VOUT
1kΩ
1kΩ
V̄OUT
0.1μF
10μF 35V TANT
0.1μF
10μF 35V TANT
+15V
−15V
tr
10V
90%
VIN
10%
0V
tr < 10ns
dI/dt = ΔV/((1kΩ) Δt) = I/Δt mA/μs
0V
0.5V
VOUT OR V̄OUT
ΔV
1.5V
−2V
Δt

Figure 3. Test Circuit For Slew Rate, Device Types 01, 02

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ANALOG SWITCHES MULTIPLEXERS

INTRODUCTION

Analog multiplexers and switches find applications in data acquisition, metrology, telemetry, process control and telephony systems. Multiplexers are multiple analog switches which share a common output. An on-chip address decoder selects the appropriate input by means of a binary code. All channels may be deactivated by an enable/disable control pin.

In the past multiplexers/switches have been manufactured with hybrid, monolithic CMOS or dielectrically isolated CMOS technologies. The merging of ion implant techniques with the standard bipolar process creates a fourth technological alternative — the BIFET process. High-quality ion implanted p-channel FET's can now be compatibly processed with bipolar devices.

The cost of hybrid devices limits their use to applications which require the extremely low "R_{ON}" resistance made possible by discrete FET's. MOS technologies are inherently plagued by SCR "latch up" problems and analog signal overvoltage destruction. The use of buried layers and expensive dielectric isolation processing can eliminate the SCR failure mode, but the overvoltage blowout problems can be solved only by adding large series input resistance with each switch. This increases system errors since the equivalent "R_{ON}" may typically be over 1000 ohms.

BIFET switches have no SCR "latch up" tendency and can withstand analog input overvoltages while maintaining low "R_{ON}" resistance. In addition, the special handling required with CMOS devices is not necessary with BIFET switches.

In selecting analog multiplexers, attention must be paid to several key specs. Break-before-make switching insures no two-channel inputs are simultaneously connected. This prevents input sensor damage and misoperation. Acquiring analog input signals within a specified time and error band are primary concerns affected by "R_{ON}" resistance and "C_{OUT}" capacitance specifications. A low "R_{ON}" insures minimum signal attenuation and maximum accuracy. The "C_{OUT}" capacitance forms on R-C time constant with "R_{ON}" placing fundamental limits on signal acquisition time. Low "R_{ON}" and "C_{OUT}" insures minimum elapsed time between the channel select command and the acquisition of data to within a specified error band. High cross talk and off isolation specifications prevent unselected input signals from affecting the signal path.

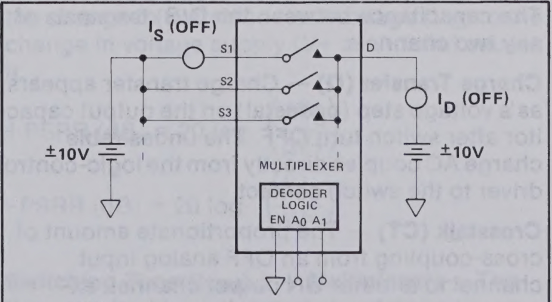
PMI offers a wide selection of single-ended and differential multiplexers and switches. Sixteen and eight-channel multiplexers as well as differential eight and four-channel devices are available. Dual and Quad SPST switches in normally closed and open configurations are also available. All devices are pin-for-pin replacements for many industry standard CMOS devices.

DEFINITIONS

Analog Input Leakage Current ($I_{S(OFF)}$) — The algebraic sum of diode current losses from an OFF-channel source input to the power supplies, ground and through the channel. Specified as an absolute value, as the direction of current flow is not predictable.

Analog Output Leakage Current ($I_{D(OFF)}$) — The algebraic sum of diode current losses from an OFF-channel "D" output to the power supplies, ground and through the channel. Specified as an absolute value, as the direction of current flow is not predictable.

$I_{D(OFF)}$, $I_{S(OFF)}$ Test Condition Definitions



NOTES:
1. SWITCHES TURNED "OFF" VIA ENABLE PIN OF DECODER LOGIC FOR I_D (OFF), I_S (OFF) MEASUREMENTS.
2. I_S (OFF) IS TESTED AT EACH INPUT (SOURCE) TERMINAL.

Analog Output-To-Input Capacitance ($C_{DS(OFF)}$) — The equivalent capacitance which shunts an open switch effectively between "S" and "D" output.

Analog Input Capacitance ($C_{S(ON)}$) — The capacitance between an analog "S" input and ground with the channel ON.

Analog Input Capacitance ($C_{S(OFF)}$) — The capacitance between and analog "S" input and ground with the channel OFF.

Analog Output Capacitance ($C_{D(OFF)}$) — The capacitance between the analog (DRAIN) output and ground with the channel OFF. High-frequency transmission and output settling time characteristics are highly influenced by this parameter in conjunction with R_{ON}.

Analog Output Capacitance ($C_{D(ON)}$) — The capacitance between the analog "D" output and ground with the channel ON.

Analog Voltage Range (V_A) — The range of analog-voltage amplitudes, with-respect-to ground, over which the analog switch operates (ON/OFF) within the R_{ON} and leakage specifications — $I_{S(OFF)}$, $I_{D(OFF)}$ and $I_{D(ON)} + I_{S(ON)}$.

Break-Before-Make Delay (t_{OPEN}) — The elapsed time between the turn-off of one analog input and the subsequent turn-on of another input as determined by the appropriate instantaneous change in the digital input code for both inputs measured between the outputs' 50% transition points.

Channel Capacitance ($C_{SS(OFF)}$, $C_{DD(OFF)}$) — The capacitance between the D(S) terminals of any two channels.

Charge Transfer (Q) — Charge transfer appears as a voltage step (pedestal) on the output capacitor after switch turn OFF. The undesirable charge AC couples directly from the logic-control driver to the switch contact.

Crosstalk (CT) — The proportionate amount of cross-coupling from an OFF analog input channel to another ON output channel, expressed in dB.

Digital Input Capacitance (C_{DIG}) — The capacitance between a digital input and ground.

Insertion Loss — Insertion loss measures the amount of signal power absorbed by the switch ON resistance at a given measurement frequency. Insertion loss is defined in decibels as a ratio of the output-voltage amplitude (V_D) versus the input-voltage amplitude (V_S) with a specified load impedance.

$$\text{Insertion Loss (dB)} = 20 \log \frac{|V_D|}{|V_S|}$$

At low frequencies this equation simplifies to:

$$\text{Insertion Loss (dB)} = 20 \log\left(\frac{R_L}{R_L + R_{ON}}\right)$$

Logic "0" Input Current (I_{INL}) — The current flowing into a digital input when a specified low-level voltage is applied to that input.

Logic "0" Input Voltage Level (V_{INL}) — The maximum (or most-positive) digital low-level input voltage for which proper operation of the device is guaranteed.

Logic "1" Input Voltage Level (V_{INH}) — The minimum (or least-positive) digital high-level input voltage for which proper operation of the device is guaranteed.

Negative Voltage Supply (V−) — The most negative voltage supply with respect to ground.

Positive Voltage Supply (V+) — The most positive voltage supply with respect to ground.

OFF Isolation ($ISO_{(OFF)}$) — The proportionate amount of a high-frequency analog input signal which is coupled through the channel of an OFF device. This feedthrough is transmitted through $C_{DS(OFF)}$ to a load comprised of $C_{D(OFF)}$ in parallel with an external load. Isolation generally decreases by 6dB/octave with increasing frequency.

ON Resistance (R_{ON}) — The series ON-channel resistance measured between "S" input and "D" output terminals under specified conditions.

ON Resistance Match (R_{ON} Match) — The channel-to-channel matching of ON resistance when channels are operated under identical conditions.

$$R_{ON}\text{ Match} = \frac{R_i - R_{AVG}}{R_{AVG}} \times 100\%$$

where

N = # of channels in package (i.e., for MUX-08 N = 8, for MUX-16 N = 16, etc.)

R_i = Each channel's ON resistance

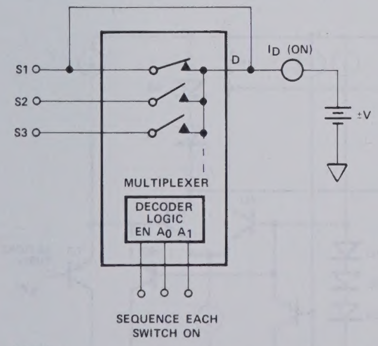
$$R_{AVG} = \frac{1}{N}\sum_{i=1}^{N} R_i$$

ON Resistance Variation (ΔR_{ON}) — The variation of ON resistance produced by the specified analog input voltage change with a constant load current.

$$\Delta R_{ON}\,(\%) = \frac{R_{ON} @ V_A = -10V - R_{ON} @ V_A = +10V}{R_{ON} @ V_A = 0V} \times 100\%$$

ON Channel Analog Leakage Current ($I_{D(ON)} + I_{S(ON)}$) Current loss (or gain) through an ON-channel resistance creating a voltage offset across the device. As the direction of current flow is not predictable, only the magnitude is specified at various temperature ranges.

$I_{(ON)}$ Test Condition Definitions



NOTES:
1. TEST IS REPEATED FOR EACH SWITCH WITH SOURCE CONNECTED TO DRAIN.
2. V_D = +10V AND −10V.

Output Enable Delay Time OFF ($t_{OFF(EN)}$) — Multiplexers — The time required to disconnect the analog output from the analog input determined by the digital address input code. It is measured from the 50% point of ENABLE input logic change to the time the output reaches 10% of the initial value.

Output Enable Delay Time ON ($t_{ON(EN)}$) — Mutiplexers — The time required to connect the analog output to the analog input determined by the digital address input code. It is measured from the 50% point of the ENABLE input logic change to the time the output is within 90% of final value.

Output ON Switching Time (t_{ON}) — The time required to connect the analog output to the analog input. The time is measured from the 50% point of the logic input change to the time the output reaches 90% of the final value.

Output OFF Switching Time (t_{OFF}) — The time required to disconnect the analog output from the analog input. The time is measured from the 50% point of the logic input change to the time the output reaches 10% of the initial value.

Output Settling Time (t_s) — The elapsed time for the analog output to reach its final value within a specified error band after the corresponding digital input code has been changed. It is measured from the 50% point of the logic input change to the time the output reaches final value within specified error band.

Power Supply Rejection (PSRR) — The ratio of the change in switch contact voltage (V_D) to the change in voltage supply (V+ or V−) that causes it.

$$+\text{PSRR (dB)} = 20 \log \left(\frac{\Delta V_D}{\Delta V+}\right)$$

$$-\text{PSRR (dB)} = 20 \log \left(\frac{\Delta V_D}{\Delta V-}\right)$$

Switching Time (t_{TRAN}) — Multiplexers— The time required to switch and slew from one analog input channel to another analog input with a full-scale differential between inputs with a high impedance output load. The time is measured from the 50% point of the logic input change to the time the output reaches 90% of the final value.

Total Harmonic Distortion (THD) — The ratio of the signal power at the fundamental frequency to the signal power of all harmonics observed at the switch output (V_D) with a pure sinusoid applied to the switch input (V_S).

QUAD SPST BIFET ANALOG SWITCHES

SW-01/02, SW-03/04

(TEMPERATURE COMPENSATED R$_{ON}$ AND DISABLE FUNCTION)

FEATURES

- **Low R$_{ON}$ vs Temperature .... 0.03%/° C**
- **Low Absolute R$_{ON}$ 85Ω**
- **Low R$_{ON}$ Variation vs Analog Signal 7%**
- **High Speed 300ns**
- **Low Leakage Current 0.2nA**
- **Overvoltage and Supply Loss Protected**
- **SW-01 is Improved Pin Compatible Device for DG201, ADG201, LF11201**
- **SW-02 is Improved Pin Compatible Device for DG202, LF11202, IH202**
- **SW-03 — Normally-Closed, with Disable. Functional Equivalent to LF11332.**
- **SW-04 — Normally-Open, with Disable. Functional Equivalent to LF11331.**

GENERAL DESCRIPTION

The SW-01 through SW-04 are four-channel single-pole, single-throw analog switches which offer operating characteristics unavailable in other JFET or CMOS devices. A unique circuit design provides a nearly constatn R$_{ON}$ over the full operating temperature span. R$_{ON}$ drift typically runs under 300ppm/° C.

The SW-01/02 are pin compatible with the DG201/202, while the SW-03/04 incorporate a chip disable pin which allows switch cascading for multiple switch systems. An Ion Implanted FET switch inherently exhibits low R$_{ON}$ variations vs analog input signals. The junction FET construction also reduces static discharge destruction prevalent in CMOS devices.

Low R$_{ON}$ sensitivity to temperature and voltage is complemented by guaranteed high-speed operation and low-leakage currents. Logic inputs may operate directly from either CMOS or TTL logic levels and are supply voltage independent. The SW-01 through SW-04 are protected during supply voltage power loss and against input signal overvoltages.

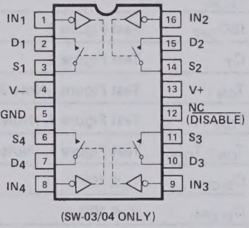
ORDERING INFORMATION†

FUNCTION	16-PIN HERMETIC DUAL-IN-LINE PACKAGE MILITARY*	 INDUSTRIAL
N.C.	SW01BQ	SW01FQ
N.C. (Disable)	SW03BQ	SW03FQ
N.O.	SW02BQ	SW02FQ
N.O. (Disable)	SW04BQ	SW04FQ

*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

PIN CONNECTIONS



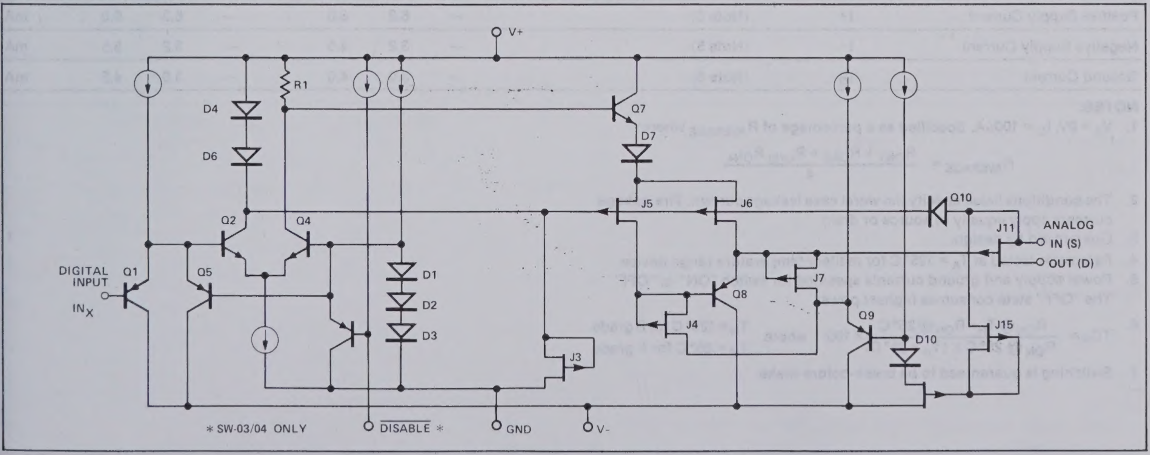
16-PIN DUAL-IN-LINE PACKAGE
(Q-Package)

CONTROL LOGIC

LOGIC		SWITCH STATE			
$\overline{DIS}$	**IN$_y$**	**SW 01**	**SW 02**	**SW 03**	**SW 04**
0	X	NA	NA	OFF	OFF
1	0	ON	OFF	ON	OFF
1	1	OFF	ON	OFF	ON

NOTES: $\overline{DIS}$ = DISABLE 1-4
INy = INPUT 1-4
X = DON'T CARE
NA = NOT APPLICABLE

SIMPLIFIED SCHEMATIC DIAGRAM (TYPICAL SWITCH)



ABSOLUTE MAXIMUM RATINGS ($T_A = 25°C$, unless otherwise noted).

Operating Temperature Range	
SW-01-04BQ	−55°C to +125°C
SW-01-04FQ	−25°C to +85°C
DICE Junction Temperature (T_j)	−65°C to +150°C
Storage Temperature Range	−65°C to +150°C
Power Dissipation (Q-Package)	900mW
Lead Temperature (Soldering, 60 sec)	300°C
Maximum Junction Temperature	150°C
V+ Supply to V− Supply	36V
V+ Supply to Ground	36V
Logic Input Voltage	(V− or −4V) to V+ Supply
Analog Input Voltage	
Continuous	V− Supply −25V to V+ Supply +25V
For V+ = V− = 0	±15V
Maximum Current Through Any Pin	30mA
Peak Current, (Pulsed at 1ms, 10% Duty Cycle)	70mA

NOTE: Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, and $T_A = 25°C$, unless otherwise noted.

			SW-01-04B			SW-01-04F			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
"ON" Resistance	R_{ON}	$-10V \leq V_A \leq 10V$, $I_D \leq 1mA$	—	85	100	—	85	120	Ω
R_{ON} Match		(Note 1)	—	4	10	—	4	10	%
Analog Voltage Range	V_A	$R_L \geq 2k\Omega$ Full Temperature Range	+10 −10	+11 −15	— —	+10 −10	+11 −15	— —	V
ΔR_{ON} vs V_A	ΔR_{ON}	$V_A \leq 10V$, $I_D \leq 1mA$	—	7	10	—	7	10	%
Analog Current Range	I_A	$V_A \leq 10V$	—	5	—	—	5	—	mA
Source Current in "OFF" Condition	$I_{S(OFF)}$	$V_S = 10V$, $V_D = -10V$	—	0.2	1	—	0.2	2	nA
Drain Current in "OFF" Condition	$I_{D(OFF)}$	$V_S = 10V$, $V_D = -10V$	—	0.2	1	—	0.2	2	nA
Leakage Current in "ON" Condition	$I_{D(ON)} + I_{S(ON)}$	$V_S = \pm 10V$, (Note 2)	—	—	1	—	—	2	nA
"OFF" Isolation	ISO_{OFF}	Test Figure 2	—	58	—	—	58	—	dB
Crosstalk	C_T	Test Figure 3	—	70	—	—	70	—	dB
Turn-On-Time	T_{ON}	Test Figure, (Note 3)	—	300	400	—	300	400	ns
Turn-Off-Time	T_{OFF}	Test Figure 1, (Note 3)	—	200	300	—	200	300	ns
Break-Before-Make Time	$T_{ON} - T_{OFF}$	Test Figure 1, (Notes 3, 7)	—	100	—	—	100	—	ns
Source Capacitance	$C_{S(OFF)}$	$V_A \leq 10V$	—	7	—	—	7	—	pF
Drain Capacitance	$C_{D(OFF)}$	$V_A \leq 10V$	—	5.5	—	—	5.5	—	pF
Logic "1" Input Voltage	V_{INH}	Full Temperature Range	2	—	—	2	—	—	V
Logical "0" Input Voltage	V_{INL}	Full Temperature Range	—	—	0.8	—	—	0.8	V
Logical "1" Input Current	I_{INH}	$2 \leq V_{IN} \leq 15V$, (Note 3)	—	1	3	—	1	3	μA
Logical "0" Input Current	I_{INL}	$0 \leq V_{IN} \leq 0.8V$	—	1	3	—	1	3	μA
Positive Supply Current	I+	(Note 5)	—	6.3	8.0	—	6.3	9.0	mA
Negative Supply Current	I−	(Note 5)	—	3.2	4.5	—	3.2	5.5	mA
Ground Current	I_G	(Note 5)	—	3.0	4.0	—	3.0	4.5	mA

NOTES:

1. $V_A = 0V$, $I_D = 100\mu A$. Specified as a percentage of $R_{AVERAGE}$ where:

$$R_{AVERAGE} = \frac{R_{ON1} + R_{ON2} + R_{ON3}\, R_{ON4}}{4}$$

2. The conditions listed specify the worst case leakage current. The leakage currents apply equally to source or drain.
3. Guaranteed by design.
4. Parameter tested at $T_A = 125°C$ for military temperature range device.
5. Power supply and ground currents specified for switch "ON" or "OFF". The "OFF" state consumes highest power.
6. $$TC_R = \frac{R_{ON}@T_H - R_{ON}@25°C}{R_{ON}@25°C \times (T_H - 25°C)} \times 100; \quad \text{where} \quad \begin{matrix} T_H = 125°C \text{ for B grade} \\ T_H = 85°C \text{ for F grade} \end{matrix}$$
7. Switching is guaranteed to be break-before-make.

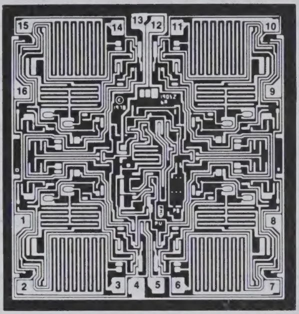
ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, and $-55°C \le T_A \le +125°C$ for SW-01-04B and $-25°C \le T_A \le 85°C$ for SW-01-04F, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-01-04B MIN	SW-01-04B TYP	SW-01-04B MAX	SW-01-04F MIN	SW-01-04F TYP	SW-01-04F MAX	UNITS
"ON" Resistance	R_{ON}	$-10V \le V_A \le 10V$, $I_D \le 1mA$	—	—	120	—	—	140	Ω
R_{ON} Match		(Note 1)	—	10	15	—	10	15	%
R_{ON} Temperature Coefficient — Average	TC_R	$V_A = 0V$, $I_D = 100\mu A$, (Notes 3, 6)	—	0.03	0.20	—	0.03	0.15	%/°C
Source Current in "OFF" Condition	$I_{S(OFF)}$	$V_S = 10V$, $V_D = -10V$, (Note 4)	—	—	10	—	—	10	nA
Drain Current in "OFF" Condition	$I_{D(OFF)}$	$V_S = 10V$, $V_D = -10V$, (Note 4)	—	—	10	—	—	10	nA
Leakage Current in "ON" Condition	$I_{D(ON)} + I_{S(ON)}$	$V_S = \pm10V$, (Notes 2, 4)	—	—	10	—	—	10	nA
Turn-On-Time	T_{ON}	Test Figure 1, (Note 3)	—	500	600	—	500	600	ns
Turn-Off-Time	T_{OFF}	Test Figure 1, (Note 3)	—	400	500	—	400	500	ns
Break-Before-Make Time	$T_{ON} - T_{OFF}$	Test Figure 1, (Notes 3, 7)	—	100	—	—	100	—	ns
Logical "1" Input Current	I_{INH}	$2 \le V_{IN} \le 15V$, (Note 3)	—	1	5	—	1	5	µA
Logical "0" Input Current	I_{INL}	$0 \le V_{IN} \le 0.8V$	—	—	5	—	—	5	µA
Positive Supply Current	$I+$	(Note 5)	—	—	11	—	—	12	mA
Negative Supply Current	$I-$	(Note 5)	—	—	6	—	—	7	mA
Ground Current	I_G	(Note 5)	—	—	5	—	—	6	mA

NOTES:

1. $V_A = 0V$, $I_D = 100\mu A$. Specified as a percentage of $R_{AVERAGE}$ where:
$$R_{AVERAGE} = \frac{R_{ON1} + R_{ON2} + R_{ON3}\ R_{ON4}}{4}$$
2. The conditions listed specify the worst case leakage current. The leakage currents apply equally to source or drain.
3. Guaranteed by design.
4. Parameter tested at $T_A = 125°C$ for military temperature range device.
5. Power supply and ground currents specified for switch "ON" or "OFF". The "OFF" state consumes highest power.
6. $$TC_R = \frac{R_{ON}@T_H - R_{ON}@25°C}{R_{ON}@25°C \times (T_H - 25°C)} \times 100; \quad \text{where} \quad \begin{array}{l} T_H = 125°C \text{ for B grade} \\ T_H = 85°C \text{ for F grade} \end{array}$$
7. Switching is guaranteed to be break-before-make.

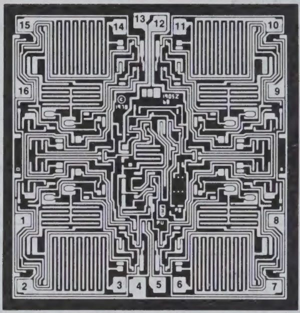
DICE CHARACTERISTICS



SW-01/03

DIE SIZE 0.100 × 0.096 inch, 9600 sq. mils
(2.540 × 2.438 mm, 6.193 sq. mm)

1. SWITCH (1) ADDRESS (IN1)
2. SWITCH (1) DRAIN (D1)
3. SWITCH (1) SOURCE (S1)
4. NEGATIVE SUPPLY (SUBSTRATE)
5. GROUND
6. SWITCH (4) SOURCE (S4)
7. SWITCH (4) DRAIN (D4)
8. SWITCH (4) ADDRESS (IN4)
9. SWITCH (3) ADDRESS (IN3)
10. SWITCH (3) DRAIN (D3)
11. SWITCH (3) SOURCE (S3)
12. DISABLE (NO CONNECTION SW-01)
13. POSITIVE SUPPLY
14. SWITCH (2) SOURCE (S2)
15. SWITCH (2) DRAIN (D2)
16. SWITCH (2) ADDRESS (IN2)



SW-02/04

DIE SIZE 0.100 × 0.096 inch, 9600 sq. mils
(2.540 × 2.438 mm, 6.193 sq. mm)

1. SWITCH (1) ADDRESS (IN1)
2. SWITCH (1) DRAIN (D1)
3. SWITCH (1) SOURCE (S1)
4. NEGATIVE SUPPLY (SUBSTRATE)
5. GROUND
6. SWITCH (4) SOURCE (S4)
7. SWITCH (4) DRAIN (D4)
8. SWITCH (4) ADDRESS (IN4)
9. SWITCH (3) ADDRESS (IN3)
10. SWITCH (3) DRAIN (D3)
11. SWITCH (3) SOURCE (S3)
12. DISABLE (NO CONNECTION SW-02)
13. POSITIVE SUPPLY
14. SWITCH (2) SOURCE (S2)
15. SWITCH (2) DRAIN (D2)
16. SWITCH (2) ADDRESS (IN2)

For additional DICE information refer to Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-01-04N LIMIT	SW-01-04G LIMIT	UNITS
"ON" Resistance	R_{ON}	$-10V \le V_A \le 10V$, $I_D \le 1mA$	100	120	Ω MAX
R_{ON} Match		$V_A = 0V$, $I_D \le 100\mu A$	10	10	% MAX
ΔR_{ON} vs V_A	ΔR_{ON}	$V_A \le 10V$, $I_D \le 1mA$	10	10	% MAX
Positive Supply Current	$I+$	(Note 1)	8	9	mA MAX
Negative Supply Current	$I-$	(Note 1)	4.5	5.5	mA MAX
Ground Current	I_G		4.0	4.5	mA MAX
Analog Voltage Range	V_A	$R_L \ge 2k\Omega$	±10	±10	V MIN
Logical "1" Input Voltage	V_{INH}		2	2	V MIN
Logical "0" Input Voltage	V_{INL}		0.8	0.8	V MAX
Logical "0" Input Current	I_{INL}	$0 \le V_{IN} \le 0.8V$	3	3	μA MAX
Logical "1" Input Current	I_{INH}	$2 \le V_{IN} \le 15V$	3	3	μA MAX

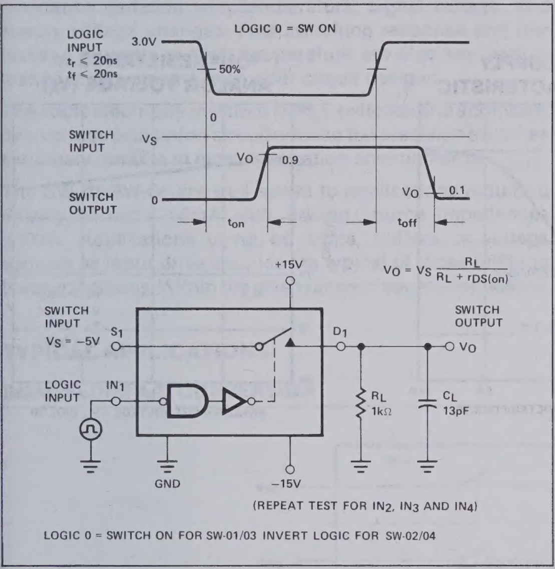
Note: Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ and $T_A = 25°C$, unless otherwise noted..

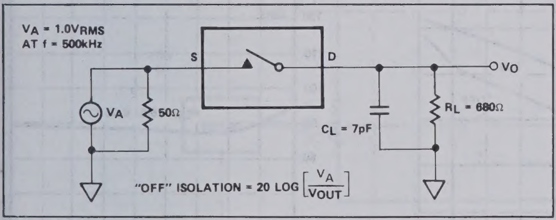
PARAMETER	SYMBOL	CONDITIONS	SW-01-04N TYPICAL	SW-01-04G TYPICAL	UNITS
"ON" Resistance	R_{ON}	$-55°C \le T_A \le 125°C$	90	90	Ω
R_{ON} Temperature Coefficient	TC_R	$V_A = 0$, $I_D = 100\mu A$	0.03	0.03	%/°C
Turn-On-Time	T_{ON}	$R_L = 1k$, $C_L = 13pF$	300	300	ns
Turn-Off-Time	T_{OFF}	$R_L = 1k$, $C_L = 13pF$	200	200	ns
Drain Current in "OFF" Condition	$I_{D(OFF)}$	$V_S = 10V$, $V_D = -10V$	0.2	0.2	nA
"OFF" Isolation	ISO_{OFF}	$f = 500kHz$, $R_L = 680\Omega$	58	58	dB
Crosstalk	C_T	$f = 500kHz$, $R_L = 680\Omega$	70	70	dB

NOTE:
1. Power supply and ground current specified for switch "ON" or "OFF".

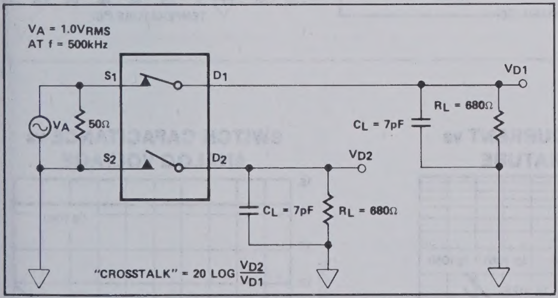
TEST CIRCUITS


LOGIC 0 = SW ON
LOGIC INPUT
$t_r \leq 20ns$
$t_f \leq 20ns$
3.0V
50%
0
SWITCH INPUT
V_S
V_O
0.9
SWITCH OUTPUT
0
V_O
0.1
t_{on}
t_{off}
+15V
$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$
SWITCH INPUT
$V_S = -5V$
S_1
D_1
SWITCH OUTPUT
V_O
LOGIC INPUT
IN_1
R_L 1kΩ
C_L 13pF
GND
−15V
(REPEAT TEST FOR IN_2, IN_3 AND IN_4)
LOGIC 0 = SWITCH ON FOR SW-01/03 INVERT LOGIC FOR SW-02/04

TEST FIGURE 1


V_A = 1.0V_{RMS}
AT f = 500kHz
S
D
V_O
V_A
50Ω
R_L = 680Ω
C_L = 7pF
"OFF" ISOLATION = 20 LOG $\left[\frac{V_A}{V_{OUT}}\right]$

TEST FIGURE 2


V_A = 1.0V_{RMS}
AT f = 500kHz
S_1
D_1
V_{D1}
R_L = 680Ω
C_L = 7pF
V_A
50Ω
S_2
D_2
V_{D2}
C_L = 7pF
R_L = 680Ω
"CROSSTALK" = 20 LOG $\frac{V_{D2}}{V_{D1}}$

TEST FIGURE 3

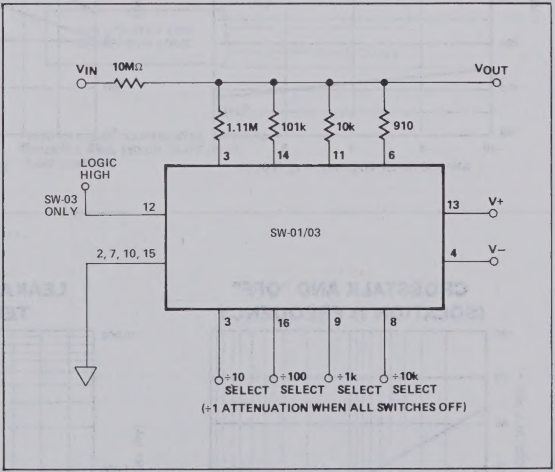
APPLICATIONS INFORMATION

This analog switch employs ion-implanted JFETs in a switch configuration designed to assure break-before-make action. The turn-off time is much faster than the turn-on time to guarantee this feature over the full operating temperature and input voltage range. Fabricated with BIFET processing rather than CMOS, special handling is not necessary to prevent damage to these switches. Because the digital inputs only require a 2V logic "1" input level, power-consuming pull-up resistors are not required for TTL compatibility to insure break-before-make switching as is most often the case with CMOS switches. The digital inputs utilize PNP input transistors where input current is maximum at the logic "0" level and drops to that of a reverse-biased diode (about 10nA) as the input voltage is raised above ≈ 1.4V.

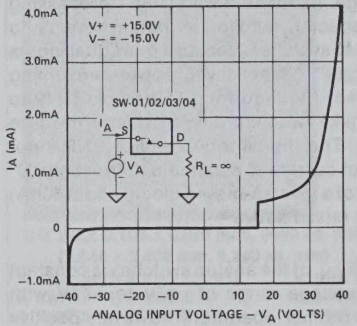
The "ON" resistance, R_{ON}, of the analog switches is constant over the wide input voltage range of −15V to +11V with $V_{SUPPLY} = \pm 15V$. For normal operation, however, positive input voltages should be restricted to 11V (or 4V less than the positive supply). This assures that the V_{GSD} of an OFF switch remains greater than its V_P, and prevents that channel from being falsely turned ON. Individual switches are "ON" without power applied.

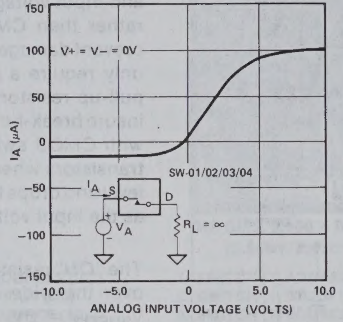
Proper switching requires the "Source" terminal to be connected to the input driving signal. If the DISABLE pin is left unconnected, the switches are controlled by the logic select pins.

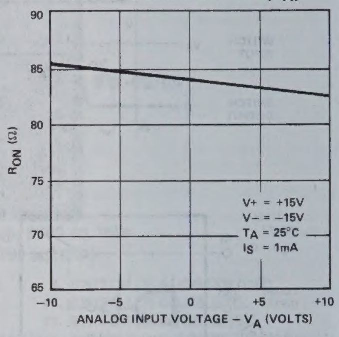
PROGRAMMABLE ATTENUATOR (1 to 0.0001)

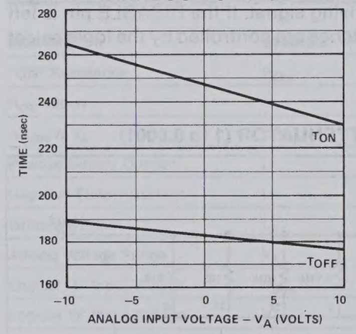

V_{IN}
10MΩ
V_{OUT}
1.11M
101k
10k
910
3
14
11
6
LOGIC HIGH
SW-03 ONLY
12
13
V+
SW-01/03
2, 7, 10, 15
4
V−
3
16
9
8
÷10 SELECT
÷100 SELECT
÷1k SELECT
÷10k SELECT
(÷1 ATTENUATION WHEN ALL SWITCHES OFF)

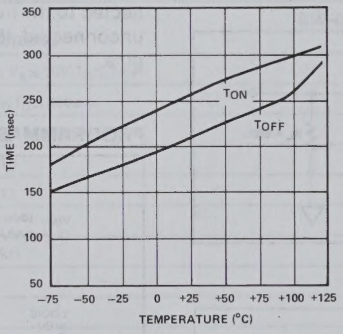
TYPICAL PERFORMANCE CHARACTERISTICS (SW-01/02/03/04)

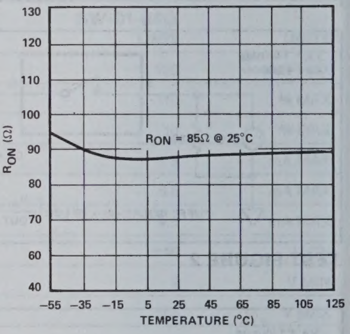

OVERVOLTAGE CHARACTERISTIC

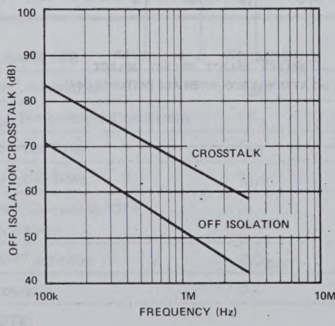

POWER SUPPLY LOSS CHARACTERISTIC

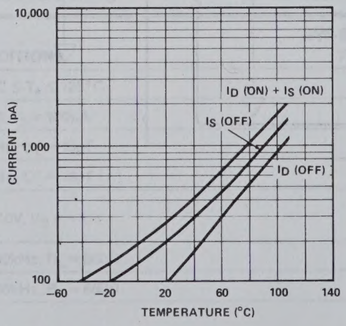

"ON" RESISTANCE vs ANALOG VOLTAGE (V_A)

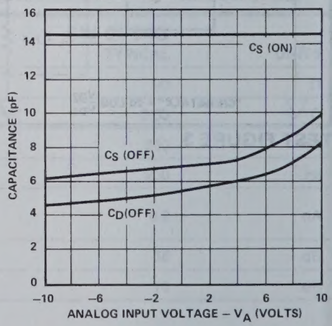

SWITCHING TIME vs ANALOG VOLTAGE


SWITCHING TIMES vs TEMPERATURE


R_{ON} vs TEMPERATURE


CROSSTALK AND "OFF" ISOLATION vs FREQUENCY


LEAKAGE CURRENT vs TEMPERATURE


SWITCH CAPACITANCE vs ANALOG VOLTAGE

The SW-01-SW-04 designs have been optimized for low "ON" resistance variation with temperature, signal voltage, and supply voltage changes. Fast switching response and low leakage currents at high temperature are also key performance improvements over older circuit designs.

The static electricity resistant BIFET switches and additional overvoltage protection circuitry make the precision switches extremely durable in most application environments.

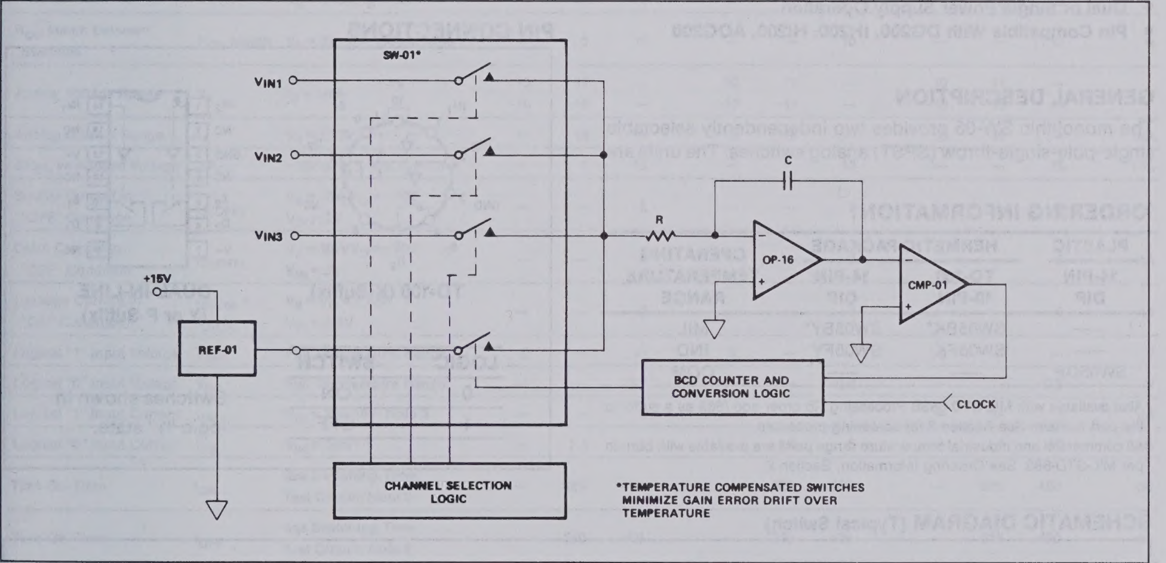
The SW-01-SW-04 are well suited to applications requiring analog currents <5mA with driving source impedances <100Ω. Applications using op amps, buffers or voltage sources as input drive sources are typical of those fulfilling these conditions. Within the given range of source impedance and analog current near ideal signal transfer accuracy is obtainable.

Applications needing very high analog current capability (>5mA) or where the switch is driven from high source impedances (>100Ω) should use the SW-201 (Pin Compatible to SW-01) or the SW-202 (Pin Compatible to SW-02) high-current Quad Switches.

Although the SW-201/SW-202 do not offer the same "ON" resistance temperature coefficient, many other premium characteristics are similar. In addition, the SW-201/SW-202 offer exceptionally low signal distortion over a wide signal voltage and frequency range.

TYPICAL APPLICATIONS

DUAL SLOPE A/D CONVERSION



*TEMPERATURE COMPENSATED SWITCHES MINIMIZE GAIN ERROR DRIFT OVER TEMPERATURE

SW-05

DUAL SPST BIFET ANALOG SWITCH

FEATURES

- **Low "ON" Resistance 25° C .... 70Ω Max**
  125° C .... 100Ω Max
- **Accurate Switching ($I_{D(ON)} \times R_{ON}$ @ 125° C)**
  V_{ERROR} Worst Case 10μV
- **Low R_{ON} Variation With Analog Input Voltage 5%**
- **Improved Switching Speed .... T_{ON} = 450ns Max**
  T_{OFF} = 400ns Max
- **Resistant to Static Discharge Damage**
- **Higher Resistance to Radiation Than Analog Switches Designed With MOS Devices.**
- **Latch Proof**
- **Digital Inputs TTL and CMOS Compatible**
- **Dual or Single Power Supply Operation**
- **Pin Compatible With DG200, IH200, HI200, ADG200**

GENERAL DESCRIPTION

The monolithic SW-05 provides two independently selectable single-pole-single-throw (SPST) analog switches. The units are fabricated with Precision Monolithics' ion-implant JFET-bipolar technology. The JFET switch structure parametrically improves R_{ON} variation with input voltages, total harmonic distortion, lowers noise, and reduces susceptibility to power supply feed-through when compared to the CMOS switch technology.

The JFET-bipolar process inherently reduces susceptibility to electrostatic voltage destruction commonly experienced in the CMOS process technology. Additionally, the elimination of MOS devices results in a circuit less susceptible to radiation.

An internal logic reference voltage maintains logic compatibility with full noise immunity over full temperature range and all variations of power supply voltage.

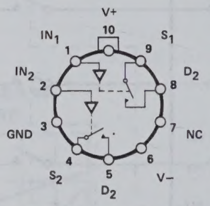
ORDERING INFORMATION†

PLASTIC	HERMETIC PACKAGE		OPERATING TEMPERATURE RANGE
14-PIN DIP	TO-100 10-PIN	14-PIN DIP	
—	SW05BK*	SW05BY*	MIL
—	SW05FK	SW05FY	IND
SW05GP	—	—	COM

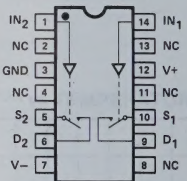
*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

PIN CONNECTIONS



TO-100 (K-Suffix)

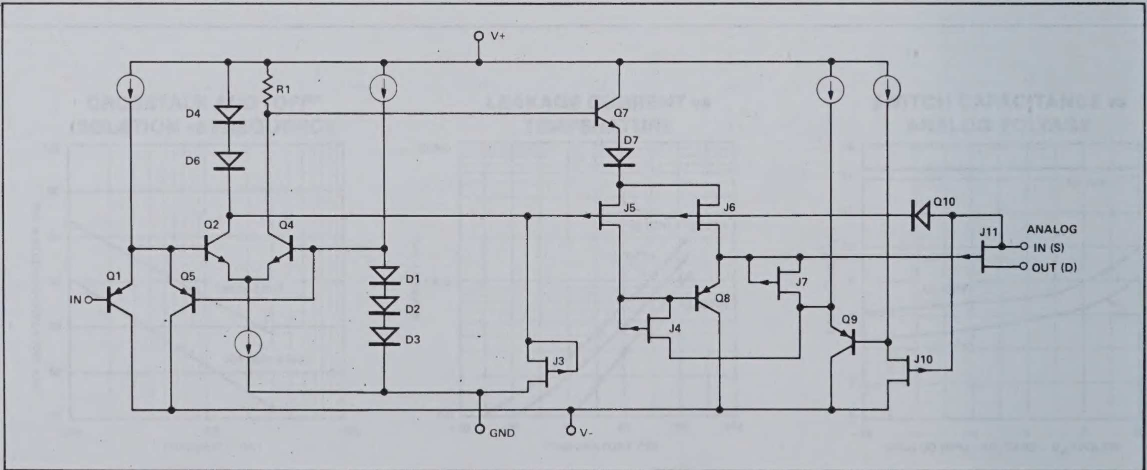


DUAL-IN-LINE (Y or P-Suffix)

LOGIC	SWITCH
0	ON
1	OFF

Switches shown in logic "1" state.

SCHEMATIC DIAGRAM (Typical Switch)



Manufactured under one or more of the following patents: 4,228,367.

ABSOLUTE MAXIMUM RATINGS ($T_A = 25°C$, unless otherwise noted)

Operating Temperature Range
SW05BY, SW05BK .... −55° C to +125° C
SW05FY, SW05FK .... −25° C to +85° C
SW05GP .... 0° C to +70° C
Storage Temperature Range .... −65° C to +150° C
Power Dissipation
K, Y Packages 900mW
P Package 500mW
Derate K, Y Package by 12mW/° C Above 75° C
Derate P Package by 10mW/° C Above 25° C
Lead Temperature (Soldering 60 sec) .... 300° C
Maximum Junction Temperature .... 150° C
V+ Supply to V− Supply 36V
V+ Supply to Ground 36V
Logic Input Voltage .... (−4V or V−) to V+ Supply
Analog Input Voltage Range
Continuous .... V− Supply to V+ Supply +20V
Maximum Current Through any Pin 30mA
Switch Current 1ms, 10% Duty Cycle Max. 100mA

ELECTRICAL CHARACTERISTICS at V+ = 15V, V− = −15V and $T_A = 25°C$, unless otherwise noted.

			SW-05B			SW-05F			SW-05G			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
"ON" Resistance	R_{ON}	$V_S = 0V$, $I_S = 1mA$	—	45	70	—	45	80	—	45	80	Ω
		$V_S = \pm 10V$, $I_S = 1mA$	—	45	70	—	45	80	—	45	80	
R_{ON} Match Between Switches	R_{ON} Match	$V_S = 0V$, $I_S = 100\mu A$; Note 1	—	5	10	—	—	10	—	—	15	%
Analog Voltage Range	V_A	$I_S = 1mA$	10	11	—	10	11	—	10	11	—	V
			−10	−15	—	−10	−15	—	−10	−15	—	
Analog Current Range	I_A	$V_S = \pm 10V$	10	15	—	8	12	—	6	10	—	mA
ΔR_{ON} vs Applied Voltage	ΔR_{ON}	$-10V \leq V_S \leq 10V$, $I_S = 1mA$	—	5	10	—	—	10	—	—	15	%
Source Current in "OFF" Condition	$I_{S(OFF)}$	$V_S = 10V$, $V_D = -10V$, $V_{IN} = 2V$	—	—	2	—	—	3	—	—	5	nA
Drain Current in "OFF" Condition	$I_{D(OFF)}$	$V_S = 10V$, $V_D = -10V$, $V_{IN} = 2V$	—	—	2	—	—	3	—	—	5	nA
Leakage Current in "ON" Condition	$I_{S(ON)} + I_{D(ON)}$	$V_S = V_D = \pm 10V$, $V_{IN} = 0.8V$	—	—	2	—	—	3	—	—	5	nA
Logical "1" Input Voltage	V_{INH}	Full Temperature Range	2	—	—	2	—	—	2	—	—	V
Logical "0" Input Voltage	V_{INL}	Full Temperature Range	—	—	0.8	—	—	0.8	—	—	0.8	V
Logical "1" Input Current	I_{INH}	$V_{IN} = 2$ to $15V$; Note 3	—	—	1	—	—	1	—	—	1	µA
Logical "0" Input Current	I_{INL}	$V_{IN} = 0.8V$	—	1.5	5	—	1.5	5	—	1.5	10	µA
Turn-On-Time	t_{ON}	See Switching Time Test Circuit; Note 2	—	325	450	—	325	450	—	325	450	ns
Turn-Off-Time	t_{OFF}	See Switching Time Test Circuit; Note 2	—	310	400	—	310	400	—	310	400	ns
Source Capacitance	$C_{S(OFF)}$	$V_S = 0V$, $V_{IN} = 2V$	—	8	—	—	8	—	—	8	—	pF
Drain Capacitance	$C_{D(OFF)}$	$V_D = 0V$, $V_{IN} = 2V$	—	5	—	—	5	—	—	5	—	pF
Channel "ON" Capacitance	$C_{D(ON)} + C_{S(ON)}$	$V_S = V_D = 0V$	—	15	—	—	15	—	—	15	—	pF
"OFF" Isolation	$I_{SO(OFF)}$	$V_S = 1V_{RMS}$, $R_L = 680\Omega$, $C_L = 7pF$, $f = 500kHz$	—	62	—	—	62	—	—	62	—	dB
Crosstalk	C_T	$V_S = 1V_{RMS}$, $R_L = 680\Omega$, $C_L = 7pF$, $f = 500kHz$	—	76	—	—	76	—	—	76	—	dB
Positive Supply Current	I+	$V_{IN} = 0$ or $2V$	—	2.6	6	—	3	6	—	4	8	mA
Negative Supply Current	I−	$V_{IN} = 0$ or $2V$	—	1.5	3	—	2	3	—	3	4	mA

NOTES:

1. $V_S = 0V$, $I_D = 100\mu A$. Specified as a percentage of $R_{AVERAGE}$ where:

$$R_{AVERAGE} = \frac{R_{ON1} + R_{ON2}}{2}$$

2. Parameter guaranteed by design.
3. Current tested at $V_{IN} = 2V$. This is worst case condition.

ELECTRICAL CHARACTERISTICS at V+ = 15V, V− = −15V, −55°C ≤ T_A ≤ +125°C for SW-05BY and SW-05BK; −25°C ≤ T_A ≤ +85°C for SW-05FY and SW-05FK; 0°C ≤ T_A ≤ 70°C for SW-05GP, unless otherwise noted.

			SW-05B			SW-05F			SW-05G			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Temperature Range	T_A	Operating	−55	—	125	−25	—	85	0	—	70	°C
"ON" Resistance	R_{ON}	V_S = 0V, I_S = 1mA V_S = ±10V, I_S = 1mA	— —	— —	100 100	— —	— —	100 100	— —	— —	100 100	Ω
R_{ON} Match Between Switches	R_{ON} Match	V_S = 0V, I_S = 100μA; Note 1	—	10	15	—	—	15	—	—	20	%
Analog Voltage Range	V_A	I_S = 1mA I_S = 1mA	10 −10	— —	— —	10 −10	— —	— —	10 −10	— —	— —	V
Analog Current Range	I_A	V_S = ±10V	10	—	—	8	—	—	6	—	—	mA
ΔR_{ON} with Applied Voltage	ΔR_{ON}	−10V ≤ V_S ≤ +10V, I_S = 100μA	—	—	10	—	—	10	—	—	15	%
Source Current in "OFF" Condition	$I_{S(OFF)}$	V_S = 10V, V_D = −10V, V_{IN} = 2V, T_A = Max. Operating Temp.; Note 4	—	—	50	—	—	50	—	—	50	nA
Drain Current in "OFF" Condition	$I_{D(OFF)}$	V_S = 10V, V_D = −10V, V_{IN} = 2V, T_A = Max. Operating Temp.; Note 4	—	—	50	—	—	50	—	—	50	nA
Leakage Current in "ON" Condition	$I_{S(ON)}$ + $I_{D(ON)}$	V_S = V_D = ±10V, V_{IN} = 0.8V T_A = Max. Operating Temp. Note 4	—	—	100	—	—	100	—	—	100	nA
Logical "1" Input Current	I_{INH}	V_{IN} = 2V to 15V, Note 3	—	—	5	—	—	5	—	—	10	μA
Logical "0" Input Current	I_{INL}	V_{IN} = 0.8V	—	4	10	—	4	10	—	5	15	μA
Turn-On-Time	t_{ON}	See Switching Time Test Circuit; Note 2	—	—	600	—	—	600	—	—	600	ns
Turn-Off-Time	t_{OFF}	See Switching Time Test Circuit; Note 2	—	—	500	—	—	500	—	—	500	ns
Positive Supply Current	I+	V_{IN} = 0 or 2V	—	—	8	—	—	8	—	—	10	mA
Negative Supply Current	I−	V_{IN} = 0 or 2V	—	—	4.5	—	—	4.5	—	—	5	mA

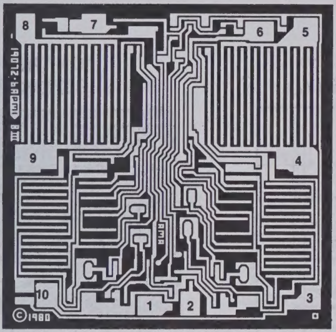
NOTES:

1. V_S = 0V, I_D = 100μA. Specified as a percentage of $R_{AVERAGE}$ where:

$$R_{AVERAGE} = \frac{R_{ON1} + R_{ON2}}{2}$$

2. Parameter guaranteed by design.
3. Current tested at V_{IN} = 2V. This is worst case condition.
4. Parameter tested only at T_A = 125°C for military grade device.

DICE CHARACTERISTICS



DIE SIZE 0.067 × 0.067 inch, 4489 sq mils
(1.702 × 1.702 mm, 2.896 sq. mm)

1. IN1
2. IN2
3. GND
4. S2
5. D2
6. V− (SUBSTRATE)
7. NC
8. D1
9. S1
10. V+

For additional DICE information refer to Section 2.

WAFER TEST LIMITS at V+ = 15V, V− = −15V, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-05N LIMIT	SW-05G LIMIT	UNITS
"ON" Resistance	R_{ON}	$-10V \le V_A \le 10V$, $I_S \le 1mA$	70	80	Ω MAX
R_{ON} Match Between Switches	R_{ON} Match	$V_A = 0V$, $I_S \le 100\mu A$	10	10	% MAX
ΔR_{ON} vs V_A	ΔR_{ON}	$-10V \le V_A \le 10V$, $I_S \le 1mA$	10	10	% MAX
Positive Supply	I+	Note 1	6	6	mA MAX
Negative Supply Current	I−	Note 1	3	3	mA MAX
Analog Voltage Range	V_A	$I_S = 1mA$	±10	±10	V MIN
Logic "1" Input Voltage	V_{INH}		2	2	V MIN
Logic "0" Input Voltage	V_{INL}		0.8	0.8	V MAX
Logic "0" Input Current	I_{INL}	$0V \le V_{IN} \le 0.8V$	5	5	µA MAX
Logic "1" Input Current	I_{INH}	$2V \le V_{IN} \le 15V$, Note 2	1	1	µA MAX
Analog Current Range	I_A	$V_S = \pm 10V$	10	8	mA MIN

Note: Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

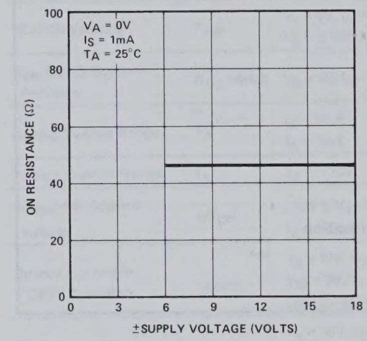
TYPICAL ELECTRICAL CHARACTERISTICS V+ = 15V, V− = −15V and $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-05N TYPICAL	SW-05G TYPICAL	UNITS
"ON" Resistance	R_{ON}	$-10V \le V_A \le 10V$, $I_S \le 1mA$	45	45	Ω
Turn-On-Time	t_{ON}		325	325	ns
Turn-Off-Time	t_{OFF}		310	310	ns
Drain Current in "OFF" Condition	$I_{D(OFF)}$	$V_S = 10V$, $V_D = -10V$	0.3	0.3	nA
Leakage Current in "ON" Condition	$I_{S(ON)} + I_{D(ON)}$	$V_S = V_D = \pm 10V$	0.3	0.3	nA
"OFF" Isolation	$I_{SO(OFF)}$	f = 500kHz, $R_L = 680\Omega$	62	62	dB
Crosstalk	C_T	f = 500kHz, $R_L = 680\Omega$	76	76	dB

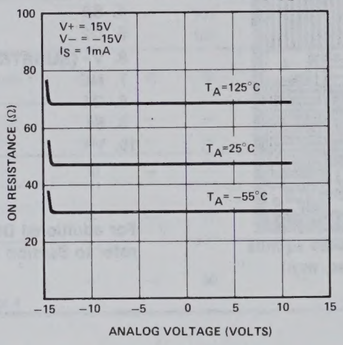
NOTES:
1. Power supply and ground current specified for switch "ON" or "OFF".
2. Current tested at $V_{IN} = 2V$. This is worst case condition.

TYPICAL PERFORMANCE CHARACTERISTICS

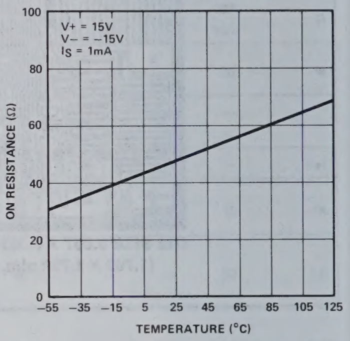
"ON" RESISTANCE vs SUPPLY VOLTAGE



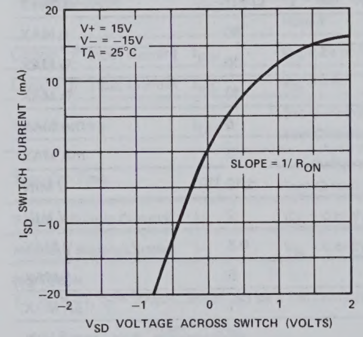
"ON" RESISTANCE vs ANALOG VOLTAGE (V_A)



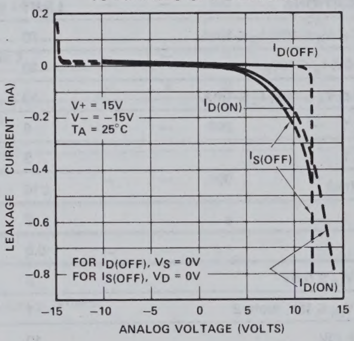
"ON" RESISTANCE vs TEMPERATURE



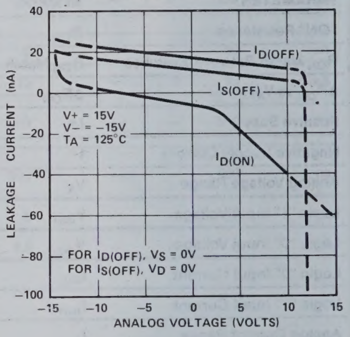
SWITCH CURRENT vs VOLTAGE



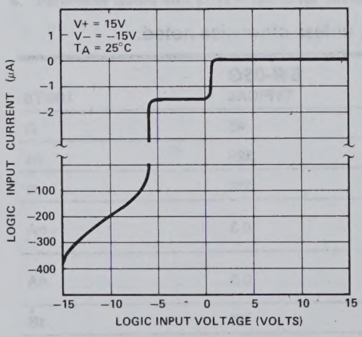
LEAKAGE CURRENT vs ANALOG VOLTAGE



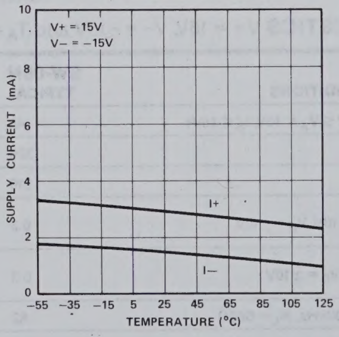
LEAKAGE CURRENT AT 125° C vs ANALOG VOLTAGE



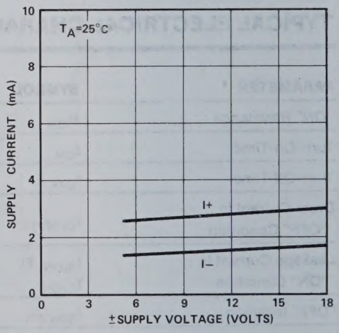
LOGIC INPUT CURRENT vs VOLTAGE



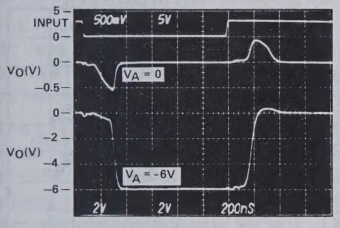
SUPPLY CURRENT vs TEMPERATURE



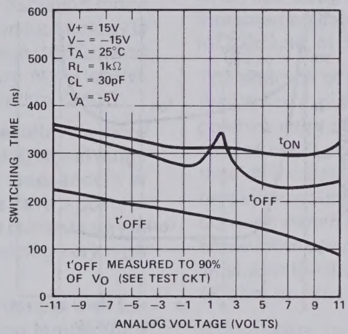
SUPPLY CURRENT vs SUPPLY VOLTAGE

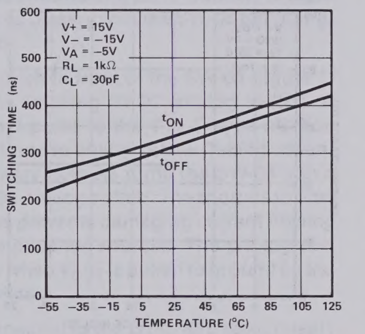


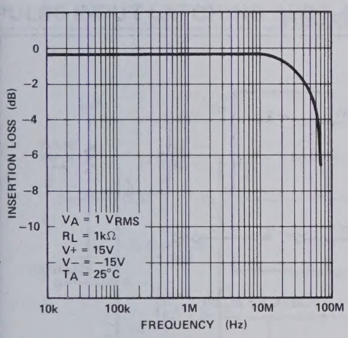
TYPICAL PERFORMANCE CHARACTERISTICS

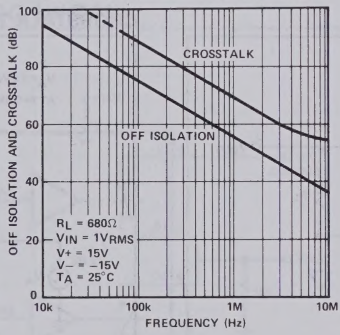

SWITCHING RESPONSE

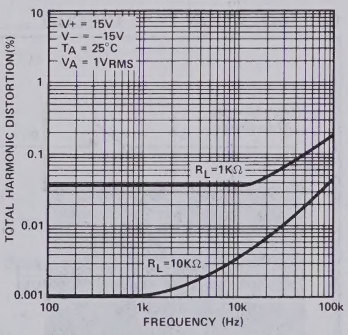
(SEE SWITCHING TIME TEST CIRCUIT)

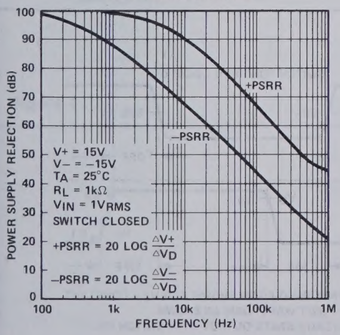

SWITCHING TIME vs ANALOG VOLTAGE

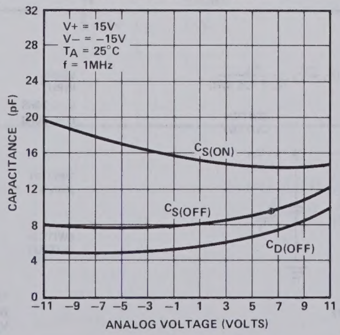

SWITCHING TIME vs TEMPERATURE

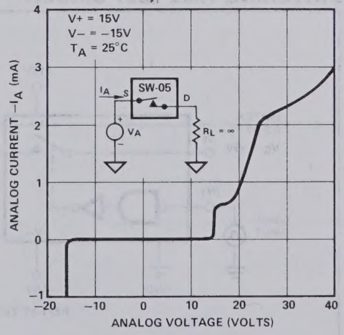

INSERTION LOSS vs FREQUENCY


OFF ISOLATION AND CROSSTALK vs FREQUENCY


DISTORTION vs FREQUENCY

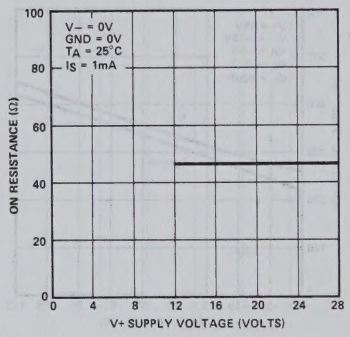

POWER SUPPLY REJECTION vs FREQUENCY


CAPACITANCE vs ANALOG VOLTAGE

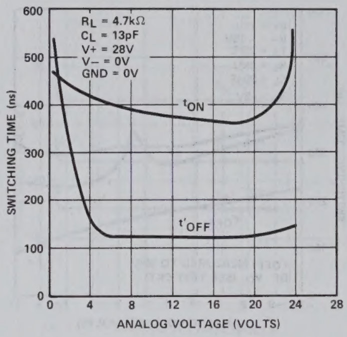

OVERVOLTAGE CHARACTERISTIC

TYPICAL PERFORMANCE CHARACTERISTICS (Single Supply Operation)

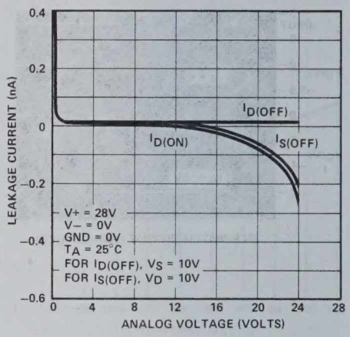
"ON" RESISTANCE vs SUPPLY VOLTAGE



SWITCHING TIME vs ANALOG VOLTAGE

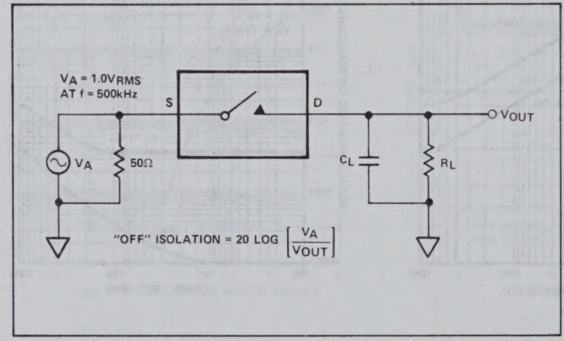


LEAKAGE CURRENT vs ANALOG VOLTAGE

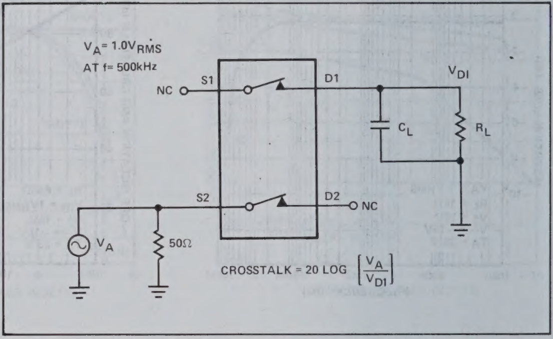


TEST CIRCUITS

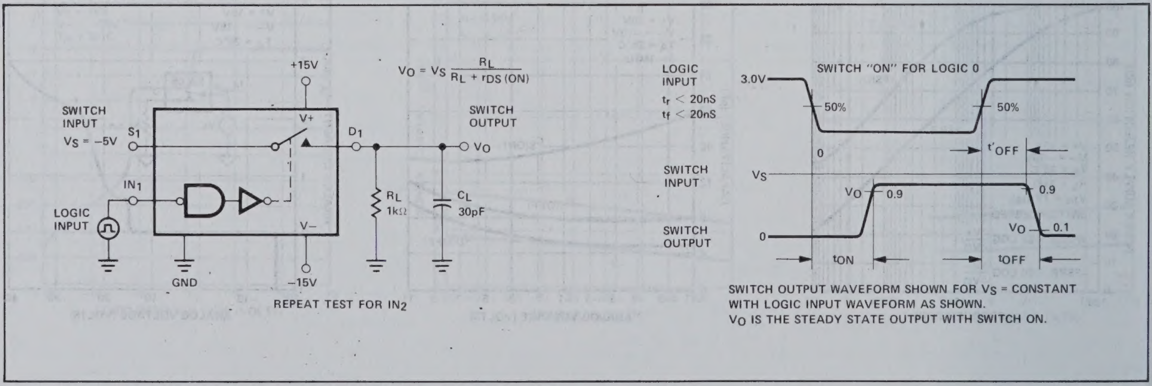
OFF ISOLATION TEST CIRCUIT


V_A = 1.0V_{RMS}
AT f = 500kHz
S
D
V_{OUT}
V_A
50Ω
C_L
R_L
"OFF" ISOLATION = 20 LOG $\left[\frac{V_A}{V_{OUT}}\right]$

CROSSTALK TEST CIRCUIT


V_A = 1.0V_{RMS}
AT f= 500kHz
NC
S1
D1
V_{DI}
C_L
R_L
S2
D2
NC
V_A
50Ω
CROSSTALK = 20 LOG $\left[\frac{V_A}{V_{DI}}\right]$

SWITCHING TIME TEST CIRCUIT


+15V
$V_O = V_S \frac{R_L}{R_L + r_{DS(ON)}}$
SWITCH INPUT
V_S = –5V
S_1
V+
D_1
SWITCH OUTPUT
V_O
IN_1
LOGIC INPUT
R_L
1kΩ
C_L
30pF
V–
GND
–15V
REPEAT TEST FOR IN_2
LOGIC INPUT
t_r < 20nS
t_f < 20nS
SWITCH INPUT
SWITCH OUTPUT
3.0V
SWITCH "ON" FOR LOGIC 0
50%
50%
0
t'_{OFF}
V_S
V_O
0.9
0.9
0
V_O
0.1
t_{ON}
t_{OFF}

SWITCH OUTPUT WAVEFORM SHOWN FOR V_S = CONSTANT WITH LOGIC INPUT WAVEFORM AS SHOWN.
V_O IS THE STEADY STATE OUTPUT WITH SWITCH ON.

APPLICATION INFORMATION

The SW-05 provides a rugged BIFET alternative to the industry standard CMOS generic DG200 device. The basic differences in process (CMOS vs BIFET) effecting switch characteristics result from the parallel connected enhancement mode FETs used in CMOS versus the single depletion mode JFET used by the BIFET process. The junction technology is far less susceptable to electrostatic damage (ESD), and offers a higher resistance to radiation exposure. No extensive threshold shifts take place as commonly found in CMOS.

The basic BIFET switch design inherently results in a more linear "ON" resistance over the designed analog signal range of −15 to +11 volts. The "ON" resistance is independent of analog voltage and supply voltage, but does have a positive temperature coefficient of 0.4%/° C. Leakage currents stay in the low picoamps at room temperature providing very high "OFF" resistance characteristics.

The logic control inputs are TTL input compatible with full 400mV noise immunity over the full operating temperature range. The PNP input structure requires very little logic drive current resulting in minimum output loading to both TTL and CMOS logic. Since the SW-05 incorporates a standard two forward diode drop logic voltage reference, pin 7 in the metal can and pin 12 in the DIP package were left unconnected. This allows direct plug-in compatibility with DG200's requiring external logic threshold adjustment to their V_{REF} pin when operating from supplies other than ±15 volts. No logic threshold adjustment is necessary with the SW-05 operating, for example, at ±12 volts.

The addition of a 7474 latch in front of the SW-05 (figure 1) results in a pulse input latching SPDT analog switch. A positive edge of an input pulse to the TTL D type flip flop causes the Q and $\overline{Q}$ outputs to change state. Taking advantage of the complementary outputs turns the SW-05 into a break-before-make SPDT analog switch. The short dead time between switch closures prevents damaging current flowing between the two low impedance sources. The photograph illustrates the dead time when V_{OUT} is pulled to ground by the 1K ohm termination resistor.

The initialize input, connected to the D flip flop reset (clear) input, resets Q_1 sending an active low to the IN_1 terminal of the SW-05 closing switch 1.

PULSE INPUT LATCHING SPDT ANALOG SWITCH

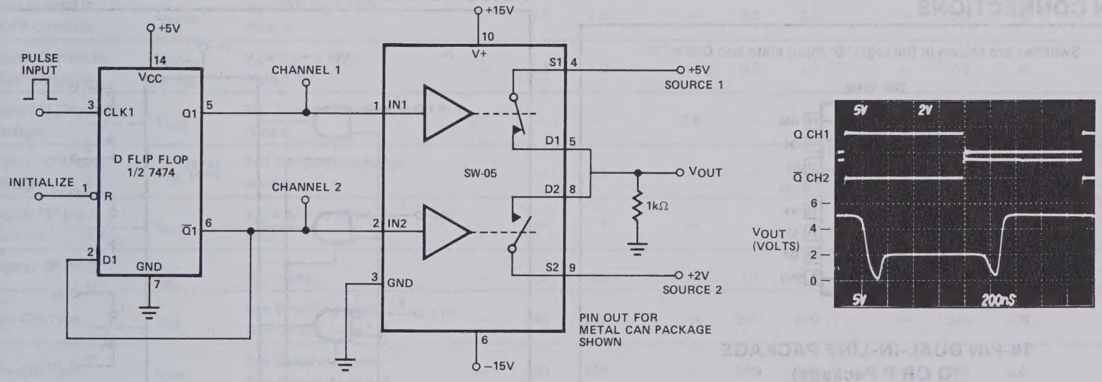


Figure 1

SW-06

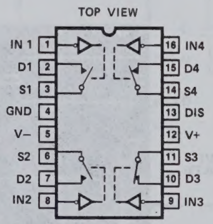
QUAD SPST BIFET ANALOG SWITCH

FEATURES

- **Two Normally Open and Two Normally Closed SPST Switches with Disable**
- **Switches can be Easily Configured as a Dual SPDT or a DPDT**
- **Highly Resistant to Static Discharge Destruction**
- **Higher Resistance to Radiation Than Analog Switches Designed with MOS Devices**
- **Guaranteed R_{ON} Matching .... 10% Max**
- **Guaranteed Switching Speeds .... T_{ON} = 500ns Max**
  T_{OFF} = 400ns Max
- **Guaranteed Break-Before-Make Switching**
- **Low "ON" Resistance .... 80Ω Max**
- **Low R_{ON} Variation from Analog Input Voltage 5%**
- **Low Total Harmonic Distortion 0.01%**
- **Low Leakage Currents at High Temperature:**
  $T_A = 125°C$ .... 100nA Max
  $T_A = 85°C$ .... 30nA Max
- **Digital Inputs TTL/CMOS Compatible and Independent of V+**
- **Improved Specifications and Pin Compatible to LF-11333/13333**
- **Dual or Single Power Supply Operation**

PIN CONNECTIONS

Switches are shown in the logic "0" input state and DIS = "1"



16-PIN DUAL-IN-LINE PACKAGE
(Q OR P Package)

ORDERING INFORMATION†

PACKAGE IS 16-PIN DIP	ORDER PART NUMBER	OPERATING TEMPERATURE RANGE
HERMETIC	SW06BQ*	MIL
	SW06FQ	IND
	SW06GQ	COM
EPOXY	SW06GP	COM

*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

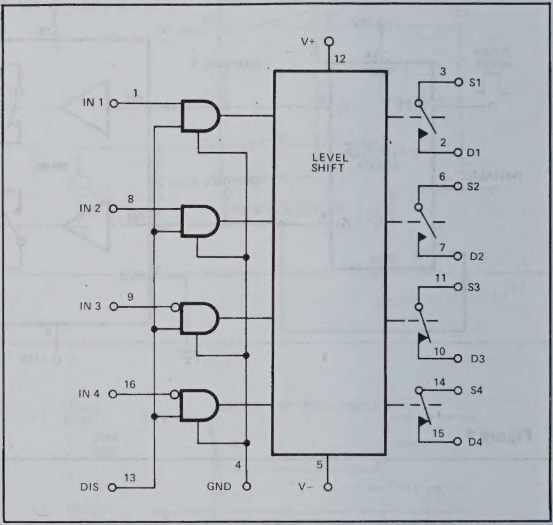
GENERAL DESCRIPTION

The SW-06 is a four channel single-pole, single-throw analog switch that employs both bipolar and ion-implanted FET devices. The SW-06 FET switches use bipolar digital logic inputs which are more resistant to static electricity than CMOS devices. Ruggedness and reliability are inherent in the SW-06 design and construction technology.

Increased reliability is complemented by excellent electrical specifications. Potential error sources are reduced by minimizing "ON" resistance and controlling leakage currents at high temperatures. The switching FET exhibits minimal R_{ON} variation over a 20V analog signal range and with power supply voltage changes. Operation from a single positive power supply voltage is possible. With V+ = 36V, V– = 0V, the analog signal range will extend from ground to +32V.

PNP logic inputs are TTL and CMOS compatible to allow the SW-06 to upgrade existing designs. The logic "0" and logic "1" input currents are at micro-ampere levels reducing loading on CMOS and TTL logic.

FUNCTIONAL DIAGRAM



TRUTH TABLE

DISABLE INPUT	LOGIC INPUT	SWITCH STATE CHANNELS 1 & 2	SWITCH STATE CHANNELS 3 & 4
0	X	OFF	OFF
1 or NC	0	OFF	ON
1 or NC	1	ON	OFF

ABSOLUTE MAXIMUM RATINGS (Note 1)

Operating Temperature Range
 SW-06BQ .... −55°C to +125°C
 SW-06FQ .... −25°C to +85°C
 SW-06GP .... 0°C to +70°C
Storage Temperature Range .... −65°C to +150°C
Power Dissipation (Note 2)
 Q Package 900mW
 P Package 500mW
Lead Temperature (Soldering 60 sec) .... 300°C
Maximum Junction Temperature .... 150°C
V+ Supply to V− Supply 36V
V+ Supply to Ground 36V
Logic Input Voltage .... (−4V or V−) to V+ Supply
Analog Input Voltage Range
 Continuous .... V− Supply to V+ Supply +20V
Maximum Current Through
 Any Pin Including Switch 30mA

NOTES:

1. Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Q Package derated 12mW/°C above 75°C, P Package derated 10mW/°C above 25°C.

ELECTRICAL CHARACTERISTICS at $V+ = 15V$, $V- = -15V$ and $T_A = 25°C$, unless otherwise noted.

			SW-06B			SW-06F			SW-06G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
"ON" Resistance	R_{ON}	$V_S = 0V$, $I_S = 1mA$ $V_S = \pm 10V$, $I_S = 1mA$	— —	60 65	80 80	— —	60 65	100 100	— —	100 100	150 150	Ω
R_{ON} Match Between Switches	R_{ON} Match	$V_S = 0V$, $I_S = 100\mu A$, Note 1	—	5	10	—	5	20	—	—	20	%
Analog Voltage Range	V_A	$I_S = 1mA$ $I_S = 1mA$	+10 −10	+11 −15	— —	+10 −10	+11 −15	— —	+10 −10	+11 −15	— —	V
Analog Current Range	I_S	$V_S = \pm 10V$	10	15	—	7	12	—	5	10	—	mA
ΔR_{ON} vs Applied Voltage	ΔR_{ON}	$-10V \le V_S \le 10V$, $I_S = 1.0mA$	—	5	15	—	10	20	—	10	20	%
Source Current in "OFF" Condition	$I_{S(OFF)}$	$V_S = 10V$, $V_D = -10V$, Note 5	—	0.3	2.0	—	0.3	2.0	—	0.3	10	nA
Drain Current in "OFF Condition	$I_{D(OFF)}$	$V_S = 10V$, $V_D = -10V$, Note 5	—	0.3	2.0	—	0.3	2.0	—	0.3	10	nA
Source Current in "ON" Condition	$I_{S(ON)}+$ $I_{D(ON)}$	$V_S = V_D = \pm 10V$, Note 5	—	0.3	2.0	—	0.3	2.0	—	0.3	10	nA
Logical "1" Input Voltage	V_{INH}	Full Temperature Range, Note 6	2.0	—	—	2.0	—	—	2.0	—	—	V
Logical "0" Input Voltage	V_{INL}	Full Temperature Range, Note 6	—	—	0.8	—	—	0.8	—	—	0.8	V
Logical "1" Input Current	I_{INH}	$V_{IN} = 2.0V$ to $15.0V$, Note 4	—	—	1	—	—	1	—	—	1	µA
Logical "0" Input	I_{INL}	$V_{IN} = 0.8V$,	—	1.5	5.0	—	1.5	5.0	—	1.5	10.0	µA
Turn-On-Time	t_{ON}	See Switching Time Test Circuit, Note 2, 6	—	340	500	—	340	600	—	340	700	ns
Turn-Off-Time	t_{OFF}	See Switching Time Test Circuit, Note 2, 6	—	200	400	—	200	400	—	200	500	ns
Break-Before-Make Time	$t_{ON}-t_{OFF}$	Notes 2, 3	50	140	—	50	140	—	50	140	—	ns
Source Capacitance	$C_{S(OFF)}$	$V_S = 0V$, Note 5	—	7.0	—	—	7.0	—	—	7.0	—	pF
Drain Capacitance	$C_{D(OFF)}$	$V_S = 0V$, Note 5	—	5.5	—	—	5.5	—	—	5.5	—	pF
Channel "ON" Capacitance	$C_{D(ON)}+$ $C_{S(ON)}$	$V_S = V_D = 0V$, Note 5	—	15	—	—	15	—	—	15	—	pF
"OFF" Isolation	$I_{SO(OFF)}$	$V_S = 1V_{RMS}$, $R_L = 680\Omega$, $C_L = 7pF$, $f = 500kHz$, Note 5	—	58	—	—	58	—	—	58	—	dB
Crosstalk	C_T	$V_S = 1V_{RMS}$, $R_L = 680\Omega$, $C_L = 7pF$, $f = 500kHz$, Note 5	—	70	—	—	70	—	—	70	—	dB
Positive Supply Current	$I+$	All Channels "OFF", Note 5	—	5.0	6.0	—	5.0	9.0	—	6.0	9.0	mA
Negative Supply Current	$I-$	All Channels "OFF", Note 5	—	3.0	5.0	—	4.0	7.0	—	4.0	7.0	mA
Ground Current	I_G	All Channels "ON" or "OFF", Note 5	—	3.0	4.0	—	3.0	4.0	—	3.0	5.0	mA

ELECTRICAL CHARACTERISTICS at $V+ = 15V$, $V- = -15V$, $-55°C \leq T_A \leq +125°C$ for SW-06BQ, $-25°C \leq T_A \leq +85°C$ for SW-06FQ and $0°C \leq T_A \leq 70°C$ for SW-06GP, unless otherwise noted.

			SW-06B			SW-06F			SW-06G			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Temperature Range	T_A	Operating	−55	—	125	−25	—	85	0	—	70	°C
"ON" Resistance	R_{ON}	$V_S = 0V$, $I_S = 1.0mA$ $V_S = \pm 10V$, $I_S = 1.0mA$	— —	75 80	110 110	— —	75 80	125 125	— —	75 80	175 175	Ω
R_{ON} Match Between Switches	R_{ON} Match	$V_S = 0V$, $I_S = 100\mu A$, Note 1	—	6	20	—	6	25	—	10	—	%
Analog Voltage Range	V_A	$I_S = 1.0mA$ $I_S = 1.0mA$	+10 −10	+11 −15	— —	+10 −10	+11 −15	— —	+10 −10	+11 −15	— —	V
Analog Current Range	I_A	$V_S = \pm 10.0V$	7	12	—	5	11	—	—	11	—	mA
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$-10V \leq V_S \leq +10V$, $I_S = 100\mu A$	—	10	—	—	12	—	—	15	—	%
Source Current in "OFF" Condition	$I_{S(OFF)}$	$V_S = 10V$, $V_D = -10V$, T_A = Max. Operating Temp., Notes 5, 7	—	—	60	—	—	30	—	—	60	nA
Drain Current in "OFF" Condition	$I_{D(OFF)}$	$V_S = 10V$, $V_D = -10V$, T_A = Max. Operating Temp., Notes 5, 7	—	—	60	—	—	30	—	—	60	nA
Leakage Current in "ON" Condition	$I_{S(ON)}+$ $I_{D(ON)}$	$V_S = V_D = \pm 10V$, T_A = Max. Operating Temp., Notes 5, 7	—	—	100	—	—	30	—	—	60	nA
Logical "1" Input Current	I_{INH}	$V_{IN} = 2.0V$ to $15.0V$, Note 4	—	—	5	—	—	5	—	—	5	μA
Logical "0" Input Current	I_{INL}	$V_{IN} = 0.8V$,	—	4	10	—	4	10	—	5	15	μA
Turn-On-Time	t_{ON}	See Switching Time Test Circuit, Notes 2, 6	—	440	900	—	500	900	—	—	1000	ns
Turn-Off-Time	t_{OFF}	See Switching Time Test Circuit, Notes 2, 6	—	300	500	—	330	500	—	—	500	ns
Break-Before-Make Time	$t_{ON}-t_{OFF}$		—	70	—	—	70	—	—	50	—	ns
Positive Supply Current	I+	All Channels "OFF", Note 5	—	—	9.0	—	—	13.5	—	—	13.5	mA
Negative Supply Current	I−	All Channels "OFF", Note 5	—	—	7.5	—	—	10.5	—	—	10.5	mA
Ground Current	I_G	All Channels "ON" or "OFF", Note 5	—	—	6.0	—	—	7.5	—	—	7.5	mA

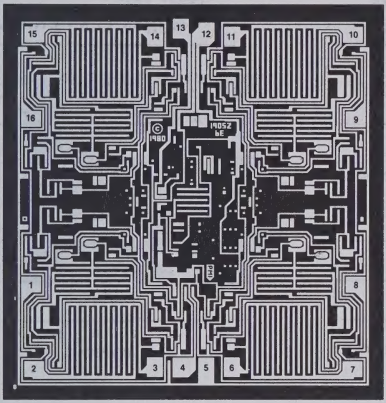
NOTES:

1. $V_S = 0V$, $I_S = 100\mu A$. specified as a percentage of $R_{AVERAGE}$ where:

$$R_{AVERAGE} = \frac{R_{ON1} + R_{ON2} + R_{ON3} + R_{ON4}}{4}$$

2. Guaranteed by design.
3. Switch is guaranteed to provide break-before-make operation.
4. Current tested at $V_{IN} = 2.0V$. This is worst case condition.
5. Switch being tested ON or OFF as indicated, $V_{INH} = 2.0V$ or $V_{INL} = 0.8V$, per logic truth table.
6. Also applies to disable pin.
7. Parameter tested only at $T_A = +125°C$ for military grade device.

DICE CHARACTERISTICS



1. IN (1)
2. D (1)
3. S (1)
4. GND
5. V− (SUBSTRATE)
6. S (2)
7. D (2)
8. IN (2)
9. IN (3)
10. D (3)
11. S (3)
12. V+
13. DISABLE
14. S (4)
15. D (4)
16. IN (4)

DIE SIZE 0.100 × 0.096 inch, 9600 sq. mils
(2.540 × 2.438 mm, 6.193 sq. mm)

For additional DICE information
refer to Section 2.

WAFER TEST LIMITS at $V+ = 15V$, $V- = -15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-06N LIMIT	SW-06G LIMIT	UNITS
"ON" Resistance	R_{ON}	$-10V \le V_A \le 10V$, $I_S \le 1mA$	80	100	Ω MAX
R_{ON} Match Between Switches	R_{ON} Match	$V_A = 0V$, $I_S \le 100\mu A$	15	20	% MAX
ΔR_{ON} vs V_A	ΔR_{ON}	$-10V \le V_A \le 10V$, $I_S \le 1mA$	10	20	% MAX
Positive Supply Current	$I+$	Note 1	6.0	9.0	mA MAX
Negative Supply Current	$I-$	Note 1	5.0	7.0	mA MAX
Ground Current	I_G	Note 1	4.0	4.0	mA MAX
Analog Voltage Range	V_A	$I_S = 1mA$	±10.0	±10.0	V MIN
Logic "1" Input Voltage	V_{INH}		2.0	2.0	V MIN
Logic "0" Input Voltage	V_{INL}		0.8	0.8	V MAX
Logic "0" Input Current	I_{INL}	$0V \le V_{IN} \le 0.8V$	5.0	5.0	µA MAX
Logic "1" Input Current	I_{INH}	$2.0V \le V_{IN} \le 15V$, Note 2	0.1	0.1	µA MAX
Analog Current Range	I_A	$V_S = \pm 10V$	10	7	mA MIN

Note: Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V+ = 15V$, $V- = -15V$ and $T_A = 25°C$, unless otherwise noted.

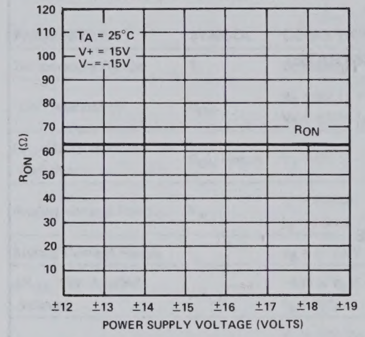
PARAMETER	SYMBOL	CONDITIONS	SW-06N TYPICAL	SW-06G TYPICAL	UNITS
"ON" Resistance	R_{ON}	$-10V \le V_A \le 10V$, $I_S \le 1mA$	60	60	Ω
Turn-On-Time	t_{ON}		340	340	ns
Turn-Off-Time	t_{OFF}		200	200	ns
Drain Current in "OFF" Condition	$I_{D(OFF)}$	$V_S = 10V$, $V_D = -10V$	0.3	0.3	nA
"OFF" Isolation	$I_{SO(OFF)}$	$f = 500kHz$, $R_L = 680\Omega$	58	58	dB
Crosstalk	C_T	$f = 500kHz$, $R_L = 680\Omega$	70	70	dB

NOTES:

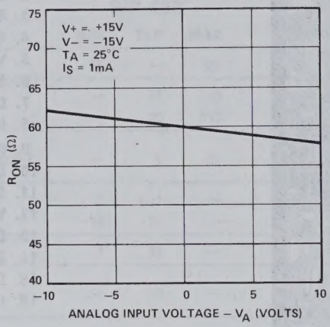
1. Power supply and ground current specified for switch "ON" or "OFF".
2. Current tested at $V_{IN} = 2.0V$. This is worst case condition.

TYPICAL PERFORMANCE CHARACTERISTICS

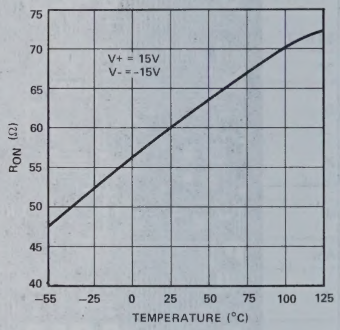
"ON" RESISTANCE vs POWER SUPPLY VOLTAGE



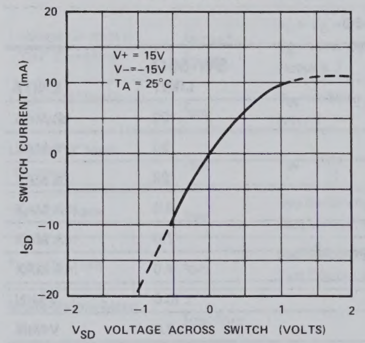
"ON" RESISTANCE vs ANALOG VOLTAGE



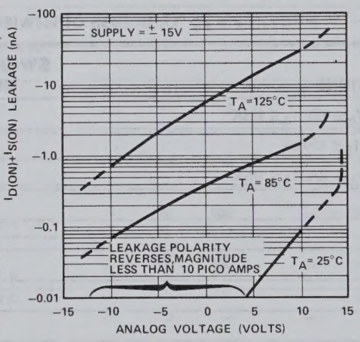
RON vs TEMPERATURE



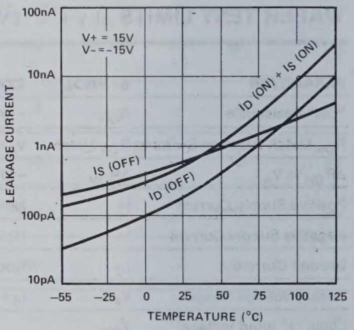
SWITCH CURRENT vs VOLTAGE



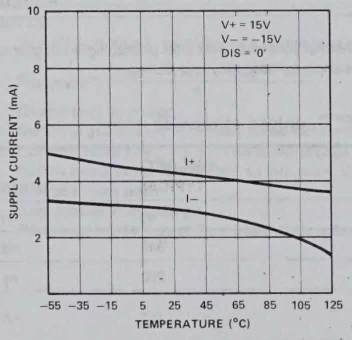
LEAKAGE CURRENT vs ANALOG VOLTAGE



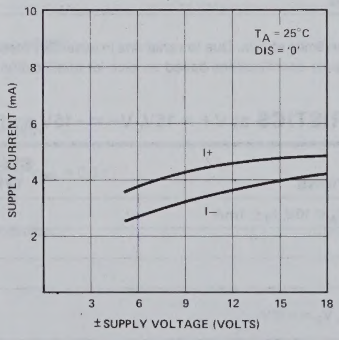
LEAKAGE CURRENT vs TEMPERATURE



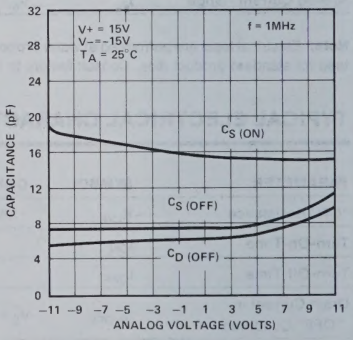
SUPPLY CURRENT vs TEMPERATURE



SUPPLY CURRENT vs SUPPLY VOLTAGE

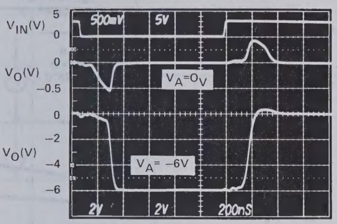


SWITCH CAPACITANCE vs ANALOG VOLTAGE

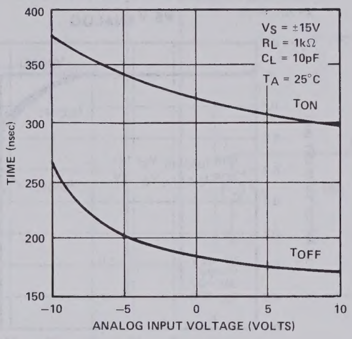


TYPICAL PERFORMANCE CHARACTERISTICS

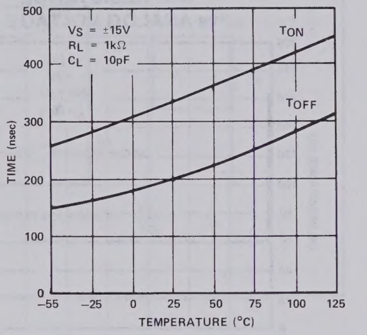
T_{ON}/T_{OFF} SWITCHING RESPONSE



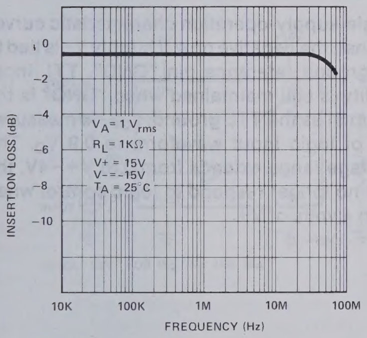
SWITCHING TIME vs ANALOG VOLTAGE



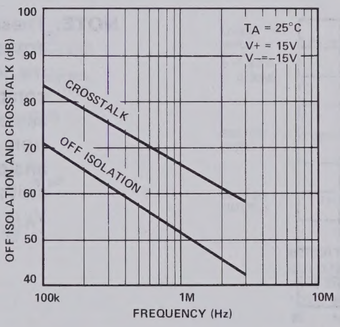
SWITCHING TIME vs TEMPERATURE



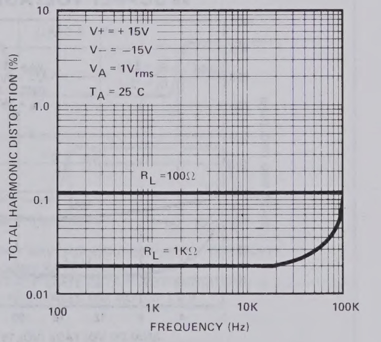
INSERTION LOSS vs FREQUENCY



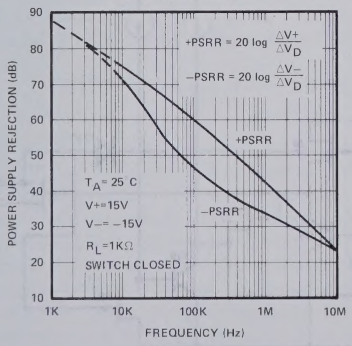
CROSSTALK AND "OFF" ISOLATION vs FREQUENCY



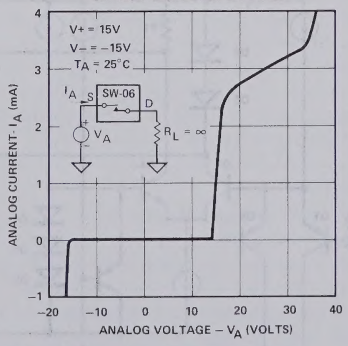
TOTAL HARMONIC DISTORTION



POWER SUPPLY REJECTION vs FREQUENCY

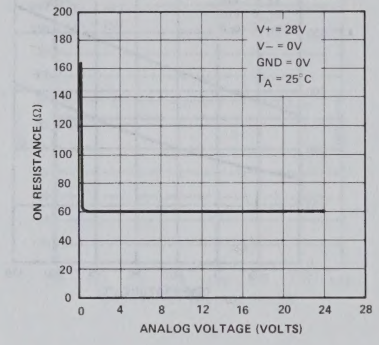


OVERVOLTAGE CHARACTERISTICS

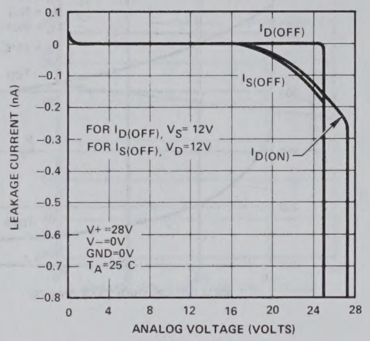


TYPICAL PERFORMANCE CHARACTERISTICS (OPERATING SINGLE SUPPLY)

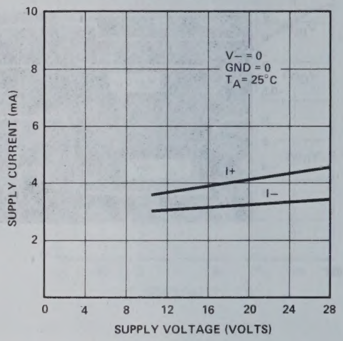
"ON" RESISTANCE vs ANALOG VOLTAGE



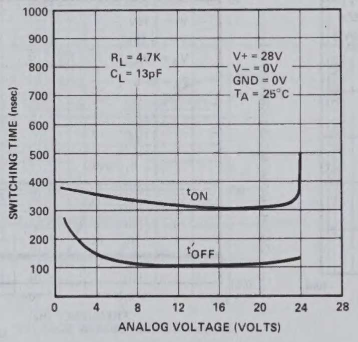
LEAKAGE CURRENT vs V_{ANALOG}



SUPPLY CURRENT vs SUPPLY VOLTAGE

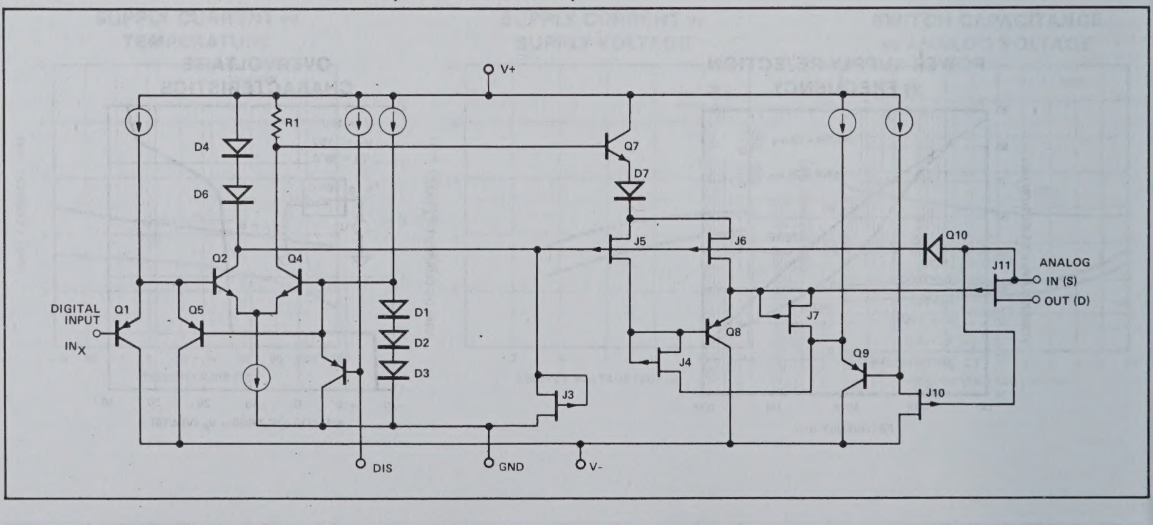


SWITCHING TIME vs SUPPLY VOLTAGE

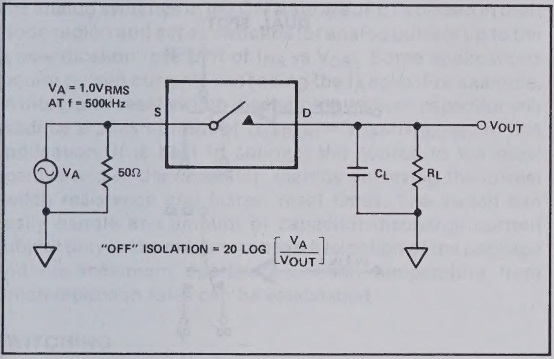


NOTE: These single-supply-operation characteristic curves are valid when the negative power supply V− is tied to the logic ground reference pin "GND". TTL input compatibility is still maintained when "GND" is the same potential as the TTL ground. t'_{OFF} is measured from 50% of logic input waveform to 0.9 V_O. The analog voltage range extends from 0 to V+ −4V, the switch will no longer respond to logic control when V_A is within 4 volts of V+.

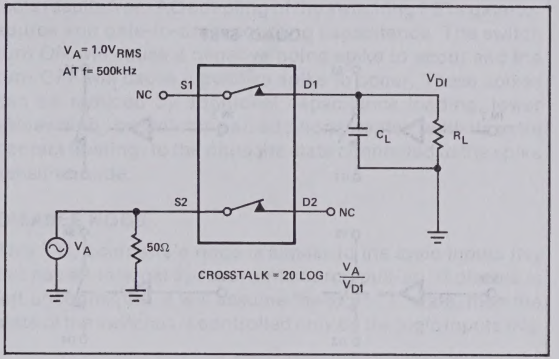
SIMPLIFIED SCHEMATIC DIAGRAM (TYPICAL SWITCH)


V+
R1
D4
D6
Q7
D7
J5
J6
Q10
Q2
Q4
J11
ANALOG
IN (S)
OUT (D)
DIGITAL
INPUT
IN_X
Q1
Q5
D1
D2
D3
J7
Q8
J4
Q9
J3
J10
DIS
GND
V-

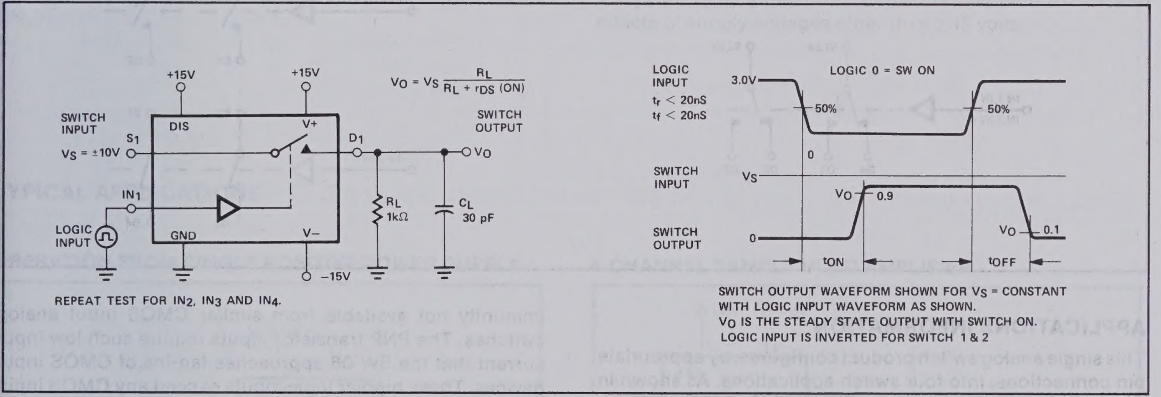
OFF ISOLATION TEST CIRCUIT


$V_A = 1.0V_{RMS}$
AT f = 500kHz
S
D
V_{OUT}
V_A
50Ω
C_L
R_L
"OFF" ISOLATION = 20 LOG $\left[\frac{V_A}{V_{OUT}}\right]$

CROSSTALK TEST CIRCUIT


$V_A = 1.0V_{RMS}$
AT f= 500kHz
NC
S1
D1
V_{DI}
C_L
R_L
S2
D2
NC
V_A
50Ω
CROSSTALK = 20 LOG $\frac{V_A}{V_{DI}}$

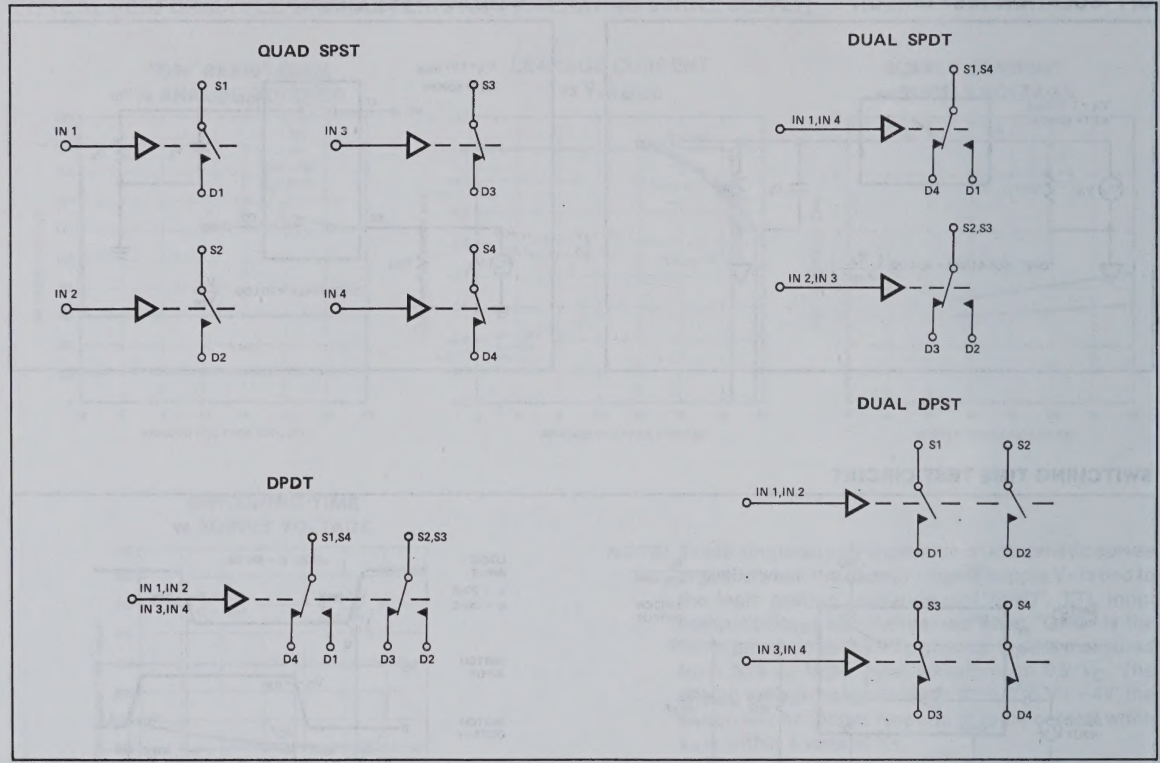
SWITCHING TIME TEST CIRCUIT


+15V
+15V
$V_O = V_S \frac{R_L}{R_L + r_{DS}(ON)}$
SWITCH INPUT
S_1
$V_S = \pm 10V$
DIS
V+
D_1
SWITCH OUTPUT
V_O
IN_1
R_L 1kΩ
C_L 30 pF
LOGIC INPUT
GND
V−
−15V
LOGIC INPUT
$t_r < 20nS$
$t_f < 20nS$
3.0V
LOGIC 0 = SW ON
50%
50%
0
SWITCH INPUT
V_S
V_O
0.9
SWITCH OUTPUT
0
V_O
0.1
t_{ON}
t_{OFF}

REPEAT TEST FOR IN_2, IN_3 AND IN_4.

SWITCH OUTPUT WAVEFORM SHOWN FOR V_S = CONSTANT WITH LOGIC INPUT WAVEFORM AS SHOWN.
V_O IS THE STEADY STATE OUTPUT WITH SWITCH ON.
LOGIC INPUT IS INVERTED FOR SWITCH 1 & 2

Figure 1: Functional Applications of SW-06



APPLICATIONS INFORMATION

This single analog switch product configures, by appropriate pin connections, into four switch applications. As shown in Figure 1, the SW-06 connects as a QUAD SPST, a DUAL SPDT, a DUAL DPST, or a DPDT analog switch. This versatility increases further when taking advantage of the disable input (DIS) which turns all switches OFF when taken active low.

Ion-implantation of the JFET analog switch achieves low ON resistance and tight channel to channel matching. Combining the low ON resistance and low leakage currents results in a worst case voltage error figure V_{ERROR} @ 125° C = $I_{D(ON)} \times R_{SD(ON)} = 100nA \times 100\Omega = 11$ microvolts. This amount of error is negligible considering dissimilar-metal thermally-induced offsets will be in the 5 to 15 microvolt range.

LOGIC INPUTS

The logic inputs (IN_X) and disable input (DIS) are referenced to a TTL logic threshold value of two forward diode drops (1.4V at 25° C) above the GND terminal. These inputs use PNP transistors which draw maximum current at a logic "0" level and drops to a leakage current of a reverse biased diode as the logic input voltage raises above 1.4 volts. Any logic input voltage greater than 2.0 volts becomes logic "1", less than 0.8 volts becomes logic "0" resulting in full TTL noise immunity not available from similar CMOS input analog switches. The PNP transistor inputs require such low input current that the SW-06 approaches fan-ins of CMOS input devices. These bipolar logic inputs exceed any CMOS input circuit in resistance to static voltage and radiation susceptability. No damage will occur to the SW-06 if logic high voltages are present when the SW-06 power supplies are OFF. When the V+ and V− supplies are OFF, the logic inputs present a reverse bias diode loading to active logic inputs. Input logic thresholds are independent of V+ and V− supplies making single V+ supply operation possible by simply connecting GND and V− together to the logic ground supply.

ANALOG VOLTAGE AND CURRENT

ANALOG VOLTAGE

These switches have constant ON resistance for analog voltages from the negative power supply (V−) to within 4 volts of the positive power supply. This characteristic shown in the plots results in good total harmonic distortion, especially when compared to CMOS analog switches that have a 20 to 30 percent variation in ON resistance versus analog voltage. Positive analog input voltages should be restricted to 4 volts less than V+ assuring the switch remains open circuit in the OFF state. No increase in switch ON resistance occurs when operating at supply voltages less than ±15 volts (see plot). Small signals have a 3dB down frequency of 70MHz (see insertion loss versus frequency plot).

ANALOG CURRENT

The analog switches in the ON state are JFETs biased in their triode region and act as switches for analog current up to the I_A specification (see plot of I_{DS} vs V_{DS}). Some applications require pulsed currents exceeding the I_A spec. For example, an integrator reset switch discharging a shunt capacitor will produce a peak current of $I_{A(PEAK)} = V_{CAP}/R_{DS(ON)}$. In this application, it is best to connect the source to the most positive end of the capacitor, thereby achieving the lowest switch resistance and fastest reset times. The switch can easily handle any amount of capacitor discharge current subject only to the maximum heat dissipation of the package and the maximum operating junction temperature from which repetition rates can be established.

SWITCHING

Switching time t_{ON} and t_{OFF} characteristics are plotted versus V_{ANALOG} and temperature. In all cases, t_{OFF} is designed faster than t_{ON} to insure a break-before-make interval for SPDT and DPDT applications. The disable input (DIS) has the same switching times (t_{ON} and t_{OFF}) as the logic inputs (IN_X).

Switching transients occurring at the source and drain contacts results from AC coupling of the switching FETs gate-to-source and gate-to-drain coupling capacitance. The switch turn ON will cause a negative going spike to occur and the turn OFF will cause a positive spike to occur. These spikes can be reduced by additional capacitance loading, lower values of R_L, or switching an additional switch (with its extra contact floating) to the opposite state connected to the spike sensitive node.

DISABLE NODE

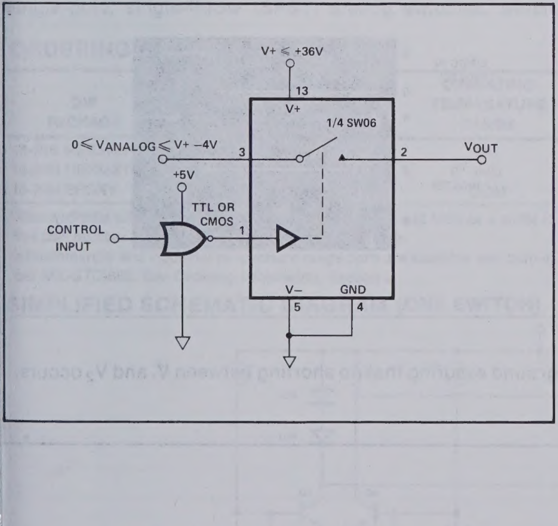
This TTL compatible node is similar to the logic inputs IN_X but has an internal 2μA current source pull-up. If disable is left unconnected, it will assume the logic "1" state, then the state of the switches is controlled only by the logic inputs IN_X.

POWER SUPPLIES

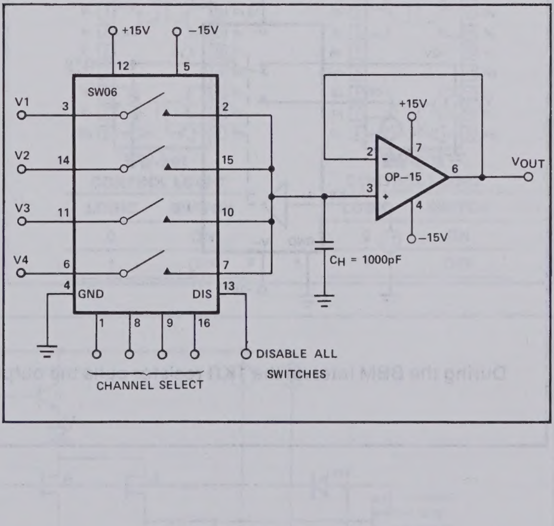
This product operates with power supply voltages ranging from ±12 to ±18 volts; however, the specifications only guarantee device parameters with ±15 volt ±5% power supplies. The power supply sensitive parameters have plots to indicate effects of supply voltages other than ±15 volts.

TYPICAL APPLICATIONS

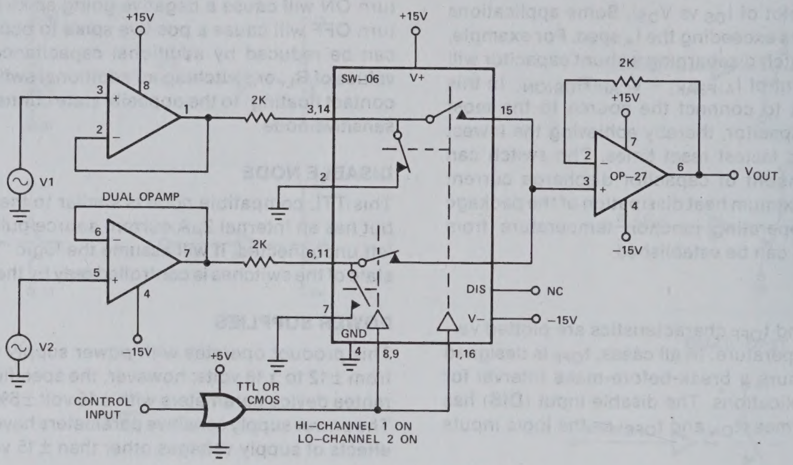
OPERATION FROM SINGLE POSITIVE POWER SUPPLY



4-CHANNEL SAMPLE HOLD AMPLIFIER

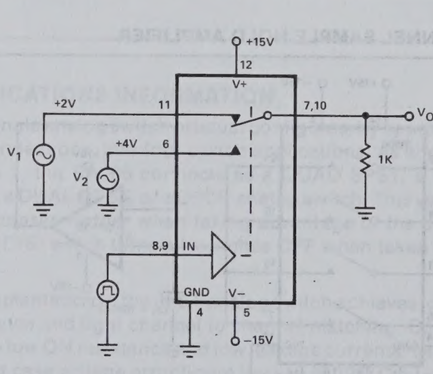


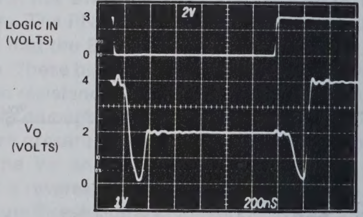
HIGH OFF ISOLATION SELECTOR SWITCH (Shunt-Series Switch)


+15V
+15V
SW–06
V+
3
8
2
1
2K
3,14
15
2K
+15V
7
2
6
3
OP–27
VOUT
4
–15V
V1
DUAL OPAMP
2
6
7
5
4
2K
6,11
DIS
NC
7
V–
–15V
V2
–15V
GND
4
8,9
1,16
+5V
TTL OR CMOS
CONTROL INPUT
HI–CHANNEL 1 ON
LO–CHANNEL 2 ON

THIS SWITCH ARRANGEMENT IMPROVES OFF ISOLATION BY 30dB

SINGLE POLE DOUBLE THROW SELECTOR SWITCH WITH BREAK-BEFORE-MAKE INTERVAL


+15V
12
V+
+2V
11
7,10
VO
+4V
6
V1
V2
1K
8,9
IN
GND
V–
4
5
–15V



During the BBM interval the 1KΩ resistor pulls the output to ground assuring that no shorting between V_1 and V_2 occurs.

QUAD SPST BIFET ANALOG SWITCHES

SW-201/SW-202

FEATURES

SW-201

- **Normally "ON" for Logic 0 Input**
- **Improved Performance and Pin Compatible With DG-201, LF11201/13201, HI201, and IH201**

SW-202

- **Normally "OFF" For Logic 0 Input**
- **Improved Performance and Pin Compatible With LF11202/12202/13202 and IH202**

Both SW-201 and SW-202

- **Highly Resistant to Static Discharge Destruction**
- **Guaranteed Break-Before-Make Switching ($t_{OFF} < t_{ON}$)**
- **Low "ON" Resistance .... 80Ω Max**
- **Guaranteed R_{ON} Matching .... 15% Max**
- **Low R_{ON} Variation from Analog Input Voltage 5%**
- **High Analog Current Operation .... 10mA Min**
- **Low Leakage Currents at High Temperatures:**
  - **$T_A = 125°C$ .... 60nA Max**
  - **$T_A = 85°C$ .... 30nA Max**
- **Guaranteed Switching Speeds:**
  - **$t_{ON} = 500ns$ Max $t_{OFF} = 400ns$ Max**
- **Digital Inputs are TTL and CMOS Compatible**
- **Dual or Single Supply Operation**

GENERAL DESCRIPTION

The SW-201 and SW-202 each consist of four independent, single-pole, single-throw (SPST) analog switches, which may be independently digitally controlled. Each SW-201 switch is normally closed (NC), whereas each SW-202 is normally open (NO) when the corresponding digital control input is a zero. The SW-201 and SW-202 are otherwise identical.

The judicious combination of bipolar and FET devices in a single monolithic IC results in a product with performance characteristics and ruggedness that are superior to those of a similar circuit fabricated using CMOS technology.

Increased reliability is complemented by excellent electrical specifications. Potential error sources are reduced by minimizing "ON" resistance and controlling leakage currents at high temperatures. The switching FET exhibits minimal R_{ON} variation over a 20V analog signal range and with power supply voltage changes. Operation from a single positive power supply voltage is possible. With V+ = 36V, V− = 0V, the analog signal range will extend from ground to +32V.

The PNP logic inputs are TTL and CMOS compatible. Logic input currents are at micro-ampere levels which improves circuit fan in.

ORDERING INFORMATION†

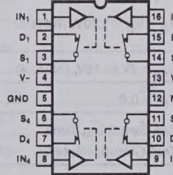
DIP PACKAGE	SWITCH CONFIGURATION NC	NO	OPERATING TEMPERATURE RANGE
16-PIN HERMETIC	SW201BQ*	SW202BQ*	MIL
16-PIN HERMETIC	SW201FQ	SW202FQ	IND
16-PIN EPOXY	SW201GP	SW202GP	COM

*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

PIN CONNECTIONS

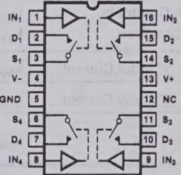
16-PIN DUAL-IN-LINE PACKAGE (Q or P Package)



SW-201

CONTROL LOGIC

LOGIC	SWITCH
0	ON
1	OFF

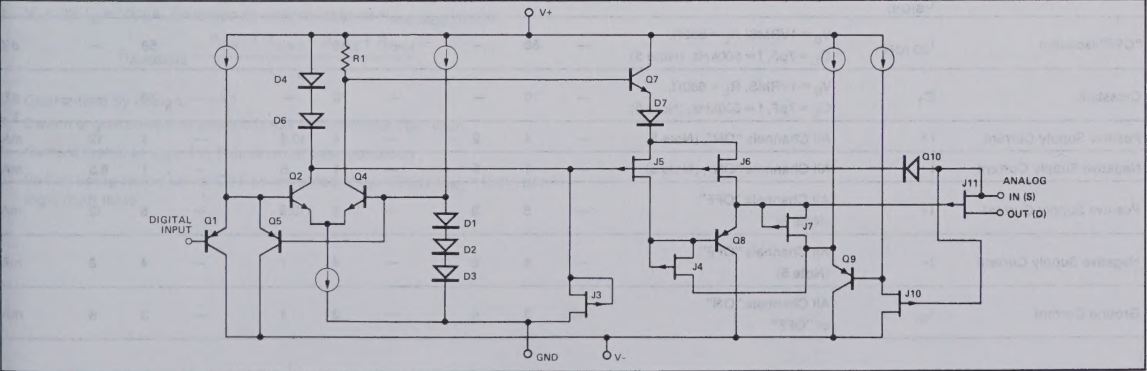


SW-202

CONTROL LOGIC

LOGIC	SWITCH
0	ON
1	OFF

SIMPLIFIED SCHEMATIC DIAGRAM (ONE SWITCH)



Manufactured under the following patent: 4,228, 367

ABSOLUTE MAXIMUM RATINGS (Note 1)

Operating Temperature Range	
SW-201BQ, SW-202BQ	−55°C to +125°C
SW-201FQ, SW-202FQ	−25°C to +85°C
SW-201GP, SW-202GP	0°C to +70°C
DICE Junction Temperature (T_j)	−65°C to +150°C
Storage Temperature Range	−65°C to +150°C
P-Suffix	−65°C to +125°C
Power Dissipation (Note 2)	900mW
Lead Temperature (Soldering, 60 sec)	300°C
Maximum Junction Temperature	150°C
V+ Supply to V− Supply	36V
V+ Supply to Ground	36V
Logic Input Voltage	(−4V or V−) to V+ Supply
Analog Input Voltage Range	
Continuous	V− Supply to V+ Supply +20V
1% Duty Cycle and Driving all 4 Inputs with 500μsec pulse	V− Supply −15V to V+ Supply +20V
Maximum Current Through Any Pin	30mA

NOTES:

1. Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Derated 12mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS at V± = ±15V and T_A = 25°C, unless otherwise noted.

			SW-201B SW-202B			SW-201F SW-202F			SW-201G SW-202G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
"ON" Resistance	R_{ON}	V_A = 0V, I_S = 1mA	—	60	80	—	60	100	—	100	150	Ω
		V_A = ±10V, I_S = 1mA	—	65	80	—	65	100	—	100	150	
R_{ON} Match Between Switches	R_{ON} Match	V_A = 0V, I_D = 100μA; (Note 1)	—	5	15	—	5	20	—	—	20	%
Analog Voltage Range	V_A	I_S = 1.0mA	+10	+11	—	+10	+11	—	+10	+11	—	V
		I_S = 1.0mA	−10	−15	—	−10	−15	—	−10	−15	—	
Analog Current Range	I_A	V_S = ±10V	10	15	—	7	12	—	5	10	—	mA
ΔR_{ON} vs Applied Voltage	ΔR_{ON}	$V_S \leq$ 10V, I_S = 1mA	—	5	15	—	10	20	—	10	20	%
Source Current in "OFF" Condition	$I_{S\,(OFF)}$	V_S = 10V, V_D = −10V, (Note 5)	—	0.3	2.0	—	0.3	2.0	—	—	10	nA
Drain Current in "OFF" Condition	$I_{D\,(OFF)}$	V_S = 10V, V_D = −10V, (Note 5)	—	0.3	2.0	—	0.3	2.0	—	—	10	nA
Leakage Current in "ON" Condition	$I_{S\,(ON)}$ + $I_{D\,(ON)}$	V_S = V_D = ±10V, (Note 5)	—	0.3	2.0	—	0.3	2.0	—	—	10	nA
Logical "1" Input Current	I_{INH}	V_{IN} = 2V to 15V, (Note 4)	—	—	1	—	—	1	—	—	1	μA
Logical "0" Input Current	I_{INL}	V_{IN} = 0.8	—	1.5	5.0	—	1.5	5.0	—	1.5	10.0	μA
Turn-On-Time	t_{ON}	See Switching Time Test Circuit, (Note 2)	—	340	500	—	340	600	—	340	700	ns
Turn-Off-Time	t_{OFF}	See Switching Time Test Circuit, (Note 2)	—	200	400	—	200	400	—	200	500	ns
Break-Before-Make Time	t_{ON}-t_{OFF}	(Notes 2, 3)	50	140	—	50	140	—	50	140	—	ns
Source Capacitance	$C_{S\,(OFF)}$	V_A = 0V, (Note 5)	—	7	—	—	7	—	—	7	—	pF
Drain Capacitance	$C_{D\,(OFF)}$	V_A = 0V, (Note 5)	—	5.5	—	—	5.5	—	—	5.5	—	pF
Channel "ON" Capacitance	$C_{D(ON)}$ + $C_{S(ON)}$	V_S = V_D = 0V, (Note 5)	—	15	—	—	15	—	—	15	—	pF
"OFF" Isolation	$I_{SO\,(OFF)}$	V_S = 1VRMS, R_L = 680Ω, C_L = 7pF, f = 500kHz, (Note 5)	—	58	—	—	58	—	—	58	—	dB
Crosstalk	C_T	V_S = 1VRMS, R_L = 680Ω, C_L = 7pF, f = 500kHz, (Note 5)	—	70	—	—	70	—	—	70	—	dB
Positive Supply Current	I+	All Channels "ON", (Note 5)	—	4	9	—	4	10.5	—	4	12	mA
Negative Supply Current	I−	All Channels "ON", (Note 5)	—	1	5	—	1	6	—	1	6.5	mA
Positive Supply Current	I+	All Channels "OFF", (Note 5)	—	5	9	—	5	10.5	—	6	12	mA
Negative Supply Current	I−	All Channels "OFF", (Note 5)	—	4	6	—	4	7	—	4	8	mA
Ground Current	I_G	All Channels "ON" or "OFF"	—	3	4	—	3	4	—	3	6	mA

ELECTRICAL CHARACTERISTICS at $V\pm = \pm 15V$; $-55°C \le T_A \le +125°C$ for SW-201BQ/202BQ; $-25°C \le T_A \le +85°C$ for SW-201FQ/202FQ; $0°C \le T_A \le 70°C$ for SW-201GP/202GP, unless otherwise noted.

			SW-201B SW-202B			SW-201F SW-202F			SW-201G SW-202G			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Temperature Range	T_A	Operating	−55	—	125	−25	—	85	0	—	70	°C
"ON" Resistance	R_{ON}	$V_A = 0V$, $I_D = 1mA$	—	75	110	—	75	125	—	—	175	Ω
		$V_A = \pm 10V$, $I_D = 1mA$	—	80	110	—	80	125	—	—	175	
R_{ON} Match Between Switches	R_{ON} Match	$V_A = 0V$, $I_D = 100\mu A$; (Note 1)	—	6	20	—	6	25	—	10	—	%
Analog Voltage Range	V_A	$I_S = 1.0mA$	+10	+11	—	+10	+11	—	+10	+11	—	V
		$I_S = 1.0mA$	−10	−15	—	−10	−15	—	−10	−15	—	
Analog Current Range	I_A	$V_S = \pm 10.0V$	7	12	—	5	11	—	—	11	—	mA
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$V_S \le +10V$ $I_S = 1mA$	—	10	—	—	12	—	—	15	—	%
Source Current in "OFF" Condition	$I_{S\,(OFF)}$	$V_S = 10V$, $V_D = -10V$, (Note 5) T_A = Max. Operating Temp.	—	—	60	—	—	30	—	—	60	nA
Drain Current in "OFF" Condition	$I_{D\,(OFF)}$	$V_S = 10V$, $V_D = -10V$, (Note 5) T_A = Max. Operating Temp.	—	—	60	—	—	30	—	—	60	nA
Leakage Current in "ON" Condition	$I_{S\,(ON)} +$ $I_{D\,(ON)}$	$V_S = V_D = \pm 10V$, (Note 5) T_A = Max. Operating Temp.	—	—	100	—	—	30	—	—	60	nA
Logical "1" Input Voltage	V_{INH}		2	—	—	2	—	—	2	—	—	V
Logic "0" Input Voltage	V_{INL}		—	—	0.8	—	—	0.8	—	—	0.8	V
Logical "1" Input Current	I_{INH}	V_{IN} = 2V to 15V, Note 4	—	—	5	—	—	5	—	—	5	μA
Logical "0" Input Current	I_{INL}	$V_{IN} = 0.8$	—	4	10	—	4	10	—	5	15	μA
Turn-On-Time	t_{ON}	See Switching Test Circuit, (Note 2)	—	440	900	—	500	900	—	—	1000	ns
Turn-Off-Time	t_{OFF}	See Switching Test Circuit, (Note 2)	—	300	500	—	330	500	—	—	500	ns
Break-Before-Make Time	t_{ON}-t_{OFF}	(Note 3)	—	70	—	—	70	—	—	50	—	ns
Positive Supply Current	I+	All Channels "ON", (Note 5)	—	—	13.5	—	—	14.0	—	—	15.8	mA
Negative Supply Current	I−	All Channels "ON", (Note 5)	—	—	8.5	—	—	11.0	—	—	14.5	mA
Positive Supply Current	I+	All Channels "OFF", (Note 5)	—	—	13.5	—	—	14.0	—	—	18	mA
Negative Supply Current	I−	All Channels "OFF", (Note 5)	—	—	8.5	—	—	11.0	—	—	14.5	mA
Ground Current	I_G	All Channels "ON" or "OFF"	—	—	6.0	—	—	7.8	—	—	10.0	mA

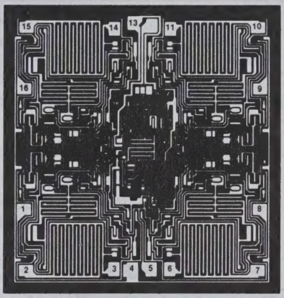
NOTES:

1. $V_A = 0V$, $I_D = 100\mu A$. Specified as a percentage of $R_{AVERAGE}$ where:

$$R_{AVERAGE} = \frac{R_{ON1} + R_{ON2} + R_{ON3} + R_{ON4}}{4}$$

2. Guaranteed by design.
3. Switch is guaranteed to provide break-before-make operation.
4. Current tested at $V_{IN} = 2V$. This is worst case condition.
5. Switch being tested ON or OFF as indicated, $V_{INH} = 2V$ or $V_{INL} = 0.8V$, per logic truth table.

DICE CHARACTERISTICS



DIE SIZE 0.100 × 0.096 inch, 9600 sq. mils
(2.540 × 2.438 mm, 6.193 sq. mm)

1. IN1
2. D1
3. S1
4. V− (SUBSTRATE)
5. GND
6. S2
7. D2
8. IN2
9. IN3
10. D3
11. S3
12. V+
14. S4
15. D4
16. IN4

For additional DICE information refer to Section 2.

WAFER TEST LIMITS at V+ = 15V, V− = −15V, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-201N SW-202N LIMIT	SW-201G SW-202G LIMIT	UNITS
"ON" Resistance	R_{ON}	$-10V \le V_A \le 10V$, $I_S \le 1mA$	80	100	Ω MAX
R_{ON} Mismatch	R_{ON} Match	$V_A = 0V$, $I_S \le 100\mu A$	15	20	% MAX
ΔR_{ON} vs V_A	ΔR_{ON}	$V_S \le 10V$, $I_S = 1mA$	15	20	% MAX
Positive Supply	I+	(Note 1)	9	10.5	mA MAX
Negative Supply Current	I−	(Note 1)	6	7	mA MAX
Ground Current	I_G		4	4	mA MAX
Analog Voltage Range	V_A	$I_S = 1mA$	±10	±10	V MIN
Logic "1" Input Voltage	V_{INH}		2	2	V MIN
Logic "0" Input Voltage	V_{INL}		0.8	0.8	V MAX
Logic "0" Input Current	I_{INL}	$0V \le V_{IN} \le 0.8V$	5	5	μA MAX
Logic "1" Input Current	I_{INH}	$2V \le V_{IN} \le 15V$, (Note 2)	1	1	μA MAX
Analog Current Range	I_A	$V_S = \pm 10V$	10	7	mA MIN

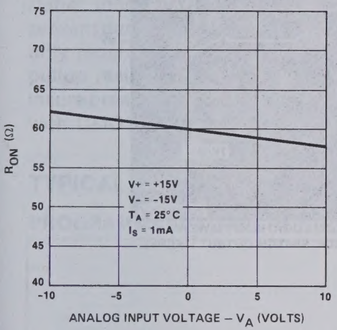
Note: Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS V+ = 15V, V− = −15V and T_A = 25° C, unless otherwise noted.

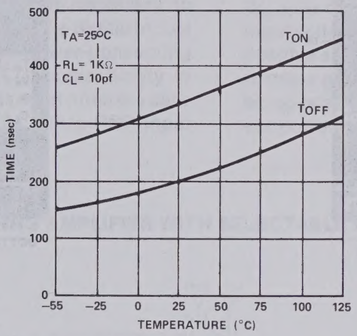
PARAMETER	SYMBOL	CONDITIONS	SW-201N SW-202N TYPICAL	SW-201G SW-202G TYPICAL	UNITS
"ON" Resistance	R_{ON}	$-10V \le V_A \le 10V$, $I_S \le 1mA$	60	60	Ω
Turn-On-Time	t_{ON}		340	340	ns
Turn-Off-Time	t_{OFF}		200	200	ns
Drain Current in "OFF" Condition	$I_{D\,(OFF)}$	$V_S = 10V$, $V_D = -10V$	0.3	0.3	nA
"OFF" Isolation	$I_{SO\,(OFF)}$	f = 500kHz, $R_L = 680\Omega$	58	58	dB
Crosstalk	C_T	f = 500kHz, $R_L = 680\Omega$	70	70	dB

NOTES:
1. Power supply and ground current specified for switch "ON" or "OFF".
2. Current tested at V_{IN} = 2V. This is worst case condition.

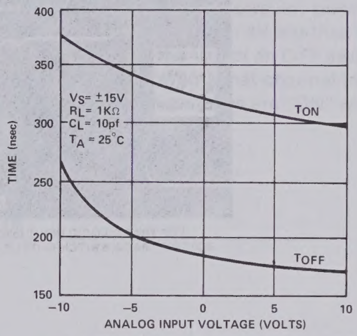
TYPICAL PERFORMANCE CHARACTERISTICS



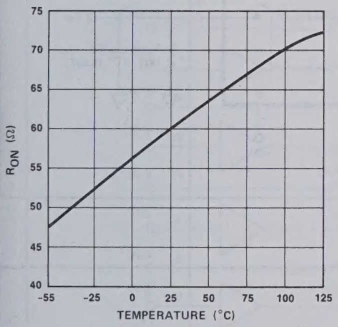
"ON" RESISTANCE vs ANALOG VOLTAGE (V_A)



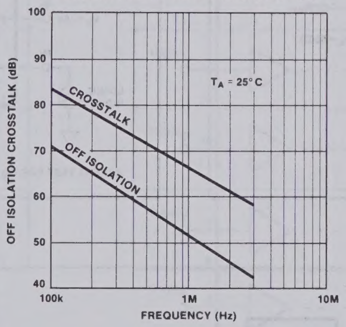
SWITCHING TIME vs TEMPERATURE



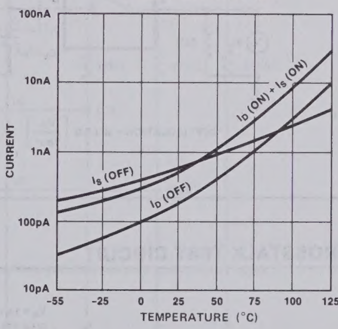
SWITCHING TIME vs ANALOG VOLTAGE



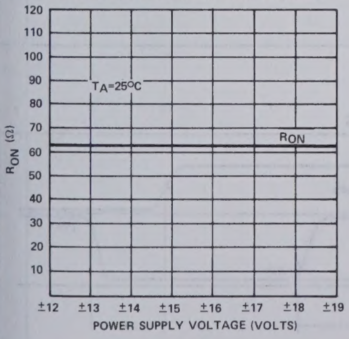
R_{ON} vs TEMPERATURE



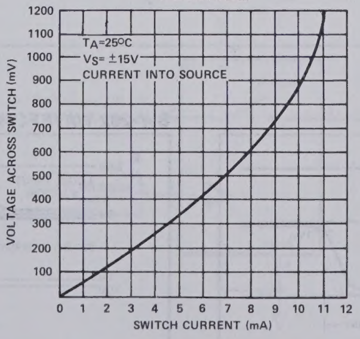
CROSSTALK AND "OFF" ISOLATION vs FREQUENCY



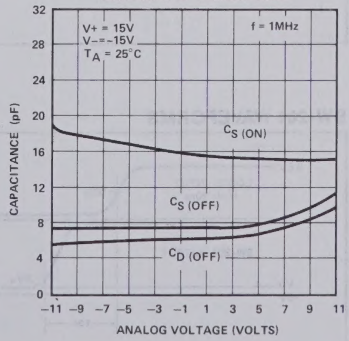
LEAKAGE CURRENT vs TEMPERATURE



"ON" RESISTANCE vs POWER SUPPLY VOLTAGE



SWITCH CURRENT vs VOLTAGE

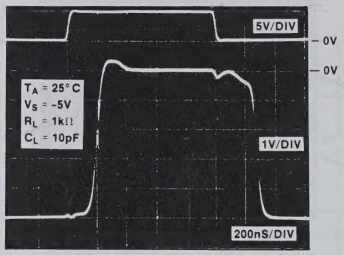


SWITCH CAPACITANCE vs ANALOG VOLTAGE

TYPICAL PERFORMANCE CHARACTERISTICS

SW-201

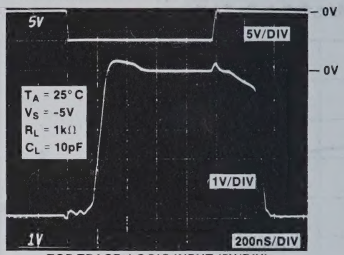
t_{ON}/t_{OFF} SWITCHING RESPONSE



TOP TRACE: LOGIC INPUT (5V/DIV)
BOTTOM TRACE: SWITCH OUTPUT (1V/DIV)

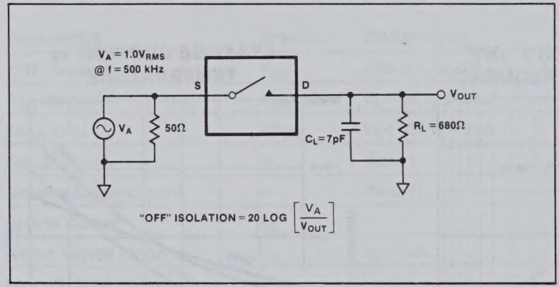
SW-202

t_{ON}/t_{OFF} SWITCHING RESPONSE

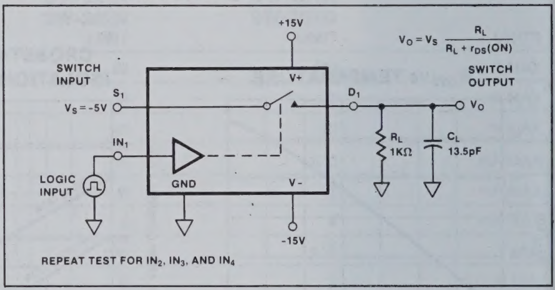


TOP TRACE: LOGIC INPUT (5V/DIV)
BOTTOM TRACE: SWITCH OUTPUT (1V/DIV)

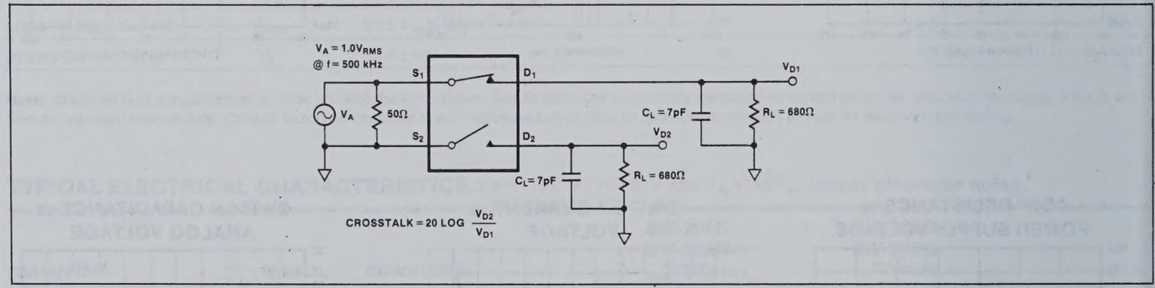
OFF ISOLATION TEST CIRCUIT


$V_A = 1.0V_{RMS}$
@ f = 500 kHz
S
D
V_{OUT}
V_A
50Ω
$C_L = 7pF$
$R_L = 680\Omega$
"OFF" ISOLATION = 20 LOG $\left[\frac{V_A}{V_{OUT}}\right]$

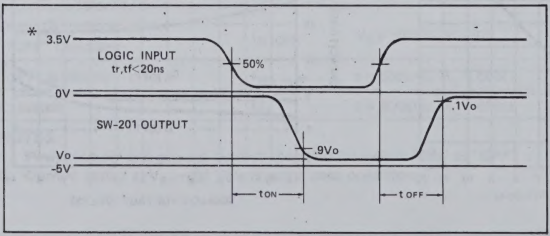
SWITCHING TIME TEST CIRCUIT


+15V
$V_O = V_S \frac{R_L}{R_L + r_{DS}(ON)}$
SWITCH INPUT
V+
SWITCH OUTPUT
S_1
D_1
$V_S = -5V$
V_O
IN_1
R_L 1KΩ
C_L 13.5pF
LOGIC INPUT
GND
V-
-15V
REPEAT TEST FOR IN_2, IN_3, AND IN_4

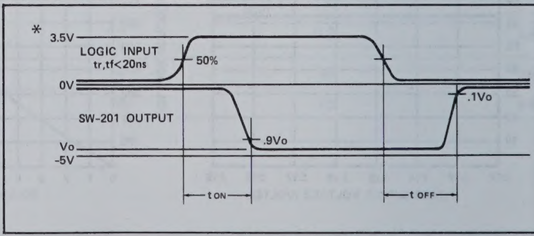
CROSSTALK TEST CIRCUIT


$V_A = 1.0V_{RMS}$
@ f = 500 kHz
S_1
D_1
V_{D1}
V_A
50Ω
$C_L = 7pF$
$R_L = 680\Omega$
S_2
D_2
V_{D2}
$C_L = 7pF$
$R_L = 680\Omega$
CROSSTALK = 20 LOG $\frac{V_{D2}}{V_{D1}}$

SW-201 WAVEFORMS


*
3.5V
LOGIC INPUT
tr,tf<20ns
50%
0V
.1Vo
SW-201 OUTPUT
.9Vo
Vo
-5V
t ON
t OFF

SW-202 WAVEFORMS


*
3.5V
LOGIC INPUT
tr,tf<20ns
50%
0V
.1Vo
SW-201 OUTPUT
.9Vo
Vo
-5V
t ON
t OFF

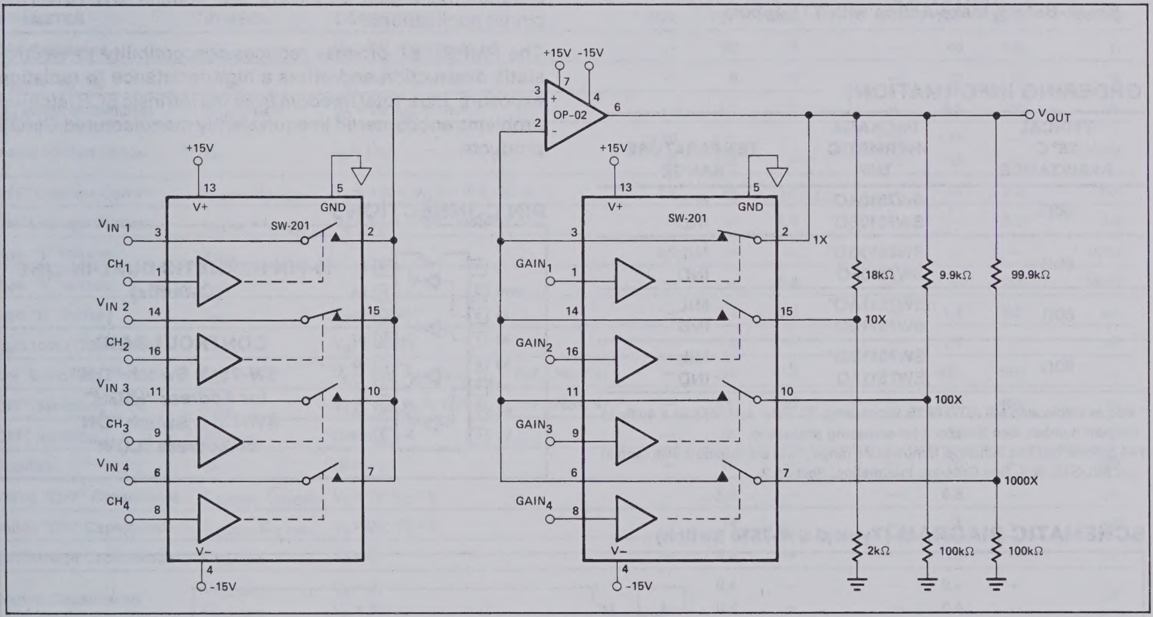
APPLICATIONS INFORMATION

This analog switch employs ion-implanted JFETs in a switch configuration designed to assure break-before-make action. The turn-off time is much faster than the turn-on time to guarantee this feature over the full operating temperature and input voltage range. Fabricated with BIFET processing rather than CMOS, special handling is not necessary to prevent damage to these switches. Because the digital inputs only require a 2V logic "1" input level, power-consuming pullup resistors are not required for TTL compatibility to insure break-before-make switching as is most often the case with CMOS switches. The digital inputs utilize PNP input transistors where input current is maximum at the logic "0" level and drops to that of a reverse-biased diode as the input voltage is raised above ≈ 1.4V.

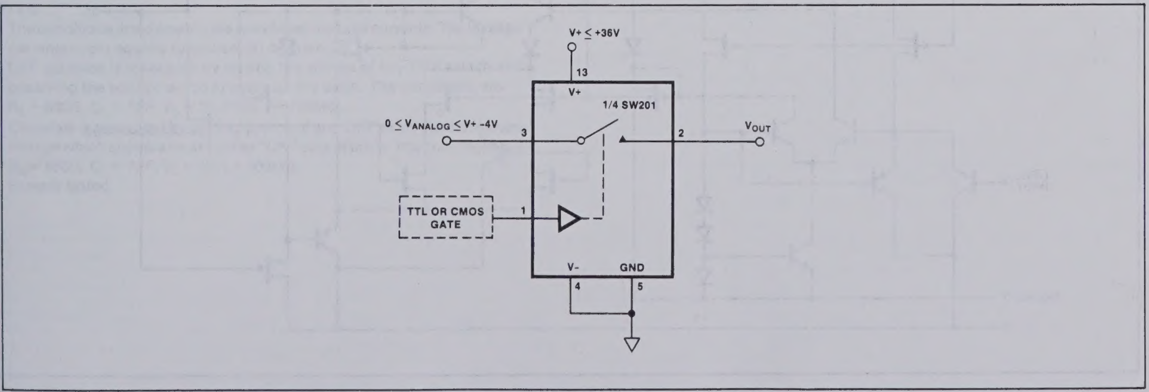
The "ON" resistance, R_{ON}, of the analog switches is constant over the wide input voltage range of −15V to +11V with $V_{SUPPLY} = \pm 15V$. For normal operation, however, positive input voltages should be restricted to 11V (or 4V less than the positive supply). This assures that the V_{GS} of an OFF switch remains greater than its V_P, and prevents that channel from being falsely turned ON. Individual switches are "ON" without power applied.

TYPICAL APPLICATIONS

PROGRAMMABLE GAIN NONINVERTING AMPLIFIER WITH SELECTABLE INPUTS


+15V
-15V
OP-02
+
−
3
2
7
4
6
VOUT
+15V
13
5
V+
GND
SW-201
VIN 1
3
2
CH1
1
VIN 2
14
15
CH2
16
VIN 3
11
10
CH3
9
VIN 4
6
7
CH4
8
V−
4
-15V
+15V
13
5
V+
GND
SW-201
3
2
1X
GAIN1
1
14
15
10X
GAIN2
16
11
10
100X
GAIN3
9
6
7
1000X
GAIN4
8
V−
4
-15V
18kΩ
9.9kΩ
99.9kΩ
2kΩ
100kΩ
100kΩ

OPERATION FROM SINGLE POSITIVE POWER SUPPLY


V+ ≤ +36V
13
V+
1/4 SW201
0 ≤ VANALOG ≤ V+ -4V
3
2
VOUT
TTL OR CMOS GATE
1
V-
GND
4
5

SW-7510/SW-7511

QUAD SPST BIFET ANALOG SWITCHES

FEATURES

- **Pin Compatible with AD7510 DI, AD7511 DI**
- **JFET Switches Rather than CMOS**
- **Highly Resistant to Static Discharge Damage**
- **Radiation Resistant**
- **No SCR Latch-up Problems**
- **Low "ON" Resistance — 75Ω Max**
- **Superior "OFF" Isolation and Crosstalk**
- **Digital Inputs Compatible with TTL and CMOS**
- **No Pull-Up Resistors Required to Insure Break-Before-Make Action with TTL Inputs**

ORDERING INFORMATION†

TYPICAL 25° C RESISTANCE	PACKAGE HERMETIC DIP	TEMPERATURE RANGE
60Ω	SW7510AQ* SW7510EQ	MIL IND
80Ω	SW7510BQ* SW7510FQ	MIL IND
60Ω	SW7511AQ* SW7511EQ	MIL IND
80Ω	SW7511BQ* SW7511FQ	MIL IND

*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

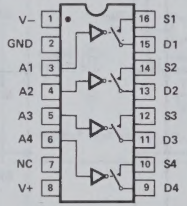
GENERAL DESCRIPTION

The SW-7510/7511 are monolithic linear devices, each containing four independently selectable SPST analog switches. The SW-7510 operates normally-open with logic-low inputs. The SW-7511 operates normally-closed with logic-low inputs. All logic inputs are fully TTL input compatible.

Performance advantages include exceptionally high "OFF" isolation, low leakage current and low crosstalk. Data conversion, position controllers, choppers, demodulators and programmable-gain amplifiers are popular SW-7510/7511 circuit applications.

The PMI BIFET process reduces susceptibility to electrostatic destruction and offers a high resistance to radiation exposure. Plus, total freedom from the intrinsic SCR latch-up problems encountered in equivalently manufactured CMOS products.

PIN CONNECTIONS



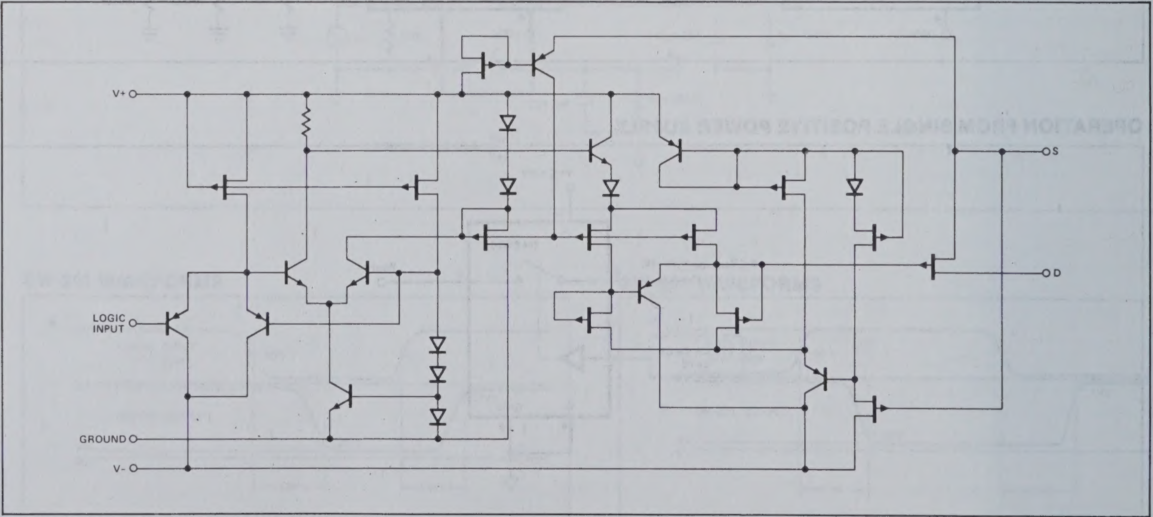
16-PIN HERMETIC DUAL-IN-LINE (Q-Suffix)

CONTROL LOGIC:

SW-7510: Switch "ON" for Address "HIGH"

SW-7511: Switch "ON" for Address "LOW"

SCHEMATIC DIAGRAM (Typical SW-7510 Switch)



ABSOLUTE MAXIMUM RATINGS ($T_A = 25°C$, unless otherwise noted).

Operating Temperature Range,
SW-7510/7511AQ, BQ .... −55°C to +125°C
SW-7510/7511EQ, FQ .... −25°C to +85°C
DICE Junction Temperature (T_j) .... −65°C to +150°C
Storage Temperature Range .... −65°C to +150°C
Power Dissipation 500mW
Derate above 100°C .... 10mW/°C
Lead Temperature (Soldering, 60 sec) .... 300°c
Maximum Junction Temperature .... 150°C
V+ Supply to V− Supply 36V
V+ Supply to Ground 36V
Logic Input Voltage .... (−2V or V−) to V+ Supply
Analog Input Voltage
Continuous .... V− Supply to V+ Supply +20V
1% Duty Cycle and Driving
all 4 Inputs with
500μs pulse .... V− Supply −15V to V+ Supply +20V
Maximum Current Through Any Pin 25mA

NOTE: Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ and $T_A = +25°C$, unless otherwise noted.

			SW-7510A/E SW-7511A/E			SW-7510B/F SW-7511B/F			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
"ON" Resistance	R_{ON}	$V_D = 0V$, $I_{DS} = 1mA$	—	60	75	—	80	100	Ω
ΔR_{ON} vs. V_D (V_S)	ΔR_{ON}	$V_D \leq 10V$, $I_D = 1mA$	—	6	10	—	10	10	%
R_{ON} Match of Switches	R_{ON} Match	$V_D = 0V$, $I_{DS} = 1mA$	—	1.5	10	—	1.5	10	%
Analog Voltage Range	V_A	$I_S = 1mA$	+10 −10	+11 −15	— —	+10 −10	+11 −15	— —	Volts
"OFF" Leakage Current	$I_{S(OFF)}$, $I_{D(OFF)}$	$V_S = +10V$, $V_D = -10V$, (Note 1)	—	—	1.0	—	—	3.0	nA
"ON" Leakage Current	$I_{S(ON)} + I_{D(ON)}$	$V_S = V_D = +10V$, (Note 1)	—	—	1.0	—	—	3.0	nA
Logic "1" Voltage	V_{INH}		2.0	—	—	2.0	—	—	Volts
Logic "0" Voltage	V_{INL}		—	—	0.8	—	—	0.8	Volts
Logic "0" Current	I_{INL}	$V_{IN} = +0.4V$	—	1.5	3.5	—	1.5	3.5	μA
Logic Input Capacitance	C_{DIG}	$V_{IN} = +0.4V$	—	1.5	—	—	1.5	—	pF
"ON" Switching Time	t_{ON}	$V_S = -5V$, $R_L = 1k\Omega$, $C_L = 7pF$, (Note 4)	—	350	450	—	450	550	ns
"OFF" Switching Time	t_{OFF}	$V_S = -5V$, $R_L = 1k\Omega$, $C_L = 7pF$, (Note 4)	—	260	300	—	350	450	ns
"OFF" Isolation	ISO_{OFF}	(Note 2)	—	66	—	—	66	—	dB
Crosstalk	C_T	(Note 3)	—	70	—	—	70	—	dB
Analog "OFF" Capacitance	$C_{S(OFF)}$, $C_{D(OFF)}$	$V_S =$)V, $V_D = 0$	—	6.5	—	—	6.5	—	pF
Analog "ON" Capacitance	$C_{S(ON)}$, $C_{D(ON)}$	$V_S = 0V$, $V_D = 0$	—	14	—	—	14	—	pF
Feedthrough Capacitance	$C_{DS(OFF)}$	$V_S = 0V$	—	0.8	—	—	0.8	—	pF
Channel Capacitance	$C_{SS(OFF)}$, $C_{DD(OFF)}$	$V_S = 0V$ $V_S = 0V$	— —	0.4 0.4	— —	— —	0.4 0.4	— —	pF
Positive Supply Current	I+	Logic Inputs at "0" or "1"	—	5.0	9.0	—	3.0	9.0	mA
Negative Supply Current	I−	Logic Inputs at "0" or "1"	—	2.8	5.0	—	1.7	5.0	mA

NOTES:

1. The conditions listed specify the worst case leakage currents. The leakage currents apply equally to source (S) or drain(D).
2. OFF isolation is measured by driving the source of any OFF switch and observing the voltage which appears on the drain. The conditions are: $R_L = 680\Omega$, $C_L = 7pF$, $V_S = 1V$, RMS, f = 100kHz.
3. Crosstalk is measured by driving source of any OFF switch and observing voltage which appears on any other "ON" output drain. The conditions are: $R_L = 680\Omega$, $C_L = 7pF$, $V_S = 1V$, f = 100kHz.
4. Sample tested.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$ for SW-7510AQ, BQ and SW-7511AQ, BQ; and $-25°C \leq T_A \leq +85°C$ for SW-7510EQ, FQ and SW-7511EQ, FQ, unless otherwise noted.

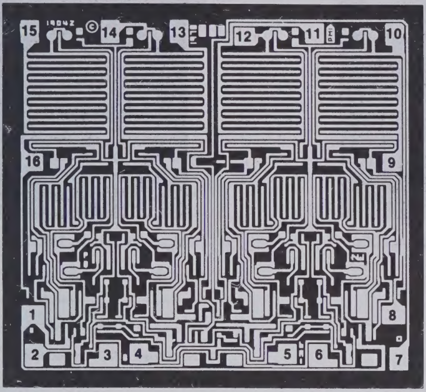
			SW-7510A/E SW-7511A/E			SW-7510B/F SW-7511B/F			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
"ON" Resistance	R_{ON}	$V_D = 0V$, $I_{DS} = 1mA$	—	—	100	—	—	150	Ω
ΔR_{ON} vs. Temperature	ΔR_{ON} Drift	$V_D = 0V$, $I_{DS} = 1mA$	—	0.4	—	—	0.5	—	%/°C
Analog Voltage Range	V_A	$I_S = 1mA$	+10 −10	+11 −15	— —	+10 −10	+11 −15	— —	Volts
"OFF" Leakage Current	$I_{S(OFF)}$, $I_{D(OFF)}$	$V_S = +10V$, $V_D = -10V$, (Note 1)	—	—	90	—	—	100	nA
"ON" Leakage Current	$I_{S(ON)} + I_{D(ON)}$	$V_S = V_D = +10V$, (Note 1)	—	—	90	—	—	100	nA
Logic "1" Voltage	V_{INH}		2.0	—	—	2.0	—	—	Volts
Logic "0" Voltage	V_{INL}		—	—	0.8	—	—	0.8	Volts
Logic "0" Current	I_{INL}	$V_{IN} = +0.4V$	—	—	5.0	—	—	7.0	μA
"ON" Switching Time	t_{ON}	$V_S = -5V$, $R_L = 1k\Omega$, $C_L = 7pF$ (Note 2)	—	—	600	—	—	1000	ns
"OFF" Switching Time	t_{OFF}	$V_S = -5V$, $R_L = 1k\Omega$, $C_L = 7pF$ (Note 2)	—	—	500	—	—	750	ns
Positive Supply Current	I+	Logic Inputs at "0" or "1"	—	—	13	—	—	13	mA
Negative Supply Current	I−	Logic Inputs at "0" or "1"	—	—	7.5	—	—	7.5	mA

NOTES:

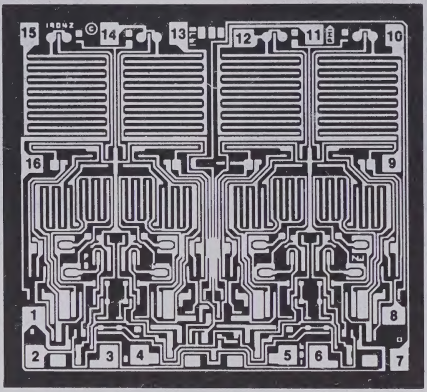
1. The conditions listed specify the worst case leakage currents. The leakage currents apply equally to source (S) or drain(D).
2. Guaranteed by design.

DICE CHARACTERISTICS

SW-7510 (SWITCH ON FOR ADDRESS HIGH)



SW-7511 (SWITCH ON FOR ADDRESS LOW)



DIE SIZE 0.091 × 0.083 inch, 7553 sq. mils
(2.311 × 2.108 mm, 1.918 sq. mm)

1. NEGATIVE SUPPLY (SUBSTRATE)
2. GROUND
3. ADDRESS (A1)
4. ADDRESS (A2)
5. ADDRESS (A3)
6. ADDRESS (A4)
7. DISABLE (NO CONNECT)
8. POSITIVE SUPPLY
9. DRAIN (D4)
10. SOURCE (S4)
11. DRAIN (D3)
12. SOURCE (S3)
13. DRAIN (D2)
14. SOURCE (S2)
15. DRAIN (D1)
16. SOURCE (S1)

---

1. NEGATIVE SUPPLY (SUBSTRATE)
2. GROUND
3. ADDRESS (A1)
4. ADDRESS (A2)
5. ADDRESS (A3)
6. ADDRESS (A4)
7. DISABLE (NO CONNECT)
8. POSITIVE SUPPLY
9. DRAIN (D4)
10. SOURCE (S4)
11. DRAIN (D3)
12. SOURCE (S3)
13. DRAIN (D2)
14. SOURCE (S2)
15. DRAIN (D1)
16. SOURCE (S1)

For additional DICE information refer to Section 2.

WAFER TEST LIMITS at V+ = +15V, V− = −15V, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-7510N/ SW-7511N LIMIT	SW-7510G/ SW-7511G LIMIT	UNITS
"ON" Resistance	R_{ON}	$V_D = 0V$, $I_{DS} = 1mA$	75	100	Ω MAX
Logic "1" Voltage	V_{INH}		2.0	2.0	V MIN
Logic "0" Voltage	V_{INL}		0.8	0.8	V MAX
Logic "0" Current	I_{INL}	$V_{IN} = +0.4V$	3.5	3.5	μA MAX
Positive Supply Current	I+	Logic Inputs at "0"	9	9	mA MAX
Negative Supply Current	I−	Logic Inputs at "0"	5	5	mA MAX

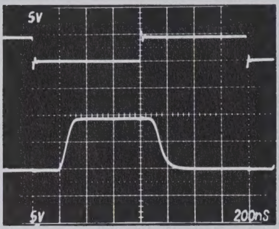
Note: Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at V+ = +15V, V− = −15V and $T_A = 25°C$, unless otherwise noted..

PARAMETER	SYMBOL	CONDITIONS	SW-7510N/ SW-7511N TYPICAL	SW-7510G/ SW-7511G TYPICAL	UNITS
"ON" Resistance	R_{ON}	$V_D = 0V$, $I_{DS} = 1mA$	60	80	Ω
R_{ON} vs. Temperature	R_{ON} Drift	$V_D = 0V$, $I_{DS} = 1mA$	0.4	0.5	%/°C
"ON" Switching Time	t_{ON}	$V_S = -5V$, $R_L = 1kΩ$, $C_L = 7pF$	350	450	ns
"OFF" Switching Time	t_{OFF}	$V_S = -5V$, $R_L = 1kΩ$, $C_L = 7pF$	260	350	ns

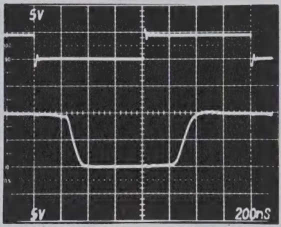
TYPICAL PERFORMANCE CHARACTERISTICS (Apply to all models, unless otherwise noted)

LARGE-SIGNAL SWITCHING



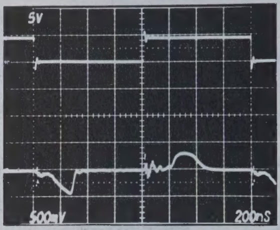
$V_A = +10V$, $R_L = 1k\Omega$, $C_L = 13pF$

LARGE-SIGNAL SWITCHING



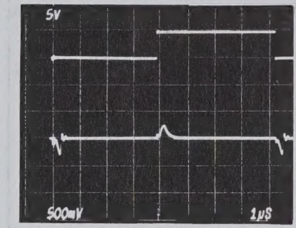
$V_A = -10V$, $R_L = 1k\Omega$, $C_L = 100pF$

SMALL-SIGNAL SWITCHING



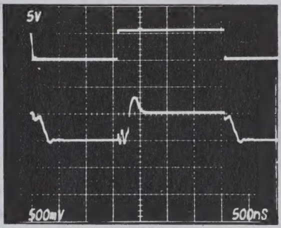
$V_A = 0V$, $R_L = 1k\Omega$, $C_L = 13pF$

SMALL-SIGNAL SWITCHING WITH FILTERING



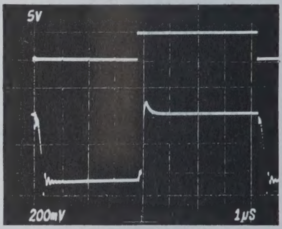
$V_A = 0V$, $R_L = 1k\Omega$, $C_L = 100pF$

SMALL-SIGNAL SWITCHING



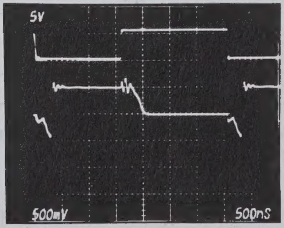
$V_A = -500mV$, $R_L = 1k\Omega$, $C_L = 13pF$

SMALL-SIGNAL SWITCHING WITH FILTERING



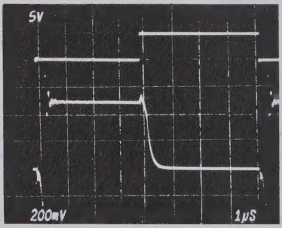
$V_A = -500mV$, $R_L = 1k\Omega$, $C_L = 100pF$

SMALL-SIGNAL SWITCHING



$V_A = 500mV$, $R_L = 1k\Omega$, $C_L = 13pF$

SMALL-SIGNAL SWITCHING WITH FILTERING

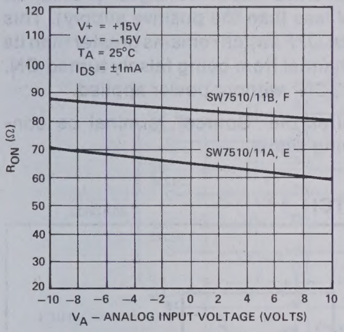


$V_A = 500mV$, $R_L = 1k\Omega$, $C_L = 100pF$

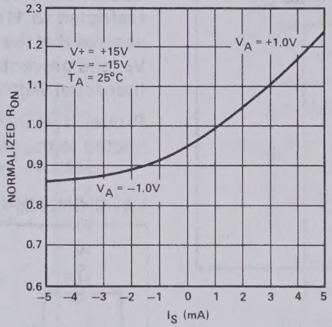
NOTE:
Upper Photo Traces: Logic Control Signal A_X
Lower Photo Traces: Switch Outputs V_D

CHARACTERISTIC CURVES (Apply to all models, unless otherwise noted)

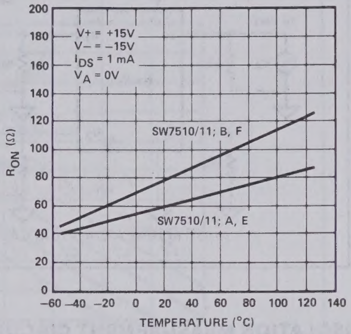
"ON" RESISTANCE (R_{ON}) vs ANALOG VOLTAGE (V_A)



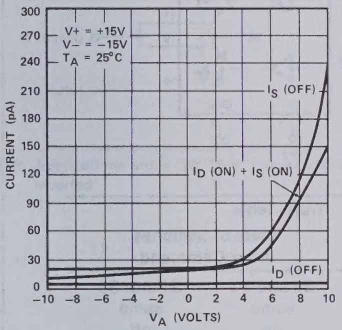
NORMALIZED R_{ON} vs SWITCH CURRENT (I_S)



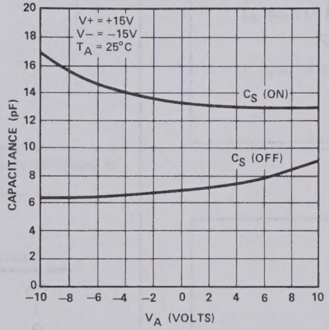
R_{ON} vs TEMPERATURE



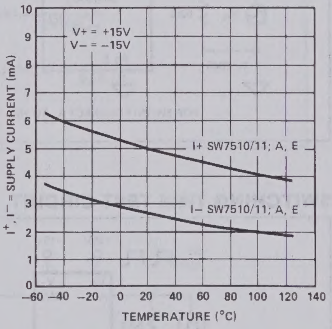
SWITCH LEAKAGE CURRENTS vs ANALOG INPUT VOLTAGE



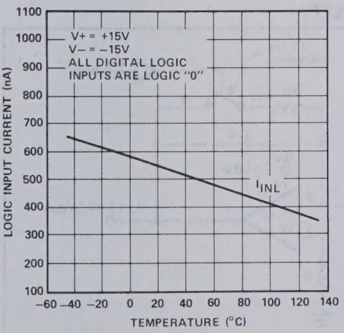
SWITCH CAPACITANCES vs ANALOG VOLTAGE (V_A)



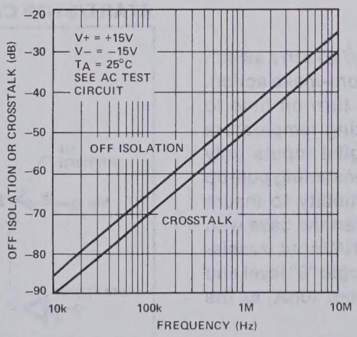
SUPPLY CURRENTS vs TEMPERATURE



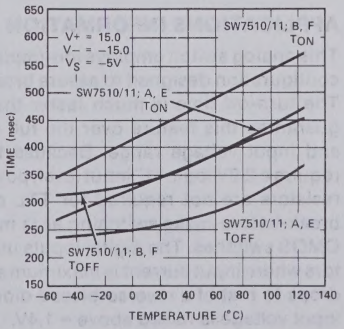
DIGITAL INPUT CURRENT I_{INL} vs TEMPERATURE



CROSSTALK AND "OFF" ISOLATION vs FREQUENCY

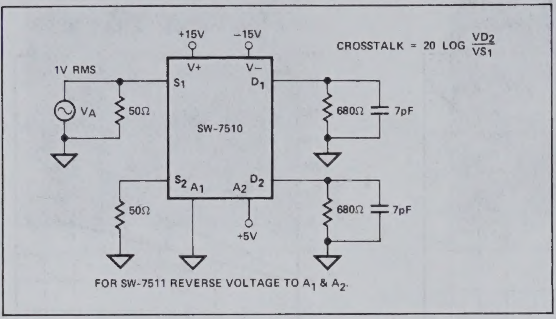


SWITCHING TIMES vs TEMPERATURE

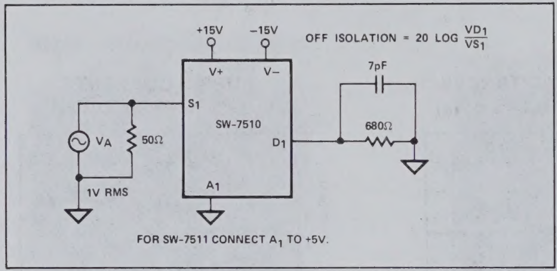


AC TEST CIRCUITS

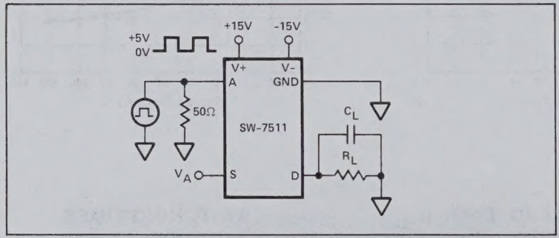
CROSSTALK MEASUREMENT CIRCUIT


+15V
−15V
CROSSTALK = 20 LOG $\frac{VD_2}{VS_1}$
1V RMS
V+
V−
S_1
D_1
V_A
50Ω
680Ω
7pF
SW-7510
S_2
A_1
A_2
D_2
50Ω
680Ω
7pF
+5V
FOR SW-7511 REVERSE VOLTAGE TO A_1 & A_2.

ISOLATION MEASUREMENT CIRCUIT


+15V
−15V
OFF ISOLATION = 20 LOG $\frac{VD_1}{VS_1}$
7pF
V+
V−
S_1
SW-7510
680Ω
V_A
50Ω
D_1
1V RMS
A_1
FOR SW-7511 CONNECT A_1 TO +5V.

SWITCHING TIME TEST CIRCUIT


+5V
0V
+15V
−15V
V+
V−
A
GND
50Ω
SW-7511
C_L
R_L
V_A
S
D

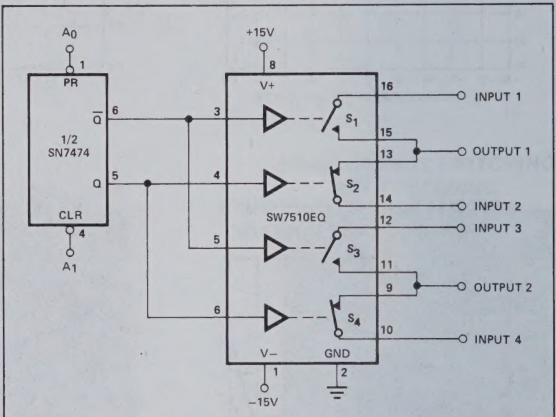
APPLICATIONS INFORMATION

This analog switch employs ion-implanted JFETs in a switch configuration designed to assure break-before-make action. The turn-off time is much faster than the turn-on time to guarantee this feature over the full operating temperature and input voltage range. Because the digital inputs only require a 2.0V logic "1" input level, power-consuming pull-up resistors are not required for TTL compatibility to insure break-before-make switching as is most often the case with CMOS switches. The digital inputs utilize PNP input transistors where input current is maximum at the logic "0" level and drops to that of a reverse-biased diode (about 10nA) as the input voltage is raised above ≈ 1.4V.

The "ON" resistance, R_{ON}, of the analog switches is constant over the wide input voltage range of −15V to +11V with $V_{SUPPLY} = \pm 15V$. Higher input voltage is tolerable provided that some form of current limiting is employed (such as that of an op-amp output stage) to avoid exceeding junction temperature and power dissipation requirements. For normal operation, however, positive input voltages should be restricted to 11V (or 4V less than the positive supply). This assures that the V_{GS} of an OFF switch remains greater than its V_P, and prevents that channel from being falsely turned ON. Individual switches are "ON" without power applied.

Proper switching requires the "Source" terminal be connected to the input driving signal.

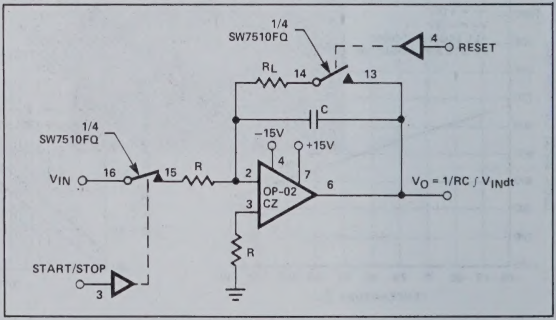
LATCHING DPDT SWITCH


A_0
1
PR
+15V
8
V+
16
INPUT 1
$\overline{Q}$
6
3
S_1
15
13
OUTPUT 1
1/2
SN7474
Q
5
4
S_2
14
INPUT 2
CLR
4
SW7510EQ
12
INPUT 3
A_1
5
S_3
11
9
OUTPUT 2
6
S_4
10
INPUT 4
V−
GND
1
2
−15V

Truth Table

Command		State of Switches After Command	
A_0	A_1	S2 and S3	S1 and S3
1	1	same	same
0	1	on	off
1	0	off	on
0	0	INDETERMINATE	

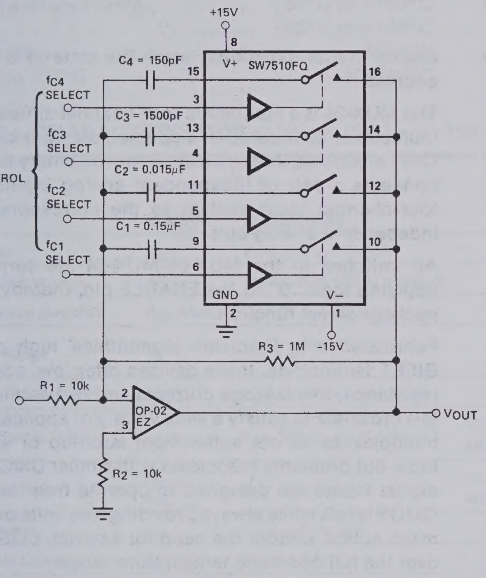
INTEGRATOR WITH ANALOG RESET AND START/STOP CAPABILITY

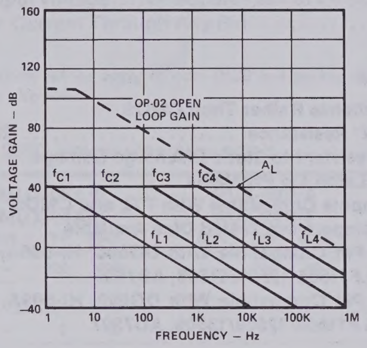

1/4
SW7510FQ
4
RESET
R_L
14
13
C
1/4
SW7510FQ
−15V
+15V
V_{IN}
16
15
R
2
4
7
OP-02
CZ
6
$V_O = 1/RC \int V_{IN}dt$
3
R
START/STOP
3

NOTE: Applications show SW-7510. For SW-7511 applications the logic is inverted.

TYPICAL APPLICATIONS

ACTIVE LOW-PASS FILTER WITH DIGITALLY SELECTED BREAK FREQUENCY


+15V
8
V+
SW7510FQ
C4 = 150pF
15
16
fC4 SELECT
3
C3 = 1500pF
13
14
fC3 SELECT
4
TTL CONTROL
C2 = 0.015μF
11
12
fC2 SELECT
5
C1 = 0.15μF
9
10
fC1 SELECT
6
GND
V−
2
1
R3 = 1M
−15V
R1 = 10k
2
OP-02 EZ
3
VOUT
R2 = 10k



A_L (VOLTAGE GAIN BELOW BREAK FREQUENCY) =

$$\frac{R_3}{R_1} = 100\ (40\text{dB})$$

$$f_C\ (\text{BREAK FREQUENCY}) = \frac{1}{2\pi R_3 C_X}$$

$$f_L\ (\text{UNITY GAIN FREQUENCY}) = \frac{1}{2\pi R_1 C_X}$$

NOTE: Applications show SW-7510. For SW-7511 applications the logic is inverted.

MUX-08/MUX-24 8-CHANNEL/DUAL 4-CHANNEL BIFET ANALOG MULTIPLEXERS

(OVERVOLTAGE AND POWER SUPPLY LOSS PROTECTED)

FEATURES

- **JFET Switches Rather Than CMOS**
- **Low "ON" Resistance .... 220Ω Typ**
- **Highly Resistant to Static Discharge Damage**
- **No SCR Latch-Up Problems**
- **Digital Inputs Compatible With TTL and CMOS**
- **125° C Temperature Tested Dice Available**
- **MUX-08 Pin Compatible With DG508, HI-508A, IH5108, IH6108, LF11508/12508/13508, AD7506**
- **MUX-24 Pin Compatible With DG509, HI-509A, IH5208, IH6208, LF11509/12509/13509, AD7507**

GENERAL DESCRIPTION

The MUX-08 is a monolithic eight-channel analog multiplexer which connects a single output to one of the eight analog inputs depending upon the state of a 3-bit binary address.

The MUX-24 is a monolithic four-channel differential analog multiplexer configured in a double pole, four-position (plus OFF) electronic switch array. A two-bit binary input address connects a pair of independent analog inputs from each four-channel input section to the corresponding pair of independent analog outputs.

All switches in the MUX-08/MUX-24 are turned OFF by applying logic "0" to the ENABLE pin, thereby providing a package select function.

Fabricated with Precision Monolithics' high performance BIFET technology, these devices offer low, constant "ON" resistance, low leakage currents and fast settling time with low crosstalk to satisfy a wide variety of applications. These multiplexers do not suffer from latch-up or static charge blow-out problems associated with similar CMOS parts. The digital inputs are designed to operate from both TTL and CMOS levels while always providing a definite break-before-make action without the need for external pull-up resistors over the full operating temperature range.

For single sixteen-channel and dual eight-channel models, refer to the MUX-16/MUX-28 data sheet.

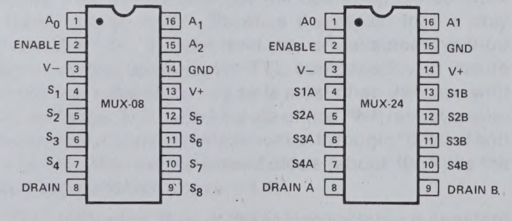
ORDERING INFORMATION†

25° C ON RESISTANCE	PACKAGE HERMETIC DIP	 PLASTIC DIP	TEMPERATURE RANGE
220Ω	MUX08AQ*	—	MIL
	MUX08EQ	—	IND
	—	MUX08EP	COM
300Ω	MUX08BQ*	—	MIN
	MUX08FQ	—	IND
	—	MUX08FP	COM
220Ω	MUX24AQ*	—	MIL
	MUX24EQ	—	IND
	—	MUX24EP	COM
300Ω	MUX24BQ*	—	MIL
	MUX24FQ	—	IND
	—	MUX24FP	COM

*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

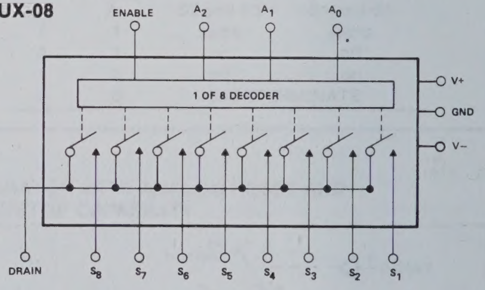
PIN CONNECTIONS


A_0 1
ENABLE 2
V− 3
S_1 4
S_2 5
S_3 6
S_4 7
DRAIN 8
16 A_1
15 A_2
14 GND
13 V+
12 S_5
11 S_6
10 S_7
9 S_8
MUX-08
A0 1
ENABLE 2
V− 3
S1A 4
S2A 5
S3A 6
S4A 7
DRAIN A 8
16 A1
15 GND
14 V+
13 S1B
12 S2B
11 S3B
10 S4B
9 DRAIN B
MUX-24

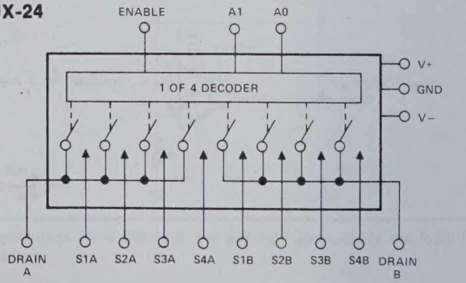
16-PIN DUAL-IN-LINE PACKAGE
(Q or P Package)

FUNCTIONAL DIAGRAMS

MUX-08


ENABLE
A_2
A_1
A_0
1 OF 8 DECODER
V+
GND
V−
DRAIN
S_8
S_7
S_6
S_5
S_4
S_3
S_2
S_1

MUX-24


ENABLE
A1
A0
1 OF 4 DECODER
V+
GND
V−
DRAIN A
S1A
S2A
S3A
S4A
S1B
S2B
S3B
S4B
DRAIN B

ABSOLUTE MAXIMUM RATINGS (Note)

Operating Temperature Range	
MUX-08/24-AQ, BQ	−55° C to +125° C
MUX-08/24-EQ, FQ	−25° C to +85° C
MUX-08/24-EP, FP	0° C to +70° C
DICE Junction Temperature (T_j)	−65° C to +150° C
Storage Temperature Range	−65° C to +150° C
P-Suffix	−65° C to +125° C
Power Dissipation	500mW
Derate above 100° C	10mW/° C
Lead Temperature (Soldering, 60 sec)	300° C
Maximum Junction Temperature	150° C
V+ Supply to V− Supply	36V
Logic Input Voltage	(−4V or V−) to V+ Supply
Analog Input Voltage	V− Supply −20V to V+ Supply +20V
Maximum Current Through Any Pin	25mA

NOTE: Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at V+ = +15V, V− = −15V and T_A = 25° C, unless otherwise noted.

				MUX-08A/E MUX-24A/E			MUX-08B/F MUX-24B/F			
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	MIN	TYP	MAX	UNITS
"ON" Resistance	R_{ON}	$V_D \leq 10V$, $I_D \leq 200\mu A$		—	220	300	—	300	400	Ω
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$-10V \leq V_D \leq 10V$, $I_S = 200\mu A$		—	1	5	—	3	7	%
R_{ON} Match Between Switches	R_{ON} Match	$V_D = 0V$, $I_S = 200\mu A$		—	7	15	—	9	20	%
Analog Voltage Range	V_A	(Note 6)		+10	+10.4	—	+10	+10.4	—	Volts
				−10	−15	—	−10	−15	—	
Source Current (Switch "OFF")	$I_{S\,(OFF)}$	$V_S = 10V$, $V_D = -10V$ (Note 1)		—	0.01	1.0	—	0.01	2.0	nA
Drain Current (Switch "OFF")	$I_{D\,(OFF)}$	$V_S = 10V$, $V_D = -10V$ (Note 1)	MUX-08	—	0.1	1.0	—	0.1	2.0	nA
			MUX-24	—	0.05	1.0	—	0.05	2.0	
Leakage Current (Switch "ON")	$I_{D\,(ON)}$ $+I_{S\,(ON)}$	$V_D = 10V$ (Note 1)	MUX-08	—	0.1	1.0	—	0.1	2.0	nA
			MUX-24	—	0.05	1.0	—	0.05	2.0	
Digital Input Current	I_{IN}	$V_{IN} = 0.4V$ to 15V		—	1	10	—	1	10	μA
Digital "0" Enable Current	$I_{INL\,(EN)}$	$V_{EN} = 0.4V$		—	4	10	—	4	10	μA
Digital Input Capacitance	C_{DIG}			—	3	—	—	3	—	pF
Switching Time	t_{TRAN}	(Notes 2, 5) Figure 1 (Test Circuit)		—	1.0	1.3	—	1.5	2.1	μs
Output Settling Time	t_S	10V Step to 0.10%		—	1.3	—	—	1.7	—	μs
		10V Step to 0.05%		—	1.5	—	—	1.9	—	
		10V Step to 0.02%		—	2.3	—	—	2.5	—	
Break-Before-Make Delay	t_{OPEN}	Figure 3 (Test Circuit)		—	0.8	—	—	1.0	—	μs
Enable Delay "ON"	$t_{ON\,(EN)}$	(Note 5) Figure 2 (Test Circuit)		—	1	2	—	1	2	μs
Enable Delay "OFF"	$t_{OFF\,(EN)}$	(Note 5) Figure 2 (Test Circuit)		—	0.1	0.4	—	0.2	0.4	μs
"OFF" Isolation	ISO_{OFF}	(Note 4) Figure 5 (Test Circuit)	MUX-08	—	60	—	—	60	—	dB
			MUX-24	—	66	—	—	66	—	
Crosstalk	CT	(Note 3) Figure 4 (Test Circuit)	MUX-08	—	70	—	—	70	—	dB
			MUX-24	—	76	—	—	76	—	
Source Capacitance	$C_{S\,(OFF)}$	Switch "OFF", $V_S = 0V$, $V_D = 0V$	MUX-08	—	2.5	—	—	2.5	—	pF
			MUX-24	—	2	—	—	2	—	
Drain Capacitance	$C_{D(OFF)}$	Switch "OFF", $V_S = 0V$, $V_D = 0V$	MUX-08	—	7	—	—	7	—	pF
			MUX-24	—	4	—	—	4	—	
Input to Output Capacitance	$C_{DS(OFF)}$	(Note 4)	MUX-08	—	0.3	—	—	0.3	—	pF
			MUX-24	—	0.15	—	—	0.15	—	
Positive Supply Current (All Digital Inputs Logic "0" or "1")	I+	V+ = 15V		—	10	12	—	6	12	mA
		V+ = 5V		—	8	—	—	5	—	
Negative Supply Current (All Digital Inputs Logic "0" or "1")	I−	V+ = −15V		—	3.0	3.8	—	2.0	3.8	mA
		V+ = −5V		—	2.5	—	—	1.8	—	

NOTES: See next page.

ELECTRICAL CHARACTERISTICS at V+ = 15V, V− = −15V and −55° C ≤ T_A ≤ 125° C, unless otherwise noted.

				MUX-08A/ MUX-24A			MUX-08B/ MUX-24B			
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	MIN	TYP	MAX	UNITS
"ON" Resistance	R_{ON}	$V_D \le 10V$, $I_D \le 200\mu A$		—	—	400	—	—	500	Ω
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$-10V \le V_D \le 10V$, $I_S = 200\mu A$		—	1.5	—	—	4.5	—	%
R_{ON} Match Between Switches	R_{ON} Match	$V_D = 0V$, $I_S = 200\mu A$		—	10	—	—	15	—	%
Analog Voltage Range	V_A	(Note 6)		+10	+10.4	—	+10	+10.4	—	Volts
				−10	−15	—	−10	−15	—	
Source Current (Switch "OFF")	$I_{S(OFF)}$	$V_S = 10V$, $V_D = -10V$ (Notes 1, 7)		—	—	25	—	—	50	nA
Drain Current (Switch "OFF")	$I_{D(OFF)}$	$V_S = 10V$, $V_D = -10V$ (Notes 1, 7)	MUX-08	—	—	100	—	—	500	nA
			MUX-24	—	—	50	—	—	500	
Leakage Current (Switch "ON")	$I_{D(ON)}$ $+I_{S(ON)}$	$V_D = 10V$ (Notes 1, 7)	MUX-08	—	—	100	—	—	500	nA
			MUX-24	—	—	50	—	—	500	
Digital "1" Input Voltage	V_{INH}			2	—	—	2	—	—	Volts
Digital "0" Input Voltage	V_{INL}			—	—	0.7	—	—	0.7	Volts
Digital Input Current	I_{IN}	$V_{IN} = 0.4V$ to 15V		—	—	20	—	—	20	μA
Digital "0" Enable Current	$I_{INL(EN)}$	$V_{EN} = 0.4V$		—	—	20	—	—	20	μA
Positive Supply Current	I+	All Digital Inputs Logic "0" or "1"		—	—	15	—	—	15	mA
Negative Supply Current	I−	All Digital Inputs Logic "0" or "1"		—	—	5	—	—	5	mA

ELECTRICAL CHARACTERISTICS at V+ = 15V, V− = −15V and −25° C ≤ T_A ≤ +85° C for MUX-08EQ, FQ and MUX-24EQ, FQ; 0° C ≤ T_A ≤ +70° C for MUX-08EP, FP and MUX-24EP, FP, unless otherwise noted.

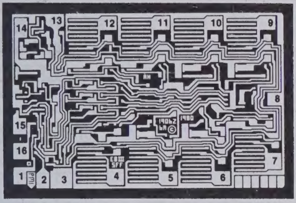
				MUX-08E/ MUX-24E			MUX-08F/ MUX-24F			
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	MIN	TYP	MAX	UNITS
"ON" Resistance	R_{ON}	$V_D \le 10V$, $I_D \le 200\mu A$		—	—	400	—	—	500	Ω
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$-10V \le V_D \le 10V$, $I_S = 200\mu A$		—	1.5	—	—	4.5	—	%
R_{ON} Match Between Switches	R_{ON} Match	$V_D = 0V$, $I_S = 200\mu A$		—	10	—	—	15	—	%
Analog Voltage Range	V_A	(Note 6)		+10	+10.4	—	+10	+10.4	—	Volts
				−10	−15	—	−10	−15	—	
Source Current (Switch "OFF")	$I_{S(OFF)}$	$V_S = 10V$, $V_D = -10V$ (Notes 1, 7)		—	—	10	—	—	10	nA
Drain Current (Switch "OFF")	$I_{D(OFF)}$	$V_S = 10V$, $V_D = -10V$ (Notes 1, 7)	MUX-08	—	—	100	—	—	100	nA
			MUX-24	—	—	50	—	—	50	
Leakage Current (Switch "ON")	$I_{D(ON)}$ $+I_{S(ON)}$	$V_D = 10V$ (Notes 1, 7)	MUX-08	—	—	100	—	—	100	nA
			MUX-24	—	—	50	—	—	50	
Digital "1" Input Voltage	V_{INH}			2	—	—	2	—	—	Volts
Digital "0" Input Voltage	V_{INL}			—	—	0.8	—	—	0.8	Volts
Digital Input Current	I_{IN}	$V_{IN} = 0.4V$ to 15V		—	—	20	—	—	20	μA
Digital "0" Enable Current	$I_{INL(EN)}$	$V_{EN} = 0.4V$		—	—	20	—	—	20	μA
Positive Supply Current	I+	All Digital Inputs Logic "0" or "1"		—	—	15	—	—	15	mA
Negative Supply Current	I−	All Digital Inputs Logic "0" or "1"		—	—	5	—	—	5	mA

NOTES:

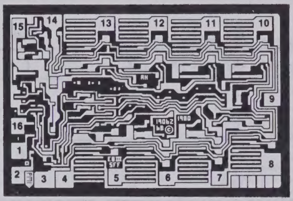
1. Conditions applied to leakage tests insure worst case leakages. Exceeding 11V on the analog input may cause an "OFF" channel to turn "ON".
2. $R_L = 10M\Omega$, $C_L = 10pF$.
3. Crosstalk is measured by driving channel 8 with channel 4 "ON". $R_L = 1M\Omega$, $C_L = 10pF$, $V_S = 5V$ RMS, f = 500kHz.
4. "OFF" isolation is measured by driving channel 8 with ALL channels "OFF". $R_L = 1k\Omega$, $C_L = 10pF$, $V_S = 5V$ RMS, f = 500kHz. C_{DS} is computed from the OFF isolation measurement.
5. Sample tested.
6. Guaranteed by leakage current and R_{ON} tests.
7. Leakage tests are performed only on military temperature grades at 125° C.

DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)

MUX-08



MUX-24



DIE SIZE 0.090 × 0.061 inch, 5490 sq. mils (2.286 × 1.549 mm, 3542 sq. mm)

MUX-08:

1. A0	**9. S8**
2. ENABLE	**10. S7**
3. V− (SUBSTRATE)	**11. S6**
4. S1	**12. S5**
5. S2	**13. V+**
6. S3	**14. GND**
7. S4	**15. A2**
8. DRAIN	**16. A1**

MUX-24:

1. A0	**9. DRAIN B**
2. ENABLE	**10. S4 B**
3. V− (SUBSTRATE)	**11. S3 B**
4. S1 A	**12. S2 B**
5. S2 A	**13. S1 B**
6. S3 A	**14. V+**
7. S4 A	**15. GND**
8. DRAIN A	**16. A1**

For additional DICE information refer to Section 2.

WAFER TEST LIMITS at V+ = 15V, V− = −15V, T_A = 25°C, unless otherwise noted. (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MUX-08/ MUX-24NT LIMIT	MUX-08/ MUX-24N LIMIT	MUX-08/ MUX-24G LIMIT	UNITS
"ON" Resistance	R_{ON}	$V_D = 0V$, $I_S = 200\mu A$		300	300	400	Ω MAX
			$T_A = 125°C$	400	—	—	
Digital "1" Input Voltage	V_{INH}			2	2	2	V MIN
Digital "0" Input Voltage	V_{INL}			0.8	0.8	0.8	V MAX
Digital "0" Input Current	I_{INL}	$V_{IN} = 0.4V$		10	10	10	μA MAX
			$T_A = 125°C$	20	—	—	
Digital "0" Enable Current	$I_{INL(EN)}$	$V_{IN} = 0.4V$		10	10	10	μA MAX
			$T_A = 125°C$	20	—	—	
Positive Supply Current (All Digital Inputs Logic "0")	I+			12	12	12	mA MAX
			$T_A = 125°C$	15	—	—	
Negative Supply Current (All Digital Inputs Logic "0")	I−			3.8	3.8	3.8	mA MAX
			$T_A = 125°C$	5	—	—	
Analog Input Range	V_A			±10	±10	±10	V MIN

Note: Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at V+ = 15V, V− = −15V and T_A = 25° C for MUX-08/24N & G, T_A = 125° C for MUX-08/24NT, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MUX-08/ MUX-24NT TYPICAL	MUX-08/ MUX-24N TYPICAL	MUX-08/ MUX-24G TYPICAL	UNITS
Switching Time	t_{TRAN}	(Note 1)	1.7	1.3	2.1	μs
Output Settling Time	t_S	10V Step to 0.1% (Note 1)	2.1	1.5	1.9	μs
Break-Before-Make Delay	t_{OPEN}	(Note 1)	0.8	0.8	1.0	μs
Crosstalk	CT	(Note 1)	70	70	70	dB
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$-10V \le V_D \le 10V$, $I_S = 200\mu A$	2	2	6	%
Leakage Current (Switch "ON")	$I_{D(ON)}$	$V_D = 10V$ (Note 1)	20	0.5	0.5	nA
Analog Input Range	V_A		+10.4/−15	+10.4/−15	+10.4/−15	V

NOTE:
1. The data shown is extrapolated from measurements made on the packaged devices.

MUX-08 LOGIC STATE

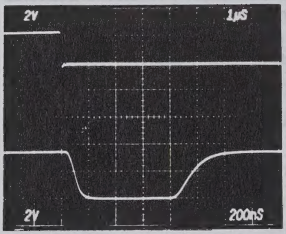
A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

MUX-24 LOGIC STATE

A_1	A_0	EN	"ON" CHANNEL
X	X	L	NONE
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

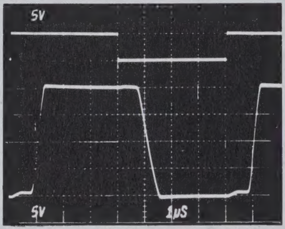
TYPICAL PERFORMANCE CHARACTERISTICS (Applies to all grades, unless otherwise noted.)

MUX-08 BREAK-BEFORE-MAKE SWITCHING



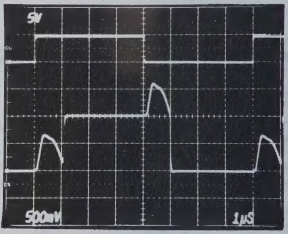
R_L = 1kΩ, C_L = 10pF, $V_{1,\ 8}$ = 10V
VOLTAGE = 2V/DIV
TIME = 200ns/DIV

MUX-08 LARGE-SIGNAL SWITCHING



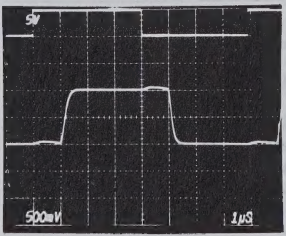
R_L = 1MΩ, C_L = 10pF, V_1 = −10V, V_8 = +10V
VOLTAGE = 5V/DIV
TIME = 1μs/DIV

MUX-08 SMALL-SIGNAL SWITCHING



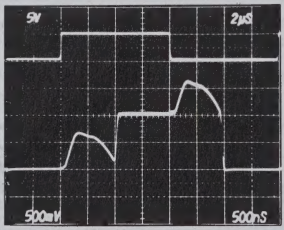
R_L = 1MΩ, C_L = 10pF, V_1 = −500mV, V_8 = +500mV
VOLTAGE = 500mV/DIV
TIME = 1μs/DIV

MUX-08 SMALL-SIGNAL SWITCHING WITH FILTERING



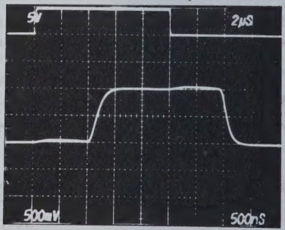
R_L = 1MΩ, C_L = 500pF, V_1 = 500mV, V_8 = +500mV
VOLTAGE = 500mV/DIV
TIME = 1μs/DIV

MUX-08 SMALL-SIGNAL SWITCHING WITH 2μs SAMPLE TIME



R_L = 1MΩ, C_L = 10pF, V_1 = −500mV, V_8 = +500mV
VOLTAGE = 500mV/DIV
TIME = 500ns/DIV

MUX-08 SMALL-SIGNAL SWITCHING WITH FILTERING AND 2.5μs SAMPLE TIME

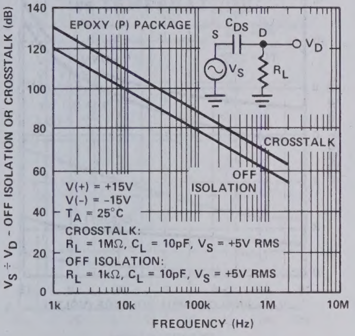


R_L = 1MΩ, C_L = 500pF, V_1 = −500mV, V_8 = +500mV
VOLTAGE = 500mV/DIV
TIME = 500ns/DIV

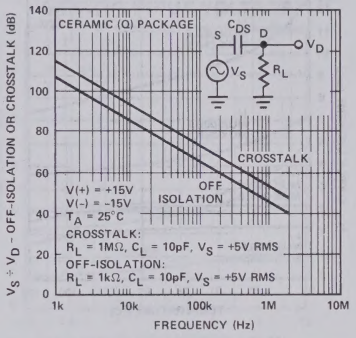
NOTE:
Top waveforms: Digital Input 5V/DIV
Bottom waveforms: Multiplexer Output

TYPICAL PERFORMANCE CHARACTERISTICS (Applies to all grades, unless otherwise noted.)

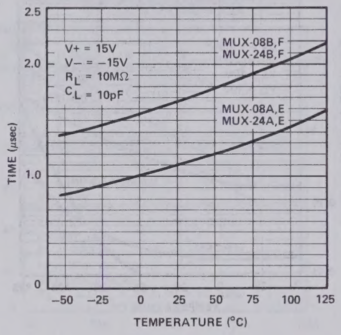
MUX-08 CROSSTALK AND OFF ISOLATION PERFORMANCE OF CHANNEL 8



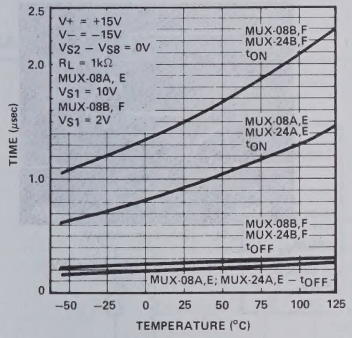
MUX-08 CROSSTALK AND OFF ISOLATION PERFORMANCE OF CHANNEL 8



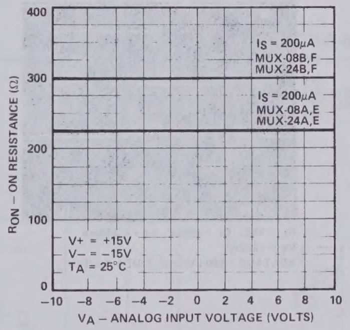
TRANSITION TIMES vs TEMPERATURE



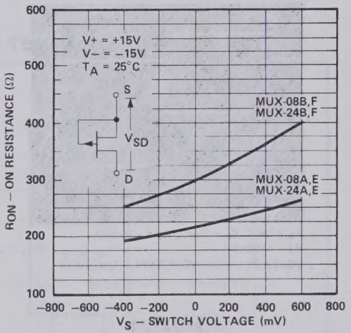
ENABLE DELAY TIMES vs TEMPERATURE



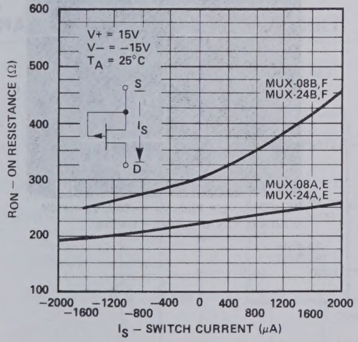
"ON" RESISTANCE (R_{ON}) vs ANALOG VOLTAGE (V_A)



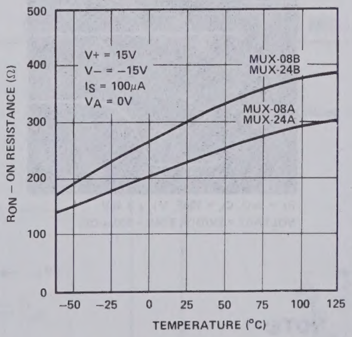
R_{ON} vs SWITCH VOLTAGE (V_{SD})



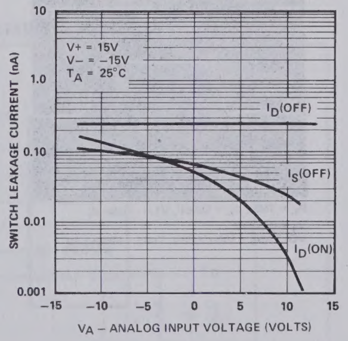
R_{ON} vs SWITCH CURRENT (I_S)



R_{ON} vs TEMPERATURE

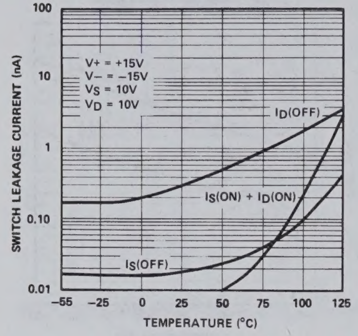


SWITCH LEAKAGE CURRENTS vs ANALOG INPUT VOLTAGE

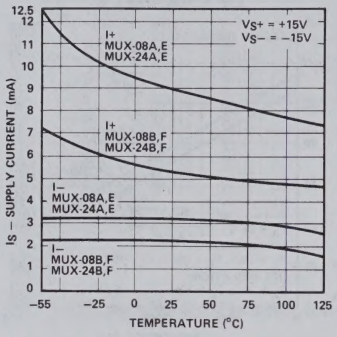


TYPICAL PERFORMANCE CHARACTERISTICS (Applies to all grades, unless otherwise noted.)

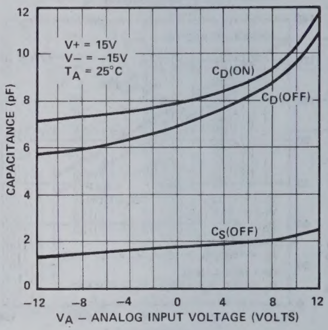
SWITCH LEAKAGE CURRENTS vs TEMPERATURE



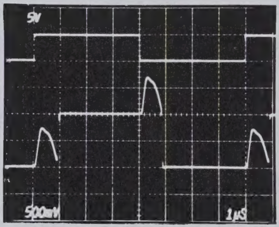
SUPPLY CURRENTS vs TEMPERATURE



MUX-08 SWITCH CAPACITANCES vs ANALOG INPUT VOLTAGE

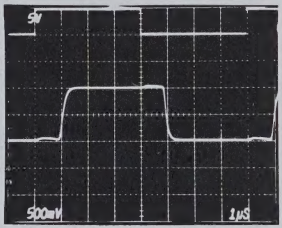


MUX-24 SMALL-SIGNAL SWITCHING



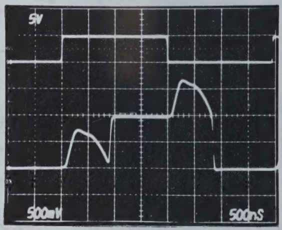
R_L = 1MΩ, C_L = 10pF, V_1 = −500mV,
V_4 = +500mV
VOLTAGE = 500mV/DIV, TIME = 1μs/DIV

MUX-24 SMALL-SIGNAL SWITCHING WITH FILTERING



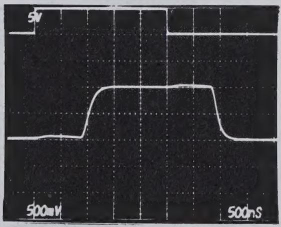
R_L = 1MΩ, C_L = 500pF, V_1 = −500mV,
V_4 = +500mV
VOLTAGE = 500mV/DIV, TIME = 1μs/DIV

MUX-24 SMALL-SIGNAL SWITCHING WITH 2μs SAMPLE TIME



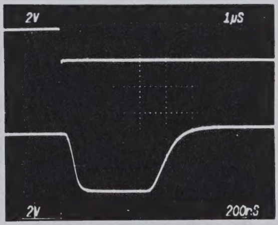
R_L = 1MΩ, C_L = 10pF, V_1 = −500mV,
V_4 = +500mV
VOLTAGE = 500mV/DIV, TIME = 500ns/DIV

MUX-24 SMALL-SIGNAL SWITCHING WITH FILTERING AND 2.5μs SAMPLE TIME



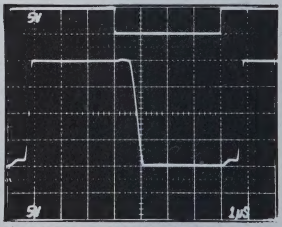
R_L = 1MΩ, C_L = 500pF, V_1 = −500mV,
V_4 = +500mV
VOLTAGE = 500mV/DIV, TIME = 500ns/DIV

MUX-24 BREAK-BEFORE-MAKE SWITCHING



R_L = 1kΩ, C_L = 10pF, $V_{1,\,4}$ = 10V
VOLTAGE = 2V/DIV, TIME = 200ns/DIV

MUX-24 LARGE-SIGNAL SWITCHING

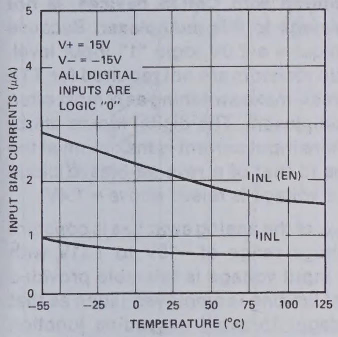


R_L = 1MΩ, C_L = 10pF, V_1 = −10V, V_4 = +10V
VOLTAGE = 5V/DIV, TIME = 1μs/DIV

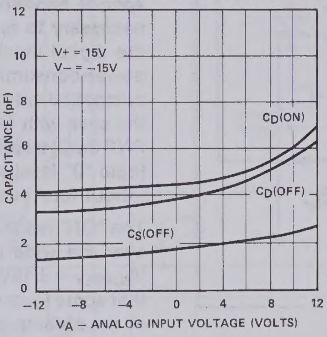
NOTE:
Top waveforms: Digital Input 5V/DIV
Bottom waveforms: Multiplexer Output

TYPICAL PERFORMANCE CHARACTERISTICS (Applies to all grades, unless otherwise noted.)

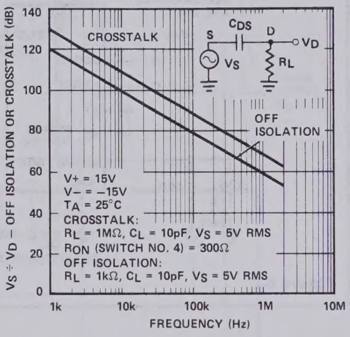
DIGITAL INPUT CURRENTS vs TEMPERATURE



MUX-24 SWITCH CAPACITANCES vs ANALOG INPUT VOLTAGE



MUX-24 CROSSTALK AND OFF ISOLATION PERFORMANCE OF CHANNEL 3A



A.C. TEST CIRCUITS

TRANSITION TIME TEST CIRCUIT

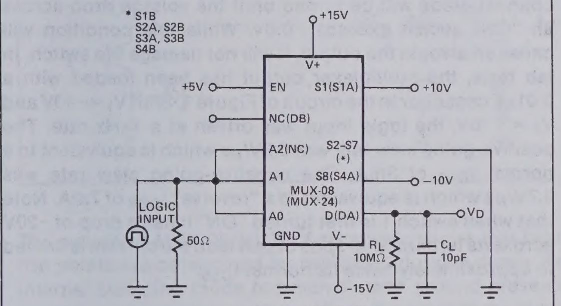

* S1B
S2A, S2B
S3A, S3B
S4B
+15V
V+
+5V
EN
S1(S1A)
+10V
NC(DB)
A2(NC)
S2-S7
(*)
A1
S8(S4A)
–10V
MUX-08
(MUX-24)
LOGIC INPUT
A0
D(DA)
VD
50Ω
GND
V-
RL
10MΩ
CL
10pF
–15V
( ) DENOTES MUX-24

Figure 1

BREAK-BEFORE-MAKE TEST CIRCUIT

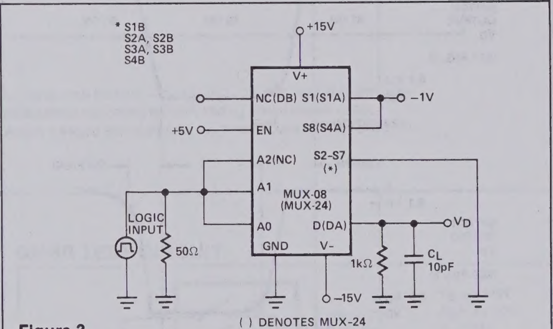

* S1B
S2A, S2B
S3A, S3B
S4B
+15V
V+
NC(DB)
S1(S1A)
–1V
+5V
EN
S8(S4A)
A2(NC)
S2-S7
(*)
A1
MUX-08
(MUX-24)
LOGIC INPUT
A0
D(DA)
VD
50Ω
GND
V-
1kΩ
CL
10pF
–15V
( ) DENOTES MUX-24

Figure 3

ENABLE DELAY TIME TEST CIRCUIT

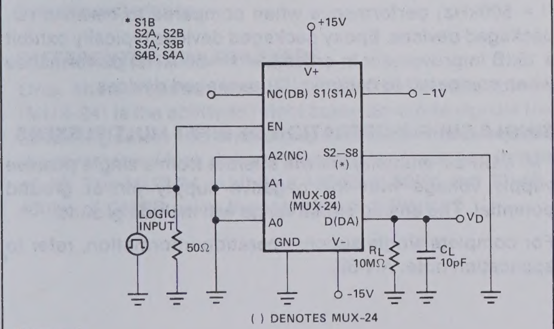

* S1B
S2A, S2B
S3A, S3B
S4B, S4A
+15V
V+
NC(DB)
S1(S1A)
–1V
EN
A2(NC)
S2–S8
(*)
A1
MUX-08
(MUX-24)
LOGIC INPUT
A0
D(DA)
VD
50Ω
GND
V-
RL
10MΩ
CL
10pF
–15V
( ) DENOTES MUX-24

Figure 2

CROSSTALK MEASUREMENT CIRCUIT

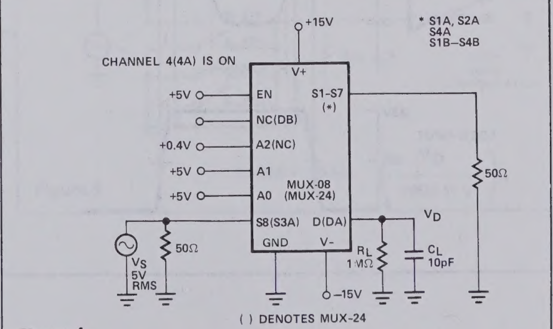

+15V
* S1A, S2A
S4A
S1B–S4B
CHANNEL 4(4A) IS ON
V+
+5V
EN
S1–S7
(*)
NC(DB)
+0.4V
A2(NC)
+5V
A1
50Ω
+5V
A0
MUX-08
(MUX-24)
VD
S8(S3A)
D(DA)
50Ω
VS
5V
RMS
GND
V-
RL
1MΩ
CL
10pF
–15V
( ) DENOTES MUX-24

Figure 4

A.C. TEST CIRCUITS

OFF-ISOLATION MEASUREMENT CIRCUIT

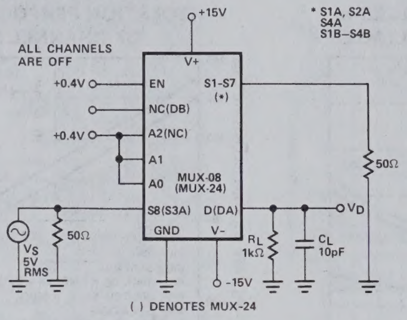
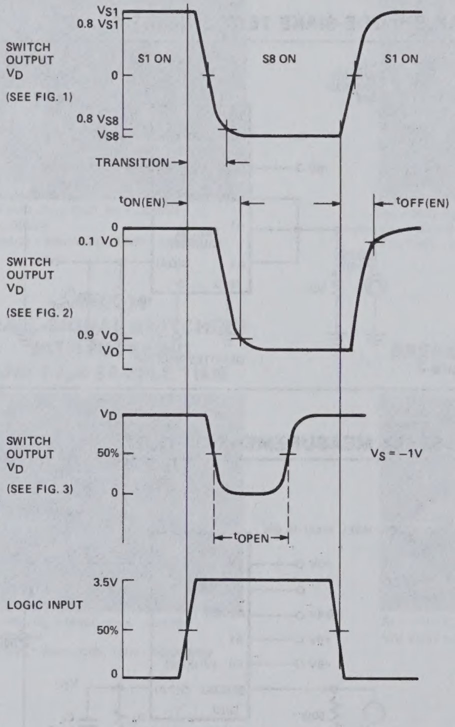

+15V
* S1A, S2A
S4A
S1B–S4B
ALL CHANNELS
ARE OFF
V+
+0.4V
EN
S1-S7
(*)
NC(DB)
+0.4V
A2(NC)
A1
50Ω
MUX-08
(MUX-24)
A0
S8(S3A)
D(DA)
V_D
GND
V-
50Ω
R_L
1kΩ
C_L
10pF
V_S
5V
RMS
-15V
( ) DENOTES MUX-24

Figure 5

SWITCHING TIME WAVEFORMS


V_{S1}
0.8 V_{S1}
SWITCH OUTPUT V_D (SEE FIG. 1)
S1 ON
S8 ON
S1 ON
0
0.8 V_{S8}
V_{S8}
TRANSITION
$t_{ON(EN)}$
$t_{OFF(EN)}$
0
0.1 V_O
SWITCH OUTPUT V_D (SEE FIG. 2)
0.9 V_O
V_O
V_D
SWITCH OUTPUT V_D (SEE FIG. 3)
50%
0
V_S = −1V
t_{OPEN}
3.5V
LOGIC INPUT
50%
0

APPLICATIONS INFORMATION

These analog multiplexers employ ion-implanted JFETs in a switch configuration designed to assure break-before-make action. The turn-off time is much faster than the turn-on time to guarantee this feature over the full operating temperature and input voltage range. Fabricated with BIFET processing, **special handling as required with CMOS devices, is not necessary to prevent damage to this multiplexer.** Because the digital inputs only require a 2.0V logic "1" input level, power-consuming pull-up resistors are not required for TTL compatibility to insure break-make switching as is most often the case with CMOS multiplexers. The digital inputs utilize PNP input transistors where input current is maximum at the logic "0" level and drops to that of a reverse-biased diode (about 10nA) as the input voltage is raised above ≈ 1.4V.

The "ON" resistance, R_{ON}, of the analog switches is constant over the wide input voltage range of −15V to +11V with $V_{SUPPLY} = \pm 15V$. Higher input voltage is tolerable provided that some form of current limiting is employed (such as that of an op-amp output stage) to avoid exceeding junction temperature and power dissipation requirements. For normal operation, however, positive input voltages should be restricted to 11V (or 4V less than the positive supply). This assures that the V_{GS} of an "OFF" switch remains greater than its V_p, and prevents that channel from being falsely turned "ON". When operating with negative input voltages, the gate-to-channel diode will be turned on if the voltage drop across an "ON" switch exceeds −0.6V. While this condition will cause an error in the output, it will not damage the switch. In lab tests, the multiplexer output has been loaded with a 0.01μF capacitor in the circuit of Figure 1. With $V_1 = -10V$ and $V_8 = +10V$, the logic input was driven at a 1kHz rate. The positive-going slew rate was 0.3V/μs which is equivalent to a normal I_{DSS} of 3mA. The negative-going slew rate was 0.7V/μs which is equivalent to a "reverse" I_{DSS} of 7mA. Note that when switch 1 is first turned "ON" it has a drop of −20V across its terminals. In spite of that fact, the current is limited to approximately twice its normal I_{DSS}.

CROSSTALK AND OFF-ISOLATION

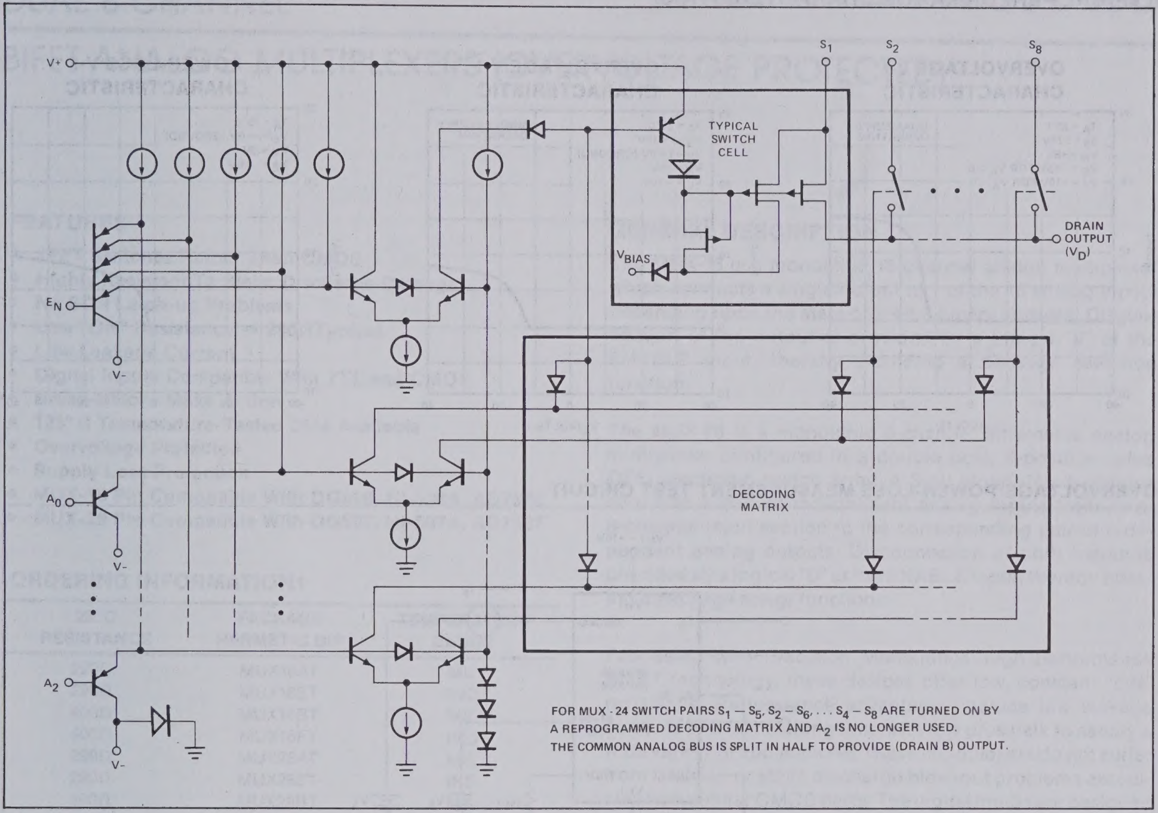
Crosstalk and off-isolation performance is influenced by the type of package selected. Epoxy (P) packaged devices typically exhibit a 12dB improvement in off-isolation (f = 500kHz) performance when compared to ceramic (Q) packaged devices. Epoxy packaged devices typically exhibit a 15dB improvement in crosstalk (f = 500kHz) performance when compared to ceramic (Q) packaged devices.

SINGLE SUPPLY OPERATION OF BIFET MULTIPLEXERS

PMI's BIFET multiplexers will operate from a single positive supply voltage with the negative supply pin at ground potential. The analog signal range will include ground.

For complete single supply operation information, refer to application note, AN-32.

SIMPLIFIED MUX-08 SCHEMATIC


V+
S1
S2
S8
TYPICAL SWITCH CELL
DRAIN OUTPUT (V_D)
V_BIAS
E_N
V-
A_0
V-
A_2
V-
DECODING MATRIX

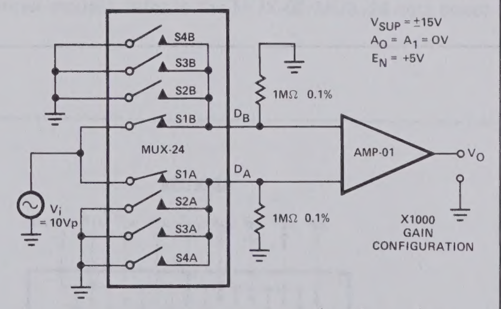
FOR MUX - 24 SWITCH PAIRS $S_1 - S_5$, $S_2 - S_6$, ... $S_4 - S_8$ ARE TURNED ON BY A REPROGRAMMED DECODING MATRIX AND A_2 IS NO LONGER USED. THE COMMON ANALOG BUS IS SPLIT IN HALF TO PROVIDE (DRAIN B) OUTPUT.

The simplified MUX-08/MUX-24 schematic shows that logic trip points are determined by two forward diode drops. An internal clamping diode between V− and ground prevents excessive current flow between V+ and ground in the event that V− becomes open circuit. The decoding matrix is accomplished by a programmed diode array. The switch cell consists of P channel JFET's with appropriate blocking diodes which ruggedizes the circuit's overvoltage and supply loss characteristics.

DIFFERENTIAL MULTIPLEXERS

One characteristic unique to differential multiplexers (MUX-24) is the ability to reject common-mode signals from becoming differential error signals. Common-mode rejection is a parameter which defines the amount of rejection in terms of dB. The MUX-24 exhibits a 106dB at 60Hz and 101dB at 400Hz of CMRR using the test circuit of Figure 6.

CMRR TEST CIRCUIT


S4B
S3B
S2B
S1B
MUX-24
S1A
S2A
S3A
S4A
D_B
D_A
1MΩ 0.1%
1MΩ 0.1%
V_i = 10Vp
AMP-01
V_O
X1000 GAIN CONFIGURATION

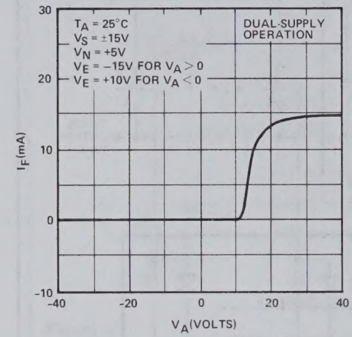
$V_{SUP} = \pm 15V$
$A_O = A_1 = 0V$
$E_N = +5V$

Figure 6

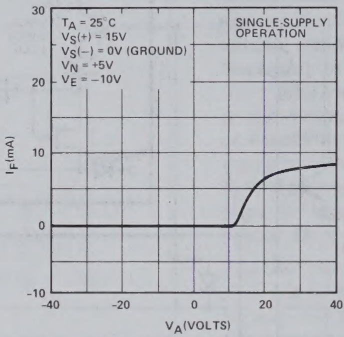
$$\text{CMRR} = 20 \log \left(\frac{V_O}{1000 \times V_i} \right)$$

TYPICAL PERFORMANCE CHARACTERISTICS

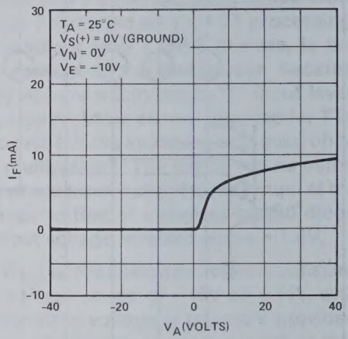
OVERVOLTAGE V-I CHARACTERISTIC



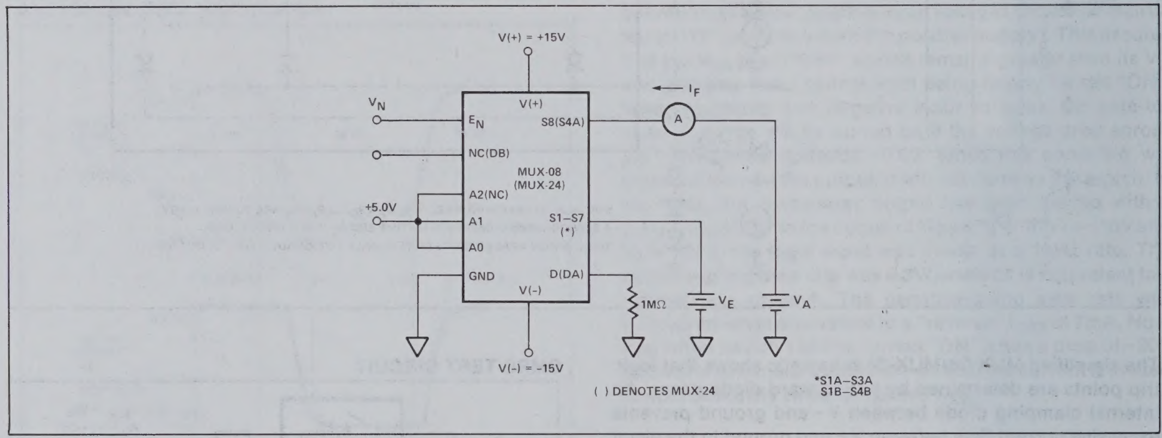
OVERVOLTAGE V-I CHARACTERISTIC



POWER-LOSS V-I CHARACTERISTIC



OVERVOLTAGE/POWER-LOSS MEASUREMENT TEST CIRCUIT


V(+) = +15V
V_N
E_N
V(+)
S8(S4A)
I_F
A
NC(DB)
MUX-08
(MUX-24)
A2(NC)
+5.0V
A1
A0
S1–S7
(*)
GND
D(DA)
V(–)
1MΩ
V_E
V_A
V(–) = –15V
( ) DENOTES MUX-24
*S1A–S3A
S1B–S4B

16-CHANNEL/
DUAL 8-CHANNEL

MUX-16/MUX-28

BIFET ANALOG MULTIPLEXERS (OVERVOLTAGE PROTECTED)

FEATURES

- **JFET Switches Rather Than CMOS**
- **Highly Resistant To Static Discharge Damage**
- **No SCR Latch-up Problems**
- **Low "ON" Resistance — 290Ω Typical**
- **Low Leakage Current**
- **Digital Inputs Compatible With TTL and CMOS**
- **Break-Before-Make Action**
- **125° C Temperature-Tested Dice Available**
- **Overvoltage Protected**
- **Supply Loss Protection**
- **MUX-16 Pin Compatible With DG506, HI-506A, AD7506**
- **MUX-28 Pin Compatible With DG507, HI-507A, AD7507**

ORDERING INFORMATION†

25° C RESISTANCE	PACKAGE HERMETIC DIP	TEMPERATURE RANGE
290Ω*	MUX16AT	MIL
290Ω	MUX16ET	IND
400Ω*	MUX16BT	MIL
400Ω	MUX16FT	IND
290Ω*	MUX28AT	MIL
290Ω	MUX28ET	IND
400Ω*	MUX28BT	MIL
400Ω	MUX28FT	IND

*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

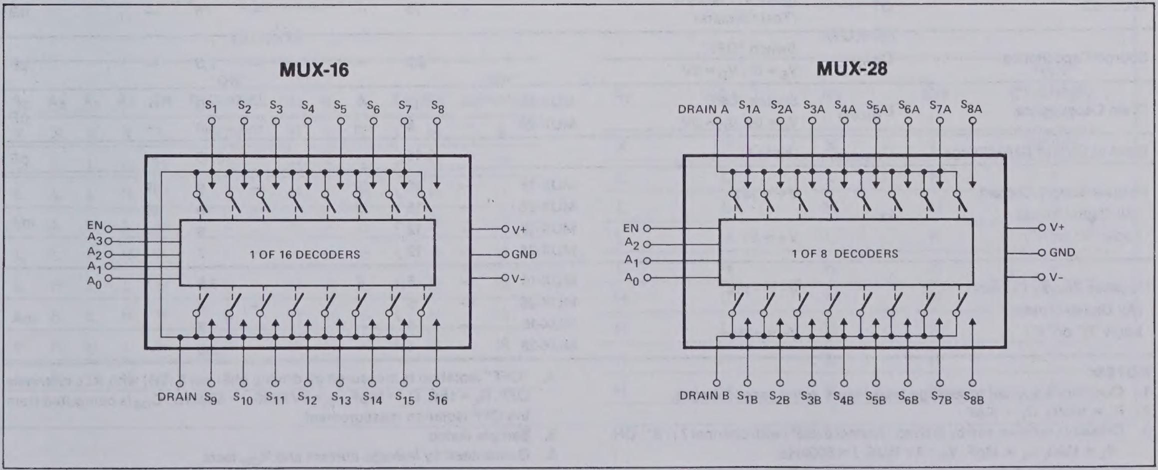
GENERAL DESCRIPTION

The MUX-16 is a monolithic 16-channel analog multiplexer which connects a single output to 1 of the 16 analog inputs depending upon the state of a 4-bit binary address. Disconnection of the output is provided by a logical "0" at the ENABLE input, thereby providing a package selection function.

The MUX-28 is a monolithic 8-channel differential analog multiplexer configured in a double pole, 8-position (plus OFF) electronic switch array. A 3-bit binary input address connects a pair of independent analog inputs from each 8-channel input section to the corresponding pair of independent analog outputs. Disconnection of both inputs is provided by a logical "0" at the ENABLE input, thereby offering a package select function.

Fabricated with Precision Monolithics' high performance BIFET technology, these devices offer low, constant "ON" resistance. Performance advantages include low leakage currents and fast settling time with low crosstalk to satisfy a wide variety of applications. These multiplexers do not suffer from latch-up or static discharge blow-out problems associated with similar CMOS parts. The digital inputs are designed to operate from both TTL and CMOS levels while always providing a definite break-before-make action without the need for external pull-up resistors. For single 8-channel and dual 4-channel models, refer to the MUX-08/MUX-24 data sheet.

FUNCTIONAL DIAGRAM


MUX-16
S_1 S_2 S_3 S_4 S_5 S_6 S_7 S_8
EN
A_3
A_2
A_1
A_0
1 OF 16 DECODERS
V+
GND
V-
DRAIN S_9 S_{10} S_{11} S_{12} S_{13} S_{14} S_{15} S_{16}
MUX-28
DRAIN A S_{1A} S_{2A} S_{3A} S_{4A} S_{5A} S_{6A} S_{7A} S_{8A}
EN
A_2
A_1
A_0
1 OF 8 DECODERS
V+
GND
V-
DRAIN B S_{1B} S_{2B} S_{3B} S_{4B} S_{5B} S_{6B} S_{7B} S_{8B}

ABSOLUTE MAXIMUM RATINGS (Ratings apply to both DICE and packaged parts, unless otherwise noted.)

Rating	Value
Operating Temperature Range,	
MUX-16/28-AT, BT	−55°C to +125°C
MUX-16/28-ET, FT	−25°C to +85°C
Dice Junction Temperature (T_j)	−65°C to +150°C
Storage Temperature Range	−65°C to +150°C
Power Dissipation	1000mW
Lead Temperature (Soldering, 60 sec)	300°C
Maximum Junction Temperature	150°C
V+ Supply to V− Supply	36V
Logic Input Voltage	(V− or −4V) to V+ Supply
Analog Input Voltage	V− Supply −20V to V+ Supply +20V
Maximum Current Through Any Pin	25mA

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ and $T_A = 25°C$, unless otherwise noted.

				MUX-16A/E MUX-28A/E			MUX-16B/F MUX-28B/F			
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	MIN	TYP	MAX	UNITS
"ON" Resistance	R_{ON}	$V_D \le 10V$, $I_D \le 200\mu A$		—	290	380	—	400	580	Ω
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$-10V \le V_D \le 10V$, $I_S = 200\mu A$		—	1.5	5	—	1.5	5	%
R_{ON} Match Between Switches	R_{ON} Match	$V_D = 0V$, $I_S = 200\mu A$		—	7	15	—	9	20	%
Analog Voltage Range	V_A	(Note 6)		+10	+11	—	+10	+11	—	Volts
				−10	−15	—	−10	−15	—	
Source Current (Switch "OFF")	I_S (OFF)	$V_S = 10V$, $V_D = -10V$ (Note 1)		—	0.01	1	—	0.01	2	nA
Drain Current (Switch "OFF")	I_D (OFF)	$V_S = 10V$, $V_D = -10V$ (Note 1)	MUX-16	—	0.2	1	—	0.2	2	nA
			MUX-28	—	0.1	1	—	0.1	2	
Leakage Current (Switch "ON")	I_D (ON) $+I_S$ (ON)	$V_D = 10V$ (Note 1)	MUX-16	—	0.2	1	—	0.2	2	nA
			MUX-28	—	0.1	1	—	0.1	2	
Digital Input Current	I_{IN}	$V_{IN} = 0.4V$ to 15V		—	1	10	—	1	10	μA
Digital "0" Enable Current	I_{INL} (EN)	$V_{EN} = 0.4V$		—	4	10	—	4	10	μA
Digital Input Capacitance	C_{DIG}			—	3	—	—	3	—	pF
Switching Time	t_{TRAN}	(Notes 2, 5) Figure 1 (Test Circuits)		—	1	1.5	—	1.5	2.1	μs
Output Settling Time	t_S	10V Step to 0.10%		—	1.5	—	—	1.9	—	μs
		10V Step to 0.05%		—	1.7	—	—	2.1	—	
		10V Step to 0.02%		—	2.5	—	—	2.7	—	
Break-Before-Make Delay	t_{OPEN}	Figure 3		—	0.7	—	—	1	—	μs
Enable Delay "ON"	$t_{ON\,(EN)}$	(Note 5) Figure 2 (Test Circuits)		—	1	2	—	1.2	2.5	μs
Enable Delay "OFF"	$t_{OFF\,(EN)}$	(Note 5) Figure 2 (Test Circuits)		—	0.25	0.5	—	0.25	0.5	μs
"OFF" Isolation	ISO_{OFF}	(Note 4) Figure 4 (Test Circuits)		—	66	—	—	66	—	dB
Crosstalk	CT	(Note 3) Figure 5 (Test Circuits)		—	75	—	—	75	—	dB
Source Capacitance	$C_{S\,(OFF)}$	Switch "OFF", $V_S = 0V$, $V_D = 0V$		—	2.5	—	—	2.5	—	pF
Drain Capacitance	$C_{D(OFF)}$	Switch "OFF", $V_S = 0V$, $V_D = 0V$	MUX-16	—	13	—	—	13	—	pF
			MUX-28	—	8	—	—	8	—	
Input to Output Capacitance	$C_{DS(OFF)}$	(Note 4)		—	0.15	—	—	0.15	—	pF
Positive Supply Current (All Digital Inputs Logic "0" or "1")	I+	V+ = 15V	MUX-16	—	15	19	—	9	19	mA
			MUX-28	—	15	19	—	8	19	
		V+ = 5V	MUX-16	—	12	—	—	8	—	
			MUX-28	—	12	—	—	7	—	
Negative Supply Current (All Digital Inputs Logic "0" or "1")	I−	V− = −15V	MUX-16	—	5	7	—	3.5	7	mA
			MUX-28	—	5	7	—	3	7	
		V− = −5V	MUX-16	—	4	—	—	3	—	
			MUX-28	—	4	—	—	2.5	—	

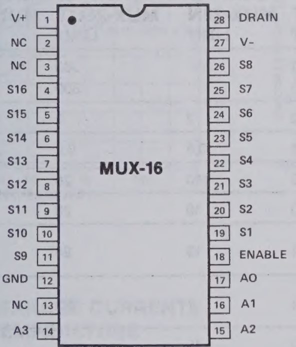
NOTES:

1. Conditions applied to leakage tests insure worst case leakages.
2. $R_L = 10M\Omega$, $C_L = 10pF$.
3. Crosstalk is measured by driving channel 8 (8B*) with channel 7 (7B*) ON. $R_L = 1M\Omega$, $C_L = 10pF$, $V_S = 5V$ RMS, f = 500kHz.
4. "OFF" isolation is measured by driving channel 8 (8B) with ALL channels OFF. $R_L = 1k\Omega$, $C_L = 10pF$, $V_S = 5V$ RMS, f = 500kHz. C_{DS} is computed from the OFF isolation measurement.
5. Sample tested.
6. Guaranteed by leakage current and R_{ON} tests.

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $-55°C \leq T_A \leq +125°C$ for MUX-16AT/BT and MUX-28AT/BT; and $-25°C \leq T_A \leq +85°C$ for MUX-16ET/FT and MUX-28ET/FT, unless otherwise noted.

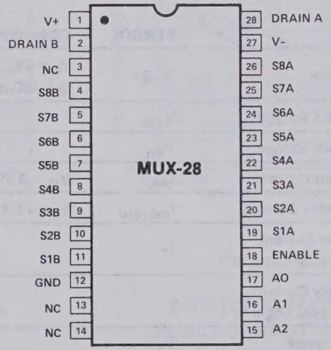
PARAMETER	SYMBOL	CONDITIONS	MUX-16A/E MUX-28A/E MIN	TYP	MAX	MUX-16B/F MUX-28B/F MIN	TYP	MAX	UNITS
"ON" Resistance	R_{ON}	$V_D \leq 10$, $I_D \leq 200\mu A$	—	—	500	—	—	800	Ω
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$-10V \leq V_D \leq 10V$, $I_S = 200\mu A$	—	2	—	—	5.5	—	%
R_{ON} Match Between Switches	R_{ON} Match	$V_D = 0V$, $I_S = 200\mu A$	—	10	—	—	15	—	%
Analog Voltage Range	V_A	(Note 6)	+10 −10	+11 −15	— —	+10 −10	+11 −15	— —	Volts
Source Current (Switch "OFF")	$I_{S\,(OFF)}$	$V_S = 10V$, $V_D = -10V$ (Note 1)	—	—	25	—	—	50	nA
Drain Current (Switch "OFF")	$I_{D\,(OFF)}$	$V_S = 10V$, $V_D = -10V$ (Note 1)	—	—	75	—	—	250	nA
Leakage Current (Switch "ON")	$I_{D\,(ON)} + I_{S\,(ON)}$	$V_D = 10V$ (Note 1)	—	—	75	—	—	250	nA
Digital "1" Input Voltage	V_{INH}		2	—	—	2	—	—	Volts
Digital "0" Input Voltage	V_{INL}		—	—	0.8	—	—	0.8	Volts
Digital Input Current	I_{IN}	$V_{IN} = 0.4V$ to 15V	—	—	20	—	—	20	μA
Digital "0" Enable Current	I_{INL} (EN)	$V_{EN} = 0.4V$	—	—	20	—	—	20	μA
Positive Supply Current	I+	All Digital Inputs Logic "0" or "1"	—	—	24	—	—	24	mA
Negative Supply Current	I−	All Digital Inputs Logic "0" or "1"	—	—	8.2	—	—	8.2	mA

PIN CONNECTIONS & TRUTH TABLES



V+ 1
NC 2
NC 3
S16 4
S15 5
S14 6
S13 7
S12 8
S11 9
S10 10
S9 11
GND 12
NC 13
A3 14
28 DRAIN
27 V−
26 S8
25 S7
24 S6
23 S5
22 S4
21 S3
20 S2
19 S1
18 ENABLE
17 AO
16 A1
15 A2
MUX-16

28-PIN HERMETIC DUAL-IN-LINE (T-Suffix)



V+ 1
DRAIN B 2
NC 3
S8B 4
S7B 5
S6B 6
S5B 7
S4B 8
S3B 9
S2B 10
S1B 11
GND 12
NC 13
NC 14
28 DRAIN A
27 V−
26 S8A
25 S7A
24 S6A
23 S5A
22 S4A
21 S3A
20 S2A
19 S1A
18 ENABLE
17 AO
16 A1
15 A2
MUX-28

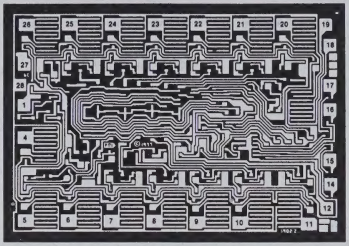
MUX-16

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL	A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	NONE	H	L	L	L	H	9
L	L	L	L	H	1	H	L	L	H	H	10
L	L	L	H	H	2	H	L	H	L	H	11
L	L	H	L	H	3	H	L	H	H	H	12
L	L	H	H	H	4	H	H	L	L	H	13
L	H	L	L	H	5	H	H	L	H	H	14
L	H	L	H	H	6	H	H	H	L	H	15
L	H	H	L	H	7	H	H	H	H	H	16
L	H	H	H	H	8						

MUX-28

A_2	A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

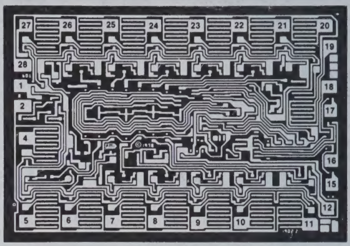
DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)



MUX-16

DIE SIZE 0.109 × 0.075 inch, 8175 sq. mils
(2.769 × 1.905 mm, 5274 sq. mm)

1. POSITIVE SUPPLY
4. SOURCE 16 (S16)
5. SOURCE 15 (S15)
6. SOURCE 14 (S14)
7. SOURCE 13 (S13)
8. SOURCE 12 (S12)
9. SOURCE 11 (S11)
10. SOURCE 10 (S10)
11. SOURCE 9 (S9)
12. GROUND
14. ADDRESS BIT 3 (A3)
15. ADDRESS BIT 2 (A2)
16. ADDRESS BIT 1 (A1)
17. ADDRESS BIT 0 (A0)
18. ENABLE
19. SOURCE 1 (S1)
20. SOURCE 2 (S2)
21. SOURCE 3 (S3)
22. SOURCE 4 (S4)
23. SOURCE 5 (S5)
24. SOURCE 6 (S6)
25. SOURCE 7 (S7)
26. SOURCE 8 (S8)
27. NEGATIVE SUPPLY (SUBSTRATE)
28. DRAIN



MUX-28

DIE SIZE 0.109 × 0.075 inch, 8175 sq. mils
(2.769 × 1.905 mm, 5274 sq. mm)

1. POSITIVE SUPPLY
2. DRAIN B
4. SOURCE 8 (S8B)
5. SOURCE 7 (S7B)
6. SOURCE 6 (S6B)
7. SOURCE 5 (S5B)
8. SOURCE 4 (S4B)
9. SOURCE 3 (S3B)
10. SOURCE 2 (S2B)
11. SOURCE 1 (S1B)
12. GROUND
15. ADDRESS BIT 2 (A2)
16. ADDRESS BIT 1 (A1)
17. ADDRESS BIT 0 (A0)
18. ENABLE
19. SOURCE 1 (S1A)
20. SOURCE 2 (S2A)
21. SOURCE 3 (S3A)
22. SOURCE 4 (S4A)
23. SOURCE 5 (S5A)
24. SOURCE 6 (S6A)
25. SOURCE 7 (S7A)
26. SOURCE 8 (S8A)
27. NEGATIVE SUPPLY (SUBSTRATE)
28. DRAIN A

For additional DICE information refer to Section 2.

WAFER TEST LIMITS at V+ = 15V, V− = −15V, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MUX-16/ MUX-28NT LIMIT	MUX-16/ MUX-28N LIMIT	MUX-16/ MUX-28GT LIMIT	MUX-16/ MUX-28G LIMIT	UNITS
"ON" Resistance	R_{ON}	$V_D = 0V$, $I_S = 100\mu A$, $T_A = 25°C$	380	380	580	580	Ω MAX
		$T_A = 125°C$	540		800		
Digital "1" Input Voltage	V_{INH}		2	2	2	2	V MIN
Digital "0" Input Voltage	V_{INL}		0.8	0.8	0.8	0.8	V MAX
Digital "0" Input Current	I_{INL}	$V_{IN} = 0.4V$	20	10	20	10	μA MAX
Digital "0" Enable Current	$I_{INL(EN)}$	$V_{EN} = 0.4V$	20	10	20	10	μA MAX
Positive Supply Current (All Digital Inputs Logic "0")	I+		24	19	24	19	mA MAX
Negative Supply Current (All Digital Inputs Logic "0")	I−		8.2	7	8.2	7	mA MAX
Analog Input Range	V_A		±10	±10	±10	±10	V MIN

Note: Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS for V+ = 15V, V− = −15V and T_A = 25° C, unless otherwise noted.

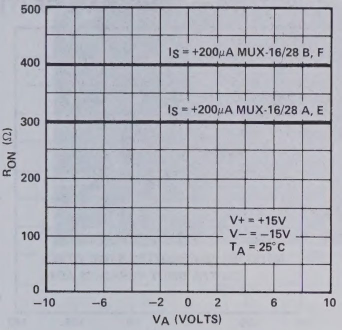
PARAMETER	SYMBOL	CONDITIONS	MUX-16/ MUX-28NT TYPICAL	MUX-16/ MUX-28N TYPICAL	MUX-16/ MUX-28GT TYPICAL	MUX-16/ MUX-28G TYPICAL	UNITS
Switching Time	t_{TRAN}	(Note 2) Figure 1	2	1	2.6	1.5	μs
Output Settling Time	t_S	10V Step to 0.1% (Note 2)	2.5	1.5	2.9	1.9	μs
Break-Before-Make Delay	t_{OPEN}	(Note 2) Figure 3 (Test Circuits)	0.8	0.8	1	1	μs
Crosstalk	CT	(Note 2) Figure 5 (Test Circuits)	70	70	70	70	dB
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$-10V \le V_D \le 10V$, $I_S = 200\mu A$	1.5	1.5	1.5	1.5	%
Leakage Current (Switch "ON")	$I_{D(ON)}$	$V_D = 10V$ (Note 2)	20	0.2	20	0.2	nA
Analog Input Range	V_A		+11 −15	+11 −15	+11 −15	+11 −15	V

NOTES:

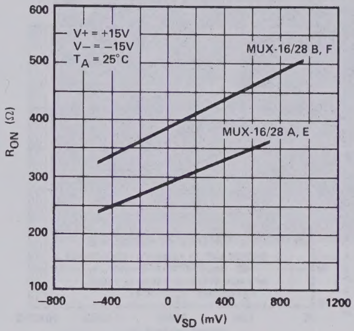
1. For MUX-16/28NT and MUX-16/28GT electrical characteristics apply at 25° C and 125° C, unless otherwise noted.
2. The data shown is extrapolated from measurements made on the packaged devices.

STATIC CHARACTERISTIC CURVES (apply to all grades, unless otherwise noted.)

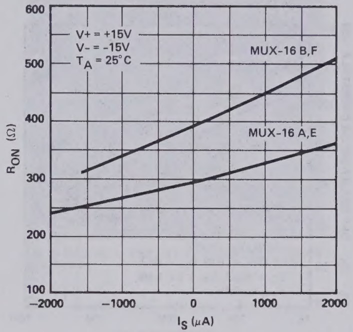
“ON” RESISTANCE (R_{ON}) vs ANALOG VOLTAGE (V_A)



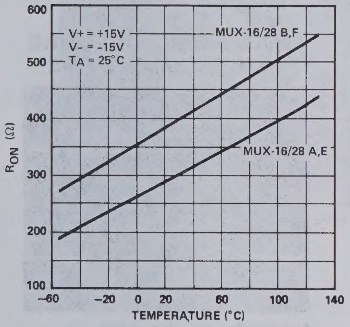
R_{ON} vs SWITCH VOLTAGE (V_{SD})



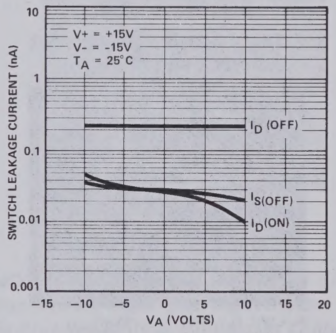
R_{ON} vs SWITCH CURRENT (I_S)



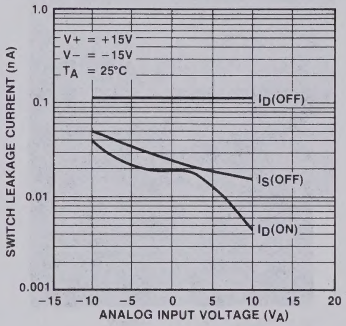
R_{ON} vs TEMPERATURE (T)



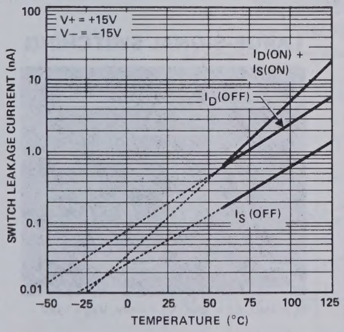
MUX-16 SWITCH LEAKAGE CURRENTS vs ANALOG INPUT VOLTAGE (V_A)



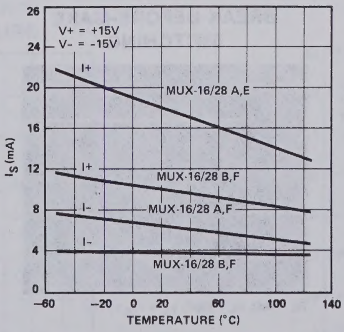
MUX-28 SWITCH LEAKAGE CURRENTS vs ANALOG INPUT VOLTAGE (V_A)



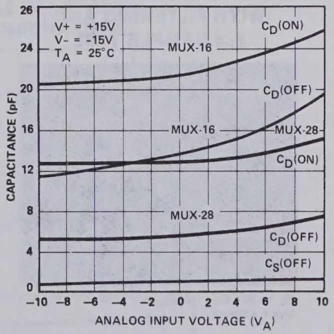
SWITCH LEAKAGE CURRENTS vs TEMPERATURE



SUPPLY CURRENTS vs TEMPERATURE (T)

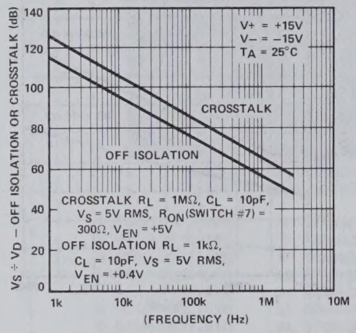


SWITCH CAPACITANCES vs ANALOG INPUT VOLTAGE (V_A)

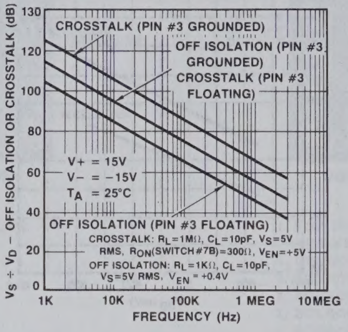


STATIC CHARACTERISTIC CURVES (apply to all grades, unless otherwise noted.)

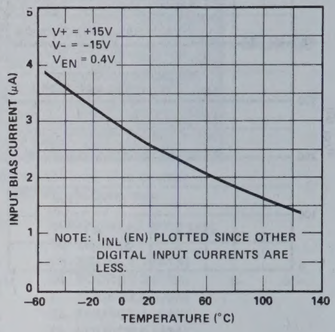
MUX-16 OFF PERFORMANCE OF CHANNEL 8



MUX-28 OFF PERFORMANCE OF CHANNEL 8

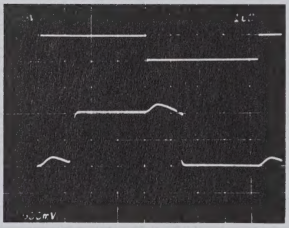


DIGITAL INPUT BIAS CURRENTS vs TEMPERATURE (T)



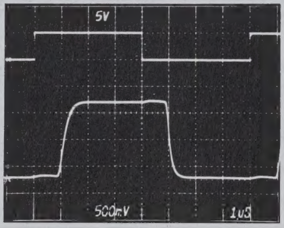
DYNAMIC CHARACTERISTIC CURVES (MUX-16)

SMALL-SIGNAL SWITCHING



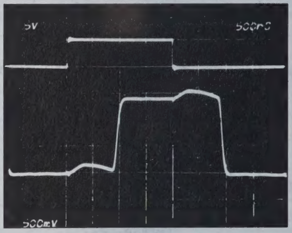
R_L = 1MΩ, C_L = 10pF, V_1 = –500mV, V_{16} = +500mV

SMALL-SIGNAL SWITCHING WITH FILTERING



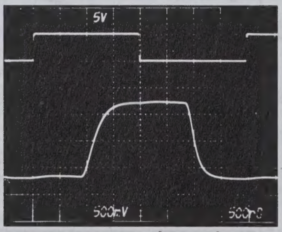
R_L = 1MΩ, C_L = 500pF, V_1 = –500mV, V_{16} = +500mV

SMALL-SIGNAL SWITCHING WITH 2µs SAMPLE TIME



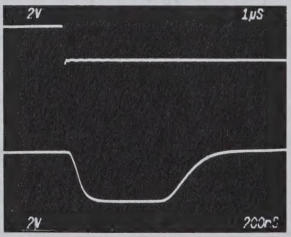
R_L = 1MΩ, C_L = 10pF, V_1 = –700mV, V_{16} = +700mV

SMALL-SIGNAL SWITCHING WITH FILTERING AND 2µs SAMPLE TIME



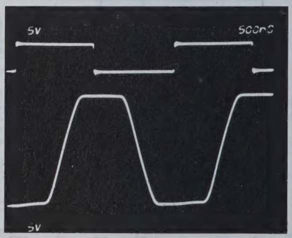
R_L = 1MΩ, C_L = 500pF, V_1 = –700mV, V_{16} = +700mV

BREAK-BEFORE-MAKE SWITCHING



R_L = 1kΩ, C_L = 10pF, V_1 = V_{16} = +10V

LARGE-SIGNAL SWITCHING

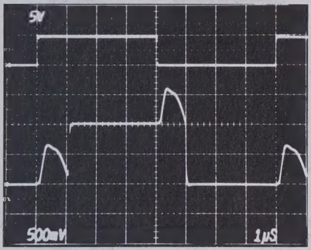


R_L = 1MΩ, C_L = 10pF, V_1 = –10V, V_{16} = +10V

NOTE:
Top Waveforms: Digital Input 5V/Div
Bottom Waveforms: Multiplexer Output (V_D)

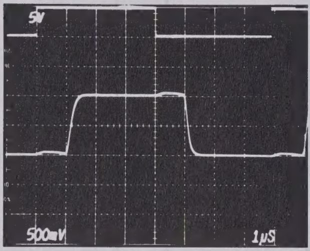
DYNAMIC CHARACTERISTIC CURVES (MUX-28)

SMALL-SIGNAL SWITCHING



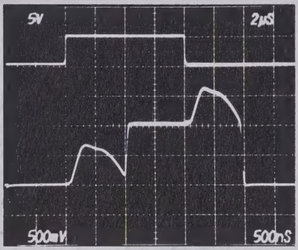
R_L = 1MΩ, C_L = 10pF, V_1 = –500mV, V_8 = +500mV

SMALL-SIGNAL SWITCHING WITH FILTERING



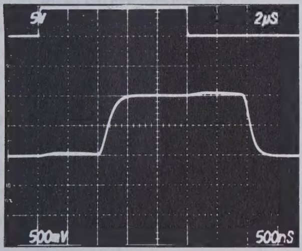
R_L = 1MΩ, C_L = 500pF, V_1 = –500mV, V_8 = +500mV

SMALL-SIGNAL SWITCHING WITH 2µs SAMPLE TIME



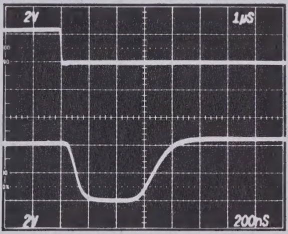
R_L = 1MΩ, C_L = 10pF, V_1 = –700mV, V_8 = +700mV

SMALL-SIGNAL SWITCHING WITH FILTERING AND 2.5µs SAMPLE TIME



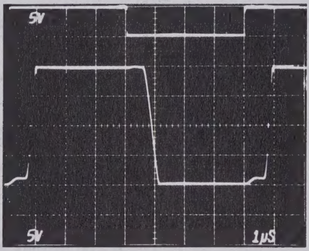
R_L = 1MΩ, C_L = 500pF, V_1 = –700mV, V_8 = +700mV

BREAK-BEFORE-MAKE SWITCHING



R_L = 1KΩ, C_L = 10pF, V_1 = V_8 = +10V

LARGE-SIGNAL SWITCHING

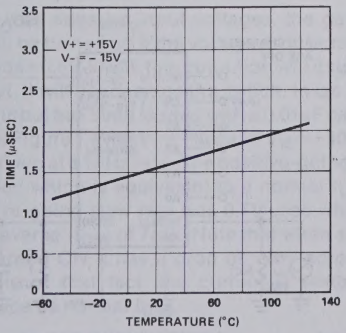


R_L = 1MΩ, C_L = 10pF, V_1 = –10V, V_8 = +10V

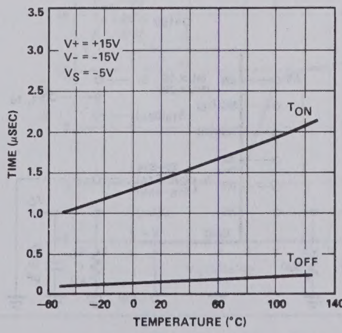
NOTE:
Top Waveforms: Digital Input 5V/Div
Bottom Waveforms: Multiplexer Output (V_D)

DYNAMIC CHARACTERISTIC CURVES (apply to all grades, unless otherwise noted.)

TRANSITION TIME vs TEMPERATURE

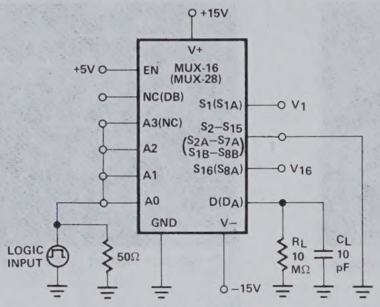


ENABLE DELAY TIME vs TEMPERATURE



A.C. TEST CIRCUITS

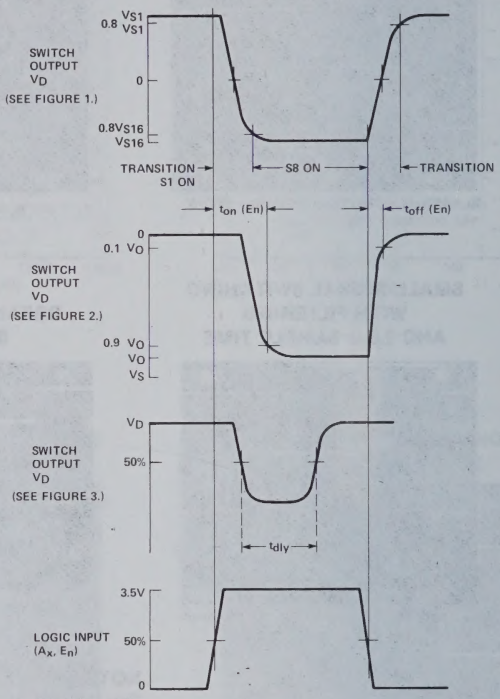
TRANSITION TIME TEST CIRCUIT


+15V
V+
+5V
EN
MUX-16
(MUX-28)
NC(DB)
S1(S1A)
V1
A3(NC)
S2–S15
(S2A–S7A)
(S1B–S8B)
A2
A1
S16(S8A)
V16
A0
D(DA)
GND
V–
LOGIC INPUT
50Ω
RL 10 MΩ
CL 10 pF
–15V

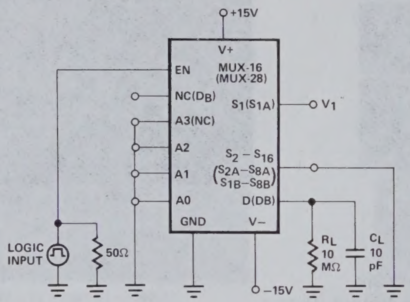
( ) DENOTES MUX-28 CONNECTIONS

Figure 1

SWITCHING TIME WAVEFORMS


0.8 VS1
VS1
SWITCH OUTPUT
VD
(SEE FIGURE 1.)
0
0.8VS16
VS16
TRANSITION
S1 ON
S8 ON
TRANSITION
ton (En)
toff (En)
0
0.1 VO
SWITCH OUTPUT
VD
(SEE FIGURE 2.)
0.9 VO
VO
VS
VD
SWITCH OUTPUT
VD
50%
(SEE FIGURE 3.)
tdly
3.5V
LOGIC INPUT
(Ax, En)
50%
0

ENABLE DELAY TIME TEST CIRCUIT


+15V
V+
EN
MUX-16
(MUX-28)
NC(DB)
S1(S1A)
V1
A3(NC)
A2
S2 – S16
(S2A–S8A)
(S1B–S8B)
A1
A0
D(DB)
GND
V–
LOGIC INPUT
50Ω
RL 10 MΩ
CL 10 pF
–15V

( ) DENOTES MUX-28 CONNECTIONS

Figure 2

BREAK-BEFORE-MAKE TEST CIRCUIT

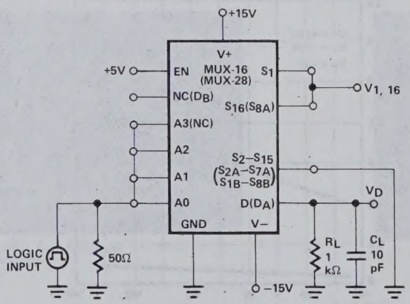

+15V
V+
+5V
EN
MUX-16
(MUX-28)
S1
V1, 16
NC(DB)
S16(S8A)
A3(NC)
A2
S2–S15
(S2A–S7A)
(S1B–S8B)
A1
VD
A0
D(DA)
GND
V–
LOGIC INPUT
50Ω
RL 1 kΩ
CL 10 pF
–15V

Figure 3

( ) DENOTES MUX-28 CONNECTIONS

OFF ISOLATION TEST CIRCUIT

$$ISO_{OFF} = 20 \log \frac{|V_S|}{|V_D|}$$

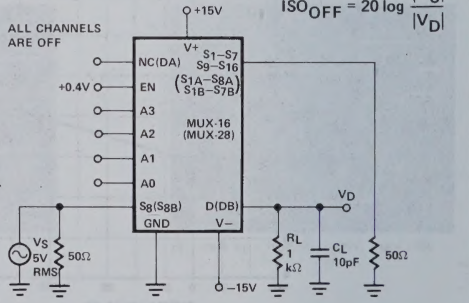
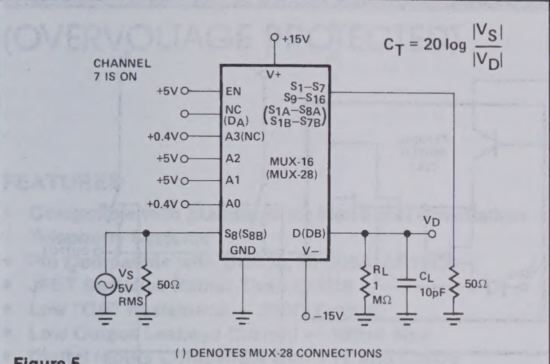

+15V
ALL CHANNELS ARE OFF
V+
NC(DA)
S1–S7
S9–S16
(S1A–S8A)
(S1B–S7B)
+0.4V
EN
A3
MUX-16
(MUX-28)
A2
A1
A0
S8(S8B)
D(DB)
VD
GND
V–
VS 5V RMS
50Ω
RL 1 kΩ
CL 10pF
50Ω
–15V

Figure 4

( ) DENOTES MUX-28 CONNECTIONS

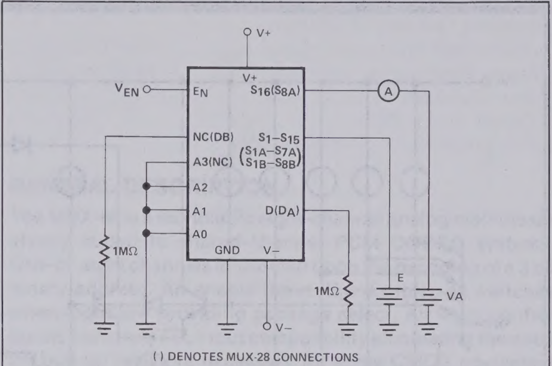
CROSSTALK MEASUREMENT CIRCUIT



( ) DENOTES MUX-28 CONNECTIONS

Figure 5

OVERVOLTAGE MEASUREMENT TEST CIRCUIT



( ) DENOTES MUX-28 CONNECTIONS

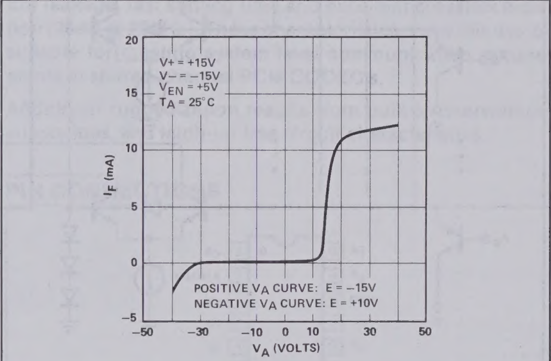
APPLICATIONS INFORMATION

These analog multiplexers employ ion-implanted JFETs in a switch configuration designed to assure break-before-make (B.B.M.) action. The turn-off time is much faster than the turn-on time to guarantee B.B.M. over the full operating temperature and input voltage range. Fabricated with BIFET processing rather than CMOS, special handling is not necessary to prevent damage to this multiplexer. Because the digital inputs only require a 2.0V logic "1" input level, power-consuming pullup resistors are not required for TTL compatibility to insure break-before-make switching as is most often the case with CMOS multiplexers. The digital inputs utilize PNP input transistors where input current is maximum at the logic "0" level and drops to that of a reverse-biased diode (about 10nA) as the input voltage is raised above ≈ 1.4V.

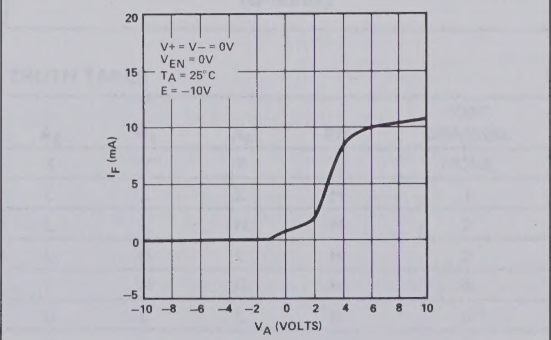
The "ON" resistance, R_{ON} of the analog switches is constant over the wide input voltage range of −55V to +11V with $V_{SUPPLY} = \pm 15V$. The overvoltage and supply-loss V-I characteristics shown indicate typical performance when the multiplexer is subjected to abnormal signals. For normal operation, however, positive input voltages should be restricted to 11V (or 4V less than the positive supply). This assures that the V_{GS} of an OFF FET switch remains greater than its V_P, preventing that channel from being falsely turned ON.

When operating with negative input voltages, the gate-to-channel diode will be turned on if the voltage drop across an ON switch exceeds −0.6V. While this condition will cause an error in the output, it will not damage the switch. In lab tests, the multiplexer output has been loaded with a 0.01μF capacitor in the circuit of Figure 1. With $V_1 = -10V$ and $V_{16} = +10V$, the logic input was driven at a 1kHz rate. The positive-going slew rate was 0.3V/μSec which is equivalent to a normal I_{DSS} of 3mA. The negative-going slew rate was 0.7V/μsec which is equivalent to a "reverse" I_{DSS} of 7mA. Note that when switch one (1) is first turned ON it has a drop of −20V across its terminals. In spite of that fact, the current is limited to approximately twice its normal I_{DSS}.

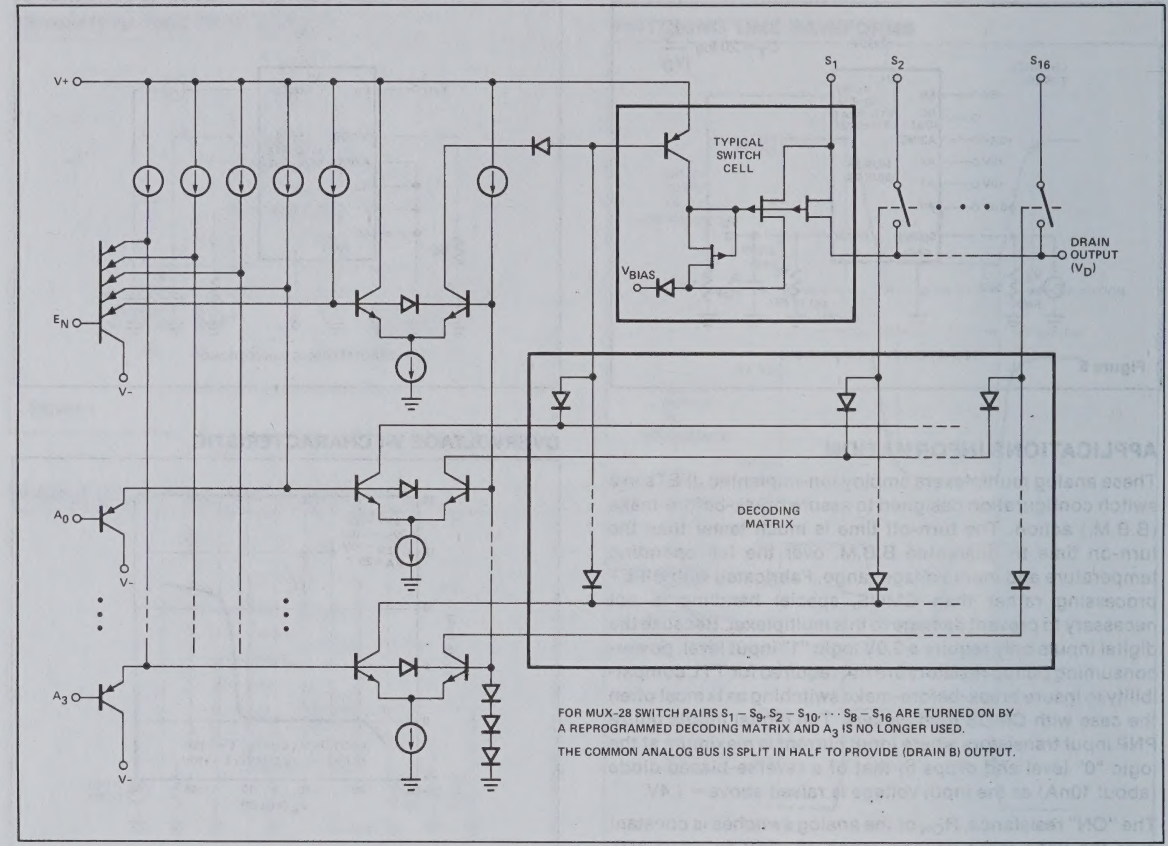
OVERVOLTAGE V-I CHARACTERISTIC



SUPPLY-LOSS V-I CHARACTERISTIC



SIMPLIFIED SCHEMATIC (MUX-16)


V+
E_N
V-
A_0
V-
A_3
V-
TYPICAL SWITCH CELL
V_{BIAS}
S_1
S_2
S_{16}
DRAIN OUTPUT (V_D)
DECODING MATRIX

FOR MUX-28 SWITCH PAIRS $S_1 - S_9$, $S_2 - S_{10}$, · · · $S_8 - S_{16}$ ARE TURNED ON BY A REPROGRAMMED DECODING MATRIX AND A_3 IS NO LONGER USED.

THE COMMON ANALOG BUS IS SPLIT IN HALF TO PROVIDE (DRAIN B) OUTPUT.

8-CHANNEL
ANALOG MULTIPLEXER FOR PCM CODECS
(OVERVOLTAGE PROTECTED)

MUX-88

FEATURES

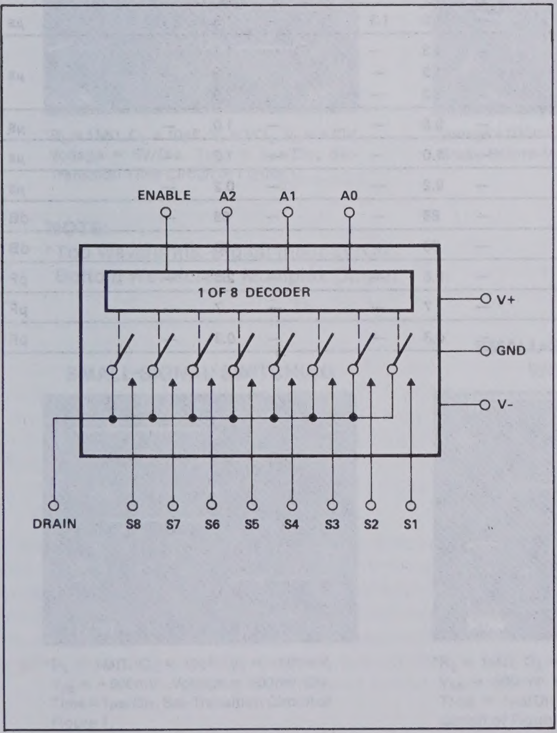
- **Compatible with Standards for Noise and Crosstalk in Telephony Systems**
- **Pin Compatible with DG508, HI-508A, LF11508**
- **JFET Switches Rather Than CMOS**
- **Low "ON" Resistance — 220Ω Typical**
- **Low Output Leakage Current — 100nA Max**
- **Digital Inputs Compatible with TTL and CMOS**
- **Input Overvoltage and Supply Loss Protected**

ORDERING INFORMATION†

R_{ON}	MODEL	TEMP RANGE
400Ω	MUX-88EQ	IND
520Ω	MUX-88FQ	IND

†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

FUNCTIONAL DIAGRAM



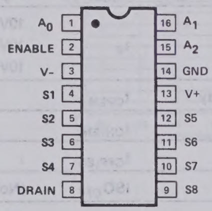
GENERAL DESCRIPTION

The MUX-88 is a monolithic eight-channel analog multiplexer ideally suited to shared-channel PCM CODEC systems. One-of-eight channels is selected upon the decoding of a 3 bit binary address. An enable input (E_n) disables all switches when logic low providing package select. All logic control inputs have true TTL input compatibility eliminating the need for pull-up resistors necessary for some CMOS equivalent products.

Fabricated with Precision Monolithics' high performance BIFET technology, this device offers low "ON" resistance, low leakage, fast settling time and excellent crosstalk isolation (98dB @ 20kHz). These characteristics make this device suitable for meeting system level communication requirements in shared-channel PCM CODEC's.

Additional ruggedization results from built-in overvoltage, supply loss, and latch-up free circuit characteristics.

PIN CONNECTIONS



TOP VIEW
16-PIN HERMETIC DUAL-IN-LINE
(Q-Suffix)

TRUTH TABLE

A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

ABSOLUTE MAXIMUM RATINGS ($T_A = 25°C$, unless otherwise noted)

Operating Temperature Range,	
MUX-88EQ, FQ	−25° C to +85° C
Storage Temperature Range	−65° C to +150° C
Power Dissipation	500mW
Derate above 100° C	10mW/° C
Lead Temperature (Soldering, 60 sec)	300° C
V+ Supply to V− Supply	36V
V+ Supply to Ground	18V
Logic Input Voltage (Note 5)	(V− or −4V) to V+
Analog Input Voltage	V− Supply −20V to V+ Supply +20V
Maximum Current Through Any Pin	25mA

ELECTRICAL CHARACTERISTICS for V+ = −15V and $-25°C \le T_A \le 85°C$, unless otherwise noted.

			MUX-88E			MUX-88F			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
"ON" Resistance	R_{ON}	$V_D = 0V, I_S = 200\mu A$	—	—	400	—	—	520	Ω
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$-10V \le V_D \le 10V, I_S = 200\mu A$	—	1.5	—	—	4.5	—	%
R_{ON} Match Between Switches	$R_{ON\ Match}$	$V_D = 0V, I_S = 200\mu A$	—	25	—	—	30	—	Ω
Source Current (Switch "OFF")	$I_{S(OFF)}$	$V_S = 10V, V_D = -10V$, (Note 1)	—	—	10	—	—	10	nA
Drain Current (Switch "OFF")	$I_{D(OFF)}$	$V_S = 10V, V_D = -10V$, (Note 1)	—	—	100	—	—	100	nA
Leakage Current (Switch "ON")	$I_{D(ON)} + I_{S(ON)}$	$V_D = 10V$, (Note 1)	—	—	100	—	—	100	nA
Digital "1" Input Voltage	V_{INH}		2	—	—	2	—	—	Volts
Digital "0" Input Voltage	V_{INL}		—	—	0.8	—	—	0.8	Volts
Digital Input Current	I_{IN}	$V_{IN} = 0.7V$ to $+5V$	—	—	20	—	—	20	μA
Digital "0" Enable Current	$I_{INL(EN)}$	$V_{EN} = 0.7V$	—	—	20	—	—	20	μA
Positive Supply Current	I+	All Digital Inputs Logic "0"	—	—	15	—	—	15	mA
Negative Supply Current	I−	All Digital Inputs Logic "0"	—	—	5	—	—	5	mA
Switching Time	t_{TRAN}	Figure 1, (Note 2)	—	1.0	1.3	—	1.5	2.1	μs
Output Settling Time	t_S	10V Step 0.10%	—	1.3	—	—	1.7	—	μs
		10V Step 0.05%	—	1.5	—	—	1.9	—	
		10V Step 0.02%	—	2.3	—	—	2.5	—	
Break-Before-Make Delay	t_{OPEN}		—	0.8	—	—	1.0	—	μs
Enable Delay "ON"	$t_{ON(EN)}$		—	1.0	—	—	1.2	—	μs
Enable Delay "OFF"	$t_{OFF(EN)}$		—	0.2	—	—	0.2	—	μs
"OFF" Isolation	ISO_{OFF}	(Note 4)	—	88	—	—	88	—	dB
Crosstalk	CT	(Note 3)	—	98	—	—	98	—	dB
Source Capacitance	$C_{S(OFF)}$	Switch "OFF", $V_S = 0V, V_D = 0V$	—	2.5	—	—	2.5	—	pF
Drain Capacitance	$C_{D(OFF)}$	Switch "OFF", $V_S = 0V, V_D = 0V$	—	7	—	—	7	—	pF
Input to Output Capacitance	$C_{DS(OFF)}$	(Note 4)	—	0.3	—	—	0.3	—	pF

NOTES:

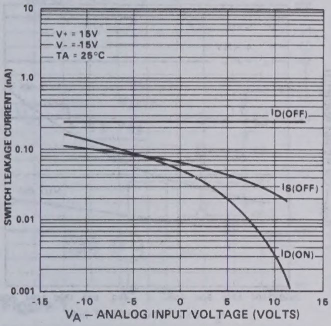
1. Conditions applied to leakage tests insure worst case leakages. Exceeding 11V on the analog input may cause an "OFF" channel to turn "ON".
2. Sample tested. The measurement conditions of Figure 1 insure worst case transition time.
3. Crosstalk is measured by driving channel 8 with channel 4 ON. $R_L = 1M\Omega$, $C_L = 10pF$, $V_S = 5V$ RMS, f = 20kHz. (See Figure 2)
4. OFF isolation is measured by driving channel 8 with ALL channels OFF. $R_L = 1k\Omega$, $C_L = 10pF$, $V_S = 5V$ RMS, f = 20kHz. C_{DS} is computed from the OFF isolation measurement.

DICE

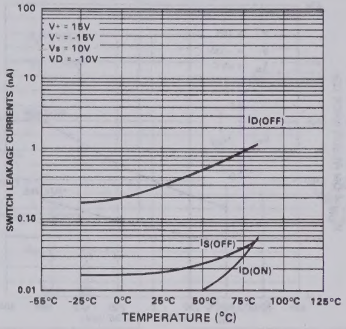
For applicable DICE information see MUX-08/MUX-24 data sheet.

TYPICAL PERFORMANCE CHARACTERISTICS

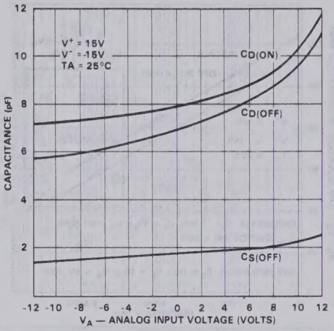
SWITCH LEAKAGE CURRENTS vs ANALOG INPUT VOLTAGE



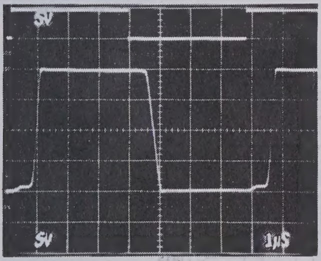
SWITCH LEAKAGE CURRENTS vs TEMPERATURE



SWITCH CAPACITANCE vs ANALOG INPUT VOLTAGE

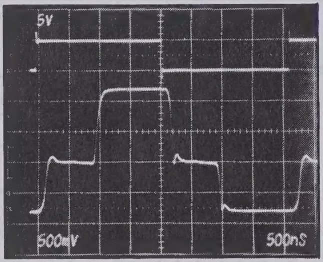


LARGE-SIGNAL SWITCHING



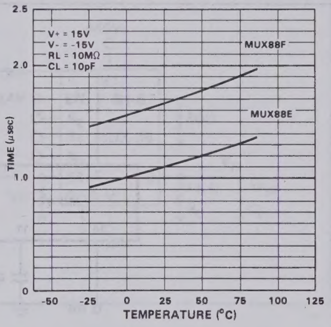
*$R_L = 1M\Omega$, $C_L = 10pF$, $V_1 = VO_L$, $V_8 = +10V$ Voltage = 5V/Div, Time = 1μs/Div, See Transition Time Circuit of Figure 1.

BREAK-BEFORE-MAKE SWITCHING



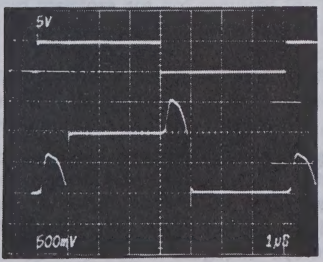
*Voltage = 500mV/Div, Time = 500ns/Div, See Break-Before-Make Circuit of Figure 3.

TRANSITION TIMES vs TEMPERATURE



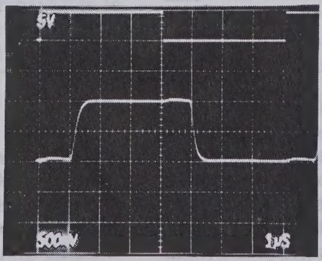
NOTE:
*Top Waveforms: Digital Input 5V/Div
Bottom Waveforms: Multiplex Output

SMALL-SIGNAL SWITCHING



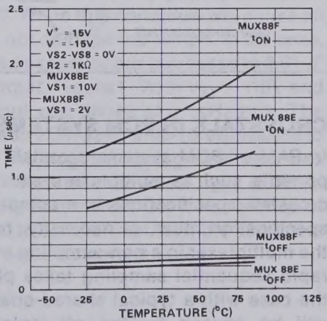
*$R_L = 1M\Omega$, $C_L = 10pF$, $V_1 = -500mV$, $V_{S8} = +500mV$ Voltage = 500mV/Div, Time = 1μs/Div, See Transition Circuit of Figure 1.

SMALL-SIGNAL SWITCHING WITH FILTERING



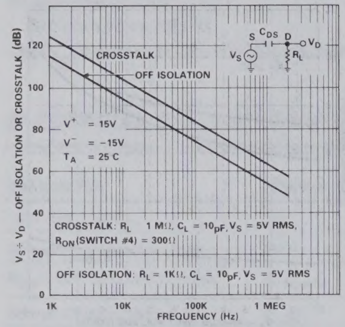
*$R_L = 1M\Omega$, $C_L = 500pF$, $V_1 = -500mV$, $V_{S8} = 500mV$ Voltage = 500mV/Div, Time = 1μs/Div, See Transition Time Circuit of Figure 1.

ENABLE DELAY TIME vs TEMPERATURE

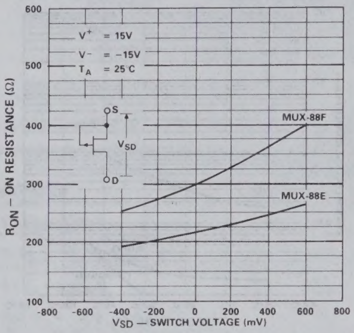


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

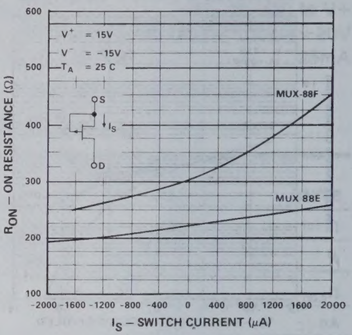
OFF PERFORMANCE OF CHANNEL 8



R_{ON} vs SWITCH VOLTAGE (V_{SD})

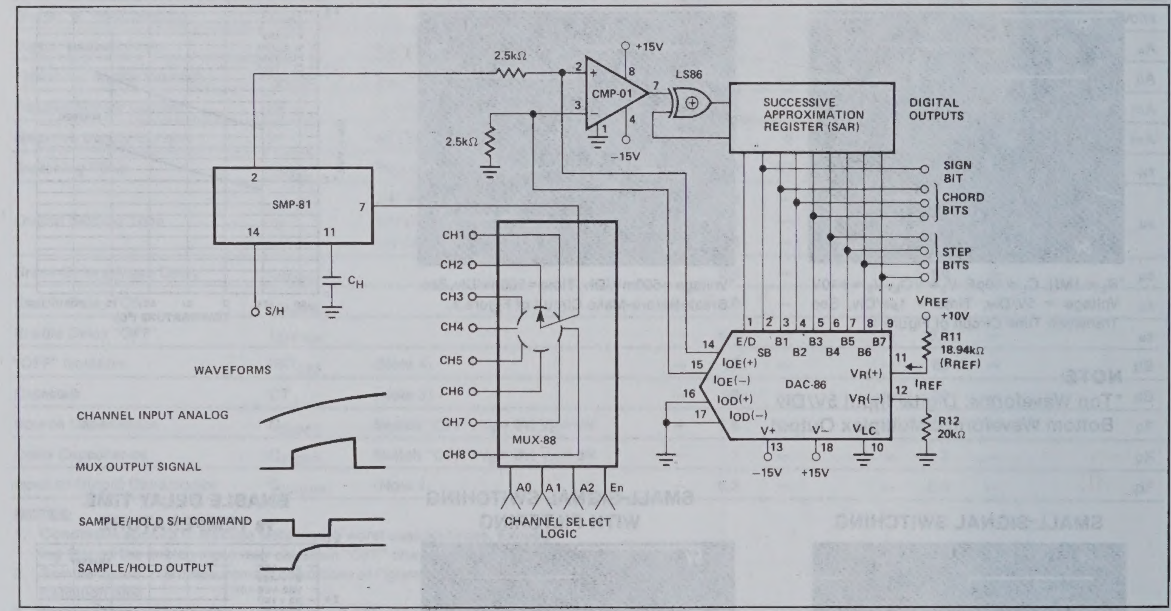


R_{ON} vs SWITCH CURRENT (I_S)



TYPICAL APPLICATION

EIGHT-CHANNEL SHARED CODEC PCM ENCODER


2.5kΩ
2.5kΩ
+15V
−15V
CMP-01
2
3
8
7
1
4
LS86
SUCCESSIVE APPROXIMATION REGISTER (SAR)
DIGITAL OUTPUTS
SIGN BIT
CHORD BITS
STEP BITS
SMP-81
2
7
14
11
CH
S/H
CH1
CH2
CH3
CH4
CH5
CH6
CH7
CH8
MUX-88
A0
A1
A2
En
CHANNEL SELECT LOGIC
DAC-86
E/D
B1
B3
B5
B7
SB
B2
B4
B6
IOE(+)
IOE(−)
IOD(+)
IOD(−)
VR(+)
VR(−)
V+
V−
VLC
1
2
3
4
5
6
7
8
9
14
15
16
17
11
12
13
18
10
−15V
+15V
VREF
+10V
R11
18.94kΩ
(RREF)
IREF
R12
20kΩ
WAVEFORMS
CHANNEL INPUT ANALOG
MUX OUTPUT SIGNAL
SAMPLE/HOLD S/H COMMAND
SAMPLE/HOLD OUTPUT

CROSSTALK IN PCM SYSTEMS

In PAM or PCM systems crosstalk specifications for components, such as multiplexers, are related to overall system crosstalk specifications in a complex manner. Component specification must, of necessity, refer to the operation of the multiplexer in a non-sampling mode of operation. When rapid sequential sampling takes place, such as would be the case with a typical shared-channel CODEC, crosstalk will be caused by the off isolation properties of the multiplexer as well as by storage elements on chip and PC card stray capacitance. For example, the capacitance has the effect of conferencing the channels and increasing crosstalk. Thus, system crosstalk in a shared-channel PCM CODEC is influenced by multiplexed characteristics as well as PC card layout and the timing relationship between the multiplexer and the sample-hold circuit.

A.C. TEST CIRCUITS

TRANSITION TIME

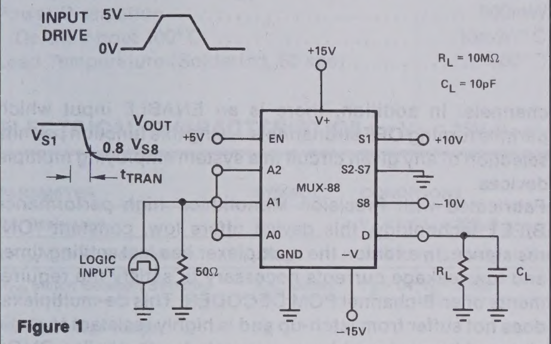

INPUT DRIVE
5V
0V
+15V
R_L = 10MΩ
C_L = 10pF
V_S1
V_OUT
0.8 V_S8
t_TRAN
+5V
EN
A2
A1
A0
V+
MUX-88
GND
S1
S2-S7
S8
D
−V
+10V
−10V
LOGIC INPUT
50Ω
R_L
C_L
−15V

Figure 1

CROSSTALK MEASUREMENT CIRCUIT

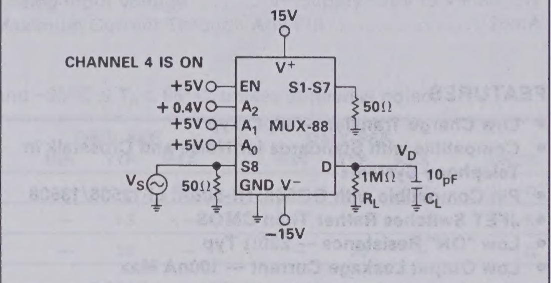

15V
CHANNEL 4 IS ON
+5V
+0.4V
+5V
+5V
EN
A2
A1
A0
S8
V+
S1-S7
MUX-88
D
GND V−
50Ω
V_D
1MΩ
10pF
R_L
C_L
V_S
50Ω
−15V

Figure 2

BREAK-BEFORE-MAKE DELAY

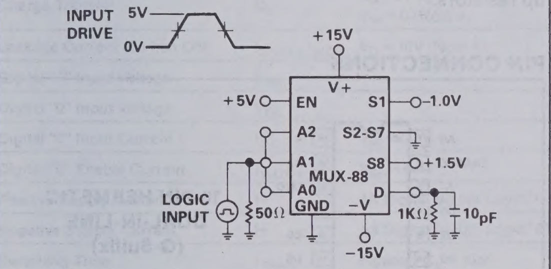

INPUT DRIVE
5V
0V
+15V
+5V
EN
A2
A1
A0
GND
V+
MUX-88
S1
S2-S7
S8
D
−V
−1.0V
+1.5V
LOGIC INPUT
50Ω
1KΩ
10pF
−15V

Figure 3

OFF ISOLATION MEASUREMENT CIRCUIT

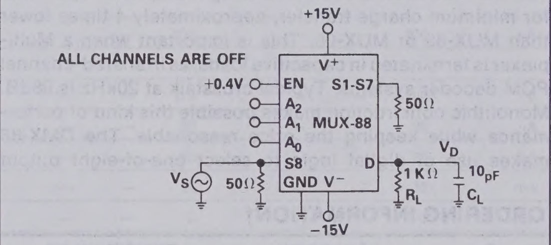

+15V
ALL CHANNELS ARE OFF
+0.4V
EN
A2
A1
A0
S8
V+
S1-S7
MUX-88
D
GND V−
50Ω
V_D
1KΩ
10pF
R_L
C_L
V_S
50Ω
−15V

Figure 4

APPLICATIONS INFORMATION

These analog multiplexers employ ion-implanted JFETs in a switch configuration designed to assure break-before-make action. The turn-off time is much faster than the turn-on time to guarantee this feature over the full operating temperature and input voltage range. Because the digital inputs only require a 2V logic "1" input level, power-consuming pull-up resistors are not required for TTL compatibility to insure break-before-make switching as is most often the case with CMOS multiplexers. The digital inputs utilize PNP input transistors where input current is maximum at the logic "0" level and drops to that of a reverse-biased diode (about 10nA) as the input voltage is raised above ≈ 1.4V.

The "ON" resistance, R_{ON}, of the analog switches is constant over the wide input voltage range of −15V to +11V with $V_{SUPPLY} = \pm 15V$. Higher input voltage is tolerable provided that some form of current limiting is employed (such as that of an op-amp output stage) to avoid exceeding junction temperature and power dissipation requirements. For normal operation, however, positive input voltages should be restricted to 11V (or 4V less than the positive supply). This assures that the V_{GS} of an OFF switch remains greater than its V_P, and prevents that channel from being falsely turned ON.

When operating with negative input voltages, the gate-to-channel diode will be turned on if the voltage drop across an ON switch exceeds −0.6V. While this condition will cause an error in the output, it will not damage the switch. In lab tests, the multiplexer output load capacitor has increased to 0.01μF in the Transition Time circuit, Figure 1. With $V_{S1} = -10V$ and $V_{S8} = +10V$, the logic input was driven at a 1kHz rate. The positive-going slew rate was 0.3V/μsec which is equivalent to a normal I_{DSS} of 3mA. The negative-going slew rate was 0.7V/μsec which is equivalent to a "reverse" I_{DSS} of 7mA. Note that when switch 1 is first turned ON it has a drop of −20V across its terminals. In spite of that fact, the current is limited to approximately twice its normal I_{DSS}.

DMX-88

8-CHANNEL ANALOG DE-MULTIPLEXER (LOW CHARGE TRANSFER)

FEATURES

- **Low Charge Transfer — 18pC Typ**
- **Compatible with Standards for Noise and Crosstalk in Telephony Systems**
- **Pin Compatible with DG508, HI-508A, LF12508/13508**
- **JFET Switches Rather Than CMOS**
- **Low "ON" Resistance — 220Ω Typ**
- **Low Output Leakage Current — 100nA Max**
- **Digital Inputs Compatible with TTL and CMOS**
- **No Pull-up Resistors Required to Ensure Break-Before-Make Action with TTL Inputs**

GENERAL DESCRIPTION

The DMX-88 is an 8-channel analog multiplexer optimized for minimum charge transfer, approximately 4 times lower than MUX-88 or MUX-08. This is important when a Multiplexer is terminated in capacitive loads, as in shared-channel PCM decoder systems. Typical crosstalk at 20kHz is 98dB. Monolithic construction makes possible this kind of performance while keeping the price reasonable. The DMX-88 makes use of digital logic to select one-of-eight output channels. In addition, there is an ENABLE input which permits turning OFF all channels. Using this function permits selection of any given circuit in a system employing multiple devices.

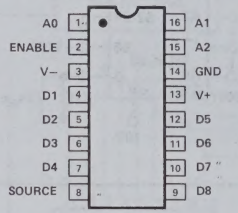
Fabricated with Precision Monolithics' high performance BIFET technology, this device offers low, constant "ON" resistance. In addition the multiplexer has fast settling times and low leakage currents necessary to satisfy the requirements of an 8-channel PCM DECODER. This de-multiplexer does not suffer from latch-up and is highly resistant to static charge blow-out problems associated with similar CMOS parts. The digital inputs are designed to operate from both TTL and CMOS levels while always providing a definite break-before-make action without the need for external pull-up resistors.

ORDERING INFORMATION†

R_{ON}	MODEL	TEMP RANGE
400Ω	DMX88EQ	IND
520Ω	DMX88FQ	IND

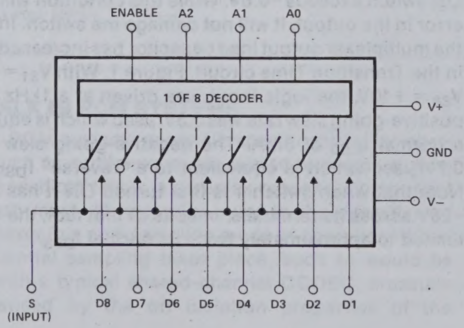
†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

PIN CONNECTIONS



16-PIN HERMETIC DUAL-IN-LINE (Q-Suffix)

FUNCTIONAL DIAGRAM & TRUTH TABLE



A_2	A_1	A_0	E_N	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

"X" = DON'T CARE

ABSOLUTE MAXIMUM RATINGS ($T_A = 25°C$, unless otherwise noted.)

Operating Temperature Range,
DMX-88EQ, FQ .... −25°C to +85°C
Storage Temperature Range .... −65°C to +150°C
Power Dissipation 500mW
Derate About 100°C .... 10mW/°C
Lead Temperature (Soldering, 60 sec) .... 300°C
V+ Supply to V− Supply 36V
V+ Supply to Ground 18V
Logic Input Voltage .... −4V to V+ Supply
Analog Input Voltage ...... V− Supply −20V to V+ Supply
Maximum Current Through Any Pin 25mA

ELECTRICAL CHARACTERISTICS for $V+ = 15V$, $V- = -15V$ and $-25°C \le T_A \le 85°C$, unless otherwise noted.

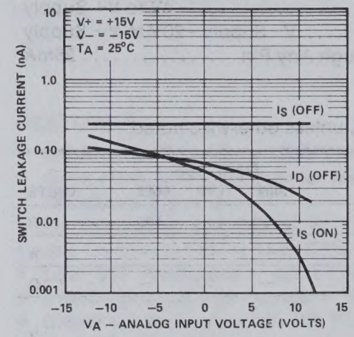
PARAMETER	SYMBOL	CONDITIONS	DMX-88E MIN	DMX-88E TYP	DMX-88E MAX	DMX-88F MIN	DMX-88F TYP	DMX-88F MAX	UNITS
ON Resistance	R_{ON}	$V_D = 0V$, $I_S = 200\mu A$	—	—	400	—	—	520	Ω
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$-10V \le V_D \le 10V$, $I_S = 200\mu A$	—	1.5	—	—	4.5	—	%
R_{ON} Match Between Switches	R_{ON} Match	$V_D = 0V$, $I_S = 200\mu A$	—	25	—	—	30	—	Ω
Analog Voltage Range	V_A		10 −10	+11 −15	— —	+10 −10	+11 −15	— —	V
Drain Current (Switch OFF)	$I_{D(OFF)}$	$V_S = 10V$, $V_D = -10V$ (Note 1)	—	—	10	—	—	10	nA
Source Current (Switch OFF)	$I_{S(OFF)}$	$V_S = 10V$, $V_D = -10V$ (Note 1)	—	—	100	—	—	100	nA
Charge Transfer	Q_t	$R_S = 0$, $C_L = 200pF$ $V_{IN} = 0$ (Note 4)	—	18	25	—	18	25	pC
Leakage Current (Switch ON)	$I_{D(ON)}+I_{S(ON)}$	$V_D = 10V$ (Note 1)	—	—	100	—	—	100	nA
Digital "1" Input Voltage	V_{INH}		2	—	—	2	—	—	V
Digital "0" Input Voltage	V_{INL}		—	—	0.8	—	—	0.8	V
Digital "0" Input Current	I_{INL}	$V_{IN} = 0.7V$	—	—	20	—	—	20	μA
Digital "0" Enable Current	$I_{INL(EN)}$	$V_{EN} = 0.7V$	—	—	20	—	—	20	μA
Positive Supply Current	I+	All Digital Inputs Logic "0"	—	—	15	—	—	15	mA
Negative Supply Current	I−	All Digital Inputs Logic "0"	—	—	5	—	—	5	mA
Switching Time	t_{TRAN}	Figure 1 $C_L = 10pF$	—	0.8	—	—	1.5	—	μs
Output Settling Time	t_S	10V Step 0.10% 10V Step 0.05% 10V Step 0.02%	— — —	1.3 1.5 2.3	— — —	— — —	1.7 1.9 2.5	— — —	μs
Break-Before-Make Delay	t_{OPEN}	Figure 3	—	0.8	—	—	1	—	μs
Enable Delay ON	$t_{ON(EN)}$	$C_L = 10pF$ (Figure 1)	—	1	—	—	1.2	—	μs
Enable Delay OFF	$t_{OFF(EN)}$	$C_L = 10pF$ (Figure 1)	—	0.2	—	—	0.2	—	μs
OFF Isolation	$ISO_{(OFF)}$	(Note 3)	—	88	—	—	88	—	dB
Crosstalk	CT	(Note 2)	—	98	—	—	98	—	dB
Drain Capacitance	$C_{D(OFF)}$	Switch OFF, $V_S = 0V$, $V_D = 0V$	—	2.5	—	—	2.5	—	pF
Source Capacitance	$C_{S(OFF)}$	Switch OFF, $V_S = 0V$, $V_D = 0V$	—	7	—	—	7	—	pF
Input to Output Capacitance	$C_{DS(OFF)}$	(Note 3)	—	0.3	—	—	0.3	—	pF

NOTES:

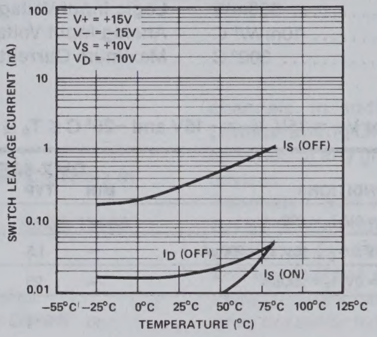
1. Conditions applied to leakage tests insure worst case leakages. Exceeding 11V on the analog input may cause an OFF channel to turn ON.
2. Crosstalk is measured by driving channel 8 with channel 4 ON. $R_L = 1M\Omega$, $C_L = 10pF$, $V_S = 5V$ RMS, f = 20kHz. (see figure 2)
3. OFF isolation is measured by monitoring channel 8 with ALL channels OFF. $R_L = 1k\Omega$, $C_L = 10pF$, $V_S = 5V$ RMS, f = 20kHz. C_{DS} is computed from the OFF isolation measurement. (see figure 4)
4. Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

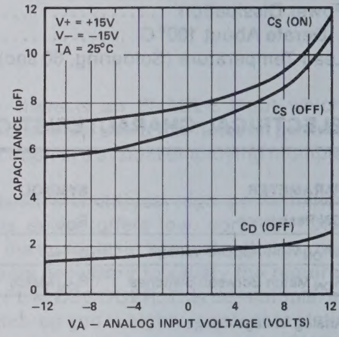
SWITCH LEAKAGE CURRENTS vs ANALOG INPUT VOLTAGE



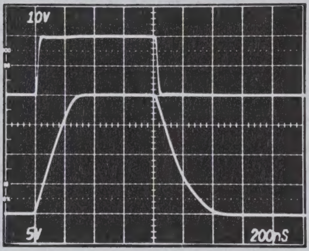
SWITCH LEAKAGE CURRENTS vs TEMPERATURE



SWITCH CAPACITANCE vs ANALOG INPUT VOLTAGE

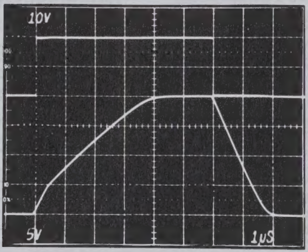


LARGE-SIGNAL TRANSIENT RESPONSE (THROUGH A CLOSED SWITCH)



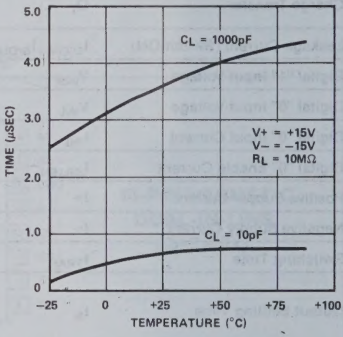
R_L = 1MΩ, C_L = 100pF, V_{IN} = ±10V

LARGE-SIGNAL TRANSIENT RESPONSE (THROUGH A CLOSED SWITCH)

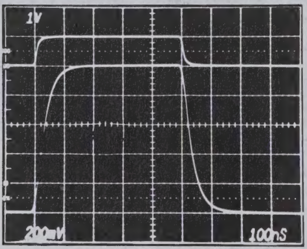


R_L = 1MΩ, C_L = 1000pF, V_{IN} = ±10V

SWITCHING TIME vs TEMPERATURE

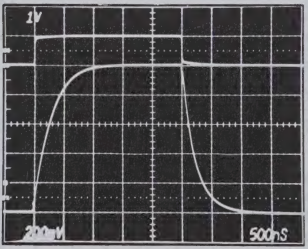


SMALL-SIGNAL TRANSIENT RESPONSE (THROUGH A CLOSED SWITCH)



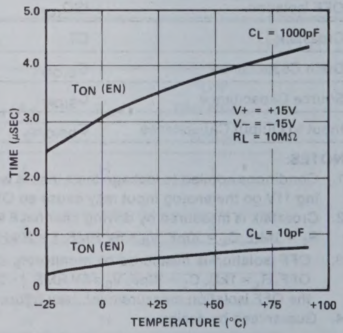
R_L = 1MΩ, C_L = 100pF, V_{IN} = ±0.5V

SMALL-SIGNAL TRANSIENT RESPONSE (THROUGH A CLOSED SWITCH)



R_L = 1MΩ, C_L = 1000pF, V_{IN} = ±0.5V

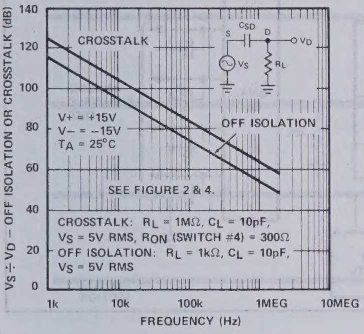
ENABLE DELAY TIME vs TEMPERATURE



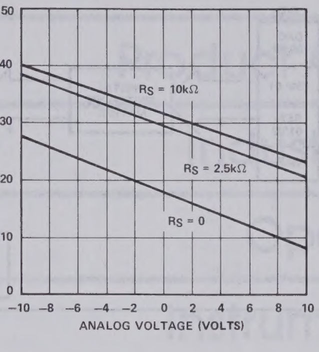
NOTE:
Upper Waveform Photos: Input Voltage on SOURCE
Lower Waveform Photos: Output Voltage on DRAIN

TYPICAL PERFORMANCE CHARACTERISTICS

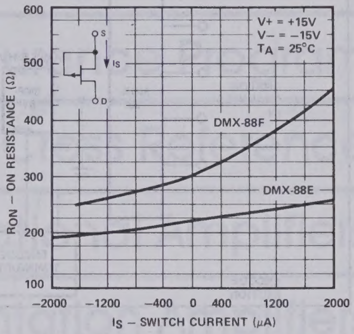
CROSSTALK AND OFF ISOLATION PERFORMANCE OF CHANNEL 8



CHARGE INJECTION vs ANALOG VOLTAGE



RON vs SWITCH CURRENT (IS)



A.C. TEST CIRCUITS

ENABLE DELAY TIME $t_{ON(EN)}$, $t_{OFF(EN)}$

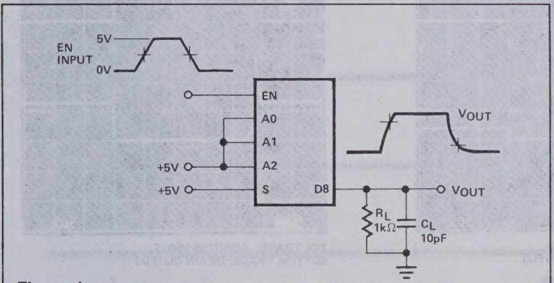

EN INPUT
5V
0V
EN
A0
A1
A2
S
D8
+5V
+5V
VOUT
VOUT
RL 1kΩ
CL 10pF

Figure 1

SWITCHING TIME t_{TRAN}, t_{OPEN}

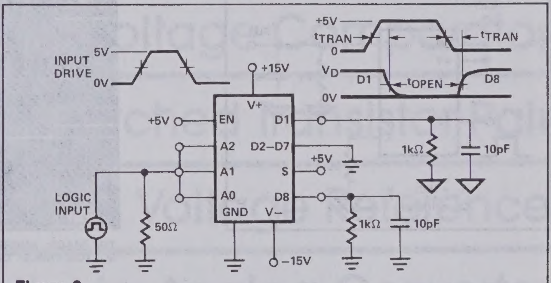

INPUT DRIVE
5V
0V
+5V
tTRAN
0
tTRAN
VD
D1
tOPEN
D8
0V
+15V
V+
+5V
EN
D1
A2
D2–D7
+5V
A1
S
A0
D8
GND
V–
LOGIC INPUT
50Ω
1kΩ
10pF
1kΩ
10pF
–15V

Figure 3

CROSSTALK MEASUREMENT CIRCUIT

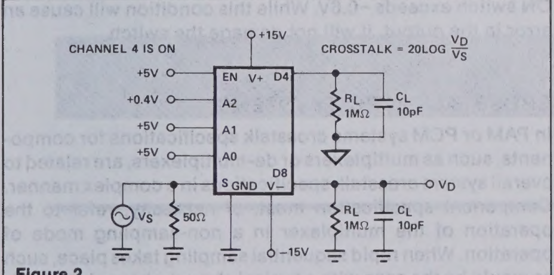

CHANNEL 4 IS ON
+15V
CROSSTALK = 20LOG VD/VS
+5V
EN
V+
D4
+0.4V
A2
+5V
A1
+5V
A0
RL 1MΩ
CL 10pF
D8
S
GND
V–
VD
VS
50Ω
RL 1MΩ
CL 10pF
–15V

Figure 2

OFF ISOLATION MEASUREMENT CIRCUIT

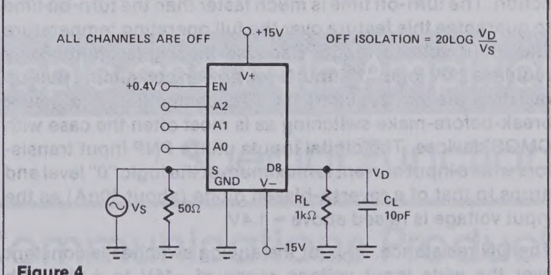
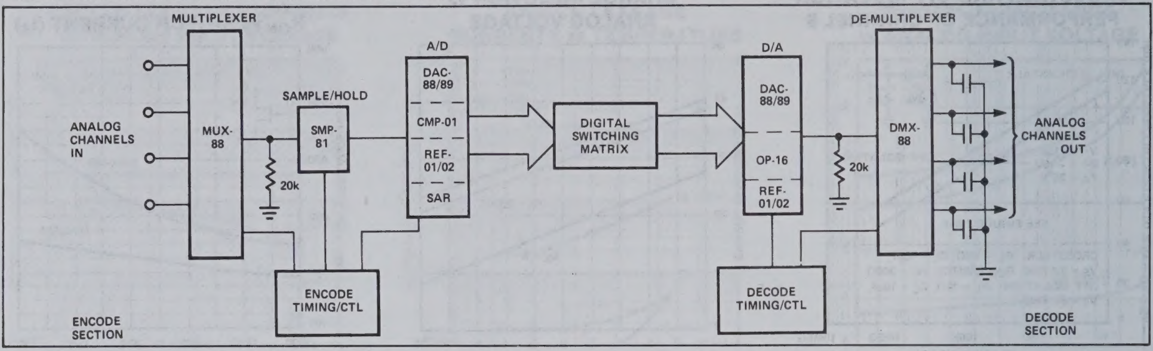

ALL CHANNELS ARE OFF
+15V
OFF ISOLATION = 20LOG VD/VS
V+
+0.4V
EN
A2
A1
A0
S
D8
GND
V–
VD
VS
50Ω
RL 1kΩ
CL 10pF
–15V

Figure 4

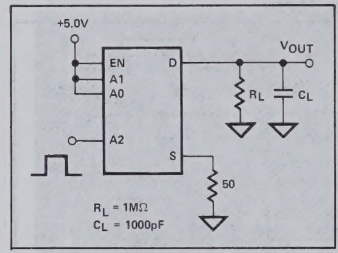
TYPICAL APPLICATION

FOUR-CHANNEL SHARED CHANNEL PCM CODEC

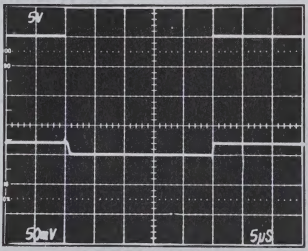


CHARGE TRANSFER

TEST CIRCUIT

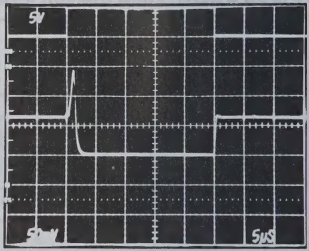


TYPICAL CHARGE TRANSFER OF DMX-88



TOP TRACE: ADDRESS INPUT
BOTTOM TRACE: DRAIN OUTPUT

TYPICAL CHARGE TRANSFER OF CONVENTIONAL BIFET SWITCH



TOP TRACE: ADDRESS INPUT
BOTTOM TRACE: DRAIN OUTPUT

APPLICATIONS INFORMATION

These de-multiplexers employ ion-implanted JFETs in a switch configuration designed to assure break-before-make action. The turn-off time is much faster than the turn-on time to guarantee this feature over the full operating temperature and input voltage range. Because the digital inputs only require a 2.0V logic "1" input level, power-consuming pull-up resistors are not required for TTL compatibility to insure break-before-make switching as is most often the case with CMOS devices. The digital inputs utilize PNP input transistors where input current is maximum at the logic "0" level and drops to that of a reverse-biased diode (about 10nA) as the input voltage is raised above ≈ 1.4V.

The ON resistance, R_{ON}, of the analog switches is constant over the wide input voltage range of −15V to +11V with $V_{SUPPLY} = \pm 15V$. Higher input voltage is tolerable provided that some form of current limiting is employed (such as that of an op-amp output stage) to avoid exceeding junction temperature and power dissipation requirements. For normal operation, however, positive input voltages should be restricted to 11V (or 4V less than the positive supply). This assures that the V_{GS} of an OFF switch remains greater than its V_P, and prevents that channel from being falsely turned ON.

When operating with negative input voltages, the gate-to-channel diode will be turned on if the voltage drop across an ON switch exceeds −0.6V. While this condition will cause an error in the output, it will not damage the switch.

CROSSTALK IN PCM SYSTEMS

In PAM or PCM systems crosstalk specifications for components, such as multiplexers or de-multiplexers, are related to overall system crosstalk specifications in a complex manner. Component specification must, of necessity, refer to the operation of the multiplexer in a non-sampling mode of operation. When rapid sequential sampling takes place, such as would be the case with a typical shared-channel CODEC, crosstalk will be caused by the off isolation properties of the multiplexer as well as by storage elements on chip and PC card stray capacitance. For example, the capacitance has the effect of conferencing the channels and increasing crosstalk. Thus, system crosstalk in a shared-channel PCM CODEC is influenced by multiplexed characteristics as well as PC card layout and the timing relationship between the multiplexer and the sample-hold circuit.

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Telecommunications Sample-and-Hold Amplifier

SAMPLE-AND-HOLD AMPLIFIERS

INTRODUCTION

Sample-and-hold amplifiers "sample" an analog input signal and then "hold" the instantaneous input value upon the command of a logic control signal. Basically the sample-and-hold is an "analog memory" where a capacitor serves as the storage element. Applications in which a time varying input cannot be tolerated require sample-and-hold circuits. A fast successive-approximation analog-to-digital converter is one application. Data acquisition, data distribution, analog delay and telephony require sample-hold circuits to "freeze" the analog signal for further signal processing.

PMI sample-and-hold amplifiers are functionally identical to track-and-hold circuits. They continously track input signals during the sample mode. PMI circuits should not be confused with AC controlled sample-and-holds. When an AC controlled sample-and-hold is commanded to sample, it will take a fast sample and immediately return to the hold mode. It can not continously track an input signal.

A sample-and-hold circuit consists of an amplifier, switch, and capacitor. Many specifications are similar to those of switches and operational amplifiers — bias currents, voltage gain, and charge injection are examples. These and other specifications pertaining uniquely to sample-and-hold circuits are defined below.

The SMP-10 and SMP-11 are precision sample-and-hold amplifiers with high accuracy, low droop rate, and fast signal acquisition time. These circuits contain a high impedance input buffer, a diode bridge switch, a transconductance or "Super-Charger" circuit to enhance slewing and a high speed output amplifier. The "Super-Charger" is capable of supplementing the capacitor charging current whenever the difference between input and output levels exceeds a given threshold. Settling to final value is under control of currents from the diode bridge, thus minimizing overshoot and instability. The inherent low offset voltage errors and low charge injection allows the residual zero-scale errors to be actively trimmed using PMI's zener-zapping technology without degrading temperature performance. "Super Beta" transistors provides the high input-impedace amplifier needed for low droop rate and minimal signal loading.

The SMP-10 and SMP-11 have different droop rate and settling hold mode times specifications.

The SMP-81 is characterized for the sampling requirements found in telecommunications applications.

In addition to precision sample-and-hold amplifiers, two products with related capabilities are available. The GAP-01 general purpose analog processor provides the user with two independently switched transconductance amplifiers, a unity gain buffer and an uncommitted voltage comparator. The GAP-01 is a non-dedicated functional block which has a wide variety of applications. The second device is the PKD-01 monolithic peak detector. This device performs the peak detector function with accuracies approaching those obtainable with high cost hybrid modules at a cost approaching the low cost, low performance discrete designs. Data sheets for the GAP-01 and PKD-01 are located in the SPECIAL FUNCTIONS SECTION of this catalog.

DEFINITIONS

Acquisition Time (t_{aq})— The minimum time for the output voltage to begin tracking the input voltage, to within a specified error band, after the inception of the sample command. By convention, acquisition time is defined for sampling of a DC level. For instance a circuit which is "holding" a 10V output signal, and operating with zero input volts, is switched to the sample mode. The acquisition time is then the time required for the output to decrease to within a ±10mV (0.01%FS) band about ground potential (see timing diagram).

Aperture Jitter (Δt_a) — The maximum amount of deviation in aperture time from sample to sample. Errors resulting from aperture jitter increase in proportion to the slew rate of the sampled analog input signal. Also called aperture uncertainty time.

Aperture Time (t_{ap}) — The time between the inception of the hold command and the time the circuit output ceases tracking the input signal (see timing diagram).

Change In Hold Step (ΔV_{HS})— Actual hold step less the hold step measured after sampling $V=0$. A change in hold step has two components: the first is a function of input voltage, the second is a function of the rise time of the S/H voltage. Note that rise time of S/H voltage $dV_{(S/H)}/dt$ also effects ZERO-SCALE ERROR.

Charge Transfer (Q_t) — The amount of charge transferred to the holding capacitor due to the action of the switch. Charge is transferred to C_H when the circuit is switched to the hold mode. Charge transfer causes a change in output voltage ΔV_{ZS} as defined by the equation:

$$\Delta V_{ZS}(V) = \frac{Q_t(pC)}{C_H(pF)}$$

Note that for $Q_t = 5pC$ and $C_H = 5000pF$ offset error $= 1mV$. The SMP-10/11/81 has been factory nulled for $C_H = 5000pF$. For other values of C_H the zero-scale shift can be calculated from the equation:

$$\Delta V_{ZS}(V) = \frac{Q_t}{C_H} - 1mV$$

Droop Rate (dV_{CH}/dt) — Droop rate dV_{CH}/dt is the rate of change of output voltage while the circuit is in the hold mode. dV_{CH}/dt is a direct function of droop current I_{DR}:

$$\frac{dV_{CH}}{dt} = \frac{I_{DR}}{C_H}$$

where dV_{CH}/dt is expressed in $\mu V/ms$, I_{DR} in nanoamperes and C_H in microfarads (see timing diagram).

Feedthrough Attenuation Ratio (F_A) — Feedthrough attenuation is a measurement of the off-isolation of the analog switch (specified in dB). The parameter is a direct function of feedthrough capacitance.

Full Power Bandwidth (F_p) — The maximum frequency at which rated output voltage E_p can be supplied without significant distortion. Full power bandwidth F_p is related to slew rate SR by the following equation:

$$F_p = \frac{SR}{2\pi E_p}$$

Using this equation F_p of 160kHz can be computed. This is applicable only for pulsed conditions. Power dissipation limits F_p to 100kHz for C.W. operation.

Gain Error — Voltage difference between input and output voltage measured over a specified voltage range, assuming the ideal gain is unity.

Hold Capacitor Charging Current (I_{CH}) — The current I_{CH} which charges, or discharges, the hold capacitor C_H while the circuit is in the sample mode.

Hold Mode Settling Time (t_{Hm}) — The time for all output transients to settle within a specified error band. Measured from the inception of the hold command (see timing diagram).

Hold Step (V_{HS}) — Magnitude of step caused in the output voltage by switching the circuit from sample mode to hold mode. Hold step is sometimes called pedestal error, or sample to hold offset (see timing diagram).

Input Bias Current (I_B) — Input terminal current with input voltage held at zero volts.

Input Resistance (R_{IN}) — AC impedance measured as a ratio of input voltage V_{IN} to input current I_{IN}.

Leakage (Droop) Current (I_{DR}) — The current which flows out of holding capacitor C_H while the circuit is operating in the hold mode. In general droop current I_{DR} is defined positive when its direction is into the C_H pin. This parameter is sometimes called drift current.

Linearity Error — The maximum deviation from an ideal straight line drawn between the output voltage when $V_{IN} = 0$ and the output voltage when V_{IN} = maximum analog voltage, expressed as a percentage of the maximum analog voltage.

Output Resistance (R_o) — An AC change in output voltage as a result of an AC change in load current.

Power Supply Rejection Ratio (PSRR) — The change in output voltage for a change in power supply voltage when the circuit is in the sample mode. The best power supply rejection ratio PSRR is obtained with the power supply voltage changing at a very low rate (DC). For essentially DC conditions PSRR for the hold mode of operation is essentially the same as the PSRR for the sample mode. PSRR is degraded as the frequency of the disturbance increases.

Sample Hold Current Ratio (I_{CH}/I_{DR}) — The ratio of the peak charging current available to the droop current.

Signal Transfer Nonlinearity — The total input to output, hold mode error caused by gain nonlinearity, feedthrough, thermal transient, charge transfer and droop rate. These error terms cannot be corrected by offset and gain adjustments.

Slew Rate (SR) — The maximum possible rate of change of the output voltage when supplying the rated output. For a sample-and-hold circuit, slew rate must be defined with a specified value of holding capacitor C_H. Slew rate can either be measured by operating the circuit in the sample mode and applying a step function to the input, or by applying an input voltage which differs from the output voltage, with the circuit in the hold mode, then switching to the sample mode and observing the rate of change of the output voltage.

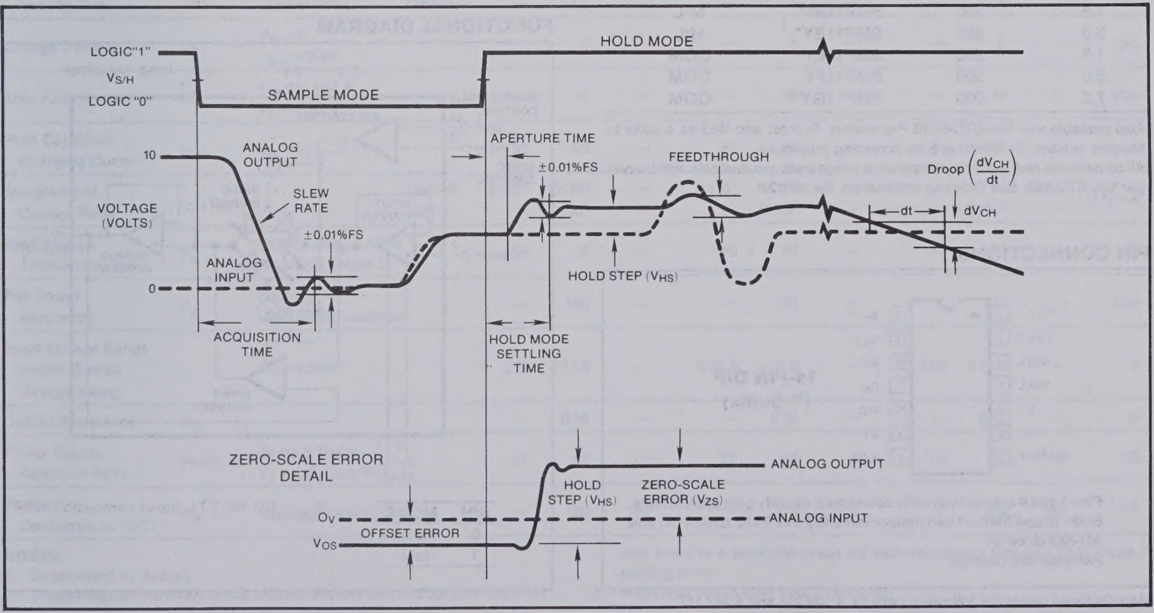
Total Error — The algebraic sum of the following factors:

i. ZERO-SCALE ERROR
ii. Gain Error
iii. Hold Step Change versus $\frac{dV_{(S/H)}}{dt}$
iv. Hold Step Change versus V_{IN}

Voltage Gain (A_V) — The ratio of the output voltage to the input voltage with the circuit operating in the sample mode.

Zero-Scale Error (V_{ZS}) — The magnitude of the output voltage when the circuit is switched from sample to hold mode while holding the input at zero volts. ZERO-SCALE ERROR V_{ZS} is the algebraic sum of the offset voltage and the charge transfer hold step voltage (see timing diagram). V_{ZS} can be adjusted to zero (see ZERO-SCALE ERROR null adjustment).

TIMING DIAGRAM


LOGIC "1"
$V_{S/H}$
LOGIC "0"
SAMPLE MODE
HOLD MODE
10
ANALOG OUTPUT
SLEW RATE
VOLTAGE (VOLTS)
±0.01%FS
ANALOG INPUT
0
ACQUISITION TIME
APERTURE TIME
±0.01%FS
FEEDTHROUGH
Droop $\left(\frac{dV_{CH}}{dt}\right)$
dt
dV_{CH}
HOLD STEP (V_{HS})
HOLD MODE SETTLING TIME
ZERO-SCALE ERROR DETAIL
ANALOG OUTPUT
HOLD STEP (V_{HS})
ZERO-SCALE ERROR (V_{ZS})
O_V
ANALOG INPUT
OFFSET ERROR
V_{OS}

SMP-10/SMP-11

LOW-DROOP-RATE/ ACCURATE SAMPLE-AND-HOLD AMPLIFIERS

FEATURES

SMP-10

- **Low Droop Rate 5.0μV/ms**
- **Low Signal Transfer Nonlinearity 0.005%**
- **High Sample/Hold Current Ratio 2x10⁹**

SMP-11

- **Low Droop Rate over Temperature 120μV/ms**
- **High Sample/Hold Current Ratio 1.7x10⁸**

BOTH SMP-10 AND SMP-11

- **Fast Acquisition Time, 10V Step to 0.1% 3.5μs**
- **High Slew Rate 10V/μs**
- **Low Aperture Time 50ns**
- **Trimmed for Minimum Zero-Scale Error 0.45mV**
- **Feedthrough Attenuation Ratio 96dB**
- **Low Power Dissipation 160mW**
- **DTL, TTL & CMOS Compatible Logic Input**
- **HA-2420, HA-2425, SHM-IC-1, and AD583 Socket Compatible**

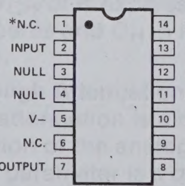
ORDERING INFORMATION†

$T_A = +25°C$		PACKAGE 14-PIN DIP	
V_{ZS} (mV)	DROOP RATE IN μV/ms	HERMETIC	OPERATING TEMPERATURE RANGE
1.5	20	SMP10AY*	MIL
3.0	50	SMP10BY*	MIL
1.5	20	SMP10EY	COM
3.0	50	SMP10FY	COM
1.5	200	SMP11AY*	MIL
3.0	500	SMP11BY*	MIL
1.5	200	SMP11EY	COM
3.0	500	SMP11FY	COM
7.0	900	SMP11GY	COM

*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

PIN CONNECTIONS



14-PIN DIP (Y-Suffix)

* Pins 1 and 8 are not internally connected, in unity gain applications, SMP-10 and SMP-11 can replace HA-2425, HA-2420, SHM-IC-1 and AD-583 directly.

** Sample/Hold Control

Manufactured under the following patents: 4,109,215 and 4,142,117.

GENERAL DESCRIPTION

The SMP-10/11 are precision sample-and-hold amplifiers that provide the high accuracy, the low droop rate and the fast acquisition time required in data acquisition and signal processing systems. Both devices are essentially noninverting unity gain circuits consisting of two very high input impedance buffer amplifiers connected together by a diode bridge switch.

HIGH ACCURACY AND LOW DROOP RATE

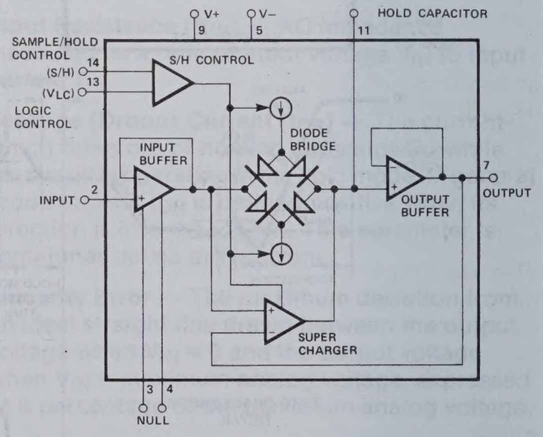
The high input impedance and the low droop rates of the SMP-10 and the SMP-11 are achieved by using bipolar Darlington circuits and an ion implant process that creates "super beta" transistors.

The output buffer's input stage converts to a super beta Darlington configuration during the hold mode, which results in a very low droop rate with no penalty in acquisition time. The use of bipolar transistors achieves a low change in droop rate over the operating temperature range.

FAST ACQUISITION

A unique super charger provides up to 50mA of charging current to the hold capacitor, which results in smooth, fast charging with minimum noise. As the hold capacitor voltage nears its final value, the low current diode bridge controls the final settling time. This unique combination of linear functions in a monolithic circuit enables the system designer to achieve superior performance.

FUNCTIONAL DIAGRAM



S/H	MODE
0	Sample
1	Hold

V_{LC} = 0V for TTL input compatibility.

ABSOLUTE MAXIMUM RATINGS (Note)

Supply Voltage (V+ minus V−)	36V
Power Dissipation	500mW
Derate Above 100°C	10mW/°C
Input Voltage	Equal to Supply Voltage
Logic and Logic Reference Voltage	Equal to Supply Voltage
Output Short-Circuit Duration	Indefinite
Hold Capacitor Short-Circuit Duration	60 sec
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C
Operating Temperature Range	
SMP-10AY, BY	−55°C to +125°C
SMP-10EY, FY	0°C to +70°C
SMP-11AY, BY	−55°C to +125°C
SMP-11EY, FY, GY	0°C to 70°C
DICE Junction Temperature (T_j)	−65°C to +150°C

NOTE: Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $C_H = 0.005\mu F$, V_{LC} connected to ground, $T_A = 25°C$, device fully warmed up, unless otherwise noted.

				SMP-10A/E SMP-11A/E			SMP-10B/F SMP-11B/F			SMP-11G		
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Zero-Scale Error (Hold Mode)	V_{ZS}	$V_{IN} = 0$ $V_{S/H} = 3.5V$, (Note 3)	—	0.45	1.5	—	0.60	3.0	—	1.5	7.0	mV
Input Bias Current	I_B	$V_{IN} = 0$	—	35	65	—	55	90	—	90	160	nA
Leakage (Droop) Current	I_{DR}	Device Warmed Up SMP-10 (See Note 2) SMP-11	— —	— —	0.10 1.00	— —	— —	0.25 2.50	— —	— —	— 4.5	nA
Droop Rate	dV_{CH}/dt	Device Warmed Up SMP-10 (See Note 2) SMP-11	— —	5 60	20 200	— —	5 70	50 500	— —	— 80	— 900	μV/ms
Input Resistance	R_{IN}	See Note 1	30	60	—	15	50	—	—	40	—	GΩ
Voltage Gain	A_V	Sample Mode $V_{IN} = \pm 10V$, $R_L = 5k\Omega$ or $V_{IN} = \pm 5V$, $R_L = 2.5k\Omega$	0.99963	0.99983	—	0.99953	0.99978	—	0.99940	0.99975	—	V/V
Acquisition Time	t_{aq}	10V step to within 10mV of final value (0.1%)	—	3.5	—	—	3.5	—	—	3.5	—	μs
		10V step to within 1.0mV of final value (0.01%)	—	5.0	—	—	5.0	—	—	5.0	—	μs
Aperture Time	t_{ap}		—	50	—	—	50	—	—	50	—	ns
Hold Mode Settling Time	t_{Hm}	Settling to 1mV SMP-10 of final value. SMP-11	— —	7 1.5	— —	— —	7 1.5	— —	— —	— 1.5	— —	μs
Charge Transfer	Qt	$V_{IN} = 0$ $V_{S/H} = 3.5V$	—	5	—	—	5	—	—	5	—	pC
Slew Rate	SR	$V_{IN} = \pm 10V$ $R_L = 2.5k\Omega$	—	10	—	—	10	—	—	10	—	V/μs
Hold Capacitor Charging Current	I_{CH}	$V_{IN} - V_{OUT} \geq \pm 3V$	30	50	—	20	50	—	—	50	—	mA
Sample/Hold Current Ratio	I_{CH}/I_{DR}	SMP-10 SMP-11	3×10^8 —	2×10^9 1.7×10^8	— —	8×10^7 —	8×10^8 1.5×10^8	— —	— —	— 1.5×10^8	— —	mA/mA
Feedthrough Attenuation Ratio	F_A	Input = $20V_{p-p}$ 1kHz $R_L = 5k\Omega$, (Note 1)	86	96	—	80	90	—	—	90	—	dB
Full Power Bandwidth	F_p	$\pm 10V_{p-p}$ (Dissipation Limited)	—	100	—	—	100	—	—	100	—	kHz
Input Voltage Range and/or Output Voltage Swing		$R_L = 2.5k\Omega$	±11	±11.5	—	±10.5	±11.5	—	±10.5	±11.5	—	V
Output Resistance	R_O		—	0.15	—	—	0.15	—	—	0.15	—	Ω
Power Supply Rejection Ratio	PSRR	Sample Mode $V_S = \pm 9V$ to $\pm 18V$	82	92	—	77	92	—	72	92	—	dB
Power Consumption (DC)	P_D	Sample Mode $V_{IN} = 0$	—	160	180	—	170	210	—	180	240	mW

NOTES:

1. Guaranteed by design.
2. These measurements are made with the devices warmed up. It can be seen that there is a selection trade off between droop rate and hold mode settling time.
3. Measured 500μs after hold command.

ELECTRICAL CHARACTERISTICS — SMP-10 ONLY at $V_S = \pm 15V$, $C_H = 0.005\mu F$, $V_{LC} = 0V$, $T_A = 25°C$, device fully warmed up, unless otherwise noted.

			SMP-10A/E			SMP-10B/F			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Hold Step	V_{HS}	$V_{IN} = 0$	−1.0	+1.5	+4.0	−3.0	+1.5	+6.0	mV
Linearity Error	NL	$V_{IN} = \pm 10V$, $R_L = 5k\Omega$	—	0.005	—	—	0.007	—	% of 10V
Output Noise	$E_{N(RMS)}$	Wideband Noise 100Hz to 100kHz Sample Mode	—	40	—	—	50	—	μV_{RMS}
Hold Mode Settling Time	t_{Hm}	Settling to 1mV of Final Value, $V_{IN} = 0V$	—	7	—	—	7	—	µs

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $C_H = 0.005\mu F$, V_{LC} connected to ground. $0°C \leq T_A \leq +70°C$, device fully warmed up, unless otherwise noted.

				SMP-10E SMP-11E			SMP-10F SMP-11F			SMP-11G			
PARAMETER	**SYMBOL**	**CONDITIONS**		**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Zero-Scale Error	V_{ZS}	$V_{IN} = 0$, $V_{S/H} = 3.5V$, (Note 3)		—	0.75	2.0	—	1.0	4.0	—	2.7	10	mV
Input Bias Current	I_B	$V_{IN} = 0V$		—	50	90	—	80	140	—	120	250	nA
Leakage (Droop) Current	I_{DR}	Device Warmed Up (See Note 2)	SMP-10	—	0.05	0.25	—	0.080	0.65	—	—	—	nA
			SMP-11	—	0.5	1.8	—	0.6	2.8	—	0.7	5	
Droop Rate	dV_{CH}/dt	Device Warmed Up (See Note 2)	SMP-10	—	10	50	—	16	130	—	—	—	µV/ms
			SMP-11	—	100	360	—	120	560	—	140	1000	
Voltage Gain	A_V	Sample Mode $V_{IN} = \pm 10V$, $R_L = 5k\Omega$ or $V_{IN} = \pm 5V$, $R_L = 2.5k\Omega$		0.99955	0.99976	—	0.99950	0.99972	—	0.99930	0.99970	—	V/V
Power Supply Rejection Ratio	PSRR	Sample Mode $V_S = \pm 9V$ to $\pm 18V$		80	90	—	75	80	—	70	90	—	dB
Logic Control Input Current	I_{LC}	$V_{LC} = 0V$		—	−1	−2	—	−1	−3	—	−1	−4	µA
Logic Input	$I_{S/H}$	Sample Mode $V_{S/H} = 0.6V$		—	−5	−15	—	−5	−15	—	−5	−15	µA
		Hold Mode $V_{S/H} = 5.0V$		—	0.2	—	—	0.2	—	—	0.2	—	nA
Differential Logic Threshold	V_{TH}			0.8	1.3	2.0	0.8	1.3	2.0	0.8	1.3	2.0	V

NOTES:

1. Guaranteed by design.
2. The measurements are made with the devices warmed up. It can be seen that there is a selection trade off between droop rate and hold mode settling time.
3. Measured 500µs after hold command.

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $C_H = 0.005\mu F$, V_{LC} connected to ground, $-55°C \le T_A \le +125°C$, device fully warmed up, unless otherwise noted.

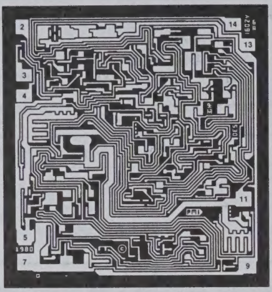
PARAMETER	SYMBOL	CONDITIONS		SMP-10A SMP-11A MIN	 TYP	 MAX	SMP-10B SMP-11B MIN	 TYP	 MAX	UNITS
Zero-Scale Error	V_{ZS}	$V_{IN} = 0$, $V_{S/H} = 3.5V$, (Note 3)		—	1.25	3.0	—	1.60	5.5	mV
Input Bias Current	I_B	$V_{IN} = 0V$		—	90	180	—	160	280	nA
Leakage (Droop) Current	I_{DR}	$T_A = -55°C$	SMP-10	—	0.050	0.50	—	0.080	1.22	nA
		$T_A = +125°C$		—	6	7.5	—	8	10	
		T_A = Full Range (See Note 2)	SMP-11	—	6	7.5	—	8	10	
Droop Rate	dV_{CH}/dt	$T_A = -55°C$	SMP-10	—	10	100	—	16	250	µV/ms
		$T_A = +125°C$		—	1200	1500	—	1600	2000	
		T_A = Full Range (See Note 2)	SMP-11	—	1200	1500	—	1600	2000	
Voltage Gain	A_V	Sample Mode $V_{IN} = \pm 10V$, $R_L = 5k\Omega$ or $V_{IN} = \pm 5V$, $R_L = 2.5k\Omega$		0.99950	0.99972	—	0.99940	0.99968	—	V/V
Power Supply Rejection Ratio	PSRR	Sample Mode $V_S = \pm 9V$ to $\pm 18V$		78	88	—	72	90	—	dB
Logic Control Input Current	I_{LC}	$V_{LC} = 0V$		—	−1	−3	—	−1	−5	µA
Logic Input	$I_{S/H}$	Sample Mode $V_{S/H} = 0.6V$		—	−5	−15	—	−5	−15	µA
		Hold Mode $V_{S/H} = 5.0V$		—	0.2	—	—	0.2	—	nA
Differential Logic Threshold	V_{TH}			0.8	1.3	2.0	0.8	1.3	2.0	V

NOTES:

1. Guaranteed by design.
2. These measurements are made with the devices warmed up. It can be seen that there is a selection trade off between droop rate and hold mode settling time.
3. Measured 500µs after hold command.

DICE CHARACTERISTICS

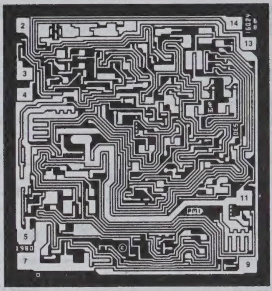
SMP-10



2. INPUT
3. NULL
4. NULL
5. NEGATIVE SUPPLY (SUBSTRATE)
7. OUTPUT
9. POSITIVE SUPPLY
11. HOLD CAPACITOR (C_H)
13. LOGIC THRESHOLD CONTROL (V_{LC})
14. SAMPLE/HOLD COMMAND

DIE SIZE 0.081 × 0.086 inch, 6966 sq. mils (2.057 × 2.184 mm, 4.772 sq. mm)

SMP-11



2. INPUT
3. NULL
4. NULL
5. NEGATIVE SUPPLY (SUBSTRATE)
7. OUTPUT
9. POSITIVE SUPPLY
11. HOLD CAPACITOR (C_H)
13. LOGIC THRESHOLD CONTROL (V_{LC})
14. SAMPLE/HOLD COMMAND

For additional DICE information refer to Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $C_H = 0.005\mu F$, V_{LC} connected to ground, $T_A = 25°C$, device fully warmed-up, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS		SMP-10N SMP-11N LIMIT	SMP-10G SMP-11G LIMIT	UNITS
Zero-Scale Error	V_{ZS}	$V_{IN} = 0$, $V_{S/H} = 3.5V$ Hold Mode, (Note 3)		1.5	3.0	mV MAX
Input Bias Current	I_B	$V_{IN} = 0V$		50	90	nA MAX
Leakage (Droop) Current	I_{DR}	Device Warmed Up	SMP-10	0.10	0.25	nA MAX
			SMP-11	1	2.5	
Droop Rate	I_{DR}	Device Warmed Up	SMP-10	20	50	μV/ms MAX
			SMP-11	200	500	
Voltage Gain	A_V	Sample Mode $V_{IN} = \pm 10V$ or $V_{IN} = \pm 5V$		0.99963	0.99953	V/V MIN
Hold Capacitor Charging Current	I_{CH}	$V_{IN} - V_{OUT} \geq \pm 3V$		30	20	mA MIN
Input Voltage Range and/or Output Voltage Swing		$R_L = 2.5k\Omega$		±11	±10.5	V MIN
Power Supply Rejection Ratio	PSRR	Sample Mode $V_S = \pm 9V$ to $\pm 18V$		82	77	dB MIN
Power Consumption	P_D	Sample Mode $V_{IN} = 0$		180	210	mW MAX
Logic Control Input Current	I_{LC}	$V_{LC} = 0V$		−2	−3	μA MAX
Logic Input	$I_{S/H}$	Sample Mode $V_{S/H} = 0.6V$		−15	−15	μA MAX
		Hold Mode $V_{S/H} = 5V$		0	0	nA MAX
Differential Logic Threshold	V_{TH}	$V_{LC} = 0$		2.0	2.0	V MAX
				0.8	0.8	V MIN

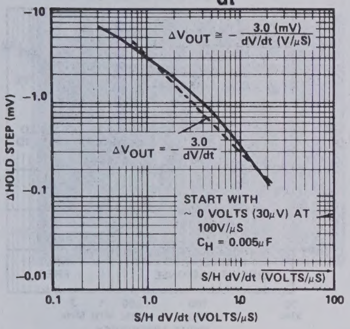
Note: Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $C_H = 0.005\mu F$, V_{LC} connected to ground, $T_A = 25°C$, device fully warmed up, unless otherwise noted.

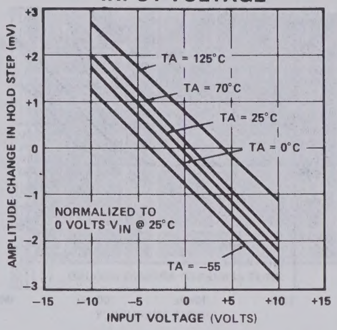
PARAMETER	SYMBOL	CONDITIONS	SMP-10N SMP-11N TYPICAL	SMP-10G SMP-11G TYPICAL	UNITS
Acquisition Time	t_{aq}	10V step to 0.1% of final value	3.5	3.5	μs
Aperture Time	t_{ap}		50	50	ns
Charge Transfer	Q_t	$V_{IN} = 0$, $V_{S/H} = 3.5V$	5	5	pC
Slew Rate	SR	$V_{IN} = \pm 10V$, $R_L = 2.5k\Omega$	10	10	V/μs

TYPICAL PERFORMANCE CHARACTERISTICS

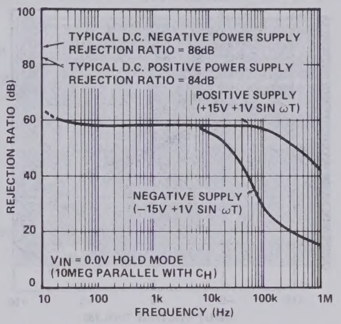
CHANGE IN HOLD STEP vs S/H $\frac{dV}{dt}$



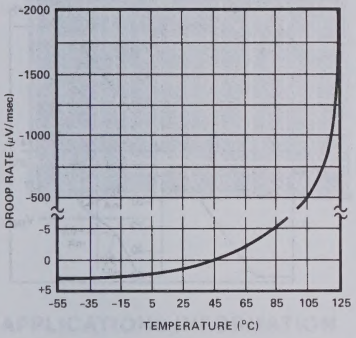
AMPLITUDE CHANGE IN HOLD STEP vs INPUT VOLTAGE



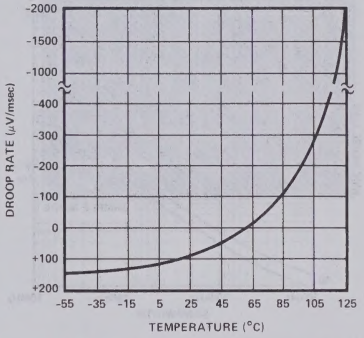
HOLD MODE POWER SUPPLY REJECTION



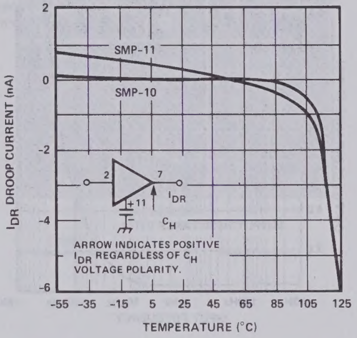
SMP-10 DROOP RATE vs TEMPERATURE



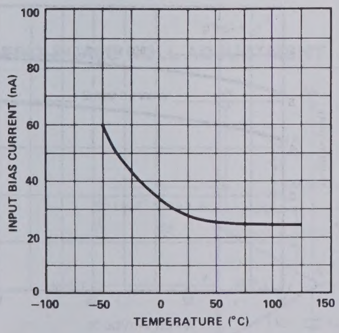
SMP-11 DROOP RATE vs TEMPERATURE



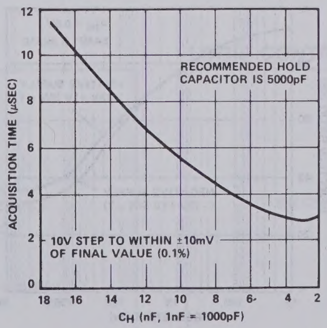
DROOP CURRENT vs TEMPERATURE



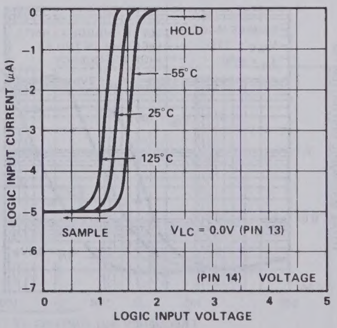
INPUT BIAS CURRENT vs TEMPERATURE



ACQUISITION TIME vs HOLD CAPACITOR

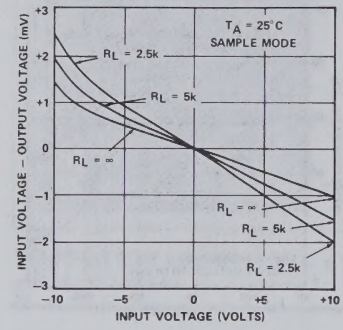


LOGIC INPUT CURRENT

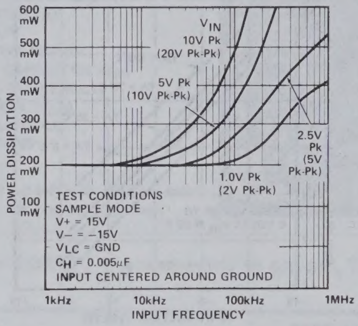


TYPICAL PERFORMANCE CHARACTERISTICS

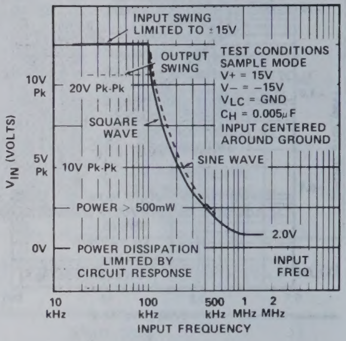
GAIN ERROR



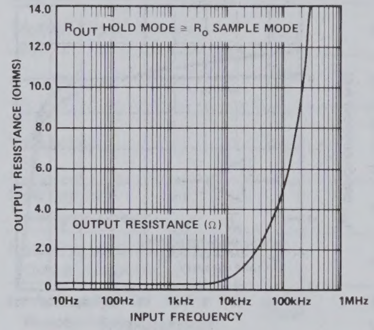
POWER DISSIPATION vs FREQUENCY INPUT = V_{pk} Sin ωt



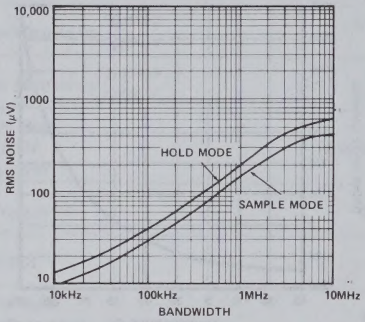
MAXIMUM INPUT SIGNAL AMPLITUDE vs FREQUENCY



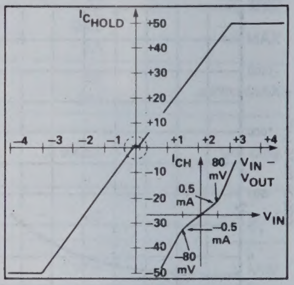
OUTPUT RESISTANCE vs FREQUENCY



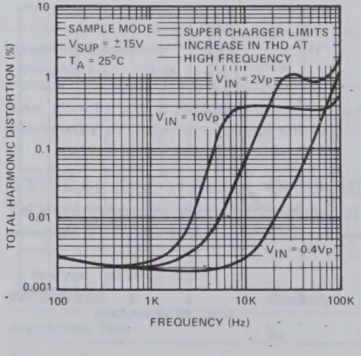
OUTPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



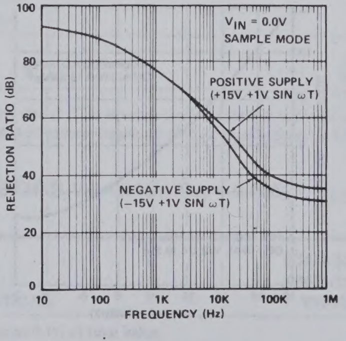
HOLD CAPACITOR CHARGING CURRENT vs INPUT OUTPUT VOLTAGE



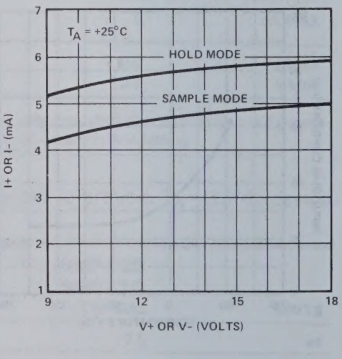
TOTAL HARMONIC DISTORTION vs FREQUENCY



SAMPLE MODE POWER SUPPLY REJECTION

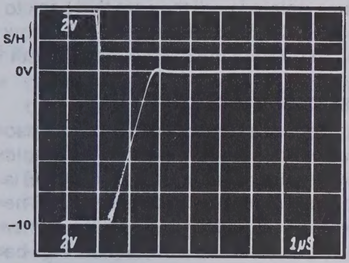


POWER SUPPLY CURRENT vs POWER SUPPLY VOLTAGE

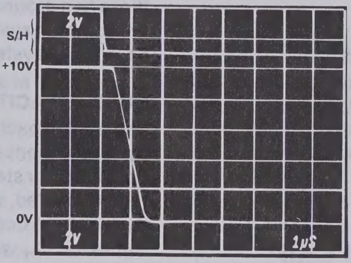


SMP-10/SMP-11 ACQUISITION TIMES

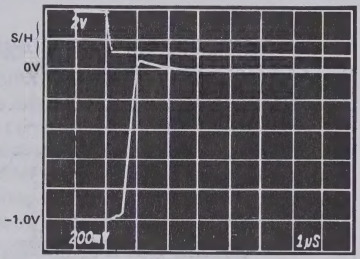
ACQUISITION TIME
−10V to 0V



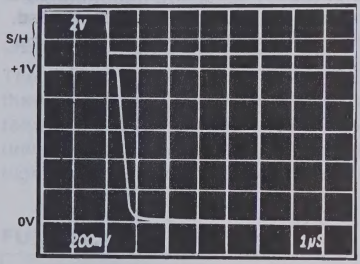
ACQUISITION TIME
+10V to 0V



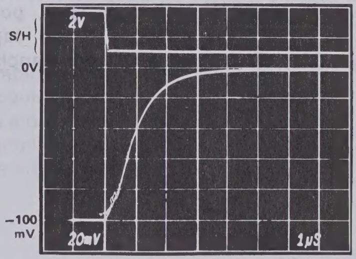
ACQUISITION TIME
−1.0V to 0V



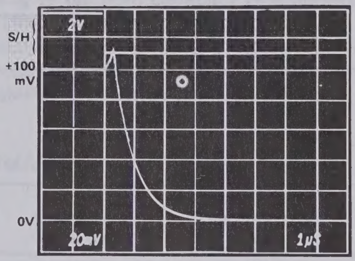
ACQUISITION TIME
+1.0V to 0V

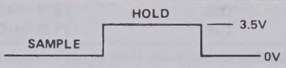


ACQUISITION TIME
−100mV to 0V



ACQUISITION TIME
+100mV to 0V

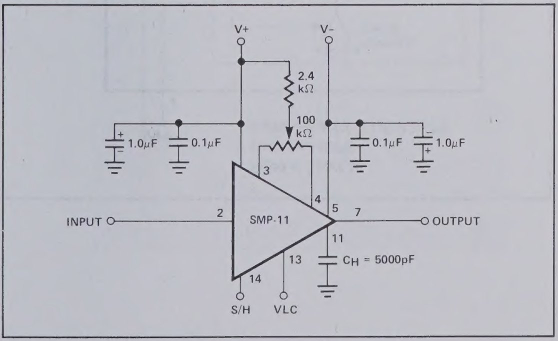



HOLD
SAMPLE
3.5V
0V

APPLICATIONS INFORMATION

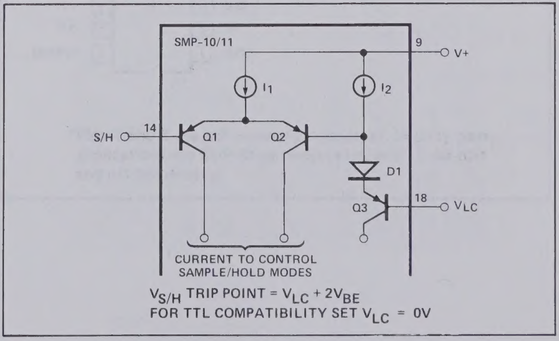
During the null adjustment, the amplifier should be switched continuously between the "sample" and "hold" mode. The error should be adjusted to read zero when the unit is in the "hold" mode. In this way, both offset voltage errors and charge transfer errors are adjusted to zero.

ZERO-SCALE NULL ADJUSTMENT


V+
V−
2.4 kΩ
100 kΩ
1.0μF
0.1μF
0.1μF
1.0μF
3
4
5
2
7
11
13
14
INPUT
SMP-11
OUTPUT
C_H = 5000pF
S/H
VLC

As shown in the Figure, the sample/hold mode control is accomplished by steering the current (I_1) through Q1 or Q2, thus providing high-speed switching and a predictable logic threshold. For TTL and DTL interface, simply ground V_{LC} (Pin 13). For CMOS, HTL and HNIL interface, the appropriate

LOGIC CONTROL

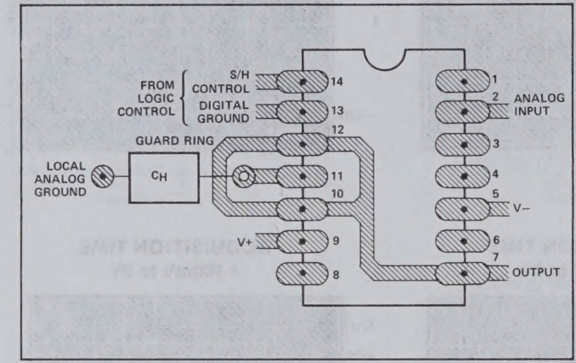

SMP-10/11
9
V+
I1
I2
14
S/H
Q1
Q2
D1
18
Q3
VLC
CURRENT TO CONTROL SAMPLE/HOLD MODES

$V_{S/H}$ TRIP POINT = $V_{LC} + 2V_{BE}$
FOR TTL COMPATIBILITY SET V_{LC} = 0V

threshold voltage, allowing for 2 diode drops for D1 and V_{BE} of Q3, should be applied to V_{LC}.

For proper operation, the V_{LC} (logic control) must always be at least 3.5V below the positive supply and 2.0V above the negative supply.

Sample-and-hold control voltage (S/H) must always be at least 2.8V above the negative supply.



GUARDING AND GROUNDING LAYOUT

The use of a ground plane is strongly recommended to minimize ground path resistances. Separate analog and digital grounds should be used, and it is advisable to keep these two ground systems isolated until they are tied back to the common system ground. Digital currents should not flow back to the system ground through the analog ground path.

HOLD CAPACITOR RECOMMENDATIONS

The hold capacitor (C_H) acts as a memory element and also as a compensating capacitor for the sample-and-hold amplifier. For stable operation, a minimum value of 2000pF is recommended, with no limit set for the maximum value. The devices have been internally trimmed for $C_H = 5000\text{pF}$. Other values of C_H will cause a zero-scale shift, which can be calculated from the following equation:

$$\Delta V_{ZS}(\text{mV}) = \frac{5\ (\text{pC}) \times 10^3}{C_H\ (\text{pF})} - 1$$

The hold capacitor should have very high insulation resistance and low dielectric absorption. For temperatures below 85° C, polystyrene capacitors are recommended, while teflon capacitors are recommended for higher temperature applications.

SAMPLE-AND-HOLD AMPLIFIER

SMP-81

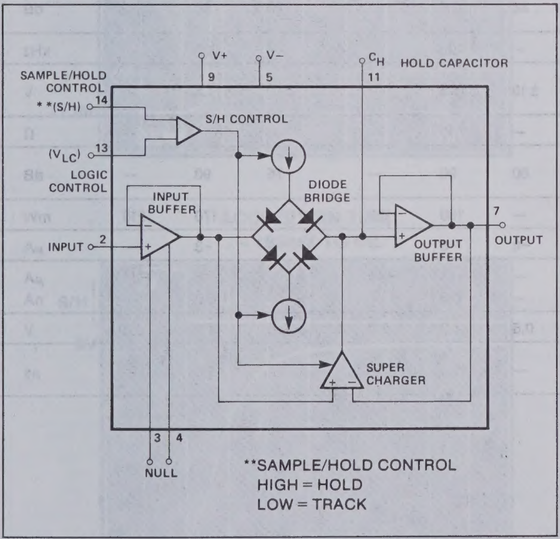
FEATURES

- **Meets System Performance Requirements in Multi-Channel CODECs**
- **Trimmed for Minimum Zero-Scale Error 0.6mV**
- **Low Droop Rate Over Temperature 0.1μV/μs**
- **Low Aperture Time 50ns**
- **Fast Acquisition Time 10V Step to 0.1% 3.5μs**
- **High Slew Rate 10V/μs**
- **High Sample-Current to Hold-Current Ratio .. 1.7 × 10^8**
- **DTL, TTL & CMOS Compatible Logic Input**
- **HA-2425, DATEL SHM-IC-1, and AD-583 Socket Compatible***
- **Low Power Dissipation**
- **Low Cost**
- **Feedthrough Attenuation Ratio 96dB**

GENERAL DESCRIPTION

The SMP-81 precision sample-and-hold amplifier provides the high accuracy, low droop rate and fast acquisition ideally required for PCM encoders. The SMP-81 is a non-inverting unity gain circuit consisting of two buffer amplifiers of very high input impedance connected by a diode bridge switch.

FUNCTIONAL DIAGRAM



V+
V−
9
5
C_H
11
HOLD CAPACITOR
SAMPLE/HOLD CONTROL
14
**(S/H)
S/H CONTROL
(V_{LC})
13
LOGIC CONTROL
INPUT BUFFER
DIODE BRIDGE
2
INPUT
7
OUTPUT
OUTPUT BUFFER
SUPER CHARGER
3
4
NULL
**SAMPLE/HOLD CONTROL
HIGH = HOLD
LOW = TRACK

HIGH ACCURACY AND LOW DROOP RATE

The high input impedance and low droop rate of the SMP-81 are achieved by PMI's ion implant super beta process. The high input impedance permits high source impedance applications without degrading accuracy, and low droop rate. Other features of the SMP-81 include high accuracy, 0.6mV of combined offset voltage and step transfer error, and very low feedthrough. A diode bridge switch design allows minimum charge transfer step. On-chip zener-zap trimming eliminates nulling for most applications.

FAST ACQUISITION

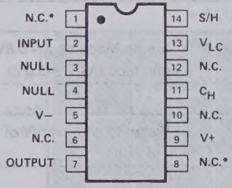
A unique super charger or transconductance amplifier provides up to 50mA charging current to the hold capacitor. As a result, smooth charging of the hold capacitor is achieved with minimum noise. The super charger, in conjunction with the high slewing rate input and output buffer amplifiers, permits fast acquisition operation. The adjustable logic input threshold makes the SMP-81 compatible to all logic families.

ORDERING INFORMATION†

V_{ZS} (mV)	HERMETIC 14-PIN DIP	OPERATING TEMPERATURE RANGE
1.6	SMP-81EY	IND
3.5	SMP-81FY	IND

†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

PIN CONNECTIONS



N.C.*
1
INPUT
2
NULL
3
NULL
4
V−
5
N.C.
6
OUTPUT
7
14
S/H
13
V_{LC}
12
N.C.
11
C_H
10
N.C.
9
V+
8
N.C.*

14-PIN HERMETIC DIP (Y-Suffix)

*Pins 1 and 8 are not internally connected. In unity gain applications, the SMP-81 can replace HA-2425, SHM-IC-1 and AD-583 directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V+ minus V−)	36V
Power Dissipation	500mW
Derate Above 100° C	10mW/° C
Input Voltage	Equal to Supply Voltage
Logic and Logic Control Voltage	Equal to Supply Voltage
Output Short-Circuit Duration	Indefinite
Hold Capacitor Short-Circuit Duration	60sec
Operating Temperature Range	−25° C to +85° C
Storage Temperature Range	−65° C to +150° C
Lead Temperature (Soldering, 60 sec)	300° C

ELECTRICAL CHARACTERISTICS at $V_S \pm 15V$, $C_H = 0.005\mu F$, V_{LC} connected to ground, $-25°C \leq T_A \leq +85°C$, device fully warmed-up, unless otherwise noted.

			SMP-81E			SMP-81F			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Zero-Scale Error (Hold Mode)	V_{ZS}	$V_{IN} = 0$, $V_{S/H} = 3.5V$ (500μsec after Hold Command)	—	0.6	1.6	—	0.9	3.5	mV
Input Bias Current	I_B	$V_{IN} = 0$	—	105	225	—	120	450	nA
Leakage (Droop) Current	I_{DR}	Device Warmed-up	—	0.5	10	—	0.5	20	nA
Droop Rate	dVCH/dt		—	0.1	2.0	—	0.1	4.0	mV/msec
Input Resistance	R_{IN}	(See Note)	30	60	—	15	50	—	GΩ
Voltage Gain	A_V	Sample Mode $V_{IN} = \pm 10V$, $R_L = 5k\Omega$ or $V_{IN} = \pm 5V$, $R_L = 2.5k\Omega$	0.99960	0.99980	—	0.99955	0.99978	—	V/V
Acquisition Time	t_{aq}	10V step to within 10mV of final value (0.1%)	—	3.5	—	—	3.5	—	μs
Aperture Time	t_{ap}		—	50	—	—	50	—	nsec
Charge Transfer	Q_t	$V_{IN} = 0$, $V_{S/H} = 3.5V$	—	5	—	—	5	—	pC
Slew Rate	SR	$V_{IN} = \pm 10V$, $R_L = 2.5k\Omega$	—	10	—	—	10	—	V/μs
Hold Capacitor Charging Current	I_{CH}	$V_{IN} - V_{OUT} \geq \pm 3$ volts	30	50	—	20	50	—	mA
Feedthrough Attenuation Ratio	F_A	Input $-20V_{p\text{-}p}$ 1kHz, $R_L = 5K\Omega$ (See Note)	86	96	—	80	90	—	dB
Full Power Bandwidth	F_P	$\pm 10V_{p\text{-}p}$ (Dissipation Limited)	—	100	—	—	100	—	kHz
Input Voltage Range and/or Output Voltage Swing		$R_L = 2.5k\Omega$	±10	±11.5	—	±10	±11.5	—	V
Output Resistance	R_O		—	0.15	—	—	0.15	—	Ω
Power Supply Rejection Ratio	PSRR	Sample Mode $V_S = \pm 9V$ to $\pm 18V$	80	90	—	75	90	—	dB
Power Consumption (DC)	P_D	Sample Mode $V_{IN} = 0$	—	160	180	—	170	210	mW
Logic Control Input Current	I_{LC}		−6	−3	—	−9	−3	—	μA
Logic Input Current	$I_{S/H}$	Sample Mode $V_{S/H} = 0.6V$ Hold Mode $V_{S/H} = 5.0V$	— —	−15 0.6	−45 —	— —	−15 0.6	−45 —	μA nA
Differential Logic Threshold	V_{TH}		0.8	1.3	2.0	0.8	1.3	2.0	V
Hold Mode Settling Time	t_{HM}	5V step to within 1mV of final value	—	1.5	—	—	1.5	—	μs

NOTE: Guaranteed by design.

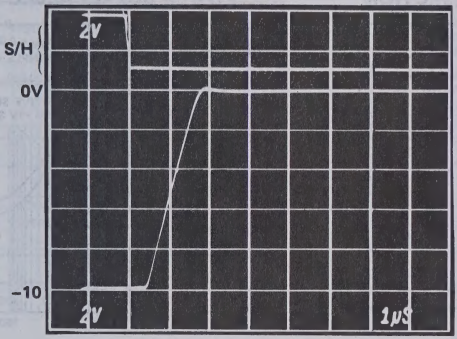
DICE

For applicable DICE information, see SMP-11 Data Sheet.

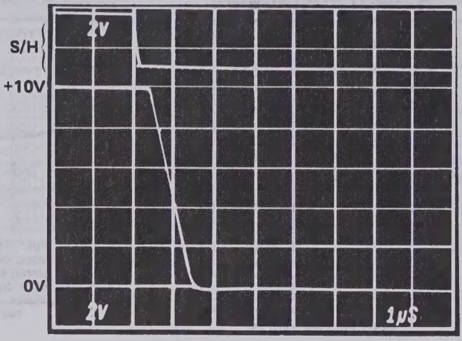
TYPICAL PERFORMANCE CHARACTERISTICS

SMP-81 ACQUISITION TIMES

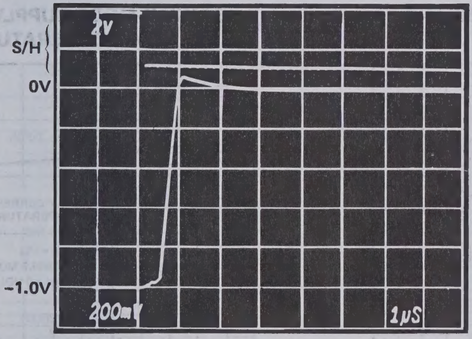
ACQUISITION TIME
– 10V TO 0V



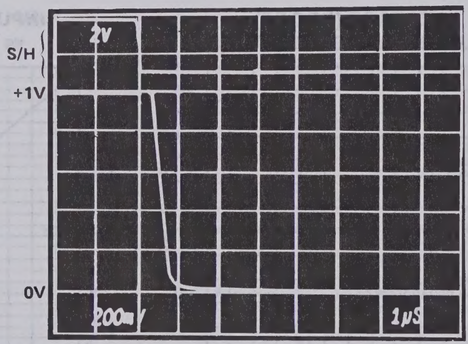
ACQUISITION TIME
+ 10V TO 0V



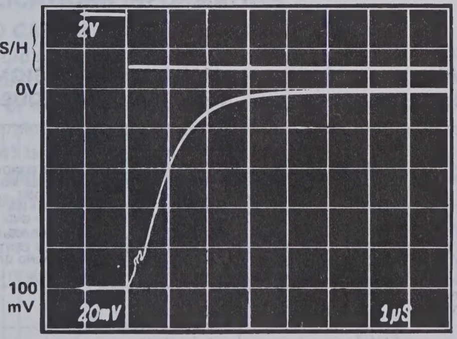
ACQUISITION TIME
– 1.0V TO 0V



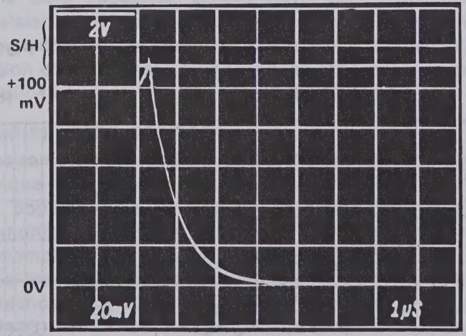
ACQUISITION TIME
+ 1.0V TO 0V

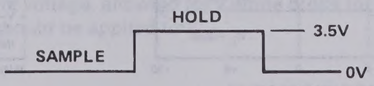


ACQUISITION TIME
– 100mV TO 0V



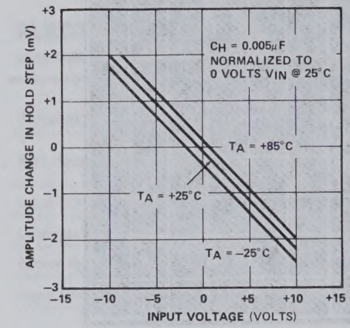
ACQUISITION TIME
+ 100mV TO 0V



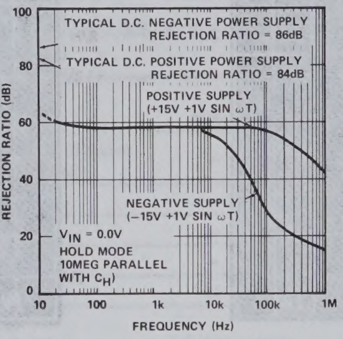


TYPICAL PERFORMANCE CHARACTERISTICS

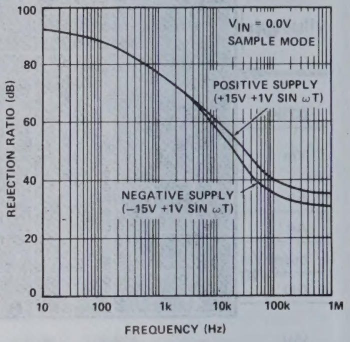
AMPLITUDE CHANGE IN HOLD STEP vs INPUT VOLTAGE



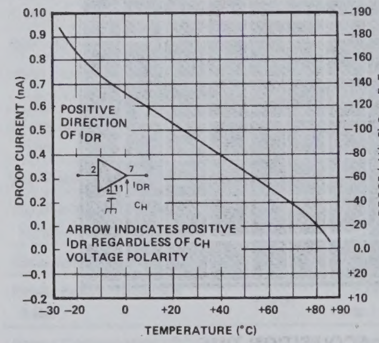
HOLD-MODE POWER SUPPLY REJECTION



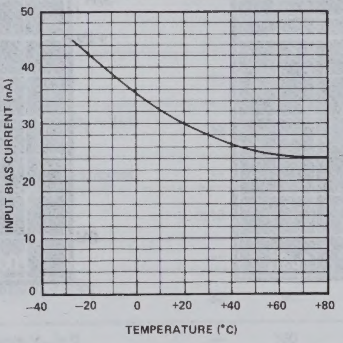
SAMPLE-MODE POWER SUPPLY REJECTION



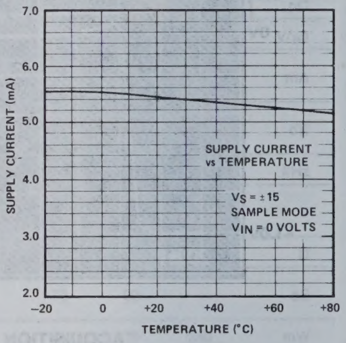
LEAKAGE (DROOP) CURRENT vs TEMPERATURE



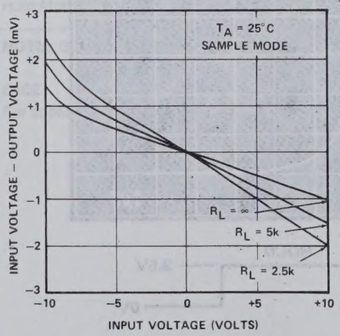
INPUT BIAS CURRENT vs TEMPERATURE



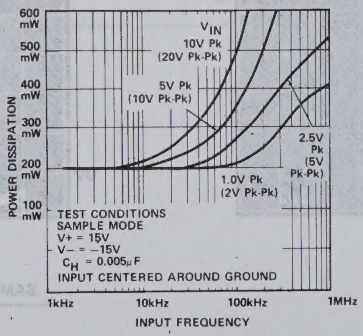
SAMPLE-MODE SUPPLY CURRENT vs TEMPERATURE



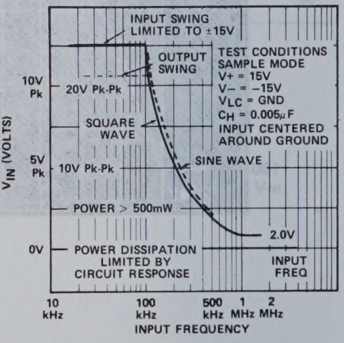
GAIN ERROR



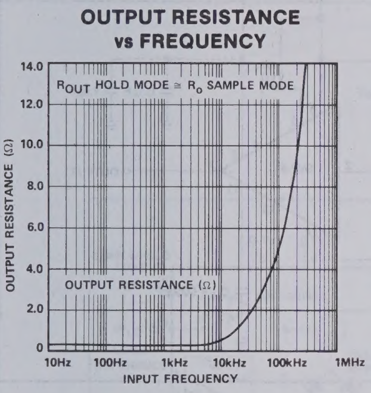
POWER DISSIPATION vs FREQUENCY INPUT = $V_P \sin \omega t$



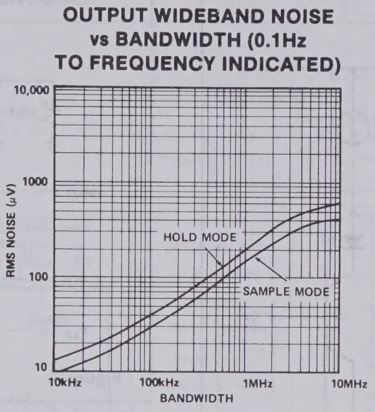
MAXIMUM INPUT SIGNAL AMPLITUDE vs FREQUENCY



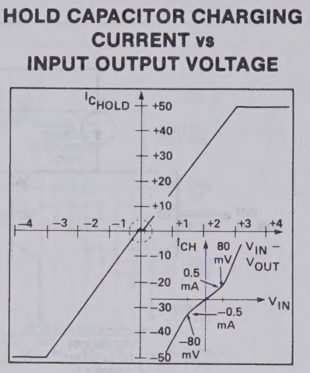
TYPICAL PERFORMANCE CHARACTERISTICS



OUTPUT RESISTANCE vs FREQUENCY

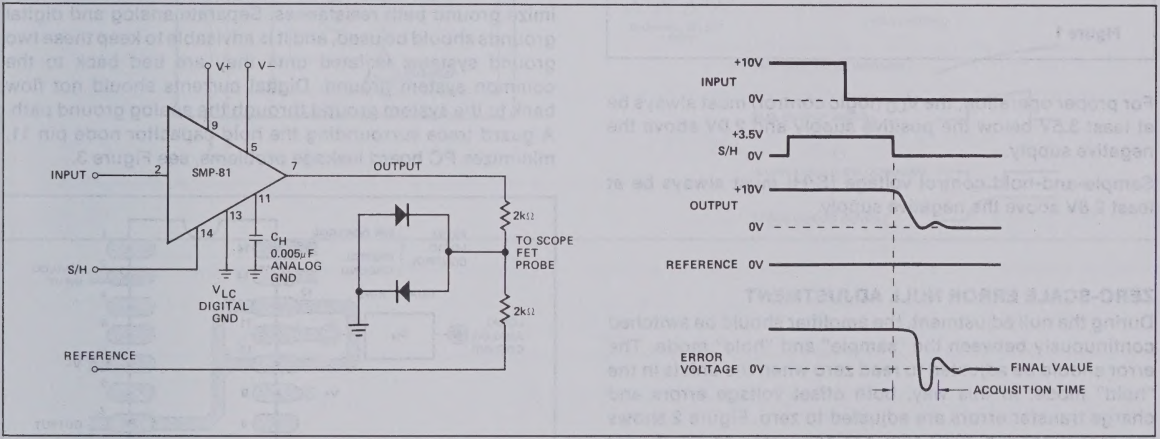


OUTPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



HOLD CAPACITOR CHARGING CURRENT vs INPUT OUTPUT VOLTAGE

ACQUISITION TIME TEST CIRCUIT



V+
V−
9
5
INPUT
2
SMP-81
7
OUTPUT
11
13
14
S/H
C_H
0.005μF
ANALOG GND
V_{LC}
DIGITAL GND
2kΩ
2kΩ
TO SCOPE FET PROBE
REFERENCE
+10V
INPUT
0V
+3.5V
S/H
0V
+10V
OUTPUT
0V
REFERENCE
0V
ERROR VOLTAGE
0V
FINAL VALUE
ACQUISITION TIME

APPLICATIONS INFORMATION

HOLD CAPACITOR RECOMMENDATIONS

The hold capacitor (C_H) acts as a memory element and also as a compensating capacitor for the sample-and-hold amplifier. For stable operation, a minimum value of 2000pF is recommended, with no limit set for the maximum value. The SMP-81 is internally trimmed for C_H = 5000pF. Other values of C_H will cause a zero-scale shift, which can be calculated from the following equation:

$$\Delta V_{ZS}\,(\text{mV}) = \frac{5\,(\text{pC}) \times 10^3}{C_H\,(\text{pF})} - 1$$

A C_H of 5000pF has been empirically determined to be an optimum value for 8-channel shared CODEC operation.

The hold capacitor should have very high insulation resistance and low dielectric absorption. For temperatures below 85° C, polystyrene capacitors are recommended, while teflon capacitors are recommended for higher temperature applications.

SMP-81 LOGIC CONTROL

The sample/hold mode control of the SMP-81 incorporates a unique logic input circuit, which enables direct interface to all popular logic families and provides maximum noise immunity. As shown in Figure 1, the mode control is accomplished by steering the current (I_1) through Q1 or Q2, thus providing high speed switching and a predictable logic threshold. For TTL and DTL interface, simply ground V_{LC} (pin 13). For CMOS, HTL and HNIL interface, the appropriate threshold voltage, allowing for 2 diode drops for D1 and V_{BE} of Q3, should be applied to V_{LC}.

SAMPLE/HOLD MODE INTERFACE CIRCUITRY

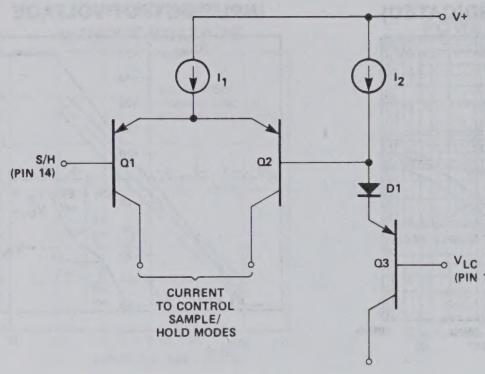

V+
I_1
I_2
S/H (PIN 14)
Q1
Q2
D1
Q3
V_{LC} (PIN 13)
CURRENT TO CONTROL SAMPLE/ HOLD MODES

Figure 1

For proper operation, the V_{LC} (logic control) must always be at least 3.5V below the positive supply and 2.0V above the negative supply.

Sample-and-hold control voltage (S/H) must always be at least 2.8V above the negative supply.

ZERO-SCALE ERROR NULL ADJUSTMENT

During the null adjustment, the amplifier should be switched continuously between the "sample" and "hold" mode. The error should be adjusted to read zero when the unit is in the "hold" mode. In this way, both offset voltage errors and charge transfer errors are adjusted to zero. Figure 2 shows the recommended 10kΩ trim pot connected to V+ if user needs better V_{ZS} than 1.6mV.

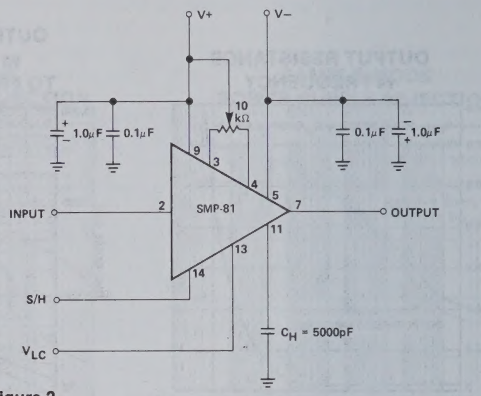

V+
V−
1.0µF
0.1µF
10 kΩ
0.1µF
1.0µF
9
3
4
5
7
2
11
13
14
INPUT
SMP-81
OUTPUT
S/H
V_{LC}
C_H = 5000pF

Figure 2

GUARDING AND GROUNDING LAYOUT

The use of a ground plane is strongly recommended to minimize ground path resistances. Separate analog and digital grounds should be used, and it is advisable to keep these two ground systems isolated until they are tied back to the common system ground. Digital currents should not flow back to the system ground through the analog ground path. A guard trace surrounding the hold capacitor node pin 11, minimizes PC board leakage problems, see Figure 3.

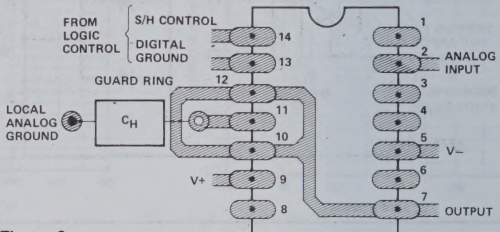
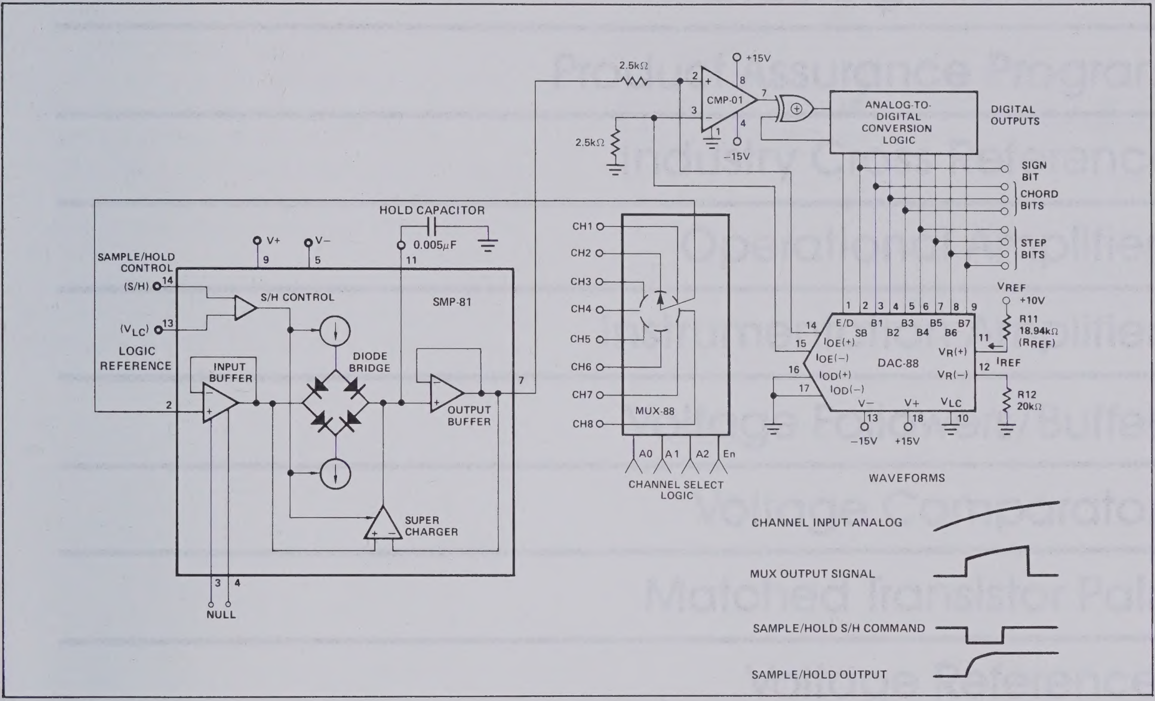

FROM LOGIC CONTROL
S/H CONTROL
DIGITAL GROUND
GUARD RING
LOCAL ANALOG GROUND
C_H
14
13
12
11
10
9
8
V+
1
2
ANALOG INPUT
3
4
5
V−
6
7
OUTPUT

Figure 3

TYPICAL APPLICATION

EIGHT-CHANNEL SHARED CODEC PCM ENCODER


+15V
2.5kΩ
2
8
CMP-01
7
3
1
4
−15V
2.5kΩ
ANALOG-TO-DIGITAL CONVERSION LOGIC
DIGITAL OUTPUTS
SIGN BIT
CHORD BITS
STEP BITS
HOLD CAPACITOR
0.005μF
V+
V−
9
5
11
SAMPLE/HOLD CONTROL
(S/H) 14
S/H CONTROL
SMP-81
(V_{LC}) 13
LOGIC REFERENCE
INPUT BUFFER
DIODE BRIDGE
OUTPUT BUFFER
7
2
SUPER CHARGER
3
4
NULL
CH1
CH2
CH3
CH4
CH5
CH6
CH7
CH8
MUX-88
A0
A1
A2
En
CHANNEL SELECT LOGIC
1 2 3 4 5 6 7 8 9
E/D
SB
B1
B2
B3
B4
B5
B6
B7
14
15
16
17
$I_{OE}(+)$
$I_{OE}(-)$
$I_{OD}(+)$
$I_{OD}(-)$
DAC-88
$V_R(+)$
$V_R(-)$
11
12
V−
V+
V_{LC}
13
18
10
−15V
+15V
V_{REF}
+10V
R11
18.94kΩ
(R_{REF})
I_{REF}
R12
20kΩ
WAVEFORMS
CHANNEL INPUT ANALOG
MUX OUTPUT SIGNAL
SAMPLE/HOLD S/H COMMAND
SAMPLE/HOLD OUTPUT

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SPECIAL FUNCTIONS

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GAP-01 .... **14-4**
General-Purpose Analog Signal
Processing Subsystem

PKD-01 .... **14-19**
Monolithic Peak Detector

SPECIAL FUNCTIONS

INTRODUCTION

Special functions are, by definition, those functions that do not fall into any of the standard categories of linear integrated circuits.

The two circuits in this section could have been placed in the Sample-and-Hold Amplifier (S/H) section of this catalog, because they are subsets of S/Hs.

The PKD-01 is functionally a S/H with a diode in series with the output of the "A channel" amplifier. In the GAP-01 this diode is removed.

DEFINITIONS

At the present time the two circuits in this section are S/Hs, so all of the definitions in the S/H section apply, and they are not repeated here.

GAP-01

GENERAL-PURPOSE ANALOG SIGNAL PROCESSING SUBSYSTEM

FEATURES

- **Low Offset Voltage 3mV**
- **Low Zero-Scale Error 4mV**
- **Low Droop Rate 0.1mV/ms**
- **Wide Bandwidth 400kHz**
- **Digitally Selected Signal Path**
- **Uncommitted Comparator On Chip**
- **Wide Application Versatility**
  - **Synchronous Demodulator**
  - **Absolute Value Amplifier**
  - **Two-Channel S/H Amplifier**
  - **Two-Channel Multiplexer With Gain**

ORDERING INFORMATION†

V_{OS} (mV)	V_{ZS} (mV)	MILITARY	HERMETIC INDUSTRIAL	PLASTIC COMMERCIAL
3	4	GAPO1AX*	GAP01EX	GAP01EP
6	7	GAPO1BX*	GAP01FX	GAP01FP

*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

GENERAL DESCRIPTION

Designed as a general-purpose analog processing subsystem, the GAP-01 combines many commonly used system building blocks within a single integrated circuit.

The basic circuit versatility stems from the GAP-01's architecture. The circuit features two differential input transconductance amplifiers, two low-glitch current mode switches, an output voltage buffer amplifier. and a precision comparator.

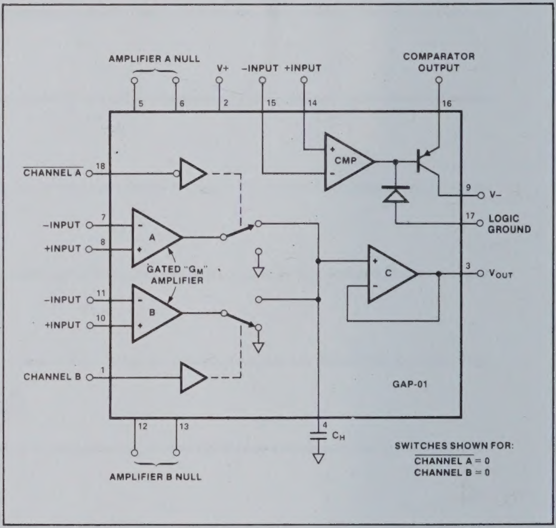
Both transconductance amplifier outputs are switched by current-mode switches into the voltage follower output buffer, thus providing two digitally selectable signal paths through the device. Gain through the two channels may be different in both sign and magnitude depending upon feedback selection. An external capacitor provides loop compensation and doubles as a hold or "memory" capacitor when the GAP-01 functions as a dual-channel sample/hold amplifier. Offset voltage and charge transfer errors are trimmed by using the "Zener-Zap" trim technique. The output buffer features a FET input stage to reduce droop rate error in S/H applications. A bias current cancellation circuit minimizes droop error at high ambient temperature.

The inclusion of a precision comparator on chip increases the GAP-01's versatility and cost effectiveness in data conversion applications. The output high voltage level is set by external resistors. This scheme maximizes noise immunity and permits interface to all standard logic families .

Manufactured under the following patent: 4,285,051.

Several applications exploit the ability to select the signal path through the GAP-01. As a two-channel multiplexer or analog switch, the GAP-01 high input impedance offers advantages when switching high impedance signals. Gain through the "MUX" is also possible. The GAP-01 operates as a sample/hold amplifier in the hold mode when both transconductance amplifiers are unselected. With the on-board comparator, a two-channel successive approximation analog-to-digital conversion (ADC) system may be constructed. Combining a sign-magnitude, digital-to-analog (DAC) converter with the GAP-01 results in a four-quadrant multiplying DAC. The GAP-01 contains all the functional devices needed to perform synchronous demodulation or implement the absolute value function.

FUNCTIONAL DIAGRAM



CONTROL LOGIC

$\overline{\text{Ch A}}$	Ch B	OUTPUT to C
0	0	Channel A
0	1	Sum
1	0	Hold Last Input
1	1	Channel B

ABSOLUTE MAXIMUM RATINGS (Note 2)

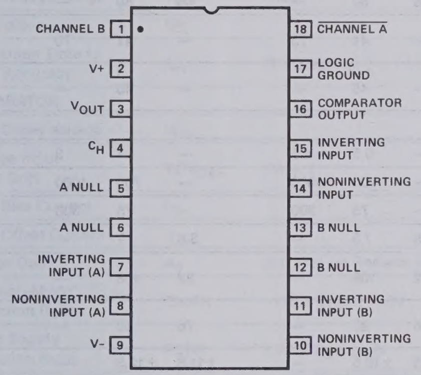
Supply Voltage	±18V
Power Dissipation	500mW
Input Voltage	Equal to Supply Voltage
Logic and Logic Ground Voltage	Equal to Supply Voltage
Output Short Circuit Duration	Indefinite
Amplifier A or B Differential Input Voltage	±24V
Comparator Differential Input Voltage	±24V
Comparator Output Voltage	Equal to Positive Supply Voltage
Hold Capacitor Short Circuit Duration	Indefinite
Storage Temperature	−65° C to +150° C
Lead Temperature (Soldering, 60 sec)	300° C
Operating Temperature Range	
GAP01AX, BX	−55° C to + 125° C
GAP01EX, FX	−25° C to +85° C
GAP01EP, FP	0° C to +70° C
DICE Junction Temperature (T_j)	−65° C to +150° C

(NOTE 1)	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
18-Pin DIP (X)	100° C	10mW/° C
18-Pin DIP (P)	50° C	10mW/° C

NOTES:

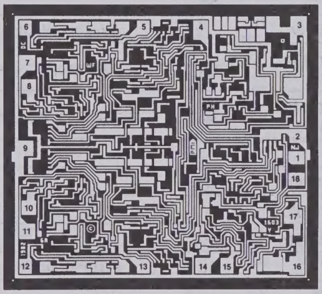
1. Maximum package power dissipation vs. ambient temperature.
2. Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

PIN CONNECTIONS


CHANNEL B 1
V+ 2
V_{OUT} 3
C_H 4
A NULL 5
A NULL 6
INVERTING INPUT (A) 7
NONINVERTING INPUT (A) 8
V- 9
18 $\overline{\text{CHANNEL A}}$
17 LOGIC GROUND
16 COMPARATOR OUTPUT
15 INVERTING INPUT
14 NONINVERTING INPUT
13 B NULL
12 B NULL
11 INVERTING INPUT (B)
10 NONINVERTING INPUT (B)

18-PIN HERMETIC DIP
(X-Suffix)
EPOXY DIP
(P-Suffix)

DICE CHARACTERISTICS


1
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DIE SIZE 0.090 × 0.100 inch, 9,000 sq. mils
(2.286 × 2.54; 5.8 sq.mm)

1. CHANNEL (B)
2. V+
3. V_{OUT}
4. C_H
5. (A) NULL
6. (A) NULL
7. INVERTING INPUT (A)
8. NONINVERTING INPUT (A)
9. V−
10. NONINVERTING INPUT (B)
11. INVERTING INPUT (B)
12. (B) NULL
13. (B) NULL
14. COMPARATOR NONINVERTING INPUT
15. COMPARATOR INVERTING INPUT
16. COMPARATOR OUTPUT
17. LOGIC GND
18. CHANNEL (A)

For additional DICE information refer to Section 2.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $C_H = 1000pF$, $T_A = 25°C$.

PARAMETER	SYMBOL	CONDITIONS	GAP01A/E MIN	GAP01A/E TYP	GAP01A/E MAX	GAP01B/F MIN	GAP01B/F TYP	GAP01B/F MAX	UNITS
"g_m" AMPLIFIERS A, B									
Zero-Scale Error	V_{ZS}		—	2	4	—	3	7	mV
Input Offset Voltage	V_{OS}		—	2	3	—	3	6	mV
Input Bias Current	I_B		—	80	150	—	80	250	nA
Input Offset Current	I_{OS}		—	20	40	—	50	100	nA
Voltage Gain	A_V		18	25	—	10	25	—	V/mV
Open-Loop Bandwidth	BW	$A_V = 1$	—	0.4	—	—	0.4	—	MHz
Common-Mode Rejection Ratio	CMRR	$-10V \le V_{CM} \le +10V$	80	90	—	74	90	—	dB
Power Supply Rejection Ratio	PSRR	$\pm 9V \le V_S \le \pm 18V$	86	96	—	76	96	—	dB
Input Voltage Range	V_{CM}	(Note 2)	±11.5	±12	—	±11.5	±12	—	V
Slew Rate	SR		—	0.5	—	—	0.5	—	V/μs
Feedthrough Error		$\Delta V_{IN} = 20V$, CHA = 1, CHB = 0 (Note 2)	66	80	—	66	80	—	dB
Acquisition Time to 0.1% Accuracy	t_{aq}	20V Step, $A_{VCL} = +1$ (Note 2)	—	41	70	—	41	70	μs
Acquisition Time to 0.01% Accuracy	t_{aq}	20V Step, $A_{VCL} = +1$ (Note 2)	—	45	—	—	45	—	μs
COMPARATOR									
Input Offset Voltage	V_{OS}		—	0.5	1.5	—	1	3	mV
Input Bias Current	I_B		—	700	1000	—	700	1000	nA
Input Offset Current	I_{OS}		—	75	300	—	75	300	nA
Voltage Gain	A_V	2kΩ Pull-up Resistor to 5V (Note 2)	5	7.5	—	3.5	7	—	V/mV
Common-Mode Rejection Ratio	CMRR	$-10V \le V_{CM} \le +10V$	82	106	—	82	106	—	dB
Power Supply Rejection Ratio	PSRR	$\pm 9V \le V_S \le \pm 18V$	76	90	—	76	90	—	dB
Input Voltage Range	V_{CM}	(Note 2)	±11.5	±12.5	—	±11.5	±12.5	—	V
Low Output Voltage	V_{OL}	$I_{SINK} \le 5mA$, Logic GND = 0V	−0.2	0.15	0.4	−0.2	0.15	0.4	V
"OFF" Output Leakage Current	I_L	$V_{OUT} = 5V$	—	25	80	—	25	80	μA
Output Short Circuit Current	I_{SC}	$V_{OUT} = 5V$	7	12	45	7	12	45	mA
Response Time	t_S	5mV Overdrive, (Note 3) 2kΩ Pull-up Resistor to 5V	—	150	—	—	150	—	ns
DIGITAL INPUTS-CHA, CHB (Note 3)									
Logic "1" Input Voltage	V_H		2	—	—	2	—	—	V
Logic "0" Input Voltage	V_L		—	—	0.8	—	—	0.8	V
Logic "1" Input Current	I_{INH}	$V_H = 3.5V$	—	0.02	1	—	0.02	1	μA
Logic "0" Input Current	I_{INL}	$V_L = 0.4V$	—	1.6	10	—	2	10	μA
MISCELLANEOUS									
Droop Rate	V_{DR}	$T_j = +25°C$ (Note 1)	—	0.02	0.07	—	—	0.1	mV/ms
Output Voltage Swing: Amplifier C	V_{OP}	$R_L = 2.5k$	±11.5	±12.5	—	±11	±12	—	V
Short Circuit Current: Amplifier C	I_{SC}		7	15	40	7	15	40	mA
Switch Aperture Time	t_{ap}		—	75	—	—	75	—	ns
Switch Switching Time	ts		—	50	—	—	50	—	ns
Slew Rate: Amplifier C	SR	$R_L = 2.5k$	—	2.5	—	—	2.5	—	V/μs
Power Supply Current	I_{SY}	No Load	—	5	7	—	6	9	mA

NOTES:

1. Due to limited production test times the droop current corresponds to junction temperature (T_j).
2. Guaranteed by design.
3. Channel A = "1", Channel B = "0".

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $C_H = 1000pF$, $-55°C \leq T_A \leq 125°C$ for GAP01AX & BX; $-25°C \leq T_A \leq 85°C$ for GAP01EX & FX, and $0°C \leq T_A \leq 70°C$ for GAP01EP & FP.

				GAP01A/E			GAP01B/F		
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
"g_m" AMPLIFIERS A, B									
Zero-Scale Error	V_{ZS}		—	4	7	—	6	12	mV
Input Offset Voltage	V_{OS}		—	3	6	—	5	10	mV
Average Input Offset Drift	TCV_{OS}	(Note 1)	—	-3	-6	—	-5	-6	μV/°C
Input Bias Current	I_B		—	160	250	—	160	500	nA
Input Offset Current	I_{OS}		—	30	100	—	30	150	nA
Voltage Gain	A_V		7.5	9	—	5	9	—	V/mV
Common-Mode Rejection Ratio	CMRR	$-10V \leq V_{CM} \leq +10V$	74	82	—	72	80	—	dB
Power Supply Rejection Ratio	PSRR	$\pm 9V \leq V_S \leq \pm 18V$	80	90	—	70	90	—	dB
Input Voltage Range	V_{CM}	(Note 1)	±11	±12	—	±10.5	±12	—	V
Slew Rate	SR		—	0.4	—	—	0.4	—	V/μs
Acquisition Time to 0.1% Accuracy	t_{aq}	20V Step, $A_{VCL} = +1$	—	60	—	—	60	—	μs
COMPARATOR									
Input Offset Voltage	V_{OS}		—	2	2.5	—	2	5	mV
Average Input Offset Drift	TCV_{OS}	(Note 1)	—	-4	-6	—	-4	-6	μV/°C
Input Bias Current	I_B		—	1000	2000	—	1100	2000	nA
Input Offset Current	I_{OS}		—	100	600	—	100	600	nA
Voltage Gain	A_V	2kΩ Pull-up Resistor to 5V (Note 1)	4	6.5	—	2.5	6.5	—	V/mV
Common-Mode Rejection Ratio	CMRR	$-10V \leq V_{CM} \leq +10V$	80	100	—	80	92	—	dB
Power Supply Rejection Ratio	PSRR	$\pm 9V \leq V_S \leq \pm 18V$	72	82	—	72	86	—	dB
Input Voltage Range	V_{CM}	(Note 1)	±11	—	—	±11	—	—	V
Low Output Voltage	V_{OL}	$I_{SINK} \leq 5mA$, Logic GND = 5V	-0.2	0.15	0.4	-0.2	0.15	0.4	V
"OFF" Output Leakage Current	I_L	$V_{OUT} = 5V$	—	25	100	—	25	160	μA
Output Short Circuit Current	I_{SC}	$V_{OUT} = 5V$	6	10	45	6	10	45	mA
Response Time	t_s	5mV Overdrive. (Note 3) 2kΩ Pull-up Resistor to 5V	—	200	—	—	200	—	ns
DIGITAL INPUTS-CHA, CHB (Note 3)									
Logic "1" Input Voltage	V_H		2	—	—	2	—	—	V
Logic "0" Input Voltage	V_L		—	—	0.8	—	—	0.8	V
Logic "1" Input Current	I_{INH}	$V_H = 3.5V$	—	0.02	1	—	0.02	1	μA
Logic "0" Input Current	I_{INL}	$V_L = 0.4V$	—	2.5	15	—	2.5	15	μA
MISCELLANEOUS									
Droop Rate	V_{DR}	T_j = Max. Operating Temp., (Note 2)	—	1	10	—	1	10	mV/ms
Output Voltage Swing: Amplifier C	V_{OP}	$R_L = 2.5k$	±11	±12	—	±10.5	±12	—	V
Short Circuit Current: Amplifier C	I_{SC}		6	12	40	6	12	40	mA
Switch Aperture Time	t_{ap}		—	75	—	—	75	—	ns
Slew Rate: Amplifier C	SR	$R_L = 2.5k$	—	2	—	—	2	—	V/μs
Power Supply Current	I_{SY}	No Load	—	5.5	8	—	6.5	10	mA

NOTES: See next page.

WAFER TEST LIMITS at $V_S = \pm 15V$, $C_H = 1000pF$, $T_A = 25°C$.

PARAMETER	SYMBOL	CONDITIONS	GAP-01N LIMIT	UNITS
"g_m" AMPLIFIERS A, B				
Zero-Scale Error	V_{ZS}		7	mV MAX
Input Offset Voltage	V_{OS}		6	mV MAX
Input Bias Current	I_B		250	nA MAX
Input Offset Current	I_{OS}		100	nA MAX
Voltage Gain	A_V		10	V/mV MIN
Common-Mode Rejection Ratio	CMRR	$-10V \le V_{CM} \le +10V$	74	dB MIN
Power Supply Rejection Ratio	PSRR	$\pm 9V \le V_S \pm 18V$	76	dB MIN
Input Voltage Range	V_{CM}	(Note 1)	±11.5	V MIN
Feedthrough Error		$\Delta V_{IN} = 20V$, $\overline{CHA} = 1$, CHB = 0 (Note 1)	66	dB MIN
COMPARATOR				
Input Offset Voltage	V_{OS}		3	mV MAX
Input Bias Current	I_B		1000	nA MAX
Input Offset Current	I_{OS}		300	nA MAX
Voltage Gain	A_V	2kΩ Pull-up Resistor to 5V (Note 1)	3.5	V/mV MIN
Common-Mode Rejection Ratio	CMRR	$-10V \le V_{CM} \le +10V$	82	dB MIN
Power Supply Rejection Ratio	PSRR	$\pm 9V \le V_S \le \pm 18V$	76	dB MIN
Input Voltage Range	V_{CM}	(Note 1)	±11.5	V MIN
Low Output Voltage	V_{OL}	$I_{SINK} \le 5mA$, Logic GND = 5V	0.4 −0.2	V MAX V MIN
"OFF" Output Leakage Current	I_L	$V_{OUT} = 5V$	80	μA MAX
Output Short Circuit Current	I_{SC}	$V_{OUT} = 5V$	45 7	mA MAX mA MIN
DIGITAL INPUTS-$\overline{\text{CHA}}$, CHB (Note 3)				
Logic "1" Input Voltage	V_H		2	V MIN
Logic "0" Input Voltage	V_L		0.8	V MAX
Logic "1" Input Current	I_{INH}	$V_H = 3.5V$	1	μA MAX
Logic "0" Input Current	I_{INL}	$V_L = 0.4V$	10	μA MAX
MISCELLANEOUS				
Droop Rate	V_{DR}	$T_j = 25°C$ $T_A = 25°C$ (See Note 2)	0.1 0.20	mV/ms MAX mV/ms MAX
Output Voltage Swing: Amplifier C	V_{OP}	$R_L = 2.5k$	±11	V MIN
Short Circuit Current: Amplifier C	I_{SC}		40 7	mA MAX mA MIN
Power Supply Current	I_{SY}	No Load	9	mA MAX

NOTES:

1. Guaranteed by design.
2. Due to limited production test times the droop current corresponds to junction temperature (T_J): The droop current vs. time (after power-on) curve clarifies this point. Since most devices (in use) are on for more than 1 second, PMI specifies droop rate for ambient temperature (T_A) also. The warmed-up (T_A) droop current specification is correlated to the junction temperature (T_j) value. PMI has a droop current cancellation circuit which minimizes droop current at high temperatures.
3. Channel $\overline{A}$ = "1", Channel B = "0".

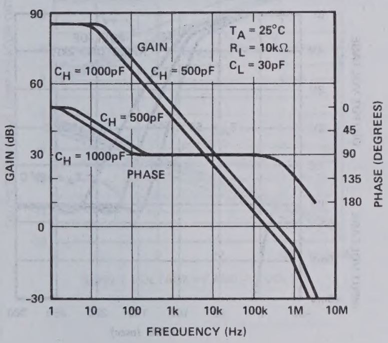
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

WAFER TEST LIMITS at $V_S = \pm 15V$, $C_H = 1000pF$, $T_A = 25°C$. (Cont'd)

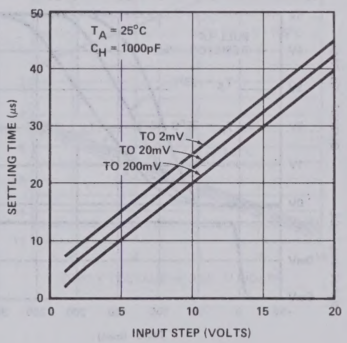
PARAMETER	SYMBOL	CONDITIONS	GAP-01N TYPICAL	UNITS
"g_m" AMPLIFIERS A, B				
Slew Rate	SR		0.5	V/μs
Acquisition Time to 0.1% Accuracy	t_{aq}	20V step, $A_{VCL} = 1$	41	μs
Acquisition Time to 0.01% Accuracy	t_{aq}	20V step, $A_{VCL} = 1$	45	μs
COMPARATOR				
Response Time	t_S	5mV Overdrive 2kΩ Pull-up Resistor to +5V	150	ns
MISCELLANEOUS				
Switch Aperture Time	t_{ap}		75	ns
Switching Time	t_S		50	ns
Slew Rate: Amplifier C	SR	$R_L = 2.5kΩ$	2.5	V/μs

TYPICAL PERFORMANCE CHARACTERISTICS

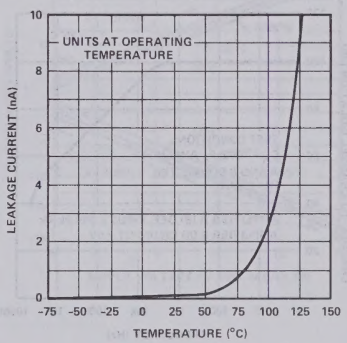
SMALL SIGNAL OPEN LOOP GAIN/PHASE vs FREQUENCY



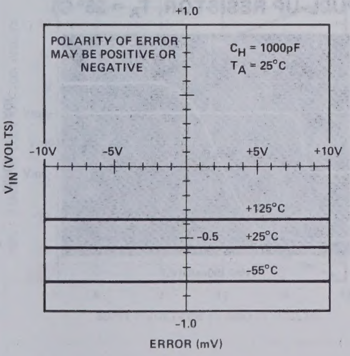
ACQUISITION TIME vs INPUT VOLTAGE STEP SIZE



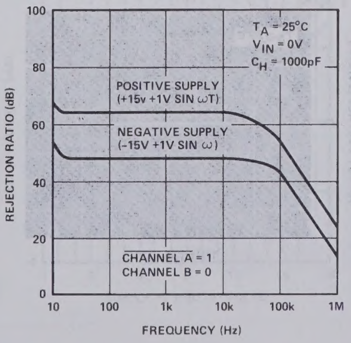
DROOP CURRENT vs TEMPERATURE



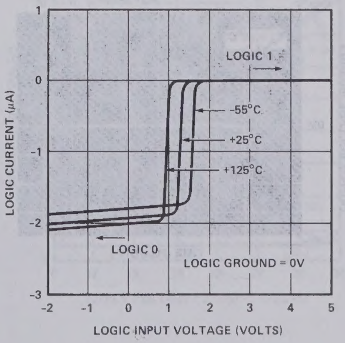
AMPLIFIER CHARGE INJECTION ERROR vs INPUT VOLTAGE AND TEMPERATURE



HOLD-MODE POWER SUPPLY REJECTION vs FREQUENCY

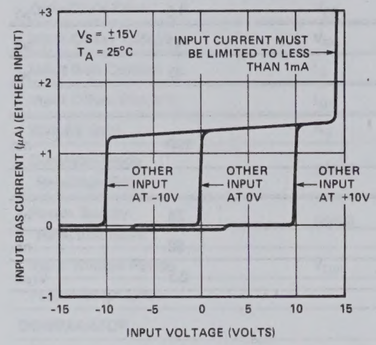


LOGIC INPUT CURRENT vs LOGIC INPUT VOLTAGE

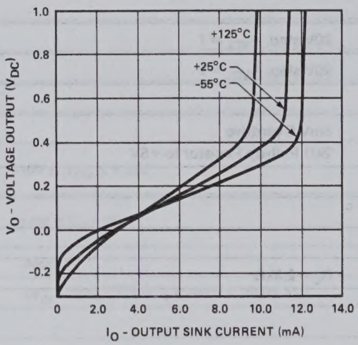


TYPICAL PERFORMANCE CHARACTERISTICS

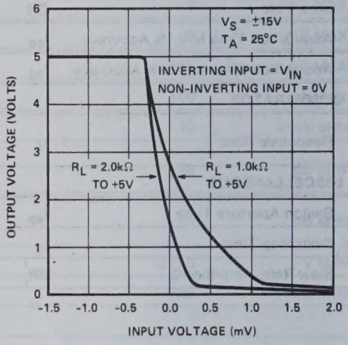
COMPARATOR INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE



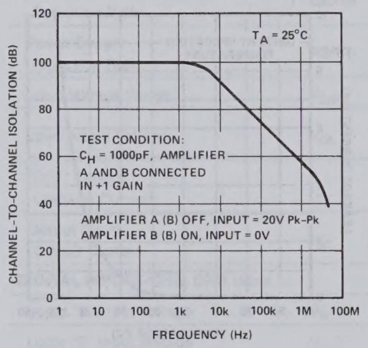
COMPARATOR OUTPUT VOLTAGE vs OUTPUT CURRENT AND TEMPERATURE



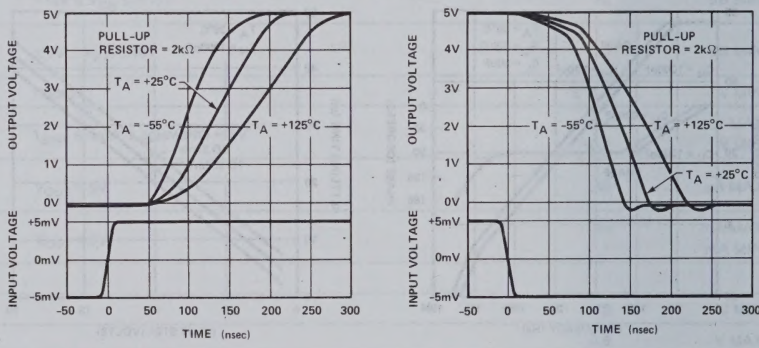
COMPARATOR TRANSFER CHARACTERISTIC



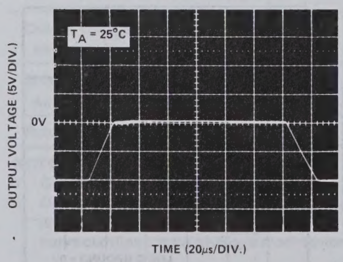
CHANNEL TO CHANNEL ISOLATION vs FREQUENCY



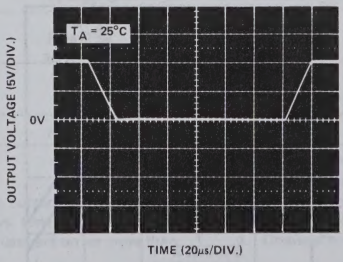
COMPARATOR RESPONSE TIME vs TEMPERATURE



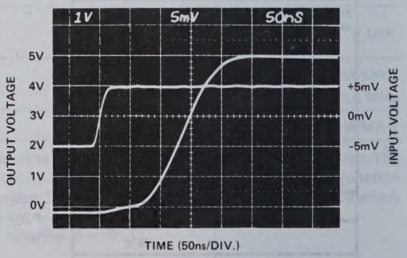
LARGE-SIGNAL INVERTING RESPONSE



LARGE-SIGNAL NONINVERTING RESPONSE

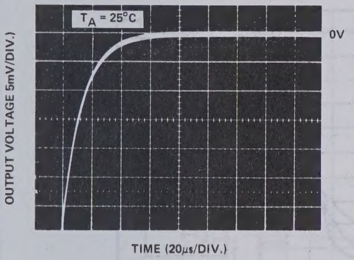


COMPARATOR OUTPUT RESPONSE TIME (2kΩ PULL-UP RESISTOR, T_A = 25° C)

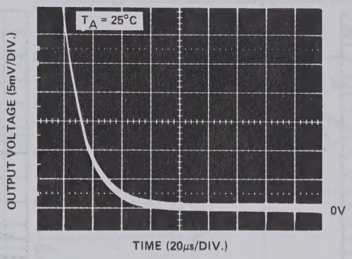


TYPICAL PERFORMANCE CHARACTERISTICS

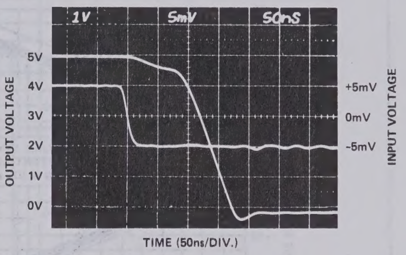
COMPARATOR SETTLING TIME FOR −10V TO 0V STEP INPUT



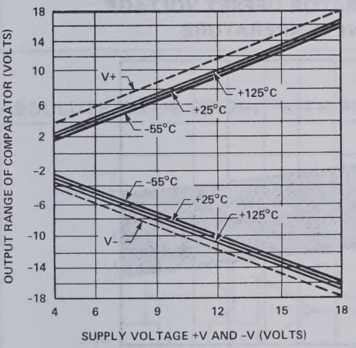
COMPARATOR SETTLING TIME FOR +10V TO 0V STEP INPUT



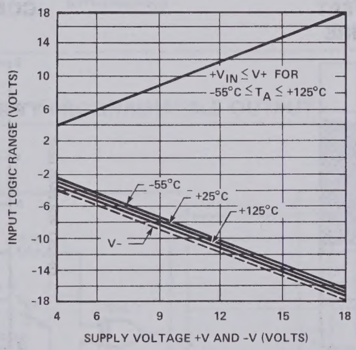
COMPARATOR OUTPUT RESPONSE TIME (2kΩ PULL-UP RESISTOR, $T_A = 25°C$)



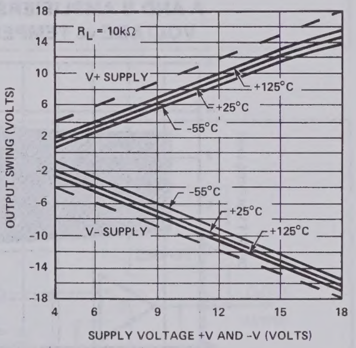
OUTPUT SWING OF COMPARATOR vs SUPPLY VOLTAGE



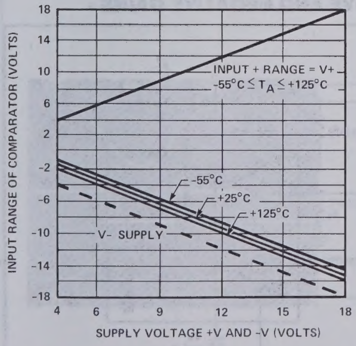
INPUT LOGIC RANGE vs SUPPLY VOLTAGE



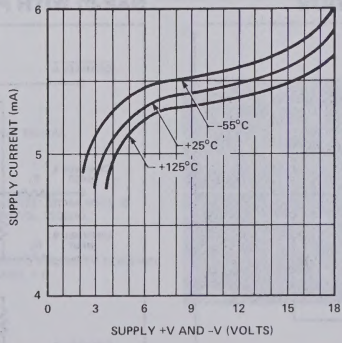
BUFFER OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE (DUAL SUPPLY OPERATION)



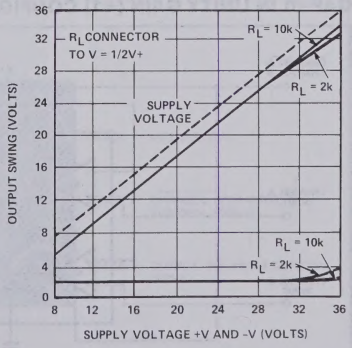
A AND B INPUT RANGE vs SUPPLY VOLTAGE



SUPPLY CURRENT vs SUPPLY VOLTAGE

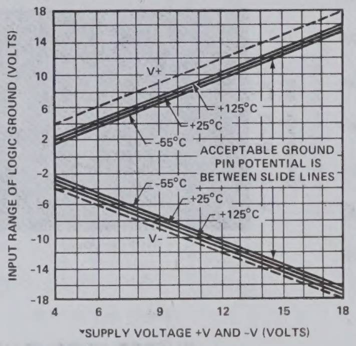


BUFFER OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE (SINGLE SUPPLY OPERATION)

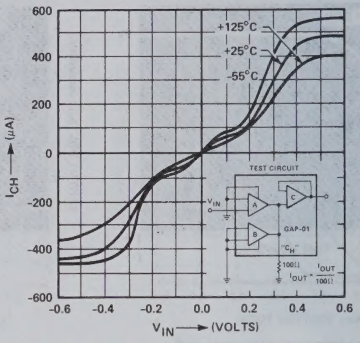


TYPICAL PERFORMANCE CHARACTERISTICS

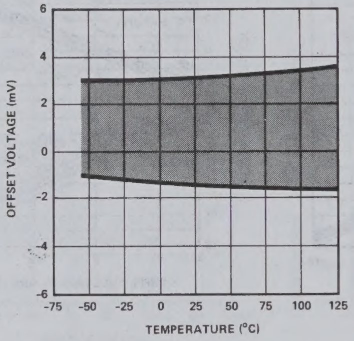
INPUT RANGE OF LOGIC GROUND vs SUPPLY VOLTAGE



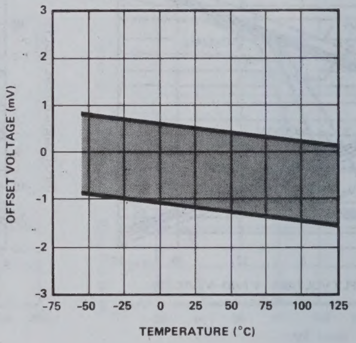
AMPLIFIER "A" OR "B" VOLTAGE TO CURRENT TRANSFER FUNCTION (V_{IN} vs I_{CH})



A AND B AMPLIFIERS OFFSET VOLTAGE vs TEMPERATURE

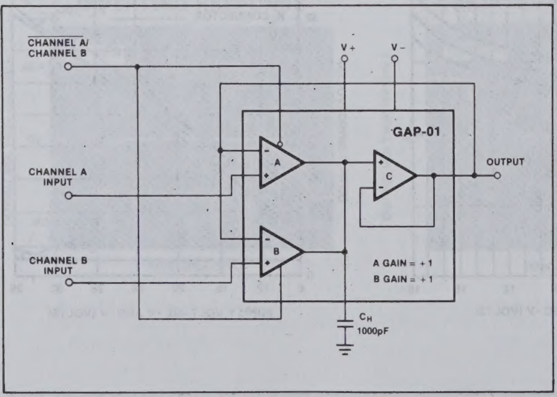


COMPARATOR OFFSET VOLTAGE vs TEMPERATURE

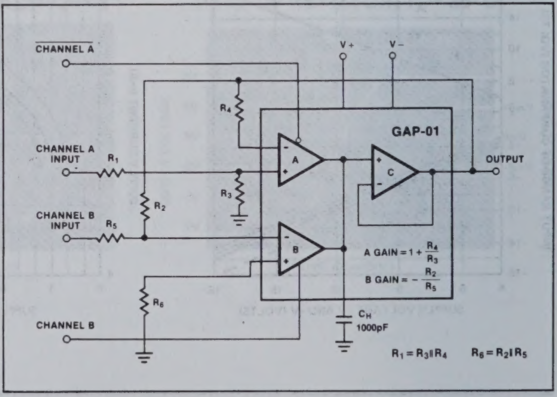


APPLICATION CIRCUITS

GAP-01 IN UNITY GAIN (+1) CONFIGURATION

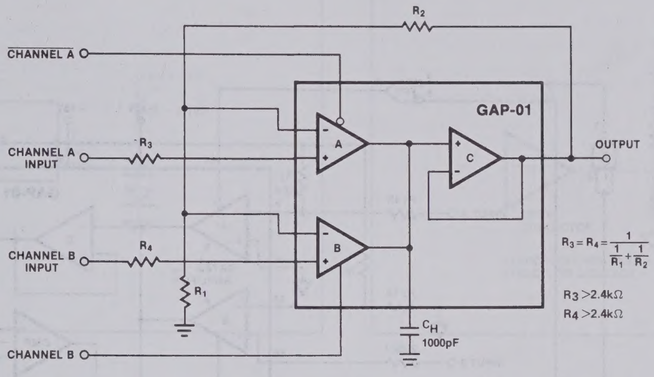

CHANNEL A/CHANNEL B
V+
V−
GAP-01
CHANNEL A INPUT
A
C
OUTPUT
CHANNEL B INPUT
B
A GAIN = +1
B GAIN = +1
C_H
1000pF

GAP-01 WITH POSITIVE AND NEGATIVE GAINS


CHANNEL A
V+
V−
R_4
GAP-01
CHANNEL A INPUT
R_1
A
C
OUTPUT
R_3
R_2
CHANNEL B INPUT
R_5
B
$\text{A GAIN} = 1 + \frac{R_4}{R_3}$
$\text{B GAIN} = -\frac{R_2}{R_5}$
R_6
C_H
1000pF
CHANNEL B
$R_1 = R_3 \| R_4$
$R_6 = R_2 \| R_5$

APPLICATION CIRCUITS

ALTERNATE GAIN CONFIGURATION

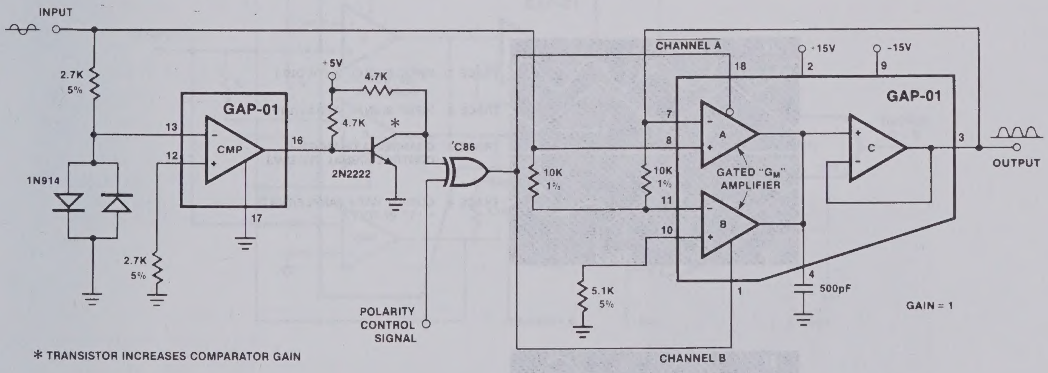

R2
CHANNEL A
GAP-01
CHANNEL A INPUT
R3
A
C
OUTPUT
CHANNEL B INPUT
R4
B
R1
CH
1000pF
CHANNEL B

$R_3 = R_4 = \frac{1}{\frac{1}{R_1} + \frac{1}{R_2}}$

$R_3 > 2.4k\Omega$
$R_4 > 2.4k\Omega$

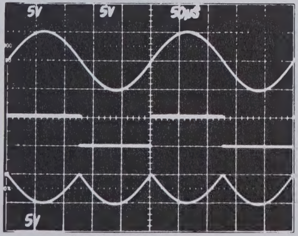
IF BOTH CHANNEL A AND CHANNEL B HAVE THE SAME POSITIVE VOLTAGE GAIN, A SINGLE VOLTAGE DIVIDER SETS THE GAIN FOR BOTH CHANNELS.

ABSOLUTE VALUE CIRCUIT WITH POLARITY PROGRAMMABLE OUTPUT


INPUT
2.7K
5%
GAP-01
13
12
CMP
16
17
1N914
2.7K
5%
+5V
4.7K
4.7K
*
2N2222
'C86
POLARITY CONTROL SIGNAL
10K
1%
10K
1%
CHANNEL A
+15V
-15V
18
2
9
GAP-01
7
8
11
10
A
B
C
3
OUTPUT
GATED "GM" AMPLIFIER
5.1K
5%
1
4
500pF
CHANNEL B

GAIN = 1

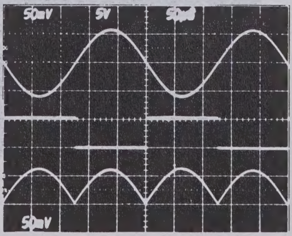
* TRANSISTOR INCREASES COMPARATOR GAIN



TRACE 1: INPUT SIGNAL

TRACE 2: CHANNEL A/CHANNEL B CONTROL SIGNAL

TRACE 3: OUTPUT. POLARITY CONTROL SIGNAL = 0

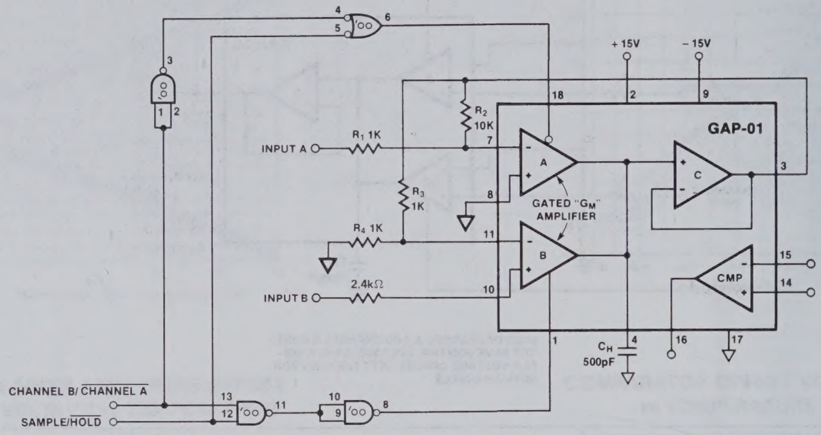


TRACE 1: INPUT SIGNAL

TRACE 2: CHANNEL A/CHANNEL B CONTROL SIGNAL

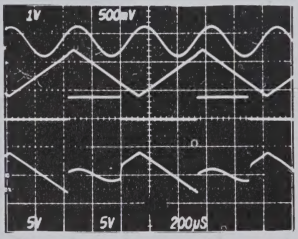
TRACE 3: OUTPUT. POLARITY CONTROL SIGNAL = 1

TWO-CHANNEL SAMPLE/HOLD AMPLIFIER


4
5
6
3
1
2
+15V
-15V
18
2
9
GAP-01
R2
10K
INPUT A
R1 1K
7
A
C
3
8
GATED "GM" AMPLIFIER
R3
1K
R4 1K
11
B
15
14
CMP
2.4kΩ
INPUT B
10
1
CH
500pF
4
16
17
CHANNEL B/CHANNEL A
SAMPLE/HOLD
13
12
11
10
9
8

CHANNEL A GAIN $= -\frac{R_2}{R_1} = -10$

CHANNEL B GAIN $= 1 + \frac{R_2}{R_1} = 2$

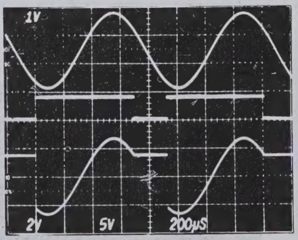


TRACE 1: INPUT SIGNAL B (1V/DIV.)

TRACE 2: INPUT SIGNAL A (0.5V/DIV.)

TRACE 3: CHANNEL A/CHANNEL B CONTROL SIGNAL (5V/DIV.)

TRACE 4: OUTPUT WITH SAMPLE/HOLD = "1" (5V/DIV.)



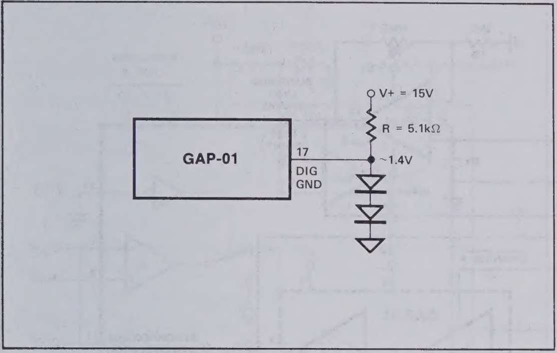
TRACE 1: INPUT SIGNAL B (1V/DIV.)

TRACE 2: SAMPLE/HOLD (5V/DIV.) CONTROL SIGNAL

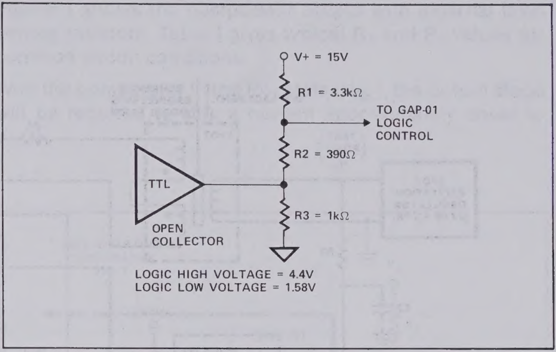
TRACE 3: OUTPUT SIGNAL (2V/DIV.) CHANNEL A/CHANNEL B = "1"

APPLICATION CIRCUITS

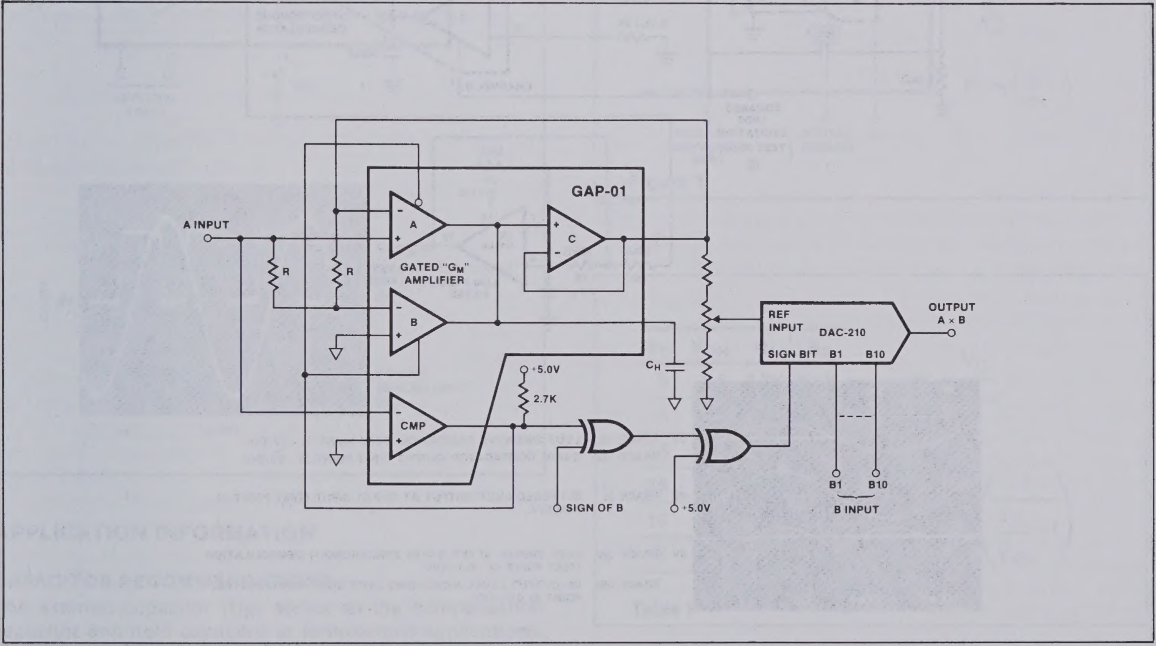
DIGITAL GROUND CONNECTION FOR SINGLE SUPPLY OPERATION


V+ = 15V
R = 5.1kΩ
GAP-01
17
DIG
GND
~1.4V

LOGIC LEVEL TRANSLATION FOR GAP-01 SINGLE SUPPLY OPERATION

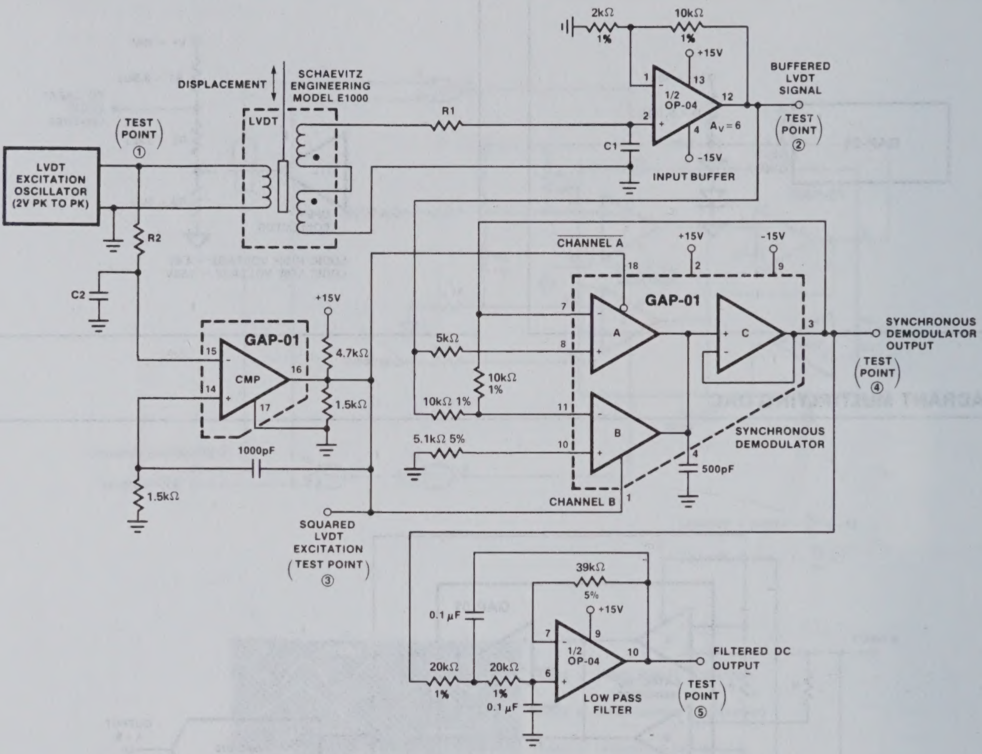

V+ = 15V
R1 = 3.3kΩ
TO GAP-01
LOGIC
CONTROL
R2 = 390Ω
TTL
R3 = 1kΩ
OPEN
COLLECTOR
LOGIC HIGH VOLTAGE = 4.4V
LOGIC LOW VOLTAGE = 1.58V

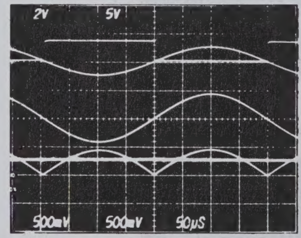
FOUR QUADRANT MULTIPLYING DAC


GAP-01
A INPUT
A
C
R
R
GATED "G_M"
AMPLIFIER
B
+5.0V
2.7K
CMP
C_H
REF
INPUT
DAC-210
SIGN BIT
B1
B10
OUTPUT
A × B
SIGN OF B
+5.0V
B1
B10
B INPUT

APPLICATION CIRCUITS

SYNCHRONOUS DEMODULATION OF LVDT SIGNAL


2kΩ 1%
10kΩ 1%
+15V
1
13
1/2 OP-04
12
2
4
$A_V = 6$
-15V
C1
INPUT BUFFER
BUFFERED LVDT SIGNAL
TEST POINT ②
DISPLACEMENT
SCHAEVITZ ENGINEERING MODEL E1000
LVDT
R1
TEST POINT ①
LVDT EXCITATION OSCILLATOR (2V PK TO PK)
R2
C2
+15V
GAP-01
15
16
14
17
CMP
4.7kΩ
1.5kΩ
1000pF
1.5kΩ
SQUARED LVDT EXCITATION
TEST POINT ③
CHANNEL A
+15V
-15V
18
2
9
GAP-01
7
A
8
5kΩ
10kΩ 1%
10kΩ 1%
11
B
5.1kΩ 5%
10
C
3
4
500pF
1
CHANNEL B
SYNCHRONOUS DEMODULATOR
SYNCHRONOUS DEMODULATOR OUTPUT
TEST POINT ④
39kΩ 5%
+15V
0.1 μF
7
9
1/2 OP-04
10
20kΩ 1%
20kΩ 1%
6
0.1 μF
LOW PASS FILTER
FILTERED DC OUTPUT
TEST POINT ⑤



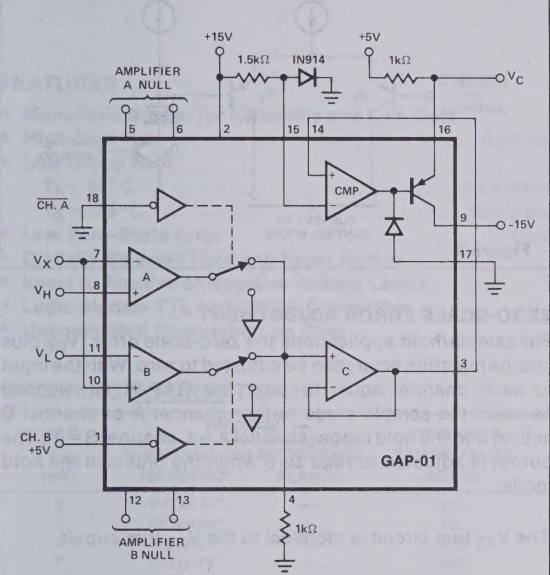
0V TRACE 1A: LVDT SINEWAVE EXCITATION (TEST POINT 1) –2V/DIV.
TRACE 1B: GAP-01 COMPARATOR OUTPUT (TEST POINT 3) –5V/DIV.

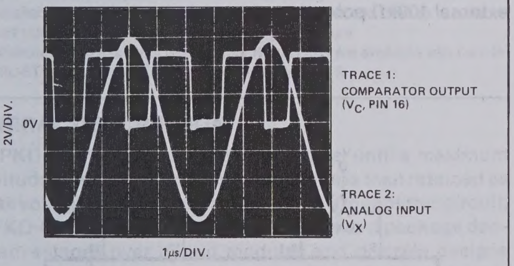
0V TRACE 2: BUFFERED LVDT OUTPUT AT GAP-01 INPUT (TEST POINT 2) 0.5V/DIV.

0V TRACE 3A: LVDT SIGNAL AFTER GAP-01 SYNCHRONOUS DEMODULATION (TEST POINT 4) –0.5V/DIV.
TRACE 3B: DC OUTPUT LEVEL INDICATING LVDT CORE POSITION (TEST POINT 5) 0.5V/DIV.

APPLICATION CIRCUITS

WINDOW COMPARATOR


+15V
1.5kΩ
IN914
+5V
1kΩ
V_C
AMPLIFIER A NULL
5
6
2
15
14
16
CMP
CH. A
18
9
-15V
V_X
7
A
V_H
8
17
V_L
11
B
10
C
3
CH. B +5V
1
GAP-01
12
13
4
1kΩ
AMPLIFIER B NULL



APPLICATION INFORMATION

CAPACITOR RECOMMENDATIONS

The external capacitor (C_H) serves as the compensation capacitor and hold capacitor in sample/hold applications. Stable operation requires a minimum value of 500pF. Larger capacitors may be used to lower droop rate errors, but acquisition time will increase and bandwidth decrease.

The capacitor should have very high insulation resistance and low dielectric absorption. For temperatures below 85° C, a polystyrene capacitor is recommended, while a Teflon capacitor is recommended for high temperature environments.

COMPARATOR

The comparator output high level (V_{OH}) is set by external resistors. It's possible to optimize noise immunity while interfacing to all standard logic families — TTL, DTL, and CMOS. Figure 1 shows the comparator output with external level setting resistors. Table I gives typical R_1 and R_2 values for common circuit conditions.

With the comparator in the low state (V_{OL}), the output stage will be required to sink a current approximately equal to V_C/R_1.

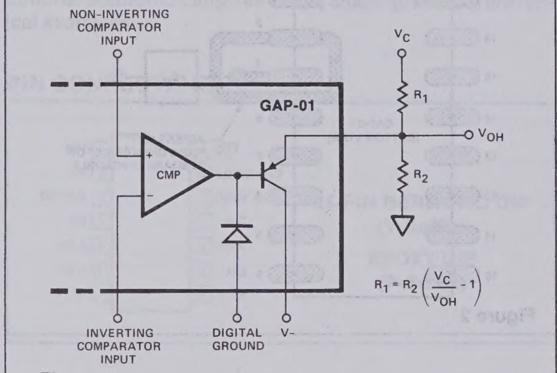

NON-INVERTING COMPARATOR INPUT
GAP-01
CMP
V_C
R_1
V_{OH}
R_2
$R_1 = R_2\left(\frac{V_C}{V_{OH}} - 1\right)$
INVERTING COMPARATOR INPUT
DIGITAL GROUND
V-

Figure 1

V_C	V_{OH}	R_1	R_2
5	3.5	2.7K	6.2K
5	5.0	2.7K	∞
15	3.5	4.7K	1.5K
15	5.0	4.7K	2.4K
15	7.5	7.5K	7.5K
15	10.0	7.5K	15K

$$R_1 \approx \frac{V_C}{I_{sink}}$$

$$R_2 \approx R_1\left(\frac{1}{\frac{V_C}{V_{OH}} - 1}\right)$$

Table I

The maximum comparator high output voltage (V_{OH}) should be constrained to: $V_{OH}\,(max) < V+ -2V$

CAPACITOR GUARDING AND GROUND LAYOUT

Ground planes are recommended to minimize ground path resistance. Separate analog and digital grounds should be used. The two ground systems are tied together only at the common system ground. This avoids digital currents returning to the system ground through the analog ground path.

The C_H terminal (Pin 4) is a high-impedance point. To minimize gain errors and maintain the GAP-01's inherently low droop rate, guarding Pin 4 as shown in Figure 2 is recommended.

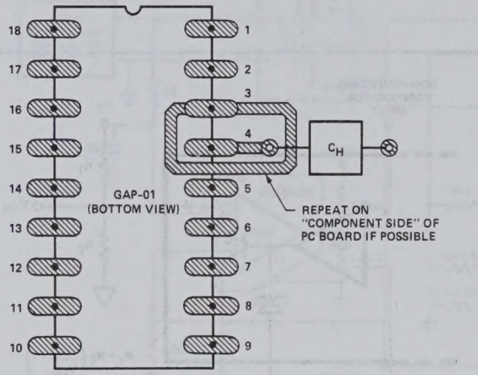

18
17
16
15
14
13
12
11
10
1
2
3
4
5
6
7
8
9
GAP-01
(BOTTOM VIEW)
C_H
REPEAT ON
"COMPONENT SIDE" OF
PC BOARD IF POSSIBLE

Figure 2

LOGIC CONTROL

The transconductance amplifier outputs are switched by the digital logic signals applied at $\overline{\text{Channel A}}$ and Channel B pins. Two signal paths through the GAP-01 are possible.

The logic threshold voltage is 1.4 volts when digital ground is at zero volts. Other threshold voltages (V_{TH}) may be selected by applying the formula:

$$V_{TH} \approx 1.4V + \text{Digital Ground Potential.}$$

Figure 3 shows the simplified logic control circuit. For proper operation, digital ground must always be at least 3.5V below the positive supply and 2.5V above the negative supply. The logic signals must always be at least 2.8V above the negative supply.

Operating the digital ground at other than zero volts does influence the comparator output low voltage. The V_{OL} level is referenced to digital ground and will follow any changes in digital ground potential:

$$V_{OL} \approx 0.2V + \text{Digital Ground Potential.}$$

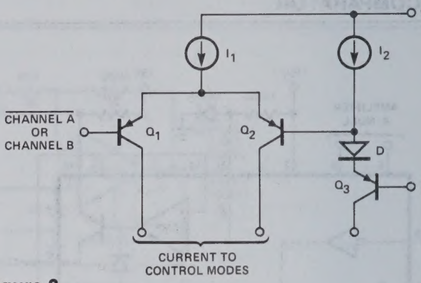

V+
I_1
I_2
CHANNEL A
OR
CHANNEL B
Q_1
Q_2
D
Q_3
DIGITAL
GROUND
CURRENT TO
CONTROL MODES

Figure 3

ZERO-SCALE ERROR ADJUSTMENT

For sample/hold applications the zero-scale error (V_{OS} plus charge injection error) can be adjusted to zero. With the input to each channel equal to zero, the GAP-01 is switched between the sample mode (either channel A or channel B active) and the hold mode ($\overline{\text{channel A}}$ = 1, channel B = 0). The output is adjusted to read zero when the unit is in the hold mode.

The V_{ZS} trim circuit is identical to the V_{OS} trim circuit.

OFFSET VOLTAGE ERROR ADJUSTMENT Offset voltage through either $\overline{\text{channel A}}$ or channel B may be nulled with an external 100kΩ potentiometer as shown below.

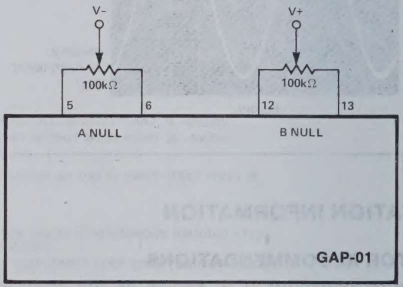

V-
V+
100kΩ
100kΩ
5
6
12
13
A NULL
B NULL
GAP-01

Figure 4

MONOLITHIC PEAK DETECTOR (WITH RESET-AND-HOLD MODE)

PKD-01

FEATURES

- **Monolithic Design for Reliability and Low Cost**
- **High Slew Rate 0.5V/μs**
- **Low Droop Rate**
  - **$T_A = 25°C$ 0.1mV/ms**
  - **$T_A = 125°C$ 10mV/ms**
- **Low Zero-Scale Error 4mV**
- **Digitally Selected Hold and Reset Modes**
- **Reset to Positive or Negative Voltage Levels**
- **Logic Signals TTL and CMOS Compatible**
- **Uncommitted Comparator on Chip**

ORDERING INFORMATION†

25°C V_{ZS} (mV)	PACKAGE 14-PIN DUAL-IN-LINE PACKAGE HERMETIC*	PLASTIC	OPERATING TEMPERATURE RANGE
4	PKD01AY*	—	MIL
7	PKD01BY*	—	MIL
4	PKD01EY	—	IND
7	PKD01FY	—	IND
4	—	PKD01EP	COM
7	—	PKD01FP	COM

*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

GENERAL DESCRIPTION

The PKD-01 tracks an analog input signal until a maximum amplitude is reached. The maximum value is then retained as a peak voltage on a hold capacitor. Being a monolithic circuit, the PKD-01 offers significant performance and package density advantages over hybrid modules and discrete designs without sacrificing system versatility. The matching characteristics attained in a monolithic circuit provide inherent advantages when charge injection and droop rate error reduction are primary goals.

Innovative design techniques maximize the advantages of monolithic technology. Transconductance (g_m) amplifiers were chosen over conventional voltage amplifier circuit building blocks. The "g_m" amplifiers simplify internal frequency compensation, minimize acquisition time and maximize circuit accuracy. Their outputs are easily switched by low glitch current steering circuits. The steered outputs are clamped to reduce charge injection errors upon entering the hold mode or exiting the reset mode. The inherently low zero-scale error is reduced further by active "Zener-Zap" trimming to optimize overall accuracy.

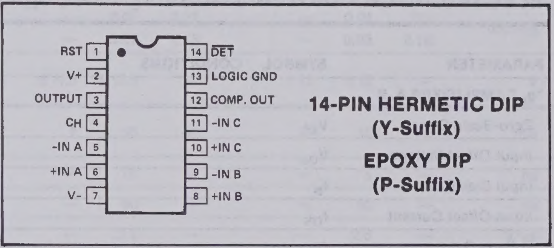
The output buffer amplifier features an FET input stage to reduce droop rate error during lengthy peak hold periods. A bias current cancellation circuit minimizes droop error at high ambient temperatures.

Through the $\overline{\text{DET}}$ control pin, new peaks may either be detected or ignored. Detected peaks are presented as positive output levels. Positive or negative peaks may be detected without additional active circuits since amplifier A can operate as an inverting or non-inverting gain stage.

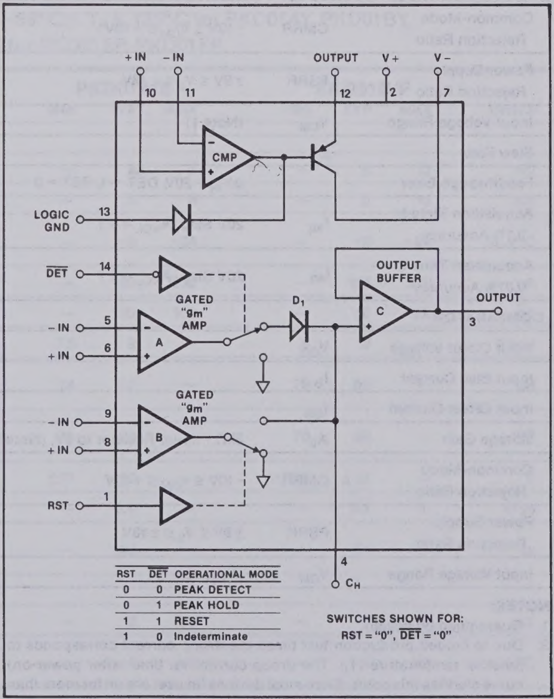
An uncommitted comparator provides many application options. Status indication and logic shaping/shifting are typical examples.

Manufactured under the following patent: 4,285,051

PIN CONNECTIONS



FUNCTIONAL DIAGRAM



RST	$\overline{\text{DET}}$	OPERATIONAL MODE
0	0	PEAK DETECT
0	1	PEAK HOLD
1	1	RESET
1	0	Indeterminate

SWITCHES SHOWN FOR:
RST = "0", $\overline{\text{DET}}$ = "0"

ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage	±18V
Power Dissipation	500mW
Input Voltage	Equal to Supply Voltage
Logic and Logic Ground Voltage	Equal to Supply Voltage
Output Short Circuit Duration	Indefinite
Amplifier A or B Differential Input Voltage	±24V
Comparator Differential Input Voltage	±24V
Comparator Output Voltage	Equal to Positive Supply Voltage
Hold Capacitor Short Circuit Duration	Indefinite
Lead Temperature (Soldering, 60 sec)	300°C
Storage Temperature Range	
PKD01AY, PKD01BY	−65°C to +150°C
PKD01EY, PKD01FY	−65°C to +150°C
PKD01EP, PKD01FP	−65°C to +125°C
Operating Temperature Range	
PKD01AY, PKD01BY	−55°C to +125°C
PKD01EY, PKD01FY	−25°C to +85°C
PKD01EP, PKD01FP	0°C to +70°C
Dice Junction Temperature	−65°C to +150°C

PACKAGE (Note 1)	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
14-Pin DIP (Y)	80°C	10mW/°C
14-Pin DIP (P)	50°C	6mW/°C

NOTES:

1. Maximum package power dissipation vs. ambient temperature.
2. Absolute ratings apply to both packaged parts and DICE, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $C_H = 1000pF$, $T_A = 25°C$.

PARAMETER	SYMBOL	CONDITIONS	PKD01A/E MIN	PKD01A/E TYP	PKD01A/E MAX	PKD01B/F MIN	PKD01B/F TYP	PKD01B/F MAX	UNITS
"g_m" AMPLIFIERS A, B									
Zero-Scale Error	V_{ZS}		—	2	4	—	3	7	mV
Input Offset Voltage	V_{OS}		—	2	3	—	3	6	mV
Input Bias Current	I_B		—	80	150	—	80	250	nA
Input Offset Current	I_{OS}		—	20	40	—	20	75	nA
Voltage Gain	A_V		18	25	—	10	25	—	V/mV
Open-Loop Bandwidth	BW	$A_V = 1$	—	0.4	—	—	0.4	—	MHz
Common-Mode Rejection Ratio	CMRR	$-10V \le V_{CM} \le +10V$	80	90	—	74	90	—	dB
Power Supply Rejection Ratio	PSRR	$\pm9V \le V_S \le \pm18V$	86	96	—	76	96	—	dB
Input Voltage Range	V_{CM}	(Note 1)	±11.5	±12	—	±11.5	±12	—	V
Slew Rate	SR		—	0.5	—	—	0.5	—	V/μs
Feedthrough Error		$\Delta V_{IN} = 20V$, $\overline{DET} = 1$, RST = 0	66	80	—	66	80	—	dB
Acquisition Time to 0.1% Accuracy	t_{aq}	20V Step, $A_{VCL} = +1$	—	41	70	—	41	70	μs
Acquisition Time to 0.01% Accuracy	t_{aq}	20V Step, $A_{VCL} = +1$	—	45	—	—	45	—	μs
COMPARATOR									
Input Offset Voltage	V_{OS}		—	0.5	1.5	—	1	3	mV
Input Bias Current	I_B		—	700	1000	—	700	1000	nA
Input Offset Current	I_{OS}		—	75	300	—	75	300	nA
Voltage Gain	A_V	2kΩ Pull-up Resistor to 5V, (Note 1)	5	7.5	—	3.5	7.5	—	V/mV
Common-Mode Rejection Ratio	CMRR	$-10V \le V_{CM} \le +10V$	82	106	—	82	106	—	dB
Power Supply Rejection Ratio	PSRR	$\pm9V \le V_S \le \pm18V$	76	90	—	76	90	—	dB
Input Voltage Range	V_{CM}	(Note 1)	±11.5	±12.5	—	±11.5	±12.5	—	V

NOTES:

1. Guaranteed by design.
2. Due to limited production test times the droop current corresponds to junction temperature (T_j). The droop current vs. time (after power-on) curve clarifies this point. Since most devices (in use) are on for more than 1 second, PMI specifies droop rate for ambient temperature (T_A) also. The warmed-up (T_A) droop current specification is correlated to the junction temperature (T_j) value. PMI has a droop current cancellation circuit which minimizes droop current at high temperature. Ambient (T_A) temperature specifications are not subject to production testing.
3. $\overline{DET} = 1$, RST = 0.

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $C_H = 1000pF$, $T_A = 25°C$. (Continued)

PARAMETER	SYMBOL	CONDITIONS	PKD01A/E			PKD01B/F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Low Output Voltage	V_{OL}	$I_{SINK} \leq 5mA$, Logic GND = 5V	−0.2	0.15	0.4	−0.2	0.15	0.4	V
"OFF" Output Leakage Current	I_L	$V_{OUT} = 5V$	—	25	80	—	25	80	μA
Output Short Circuit Current	I_{SC}	$V_{OUT} = 5V$	7	12	45	7	12	45	mA
Response Time	t_S	5mV Overdrive, (Note 3) 2kΩ Pull-up Resistor to 5V	—	150	—	—	150	—	ns
DIGITAL INPUTS-RST, $\overline{DET}$ (See Note 3)									
Logic "1" Input Voltage	V_H		2	—	—	2	—	—	V
Logic "0" Input Voltage	V_L		—	—	0.8	—	—	0.8	V
Logic "1" Input Current	I_{INH}	$V_H = 3.5V$	—	0.02	1	—	0.02	1	μA
Logic "0" Input Current	I_{INL}	$V_L = 0.4V$	—	1.6	10	—	1.6	10	μA
MISCELLANEOUS									
Droop Rate	V_{DR}	$T_j = 25°C$, (See Note 2) $T_A = 25°C$	— —	0.01 0.02	0.07 0.15	— —	0.01 0.03	0.1 0.20	mV/ms
Output Voltage Swing: Amplifier C	V_{OP}	$\overline{DET} = 1$ $R_L = 2.5k$	±11.5	±12.5	—	±11	±12	—	V
Short Circuit Current: Amplifier C	I_{SC}		7	15	40	7	15	40	mA
Switch Aperture Time	t_{ap}		—	75	—	—	75	—	ns
Switch Switching Time	ts		—	50	—	—	50	—	ns
Slew Rate: Amplifier C	SR	$R_L = 2.5k$	—	2.5	—	—	2.5	—	V/μs
Power Supply Current	I_{SY}	No Load	—	5	7	—	6	9	mA

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $C_H = 1000pF$, $-55°C \leq T_A \leq 125°C$ for PKD01AY, PKD01BY, $-25°C \leq T_A \leq 85°C$ for PKD01EY, PKD01FY and $0°C \leq T_A \leq 70°C$ for PKD01EP, PKD01FP.

PARAMETER	SYMBOL	CONDITIONS	PKD01A/E			PKD01B/F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
"g_m" AMPLIFIERS A, B									
Zero-Scale Error	V_{ZS}		—	4	7	—	6	12	mV
Input Offset Voltage	V_{OS}		—	3	6	—	5	10	mV
Average Input Offset Drift	TCV_{OS}	(Note 1)	—	−9	−24	—	−9	−24	μV/°C
Input Bias Current	I_B		—	160	250	—	160	500	nA
Input Offset Current	I_{OS}		—	30	100	—	30	150	nA
Voltage Gain	A_V		7.5	9	—	5	9	—	V/mV
Common-Mode Rejection Ratio	CMRR	$-10V \leq V_{CM} \leq +10V$	74	82	—	72	80	—	dB
Power Supply Rejection Ratio	PSRR	$\pm9V \leq V_S \leq \pm18V$	80	90	—	70	90	—	dB
Input Voltage Range	V_{CM}	(Note 1)	±11	±12	—	±10.5	±12	—	V
Slew Rate	SR		—	0.4	—	—	0.4	—	V/μs
Acquisition Time to 0.1% Accuracy	t_{aq}	20V Step, $A_{VCL} = +1$	—	60	—	—	60	—	μs
COMPARATOR									
Input Offset Voltage	V_{OS}		—	2	2.5	—	2	5	mV
Average Input Offset Drift	TCV_{OS}	(Note 1)	—	−4	−6	—	−4	−6	μV/°C
Input Bias Current	I_B		—	1000	2000	—	1100	2000	nA

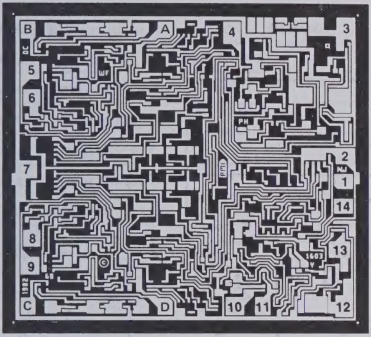
ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $C_H = 1000pF$, $-55°C \le T_A \le 125°C$ for PKD01AY, PKD01BY, $-25°C \le T_A \le 85°C$ for PKD01EY, PKD01FY and $0°C \le T_A \le 70°C$ for PKD01EP, PKD01FP. (Continued)

PARAMETER	SYMBOL	CONDITIONS	PKD01A/E			PKD01B/F			
			MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Current	I_{OS}		—	100	600	—	100	600	nA
Voltage Gain	A_V	2kΩ Pull-up Resistor to 5V	4	6.5	—	2.5	6.5	—	V/mV
Common-Mode Rejection Ratio	CMRR	$-10V \le V_{CM} \le +10V$	80	100	—	80	92	—	dB
Power Supply Rejection Ratio	PSRR	$\pm9V \le V_S \le \pm18V$	72	82	—	72	86	—	dB
Input Voltage Range	V_{CM}	(Note 1)	±11	—	—	±11	—	—	V
Low Output Voltage	V_{OL}	$I_{SINK} \le 5mA$, Logic GND = 5V	−0.2	0.15	0.4	−0.2	0.15	0.4	V
"OFF" Output Leakage Current	I_L	$V_{OUT} = 5V$	—	25	100	—	100	180	μA
Output Short Circuit Current	I_{SC}	$V_{OUT} = 5V$	6	10	45	6	10	45	mA
Response Time	t_S	5mV Overdrive, 2kΩ Pull-up Resistor to 5V	—	200	—	—	200	—	ns
DIGITAL INPUTS-RST, DET (See Note 3)									
Logic "1" Input Voltage	V_H		2	—	—	2	—	—	V
Logic "0" Input Voltage	V_L		—	—	0.8	—	—	0.8	V
Logic "1" Input Current	I_{INH}	$V_H = 3.5V$	—	0.02	1	—	0.02	1	μA
Logic "0" Input Current	I_{INL}	$V_L = 0.4V$	—	2.5	15	—	2.5	15	μA
MISCELLANEOUS									
Droop Rate	V_{DR}	T_j = Max. Operating Temp T_A = Max. Operating Temp. $\overline{DET} = 1$, (Note 2)	— —	1.2 2.4	10 20	— —	3 6	15 20	mV/ms
Output Voltage Swing: Amplifier C	V_{OP}	$R_L = 2.5k$	±11	±12	—	±10.5	±12	—	V
Short Circuit Current: Amplifier C	I_{SC}		6	12	40	6	12	40	mA
Switch Aperture Time	t_{ap}		—	75	—	—	75	—	ns
Slew Rate: Amplifier C	SR	$R_L = 2.5k$	—	2	—	—	2	—	V/μs
Power Supply Current	I_{SY}	No Load	—	5.5	8	—	6.5	10	mA

NOTES:

1. Guaranteed by design.
2. Due to limited production test times the droop current corresponds to junction temperature (T_j). The droop current vs. time (after power-on) curve clarifies this point. Since most devices (in use) are on for more than 1 second, PMI specifies droop rate for ambient temperature (T_A) also. The warmed-up (T_A) droop current specification is correlated to the junction temperature (T_j) value. PMI has a droop current cancellation circuit which minimizes droop current at high temperature. Ambient (T_A) temperature specifications are not subject to production testing.
3. $\overline{DET} = 1$, RST = 0.

DICE CHARACTERISTICS



1. RST (RESET CONTROL)
2. V+
3. OUTPUT
4. C_H (HOLD CAPACITOR)
5. INVERTING INPUT (A)
6. NON-INVERTING INPUT (A)
7. V−
8. NON-INVERTING INPUT (B)
9. INVERTING INPUT (B)
10. COMPARATOR NON-INVERTING INPUT
11. COMPARATOR INVERTING INPUT
12. COMPARATOR OUTPUT
13. LOGIC GROUND
14. $\overline{\text{DET}}$ (PEAK DETECT CONTROL)

A,B (A) NULL
C,D (B) NULL

DIE SIZE 0.090 × 0.100 inch, 9000 sq. mils
(2.286 × 2.54mm, 5.8 sq mm)

For additional DICE information
refer to Section 2.

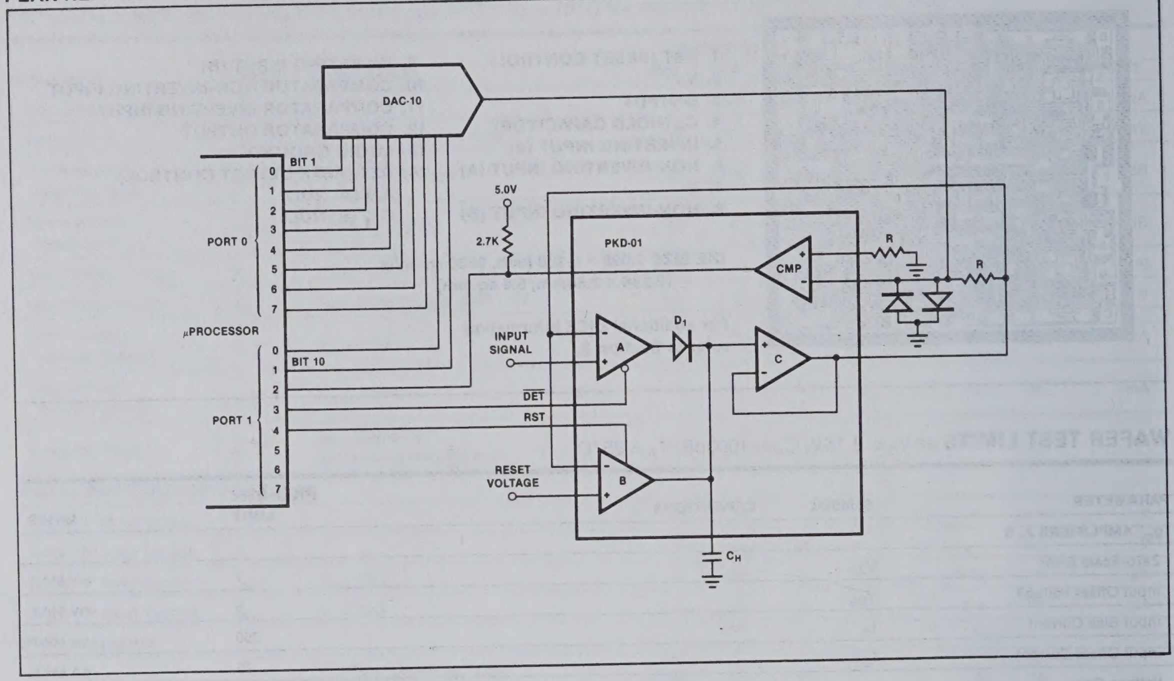
WAFER TEST LIMITS at $V_S = \pm 15V$, $C_H = 1000pF$, $T_A = 25°C$.

PARAMETER	SYMBOL	CONDITIONS	PKD-01N LIMIT	UNITS
"g_m" AMPLIFIERS A, B				
Zero-Scale Error	V_{ZS}		7	mV MAX
Input Offset Voltage	V_{OS}		6	mV MAX
Input Bias Current	I_B		250	nA MAX
Input Offset Current	I_{OS}		75	nA MAX
Voltage Gain	A_V		10	V/mV MIN
Common-Mode Rejection Ratio	CMRR	$-10V \le V_{CM} \le +10V$	74	dB MIN
Power Supply Rejection Ratio	PSRR	$\pm 9V \le V_S \pm 18V$	76	dB MIN
Input Voltage Range	V_{CM}	(Note 1)	±11.5	V MIN
Feedthrough Error		$\Delta V_{IN} = 20V$, $\overline{DET} = 1$, RST = 0	66	dB MIN
COMPARATOR				
Input Offset Voltage	V_{OS}		3	mV MAX
Input Bias Current	I_B		1000	nA MAX
Input Offset Current	I_{OS}		300	nA MAX
Voltage Gain	A_V	2kΩ Pull-up Resistor to 5V, (Note 1)	3.5	V/mV MIN
Common-Mode Rejection Ratio	CMRR	$-10V \le V_{CM} \le +10V$	82	dB MIN
Power Supply Rejection Ratio	PSRR	$\pm 9V \le V_S \le \pm 18V$	76	dB MIN
Input Voltage Range	V_{CM}	(Note 1)	±11.5	V MIN
Low Output Voltage	V_{OL}	$I_{SINK} \le 5mA$, Logic GND = 5V	0.4 −0.2	V MAX V MIN
"OFF" Output Leakage Current	I_L	$V_{OUT} = 5V$	80	μA MAX
Output Short Circuit Current	I_{SC}	$V_{OUT} = 5V$	45 7	mA MAX mA MIN

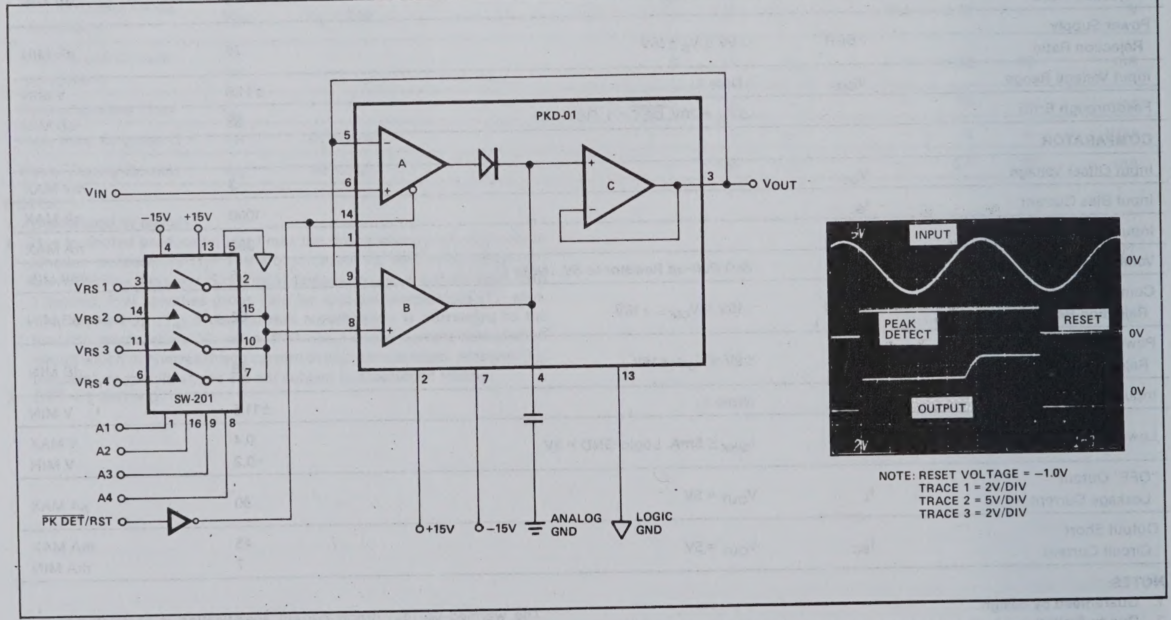
NOTES:

1. Guaranteed by design.
2. Due to limited production test times the droop current corresponds to junction temperature (T_j). The droop current vs. time (after power-on) curve clarifies this point. Since most devices (in use) are on for more than 1 second, PMI specifies droop rate for ambient temperature (T_A) also. The warmed-up (T_A) droop current specification is correlated to the junction temperature (T_j) value. PMI has a droop current cancellation circuit which minimizes droop current at high temperature. Ambient (T_A) temperature specifications are not subject to production testing.
3. $\overline{DET} = 1$, RST = 0.

PEAK READING A/D CONVERTER


DAC-10
BIT 1
0
1
2
3
PORT 0
4
5
6
7
μPROCESSOR
0
BIT 10
1
2
3
PORT 1
4
5
6
7
5.0V
2.7K
PKD-01
CMP
R
R
INPUT SIGNAL
A
D1
C
DET
RST
RESET VOLTAGE
B
CH

POSITIVE PEAK DETECTOR WITH SELECTABLE RESET VOLTAGE


PKD-01
5
A
6
C
3
VOUT
VIN
−15V
+15V
4
13
5
14
1
9
B
8
VRS 1
3
2
VRS 2
14
15
VRS 3
11
10
VRS 4
6
7
SW-201
1
16
9
8
A1
A2
A3
A4
PK DET/RST
2
7
4
13
+15V
−15V
ANALOG GND
LOGIC GND
INPUT
0V
PEAK DETECT
RESET
0V
0V
OUTPUT

NOTE: RESET VOLTAGE = −1.0V
TRACE 1 = 2V/DIV
TRACE 2 = 5V/DIV
TRACE 3 = 2V/DIV

WAFER TEST LIMITS at $V_S = \pm15V$, $C_H = 1000pF$, $T_A = 25°C$. (Cont'd)

PARAMETER	SYMBOL	CONDITIONS	PKD-01N LIMIT	UNITS
DIGITAL INPUTS-RST, DET (See Note 3)				
Logic "1" Input Voltage	V_H		2	V MIN
Logic "0" Input Voltage	V_L		0.8	V MAX
Logic "1" Input Current	I_{INH}	$V_H = 3.5V$	1	μA MAX
Logic "0" Input Current	I_{INL}	$V_L = 0.4V$	10	μA MAX
MISCELLANEOUS				
Droop Rate	V_{DR}	$T_j = 25°C$, $T_A = 25°C$ (See Note 2)	0.1 0.20	mV/ms MAX mV/ms MAX
Output Voltage Swing: Amplifier C	V_{OP}	$R_L = 2.5k$	±11	V MIN
Short Circuit Current: Amplifier C	I_{SC}		40 7	mA MAX mA MIN
Power Supply Current	I_{SY}	No Load	9	mA MAX

NOTES:

1. Guaranteed by design.
2. Due to limited production test times the droop current corresponds to junction temperature (T_j). The droop current vs. time (after power-on) curve clarifies this point. Since most devices (in use) are on for more than 1 second, PMI specifies droop rate for ambient temperature (T_A) also. The warmed-up (T_A) droop current specification is correlated to the junction temperature (T_j) value. PMI has a droop current cancellation circuit which minimizes droop current at high temperatures.
3. $\overline{DET} = 1$, RST = 0.

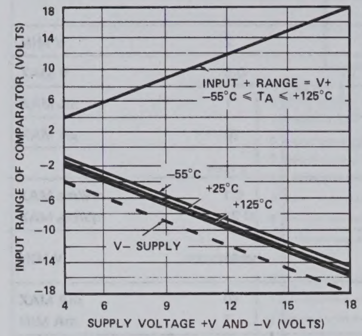
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $C_H = 1000pF$, and $T_A = 25°C$, unless otherwise noted.

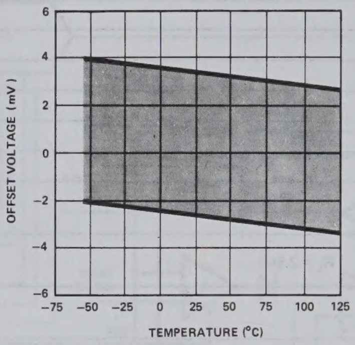
PARAMETER	SYMBOL	CONDITIONS	PKD-01N TYPICAL	UNITS
"g_m" AMPLIFIERS A, B				
Slew Rate	SR		0.5	V/μs
Acquisition Time	t_a	0.1% Accuracy, 20V step, $A_{VCL} = 1$	41	μs
Acquisition Time	t_a	0.01% Accuracy, 20V step, $A_{VCL} = 1$	45	μs
COMPARATOR				
Response Time		5mV Overdrive, 2kΩ Pull-up Resistor to +5V	150	ns
MISCELLANEOUS				
Switch Aperature Time	t_{ap}		75	ns
Switching Time	t_S		50	ns
Buffer Slew Rate	SR	$R_L = 2.5k\Omega$	2.5	V/μs

TYPICAL PERFORMANCE CHARACTERISTICS

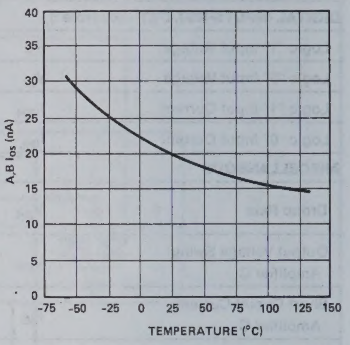
A AND B INPUT RANGE vs SUPPLY VOLTAGE



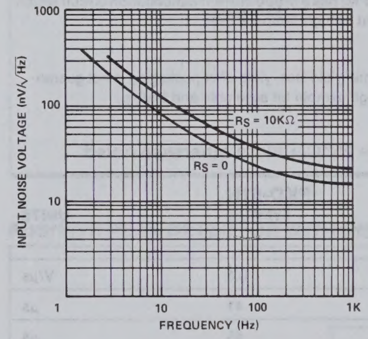
A AND B AMPLIFIERS OFFSET VOLTAGE vs TEMPERATURE



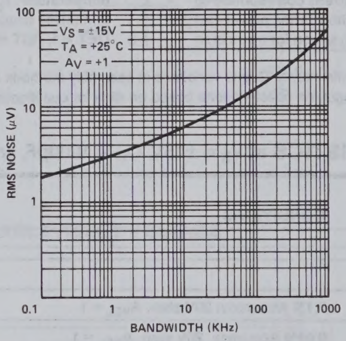
A, B I_{OS} vs TEMPERATURE



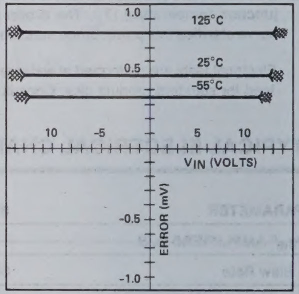
INPUT SPOT NOISE vs FREQUENCY



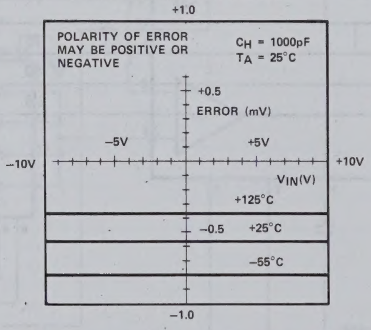
WIDEBAND NOISE vs BANDWIDTH



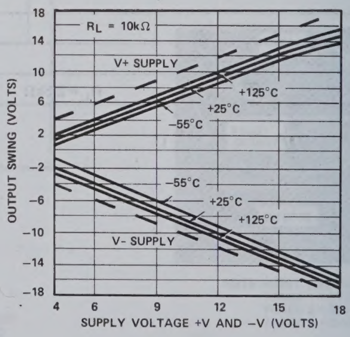
AMPLIFIER B CHARGE INJECTION ERROR vs INPUT VOLTAGE AND TEMPERATURE



AMPLIFIER CHARGE INJECTION ERROR vs INPUT VOLTAGE AND TEMPERATURE

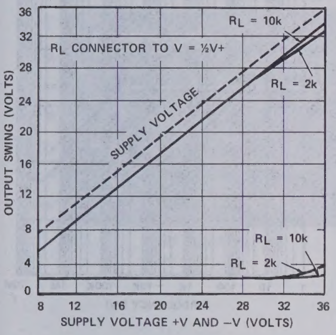


OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE (DUAL SUPPLY OPERATION)

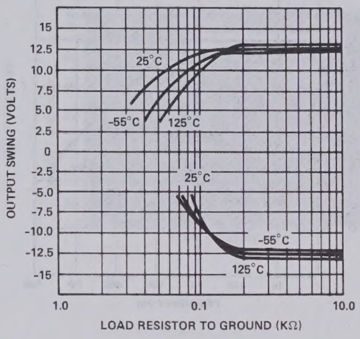


TYPICAL PERFORMANCE CHARACTERISTICS

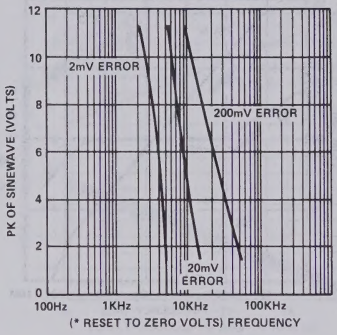
OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE (SINGLE SUPPLY OPERATION



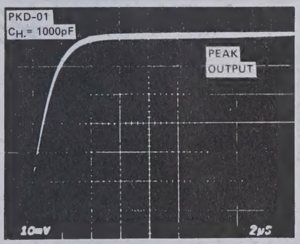
OUTPUT VOLTAGE vs LOAD RESISTANCE



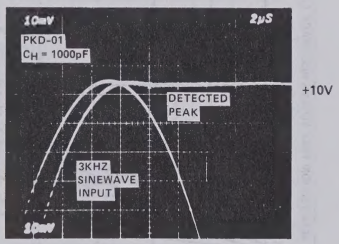
OUTPUT ERROR FOR FREQUENCY vs INPUT VOLTAGE



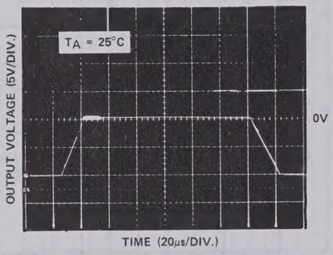
PKD-01 SETTLING RESPONSE



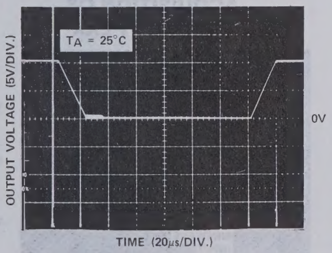
PKD-01 SETTLING RESPONSE



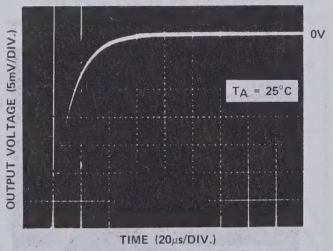
LARGE-SIGNAL INVERTING RESPONSE



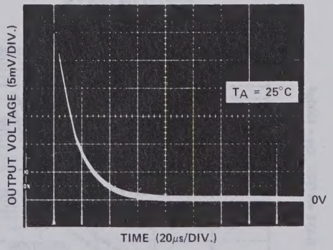
LARGE-SIGNAL NONINVERTING RESPONSE



SETTLING TIME FOR −10V TO 0V STEP INPUT

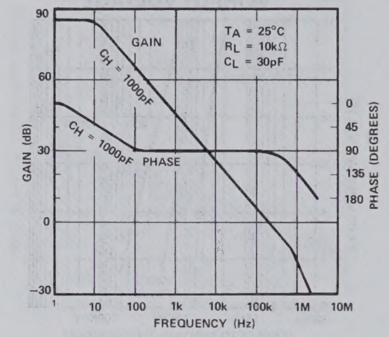


SETTLING TIME FOR +10V TO 0V STEP INPUT

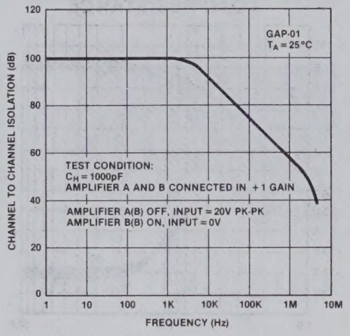


TYPICAL PERFORMANCE CHARACTERISTICS

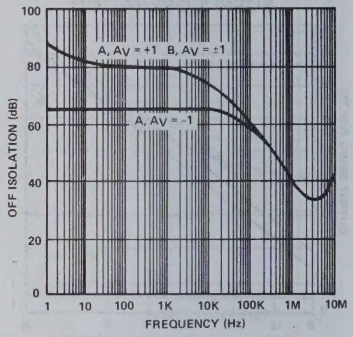
SMALL-SIGNAL OPEN LOOP GAIN/PHASE vs FREQUENCY



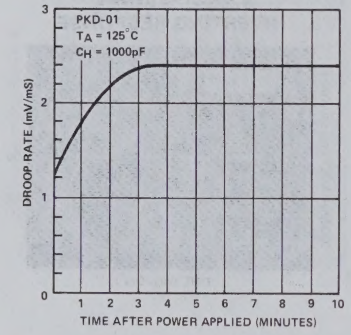
CHANNEL TO CHANNEL ISOLATION vs FREQUENCY



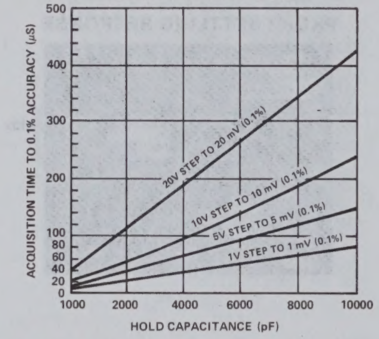
OFF ISOLATION vs FREQUENCY



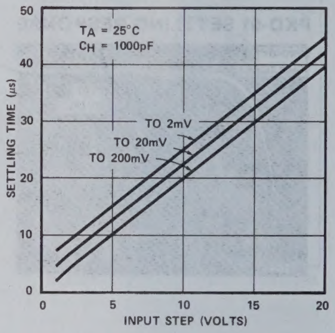
DROOP RATE vs TIME AFTER POWER ON



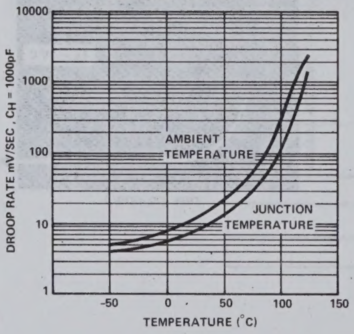
ACQUISITION TIME vs EXTERNAL HOLD CAPACITOR AND ACQUISITION STEP



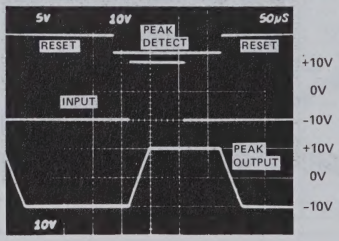
ACQUISITION TIME vs INPUT VOLTAGE STEP SIZE



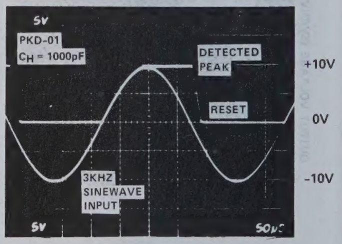
DROOP RATE vs TEMPERATURE



ACQUISITION OF STEP INPUT

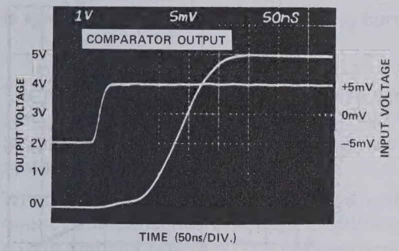


ACQUISITION OF SINEWAVE PEAK

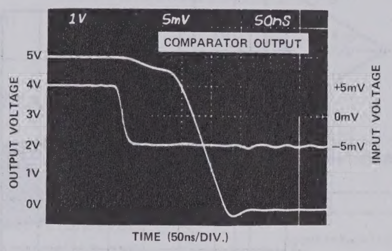


TYPICAL PERFORMANCE CHARACTERISTICS

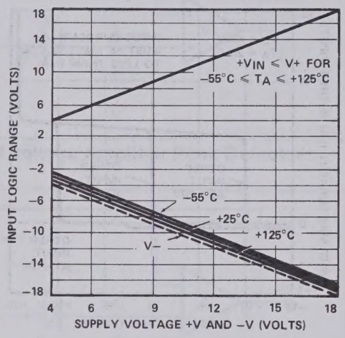
COMPARATOR OUTPUT RESPONSE TIME (2kΩ PULL-UP RESISTOR, $T_A = 25°C$)



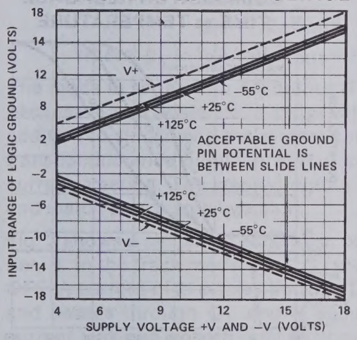
COMPARATOR OUTPUT RESPONSE TIME (2kΩ PULL-UP RESISTOR, $T_A = 25°C$)



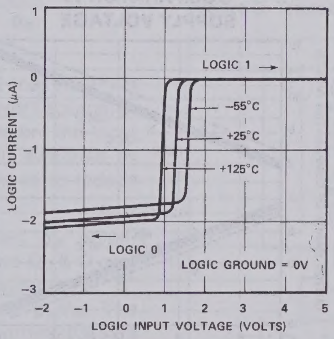
INPUT LOGIC RANGE vs SUPPLY VOLTAGE



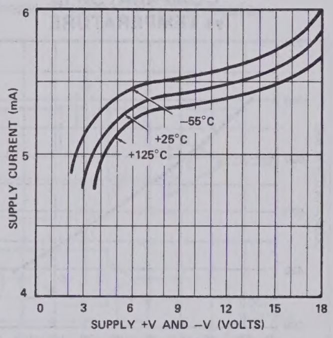
INPUT RANGE OF LOGIC GROUND vs SUPPLY VOLTAGE



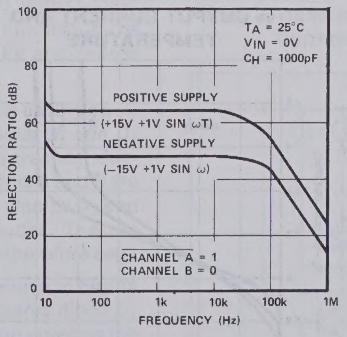
LOGIC INPUT CURRENT vs LOGIC INPUT VOLTAGE



SUPPLY CURRENT vs SUPPLY VOLTAGE

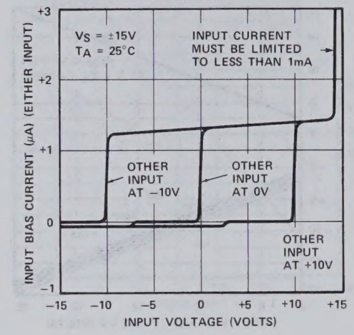


HOLD MODE POWER SUPPLY REJECTION vs FREQUENCY

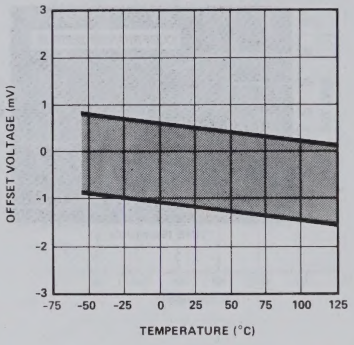


TYPICAL PERFORMANCE CHARACTERISTICS

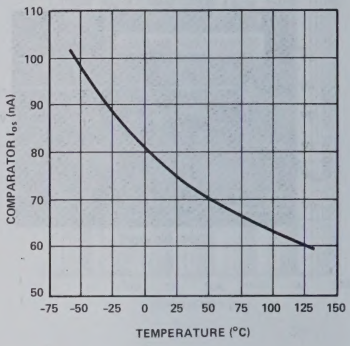
COMPARATOR INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE



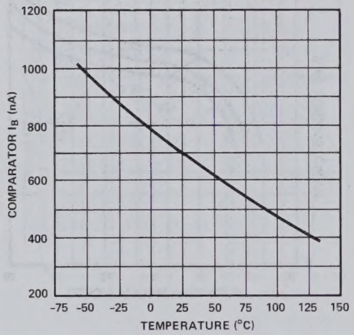
COMPARATOR OFFSET VOLTAGE vs TEMPERATURE



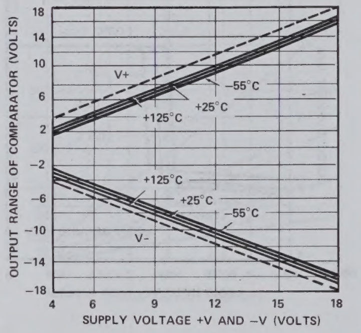
COMPARATOR I_{OS} vs TEMPERATURE



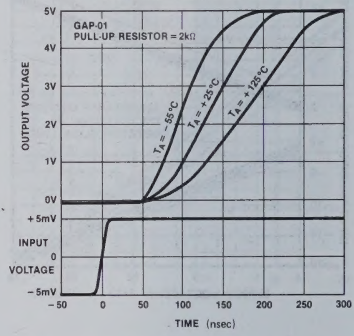
COMPARATOR I_B vs TEMPERATURE



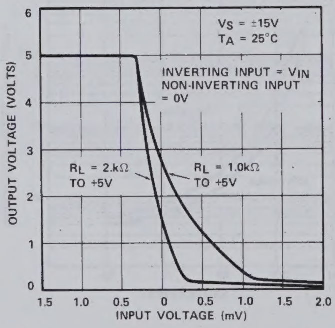
OUTPUT SWING OF COMPARATOR vs SUPPLY VOLTAGE



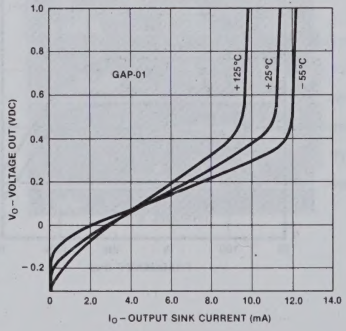
COMPARATOR RESPONSE TIME vs TEMPERATURE



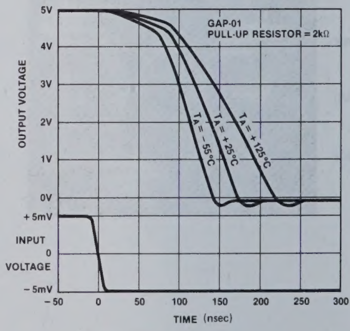
COMPARATOR TRANSFER CHARACTERISTIC



COMPARATOR OUTPUT VOLTAGE vs OUTPUT CURRENT AND TEMPERATURE



COMPARATOR RESPONSE TIME vs TEMPERATURE



THEORY OF OPERATION

The typical peak detector uses voltage amplifiers and a diode or an emitter follower to charge the hold capacitor, C_H, unidirectionally (Figure 1). The output impedance of A plus D_1's dynamic impedance, r_d, make up the resistance which determines the feedback loop pole. The dynamic impedance is $r_d = \frac{kT}{qI_d}$. I_d is the capacitor charging current.

The pole moves toward the origin of the S plane as I_d goes to zero. The pole movement in itself will not significantly lengthen the acquisition time since the pole is enclosed in the system feedback loop.

When the moving pole is considered with the typical frequency compensation of voltage amplifiers there is however, a loop stability problem. The necessary compensation can increase the required acquisition time. PMI's approach replaces the input voltage amplifier with a transconductance amplifier; Figure 2.

The PKD-01 transfer function can be reduced to:

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1 + \frac{sC_H}{g_m} + \frac{1}{g_m R_{OUT}}} \approx \frac{1}{1 + \frac{sC_H}{g_m}}$$

Where: $g_m \approx 1\mu A/mV$, $R_{OUT} \approx 20M\Omega$.

The diode in series with A's output (Figure 2) has no effect because it is a resistance in series with a current source. In addition to simplifying the system compensation, the input transconductance amplifier output current is switched by current steering. The steered output is clamped to reduce and match any charge injection.

Fig. 3 shows a simplified schematic of the reset "g_m" amplifier, B. In the track mode, Q_1 & Q_4 are ON and Q_2 & Q_3 are OFF. A current of 2I passes through D_1, I is summed at "B" and passes through Q_1, and is summed with g_mV_{IN}. The current sink can absorb only 3I, thus, the current passing through D_2 can only be: $2K - g_mV_{IN}$. The net current into the hold capacitor node then, is $g_mV_{IN} (C_H = 2I - (2I - g_mV_{IN})$. The hold mode, Q_2 & Q_3 are ON while Q_1 & Q_4 are OFF. The net current into the top of D_1 is $-I$ until D_3 turns ON. With Q_1 OFF, the bottom of D_2 is pulled up with a current I until D_4 turns ON, thus D_1 & D_2 are reverse biased by ≈0.6V and charge injection is independent of input level.

The monolithic layout results in points A and B having equal nodal capacitance. In addition, matched diodes D_1 and D_2 have equal diffusion capacitance. When the transconductance amplifier outputs are switched open, points A and B are ramped equally but in opposite phase. Diode clamps D_3 and D_4 cause the swings to have equal amplitudes. The net charge injection (voltage change) at node C is therefore zero.

The peak transconductance amplifier, A, is shown in Figure 4. Unidirectional hold capacitor charging requires diode D_1 to be connected in series with the output. Upon entering the peak hold mode D_1 is reverse biased. The voltage clamp limits charge injection to approximately 1pC and the hold step to 0.6mV.

Minimizing acquisition time dictated a small C_H capacitance. A 1000pF value was selected. Droop rate was also minimized by providing the output buffer with an FET input stage. A current cancellation circuit further reduces droop current and minimizes the gate current's tendency to double for every 10° C temperature change.

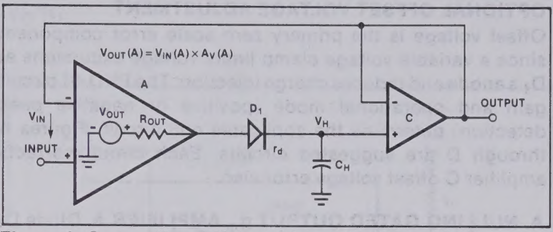


Figure 1. Conventional Voltage Amplifier Peak Detector

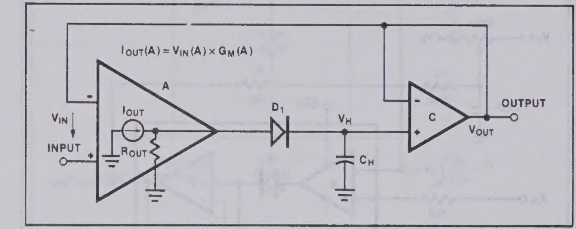


Figure 2. Transconductance Amplifier Peak Detector

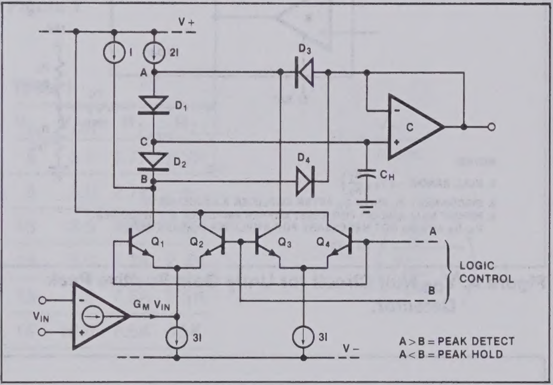


Figure 3. Transconductance Amplifier with Low Glitch Current Switch.

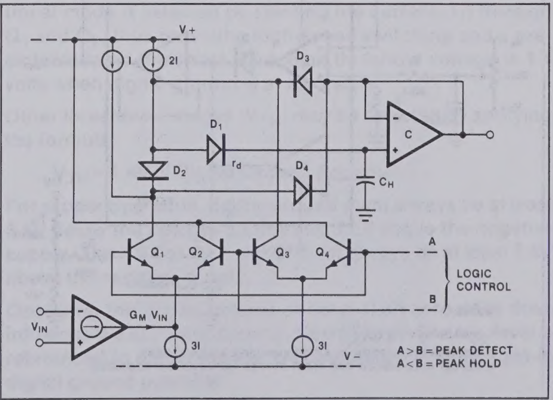


Figure 4. Peak Detecting Transconductance Amplifier with Switched Output.

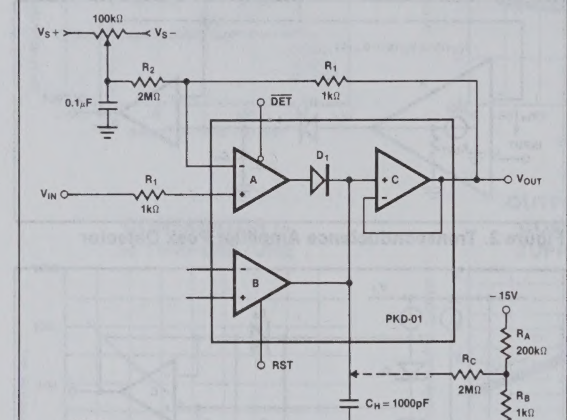
APPLICATION INFORMATION

OPTIONAL OFFSET VOLTAGE ADJUSTMENT

Offset voltage is the primary zero scale error component since a variable voltage clamp limits voltage excursions at D_1's anode and reduces charge injection. The PKD-01 circuit gain and operational mode (positive or negative peak detection) determine the applicable null circuit. Figures A through D are suggested circuits. Each circuit corrects amplifier C offset voltage error also.

A. NULLING GATED OUTPUT g_m AMPLIFIER A. Diode D_1 must be conducting to close the feedback circuit during amplifier A V_{OS} adjustment. Resistor network $R_A - R_C$ cause D_1 to conduct slightly. With DET = 0 and V_{IN} = 0V monitor the PKD-01 output. Adjust the null potentiometer until V_{OUT} = 0V. After adjustment, disconnect R_C from C_H.

B. NULLING GATED g_m AMPLIFIER B. Set amplifier B signal input to V_{IN} = 0V and monitor the PKD-01 output. Set DET = 1, RST = 1 and adjust the null potentiometer for V_{OUT} = 0V. The circuit gain — inverting or noninverting — will determine which null circuit illustrated in Figures A through D is applicable.

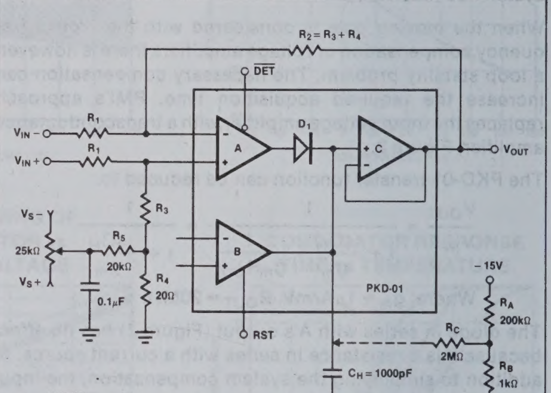


VS+
100kΩ
VS−
R2
2MΩ
0.1μF
R1
1kΩ
DET
VIN
R1
1kΩ
A
D1
C
VOUT
B
PKD-01
−15V
RA
200kΩ
RST
RC
2MΩ
CH = 1000pF
RB
1kΩ

NOTES:

1. NULL RANGE = $\pm V_S \left(\frac{R_1}{R_2}\right)$
2. DISCONNECT R_C FROM C_H AFTER AMPLIFIER A ADJUSTMENT.
3. REPEAT NULL CIRCUIT FOR RESET BUFFER AMPLIFIER B IF REQUIRED. R_A, R_B AND R_C NOT NECESSARY FOR AMPLIFIER B ADJUSTMENT.

Figure A. V_{OS} Null Circuit for Unity Gain Positive Peak Detector.

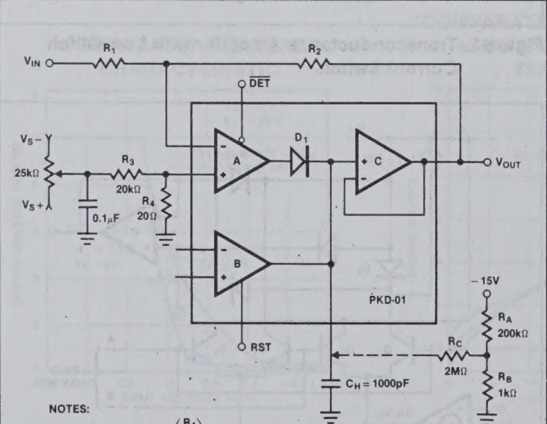


R2 = R3 + R4
DET
R1
VIN −
R1
VIN +
A
D1
C
VOUT
R3
VS−
25kΩ
R5
20kΩ
VS+
0.1μF
R4
20Ω
B
PKD-01
−15V
RA
200kΩ
RST
RC
2MΩ
CH = 1000pF
RB
1kΩ

NOTES:

1. NULL RANGE = $\pm V_S \left(\frac{R_5}{R_4}\right)\left(\frac{R_1}{R_1+R_3}\right)$
2. DISCONNECT R_C FROM C_H AFTER AMPLIFIER A ADJUSTMENT.
3. REPEAT NULL CIRCUIT FOR RESET BUFFER AMPLIFIER B IF REQUIRED.

Figure B. V_{OS} Null Circuit for Differential Peak Detector.

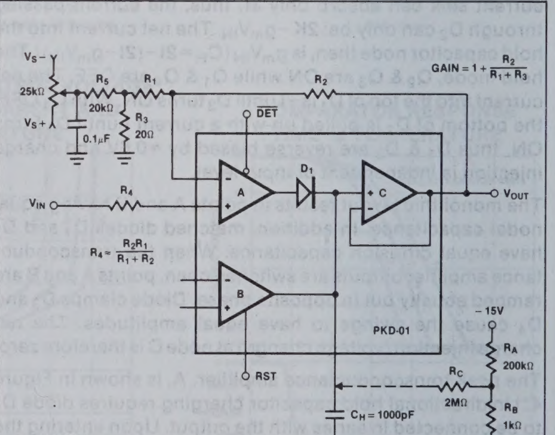


VIN
R1
R2
DET
VS−
25kΩ
VS+
R3
20kΩ
0.1μF
R4
20Ω
A
D1
C
VOUT
B
PKD-01
−15V
RA
200kΩ
RST
RC
2MΩ
CH = 1000pF
RB
1kΩ

NOTES:

1. NULL RANGE = $\pm V_S \left(\frac{R_4}{R_3}\right)$
2. DISCONNECT R_C FROM C_H AFTER AMPLIFIER A ADJUSTMENT.
3. REPEAT NULL CIRCUIT FOR RESET BUFFER AMPLIFIER B IF REQUIRED.

Figure C. V_{OS} Null Circuit for Negative Peak Detector.



VS−
25kΩ
VS+
R5
20kΩ
0.1μF
R1
R3
20Ω
R2
GAIN = 1 + R2/(R1 + R3)
DET
R4
VIN
R4 = R2R1/(R1 + R2)
A
D1
C
VOUT
B
PKD-01
−15V
RA
200kΩ
RST
RC
2MΩ
CH = 1000pF
RB
1kΩ

NOTES:

1. NULL RANGE = $\pm V_S \left(\frac{R_3}{R_5}\right)$
2. DISCONNECT R_C FROM C_H AFTER AMPLIFIER A ADJUSTMENT.
3. REPEAT NULL CIRCUIT FOR RESET BUFFER AMPLIFIER B IF REQUIRED.

Figure D. V_{OS} Null Circuit for Positive Peak Detector With Gain.

PEAK HOLD CAPACITOR RECOMMENDATIONS

The hold capacitor (C_H) serves as the peak memory element and compensating capacitor. Stable operation requires a minimum value of 1000pF. Larger capacitors may be used to lower droop rate errors, but acquisition time will increase.

Zero scale error is internally trimmed for $C_H = 1000pF$. Other C_H values will cause a zero scale shift which can be approximated with the following equation.

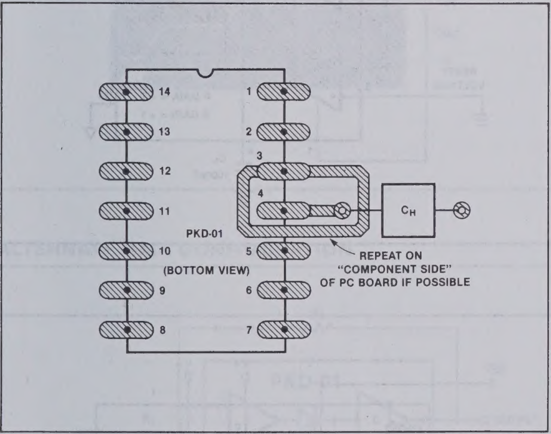
$$\Delta V_{ZS}(mV) = \frac{1 \times 10^3 (pC)}{C_H (nF)} - 0.6mV$$

The peak hold capacitor should have very high insulation resistance and low dielectric absorption. For temperatures below 85° C, a polystyrene capacitor is recommended, while a Teflon capacitor is recommended for high temperature environments.

CAPACITOR GUARDING AND GROUND LAYOUT

Ground planes are recommended to minimize ground path resistance. Separate analog and digital grounds should be used. The two ground systems are tied together only at the common system ground. This avoids digital currents returning to the system ground through the analog ground path.

The C_H terminal (Pin 4) is a high-impedance point. To minimize gain errors and maintain the PKD-01's inherently low droop rate, guarding Pin 4 is recommended.



COMPARATOR

The comparator output high level (V_{OH}) is set by external resistors. It's possible to optimize noise immunity while interfacing to all standard logic families — TTL, DTL, and CMOS. Figure 1 shows the comparator output with external level setting resistors. Table I gives typical R_1 and R_2 values for common circuit conditions.

The maximum comparator high output voltage (V_{OH}) should be limited to:

$V_{OH}(\text{maximum}) < V^+ - 2.0V$

With the comparator in the low state (V_{OL}), the output stage will be required to sink a current approximately equal to V_C/R_1.

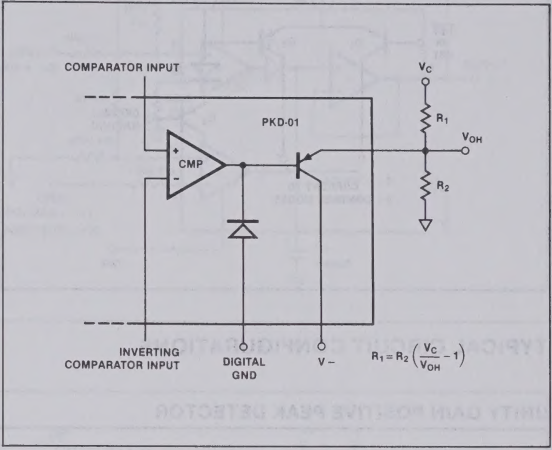


Figure 1

Table I.

V_C	V_{OH}	R_1	R_2
5	3.5	2.7K	6.2K
5	5.0	2.7K	∞
15	3.5	4.7K	1.5K
15	5.0	4.7K	2.4K
15	7.5	7.5K	7.5K
15	10.0	7.5K	15K

$$R_1 \approx \frac{V_C}{I_{SINK}}$$

$$R_2 \approx \left(\frac{1}{\frac{V_C}{V_{OH}} - 1} \right)$$

PEAK DETECTOR LOGIC CONTROL (RST, $\overline{DET}$)

The transconductance amplifier outputs are controlled by the digital logic signals RST and $\overline{DET}$. The PKD-01 operational mode is selected by steering the current (I_1) through Q_1 and Q_2, thus providing high-speed switching and a predictable logic threshold. The logic threshold voltage is 1.4 volts when digital ground is at zero volts.

Other threshold voltages (V_{TH}) may be selected by applying the formula:

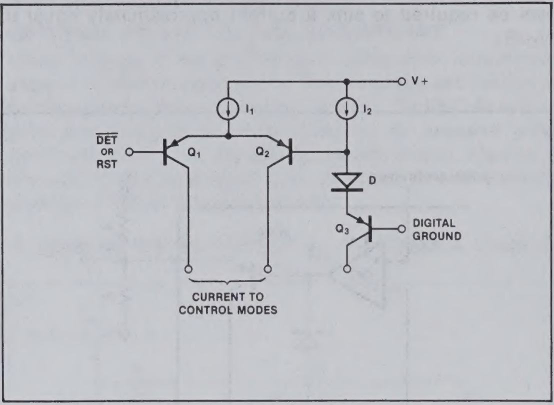
$V_{TH} \approx 1.4V +$ Digital Ground Potential.

For proper operation, digital ground must always be at least 3.5V below the positive supply and 2.5V above the negative supply. The RST or $\overline{DET}$ signal must always be at least 2.8V above the negative supply.

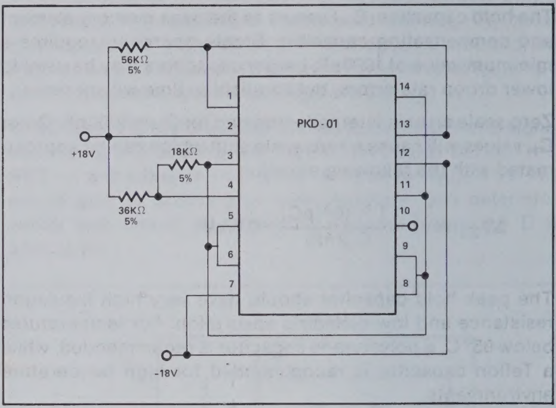
Operating the digital ground at other than zero volts does influence the comparator output low voltage. The V_{OL} level is referenced to digital ground and will follow any changes in digital ground potential:

$V_{OL} \approx 0.2V +$ Digital Ground Potential.

PKD-01 LOGIC CONTROL

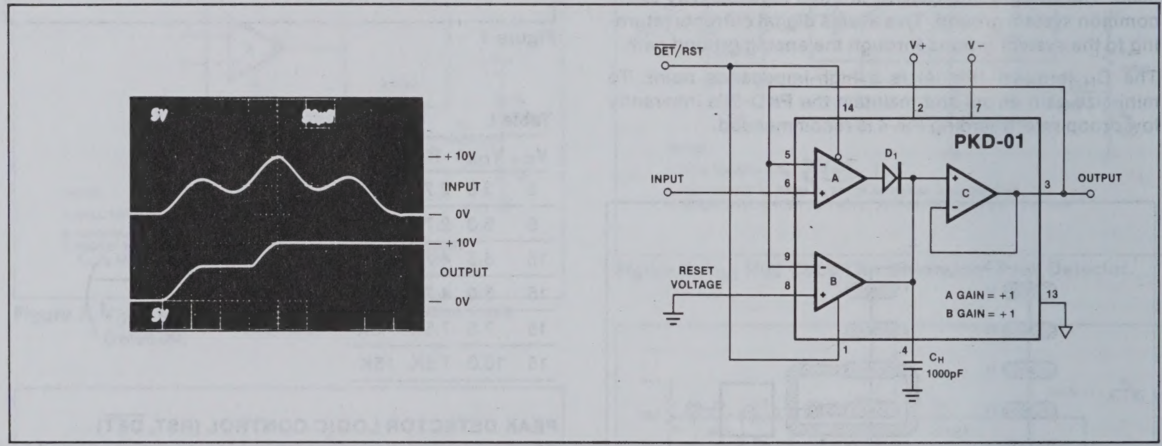

V+
I_1
I_2
DET OR RST
Q_1
Q_2
D
Q_3
DIGITAL GROUND
CURRENT TO CONTROL MODES

BURN-IN CIRCUIT

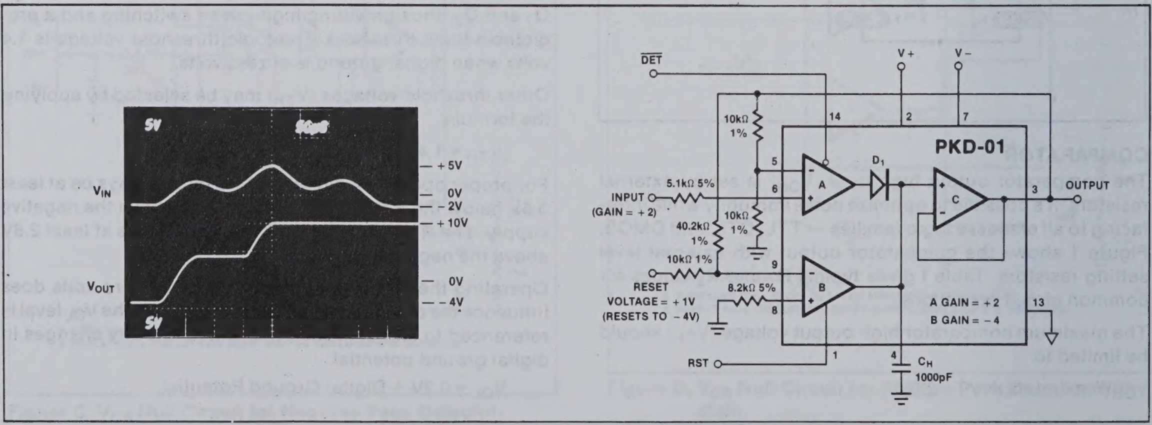

56KΩ 5%
+18V
18KΩ 5%
36KΩ 5%
PKD-01
1
2
3
4
5
6
7
8
9
10
11
12
13
14
-18V

TYPICAL CIRCUIT CONFIGURATIONS

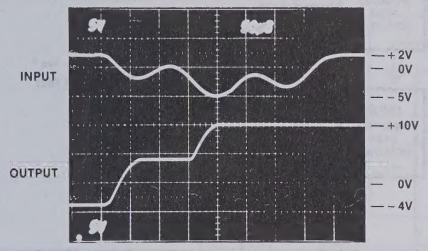
UNITY GAIN POSITIVE PEAK DETECTOR

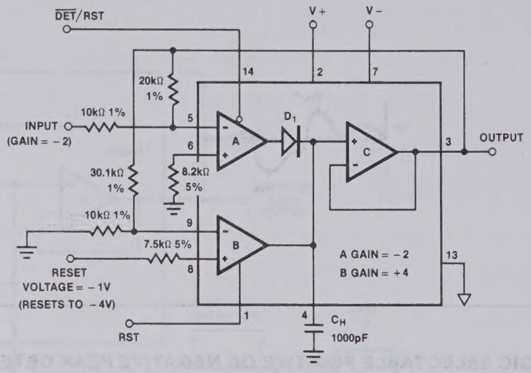

5V
50µS
5V
+10V
INPUT
0V
+10V
OUTPUT
0V
DET/RST
V+
V−
14
2
7
PKD-01
5
6
INPUT
A
D_1
C
3
OUTPUT
9
8
RESET VOLTAGE
B
A GAIN = +1
B GAIN = +1
13
1
4
C_H 1000pF

POSITIVE PEAK DETECTOR WITH GAIN

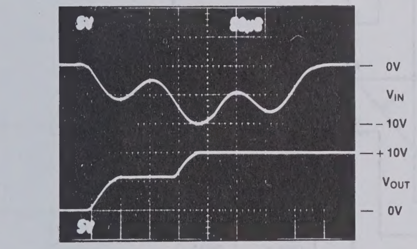

5V
50µS
5V
V_{IN}
+5V
0V
−2V
+10V
V_{OUT}
0V
−4V
DET
V+
V−
10kΩ 1%
14
2
7
PKD-01
5
5.1kΩ 5%
INPUT (GAIN = +2)
6
A
D_1
C
3
OUTPUT
40.2kΩ 1%
10kΩ 1%
10kΩ 1%
9
RESET VOLTAGE = +1V (RESETS TO −4V)
8.2kΩ 5%
8
B
A GAIN = +2
B GAIN = −4
13
RST
1
4
C_H 1000pF

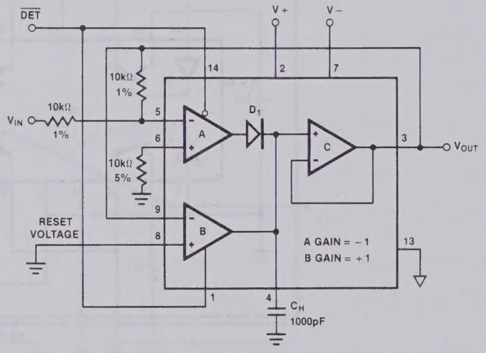
NEGATIVE PEAK DETECTOR WITH GAIN



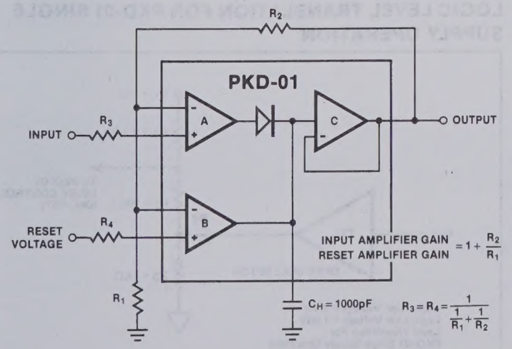

DET/RST
V+
V−
20kΩ 1%
14
2
7
10kΩ 1%
INPUT
(GAIN = −2)
5
6
A
D₁
C
3
OUTPUT
30.1kΩ 1%
8.2kΩ 5%
10kΩ 1%
9
B
7.5kΩ 5%
8
RESET VOLTAGE = −1V
(RESETS TO −4V)
A GAIN = −2
B GAIN = +4
13
1
4
C_H
1000pF
RST

UNITY GAIN NEGATIVE PEAK DETECTOR




DET
V+
V−
10kΩ 1%
14
2
7
10kΩ 1%
V_IN
5
6
A
D₁
C
3
V_OUT
10kΩ 5%
9
RESET VOLTAGE
8
B
A GAIN = −1
B GAIN = +1
13
1
4
C_H
1000pF

ALTERNATE GAIN CONFIGURATION


R₂
PKD-01
A
C
OUTPUT
R₃
INPUT
B
R₄
RESET VOLTAGE
R₁
C_H = 1000pF

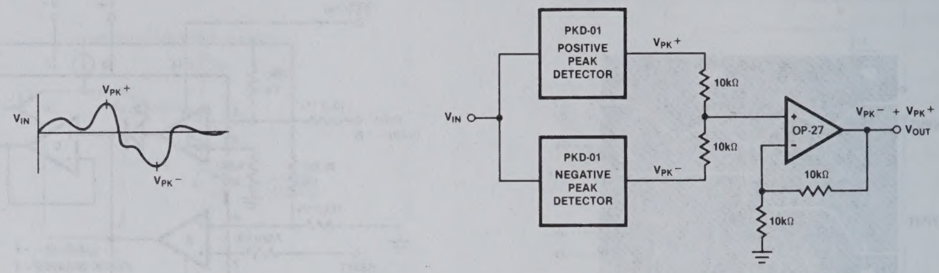
$$\frac{\text{INPUT AMPLIFIER GAIN}}{\text{RESET AMPLIFIER GAIN}} = 1 + \frac{R_2}{R_1}$$

$$R_3 = R_4 = \frac{1}{\frac{1}{R_1} + \frac{1}{R_2}}$$

IF BOTH INPUT SIGNAL (AMPLIFIER A INPUT) AND THE RESET VOLTAGE (AMPLIFIER B INPUT) HAVE THE SAME POSITIVE VOLTAGE GAIN THE GAIN CAN BE SET BY A SINGLE VOLTAGE DIVIDER FOR BOTH INPUT AMPLIFIERS.

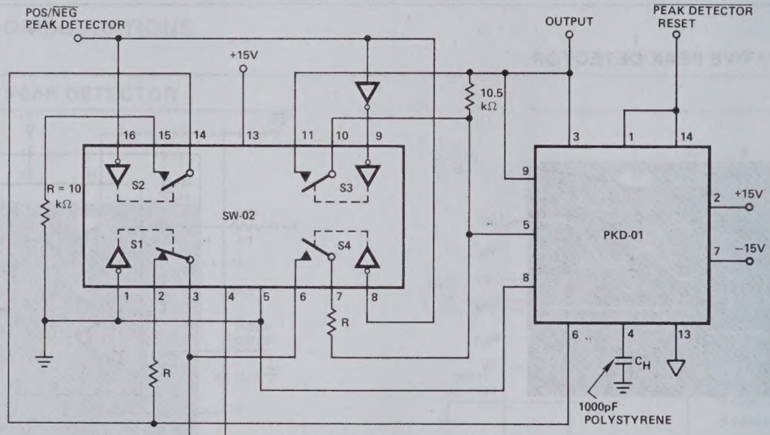
NOTE:
R1, R2, R3 AND R4 > 5kΩ

PEAK-TO-PEAK DETECTOR



$V_{PK}+$
V_{IN}
$V_{PK}-$
PKD-01 POSITIVE PEAK DETECTOR
PKD-01 NEGATIVE PEAK DETECTOR
V_{IN}
$V_{PK}+$
$V_{PK}-$
10kΩ
10kΩ
OP-27
10kΩ
10kΩ
$V_{PK}- + V_{PK}+$
V_{OUT}

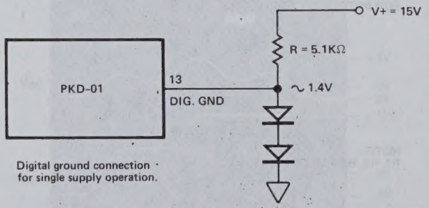
LOGIC SELECTABLE POSITIVE OR NEGATIVE PEAK DETECTOR



POS/$\overline{NEG}$ PEAK DETECTOR
+15V
OUTPUT
$\overline{PEAK\ DETECTOR}$ RESET
10.5 kΩ
16
15
14
13
11
10
9
S2
S3
SW-02
S1
S4
R = 10 kΩ
1
2
3
4
5
6
7
8
R
R
9
5
8
3
1
14
2
+15V
PKD-01
7
−15V
6
4
13
C_H
1000pF POLYSTYRENE
IN
−15V

NOTES: 1. DEVICE IS RESET TO 0 VOLTS.
2. DETECTED PEAKS ARE PRESENTED AS POSITIVE OUTPUT LEVELS.
3. R = 10kΩ.
4. R ⩾ 2.7kΩ.

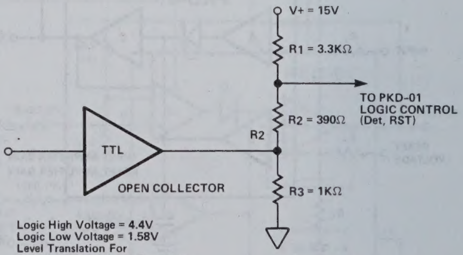
DIGITAL GROUND CONNECTION FOR SINGLE SUPPLY OPERATION



V+ = 15V
R = 5.1KΩ
PKD-01
13
DIG. GND
~1.4V

Digital ground connection for single supply operation.

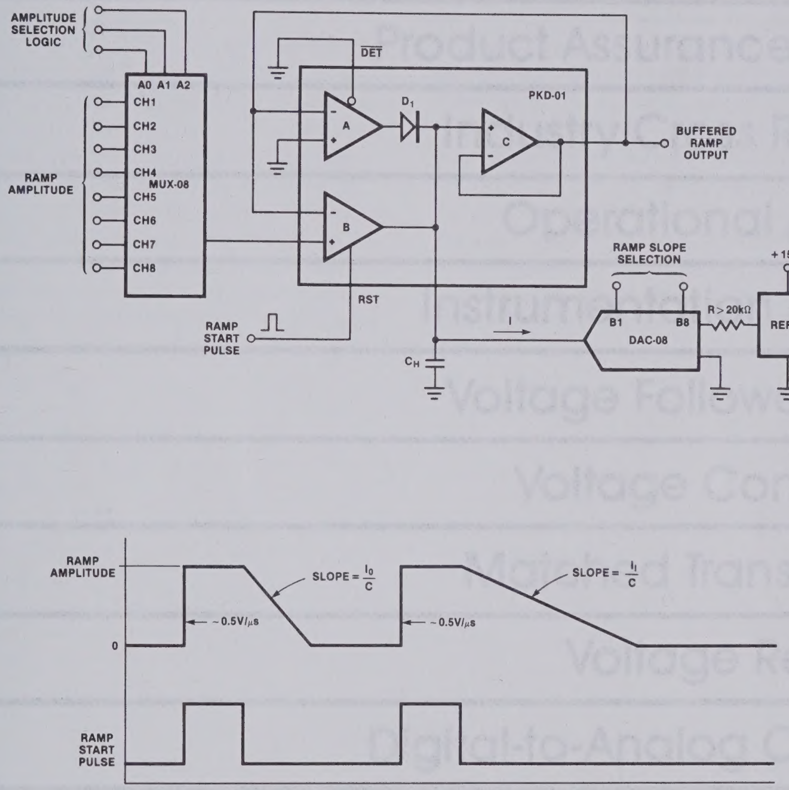
LOGIC LEVEL TRANSLATION FOR PKD-01 SINGLE SUPPLY OPERATION



V+ = 15V
R1 = 3.3KΩ
TO PKD-01 LOGIC CONTROL (Det, RST)
R2 = 390Ω
R2
TTL
OPEN COLLECTOR
R3 = 1KΩ

Logic High Voltage = 4.4V
Logic Low Voltage = 1.58V
Level Translation For
PKD-01 Single Supply Operation.

PROGRAMMABLE LOW FREQUENCY RAMP GENERATOR


AMPLITUDE SELECTION LOGIC
A0 A1 A2
CH1
CH2
CH3
CH4
CH5
CH6
CH7
CH8
MUX-08
RAMP AMPLITUDE
DET
PKD-01
A
B
C
D1
BUFFERED RAMP OUTPUT
RST
RAMP START PULSE
CH
I
RAMP SLOPE SELECTION
B1
B8
DAC-08
R > 20kΩ
REF-01
+15V
RAMP AMPLITUDE
0
SLOPE = $\frac{I_0}{C}$
SLOPE = $\frac{I_1}{C}$
~0.5V/μs
~0.5V/μs
RAMP START PULSE

NOTES: 1. NEGATIVE SLOPE OF RAMP IS SET BY DAC-08 OUTPUT CURRENT.
2. DAC-08 IS DIGITALLY CONTROLLED CURRENT GENERATOR. THE MAXIMUM FULL SCALE CURRENT MUST BE LESS THAN 0.5mA.

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PCM Repeaters

COMMUNICATIONS PRODUCTS

INTRODUCTION

PCM repeater circuits are used to regenerate alternate-mark-inversion pulses in PCM carrier systems operating at the 1.444-2.048 Mega-bits-per-second data rate. Information in a PCM system is transmitted over cable pairs by the presence or absence of pulses within specific time slots. A repeater-circuit amplifies degraded PCM pulses, sets an output flip-flop, and drives an output transformer that connects to the PCM cable pair. In addition, repeater amplifiers can be used for clock-recovery circuits in high-data-rate pulse transmission systems.

The PMI repeater amplifiers, RPT-81 and RPT-82, are monolithic integrated circuits that perform all of the necessary active functions for a PCM repeater. RPT-81 and RPT-82 are very similar; the primary functional difference is the incorporation of an automatic-clock-shutdown circuit in the RPT-81. When the signal into the RPT-81 becomes too low, the clock amplifier is automatically shut down to prevent the transmission of erroneous data. Both repeaters are fully described and specified in this section of the catalog.

RPT-81/RPT-82

PCM REPEATERS

FEATURES

- **On-Chip ALBO Diode**
- **Clock Shutdown Circuit (RPT-81)**
- **On-Chip Voltage Regulator (RPT-81)**
- **Low Power Operation (100mW)**
- **Pin-Compatible with XR-C277**
- **Improved Pre-Amplifier Response (RPT-82)**

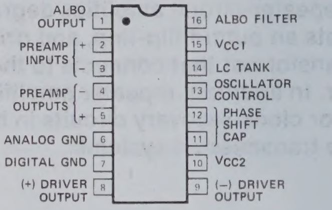
GENERAL DESCRIPTION

The PMI PCM Repeater Circuits are monolithic integrated circuits which perform all the active functions required for a regenerative repeater operating at 1.544-2.048 Mega-bits per second (Mbps) data rates on PCM lines.

In a PCM carrier system, coded information is transmitted over paired cables by the presence or absence of pulses in specified time slots. The RPT-81/RPT-82 regenerate all pulses that meet threshold requirements without inserting pulses incorrectly during empty time slots.

Additional system functions have been incorporated on-chip. These include an Automatic Line Build Out (ALBO) circuit that compensates for up to 36dB of line loss and an oscillator control pin that permits injectioned-locked (free-running) or pulsed-tank operation. The RPT-81 also incorporates an automatic clock shutdown circuit. The clock shutdown inhibits the clock amplifier when the input signal is too low to provide reliable data transmission.

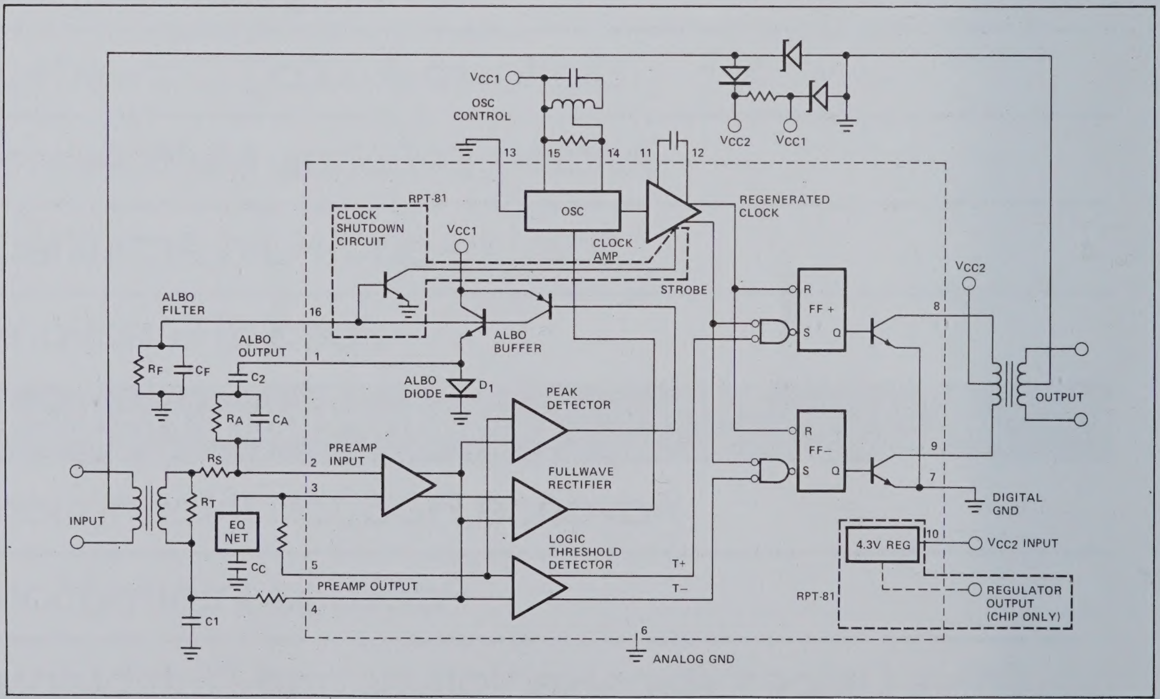
PIN CONNECTIONS & ORDERING INFORMATION


ALBO OUTPUT 1
PREAMP INPUTS + 2
– 3
PREAMP OUTPUTS – 4
+ 5
ANALOG GND 6
DIGITAL GND 7
(+) DRIVER OUTPUT 8
16 ALBO FILTER
15 VCC1
14 LC TANK
13 OSCILLATOR CONTROL
12 PHASE SHIFT CAP
11
10 VCC2
9 (–) DRIVER OUTPUT

16-PIN HERMETIC DUAL-IN-LINE
(Q-Suffix)
RPT-81FQ
RPT-82FQ

*The on-chip (RPT-81) 4.3V regulated output voltage is not available for external use in 16-Pin package.

FUNCTIONAL BLOCK DIAGRAM


VCC1
OSC CONTROL
13
15
14
11
12
VCC2
VCC1
RPT-81
CLOCK SHUTDOWN CIRCUIT
VCC1
OSC
CLOCK AMP
REGENERATED CLOCK
STROBE
ALBO FILTER
16
ALBO BUFFER
ALBO OUTPUT
1
C2
RF
CF
RA
CA
ALBO DIODE
D1
PEAK DETECTOR
RS
PREAMP INPUT
2
3
FULLWAVE RECTIFIER
INPUT
RT
EQ NET
CC
LOGIC THRESHOLD DETECTOR
5
PREAMP OUTPUT
T+
T–
4
C1
6
ANALOG GND
R
FF +
S
Q
R
FF–
S
Q
VCC2
8
9
7
OUTPUT
DIGITAL GND
4.3V REG
10
VCC2 INPUT
RPT-81
REGULATOR OUTPUT (CHIP ONLY)

FUNCTIONAL DESCRIPTION

Biopolar pulse transmission, the transmission of alternately positive and negative pulses, is used on repeatered lines to remove the DC component from the unipolar PCM pulse train. This also places the principle energy components in the 0-1.544MHz band, as opposed to the 0-3.088MHz band for the unipolar pulse train. The absence of a DC component in the bipolar pulse train permits the repeater to be transformer coupled to the line and helps to prevent time shifting of the regenerator firing level with variation in input pulse density.

The bipolar PCM pulse train is transformer coupled into the preamplifier as shown in the RPT-81/RPT-82 functional block diagram. The secondary of the input transformer is loaded with the proper terminating resistor R_T to match the line impedance. One side of the transformer secondary is AC coupled to ground by capacitor C1, the other side of the secondary winding is in series with resistance R_S. Resistor R_S and RC network $R_A C_A$ are AC coupled to the ALBO output by capacitor C2. The impedance from the ALBO output to ground is governed by the amount of current through the ALBO diode. R_S in series with $R_A C_A$ provides maximum signal attenuation when maximum current flows through the ALBO diode. When minimum current flows through the ALBO, diode C2 is effectively isolated from ground and the input signal attenuation is minimal. The RPT-81/RPT-82 ALBO circuits can compensate for 36dB of line loss.

The preamplifier amplifies the signal and applies it to the three comparators labeled *logic threshold detector, fullwave rectifier,* and *peak detector,* respectively. Each comparator is set to trigger on both positive and negative pulses. Each comparator trips at a different threshold. The logic threshold is set to trip at the 50% point, the fullwave rectifier trips at the 65% point, and the peak detector trips at peak amplitude. Thresholds and waveforms are drawn on the RPT-81/RPT-82 waveforms and thresholds diagram.

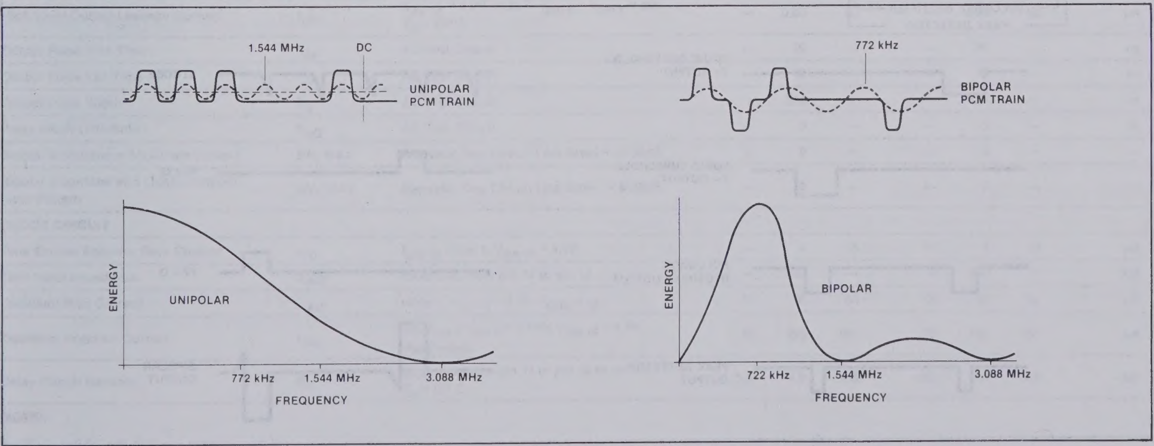
The peak detector output charges the capacitor of the ALBO filter. The voltage on this capacitor causes a relatively constant current to flow through D1 by means of the emitter follower ALBO buffer. A decaying voltage on the ALBO filter enables the clock shutdown circuit when there is no input signal. The clock shutdown circuit turns off the clock amplifier so that neither the regenerated clock nor the strobe outputs are sent to FF+ or FF− flip flops.

The fullwave detector output injection locks the oscillator to the input frequency. The clock amplifier shapes the oscillator output and shifts it in time. To optimize noise rejection, select the phase-shift capacitor (0 to 30pF, 10pF typical) such that the strobe pulse occurs at the center of the incoming pulses.

The logic threshold detector produces an output on the T+ line for a positive pulse and an output on the T− line for a negative pulse. The T+ line enables the NAND gate of FF+ and the T− line enables the NAND gate of FF−. A T+ output pulse from the logic threshold detector is ANDed with the strobe pulse to set the FF+ flip flop which turns on its corresponding output transistor, causing current to flow through one half of the output transformer primary. A positive output pulse results. Similarly, A T− output pulse and a strobe pulse are ANDed to set the FF− flip flop, thus causing a negative output pulse. The flip flops are turned off (and the output pulse terminated) by the regenerated clock pulse. In this way the output pulse is controlled by the oscillator tank circuit and not the incoming pulse.

When pin 13 is grounded, the full-wave detector injection-locks the oscillator to the input frequency. With pin 13 ungrounded, the system operates in the "pulsed tank" mode.

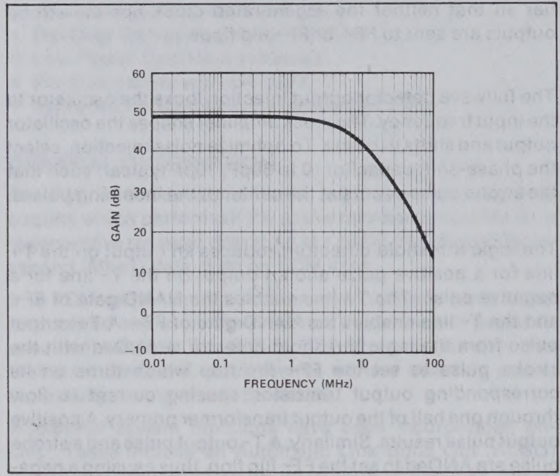
ENERGY SPECTRA OF BIPOLAR AND UNIPOLAR PULSE TRAINS



PREAMPLIFIER

The preamplifier has wideband frequency response in order to amplify the 1.544Mb/sec pulse train. In addition it has well-behaved roll-off characteristics to simplify the application of feedback.

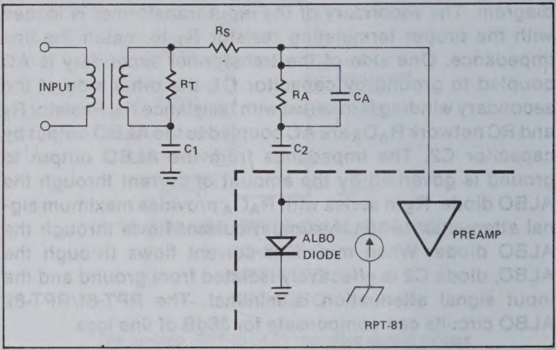
PREAMPLIFIER FREQUENCY RESPONSE



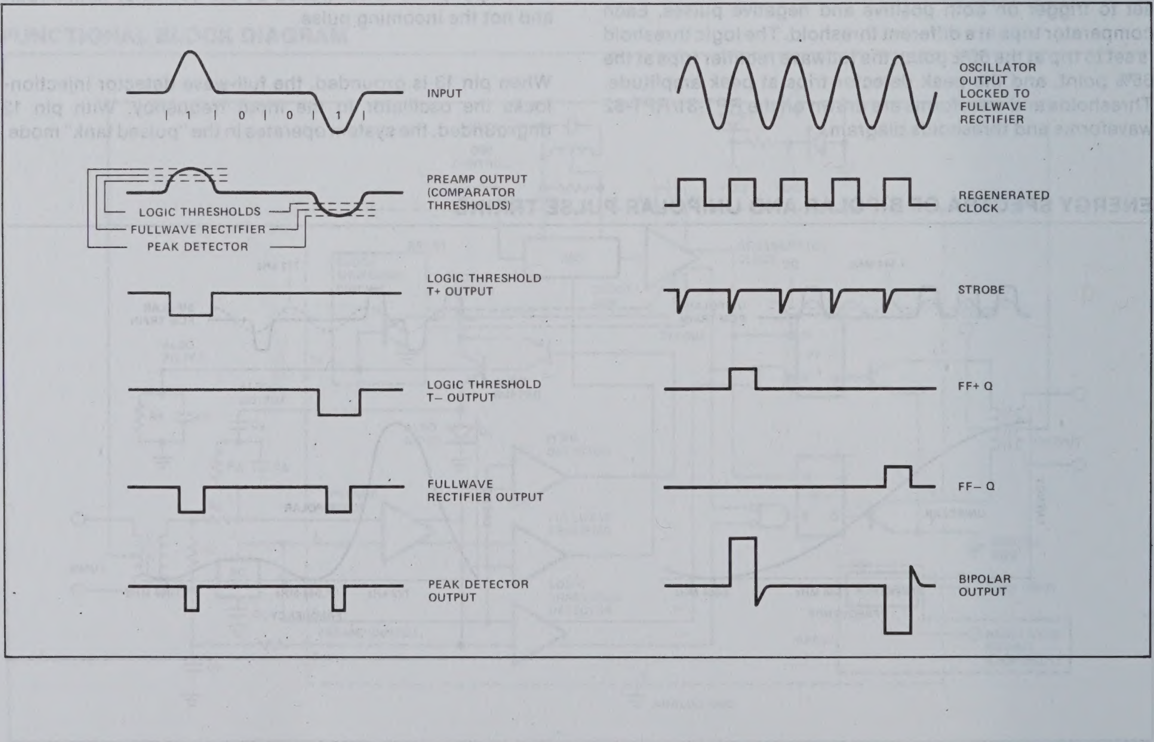
AUTOMATIC LINE BUILDOUT EXTERNAL CIRCUIT

The external circuitry required to achieve automatic line buildout must attenuate the signal while simultaneously matching the transformer to the line. Capacitors C1 and C2 are blocking capacitors. R_A and C_A in parallel shape the frequency response of the attenuator network to compensate for the reactive source impedance of the line. Resistor R_T provides an input match to this line. R_S is the series branch of the attenuator.

AUTOMATIC LINE BUILDOUT EXTERNAL CIRCUITRY


RS
INPUT
RT
RA
CA
C1
C2
ALBO
DIODE
PREAMP
RPT-81

WAVEFORMS AND THRESHOLDS


1
1
0
1
0
1
1
INPUT
PREAMP OUTPUT
(COMPARATOR
THRESHOLDS)
LOGIC THRESHOLDS
FULLWAVE RECTIFIER
PEAK DETECTOR
LOGIC THRESHOLD
T+ OUTPUT
LOGIC THRESHOLD
T− OUTPUT
FULLWAVE
RECTIFIER OUTPUT
PEAK DETECTOR
OUTPUT
OSCILLATOR
OUTPUT
LOCKED TO
FULLWAVE
RECTIFIER
REGENERATED
CLOCK
STROBE
FF+ Q
FF− Q
BIPOLAR
OUTPUT

ABSOLUTE MAXIMUM RATINGS

Pin 10 to Pin 7 or 6	16.0V, −0.2V
Pin 15 to Pin 7 or 6	8.0V, −0.2V
Maximum Voltage at Pins 8 or 9	30V, −0.2V
Maximum Voltage at Pins 2, 3, 4, 5, 11, 12, 14	V_{CC2}
Maximum Sinking Current at Pin 8 or 9	300mA
Operating Temperature Range	−40° C to +85° C
Storage Temperature Range	−65° C to +150° C
Power Dissipation	500mW
Lead Soldering Temperature	300° C

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
16-Pin Hermetic DIP (Q)	100° C	10mW/° C

ELECTRICAL CHARACTERISTICS at $V_{CC1} = 4.4V$, $V_{CC2} = 6.8V$, $-40° C \leq T_A \leq +85° C$, unless otherwise noted. $V_{pin\ 6} = V_{pin\ 7} = V_{pin\ 13} = GND$.

PARAMETER	SYMBOL	CONDITIONS	RPT-81 MIN	 TYP	 MAX	RPT-82 MIN	 TYP	 MAX	UNITS
SUPPLY									
Differential Output Voltage (Low Level)	V_{CC1}	Power Supply Range over which device will function	4.3	4.4	4.7	4.1	4.4	4.7	V
Power Supply Voltage	V_{CC2}	Power Supply Range over wich device will function	5.0	6.8	7.25	5.0	6.8	7.5	V
Supply Current	I_{CC1}	$T_A = 25° C$, Note 1	—	8.5	—	—	8.5	—	mA
Supply Current	I_{CC2}	$T_A = 25° C$, Note 1	—	2.5	—	—	2.5	—	mA
PREAMPLIFIER									
Total Supply Current	$I_{CC1} + I_{CC2}$	$T_A = 25° C$, Note 1	6.0	11.0	13	6.0	11.0	13	mA
Preamplifier Open-Loop $\frac{\Delta V_{pin\ 5}}{\Delta V_{pin\ 2}}$	A_0	Measure $\Delta V_{pin\ 2}$ necessary to change pins from 1.8V to 3.3V	44	48	52	44	48	52	dB
Preamplifier Bandwidth	B_W	3dB Points	—	5	—	—	7	—	MHz
Preamplifier Input Impedance	Z_{IN}	Shunted by 2pF	—	600	—	—	600	—	kΩ
Preamplifier Input Offset Voltage	V_{OS}	Note 1, $V_{pin\ 2}$-$V_{pin\ 3}$	—	1	15	—	1	15	mV
Preamplifier Output Impedance	Z_{OUT}		—	80	—	—	80	—	Ω
Preamplifier Output High Voltage	V_{OHA}	$T_A = 25° C$, $V_{pin\ 4}$, $V_{pin\ 2} = 2.5V$, $V_{pin\ 3} = 2.7V$	3.25	3.45	3.75	3.4	3.5	3.75	V
Preamplifier Output Low Voltage	V_{OHL}	$T_A = 25° C$, $V_{pin\ 4}$, $V_{pin\ 2} = 2.5V$, $V_{pin\ 3} = 2.3V$	1.25	1.4	1.55	1.2	1.4	1.5	V
Preamplifier Input Bias Current	I_B	$I_{pin\ 2}$ or $I_{pin\ 3}$, Note 1	—	1.0	4	—	1.0	4	μA
Preamplifier Input Offset Current	I_{OS}	$I_{pin\ 2}$-$I_{pin\ 3}$, Note 1	—	0.05	2	—	0.05	2	μA
OUTPUT DRIVE									
Output Voltage Swing	V_{OP}	$V_{pin\ 8\ High}$-$V_{pin\ 8\ Low}$, $V_{pin\ 9\ High}$-$V_{pin\ 9\ Low}$	—	6.0	—	—	6.0	—	V
Low Level Output Voltage	V_{OL}	$T_A = 25° C$, $I_{LOAD} = 15mA$, Note 2	0.65	0.8	0.95	0.65	0.8	0.95	V
Differential Output Voltage (Low Level)	V_{OLD}	$T_A = 25° C$, $I_{LOAD} = 15mA$, Note 2	—	0.02	0.15	—	0.02	0.15	V
High Level Output Leakage Current	I_{OH}	$V_{pin\ 14} = 4.9V$, Note 1, $V_{pin\ 8} = V_{pin\ 9} = 20V$, $T_A = 25° C$	—	0.05	50	—	0.05	50	μA
Output Pulse Rise Time	T_{os}	AC Test Circuit	—	30	—	—	30	—	ns
Output Pulse Fall Time	T_{of}	AC Test Circuit	—	10	—	—	10	—	ns
Output Pulse Width	P_W	AC Test Circuit	—	324	—	—	324	—	ns
Pulse Width Differential	P_{WD}	AC Test Circuit	—	3	—	—	3	—	ns
Bipolar Violations at Maximum Density	BV_1 MAX	Repeater Test Circuit Line Atten. = 6-36dB	—	0	—	—	0	—	—
Bipolar Violations with Quasi-Random Input Pattern	BV_R MAX	Repeater Test Circuit Line Atten. = 6-36dB	—	0	—	—	0	—	—
CLOCK CIRCUIT									
Tank Emitter Follower Base Current	I_{TB}	$I_{pin\ 14}$, Note 1, $V_{pin\ 14} = 4.9V$	—	4	15	—	4	15	μA
Tank Input Impedance	Z_{INT}	Measured from pin 14 to pin 15	—	300	—	—	300	—	kΩ
Oscillator Bias Current	I_{OSC}	Note 1, $V_{pin\ 14} = 3.9V$ (I_{OSC}-I_{TB})	10	30	50	10	30	50	μA
Oscillator Injection Current	I_{INJ}	Set $V_{pin\ 4}$-$V_{pin\ 5} = \pm 1.4V$, $V_{pin\ 14} = 3.9V$ (I_{INJ}-I_{OSC})	75	120	160	75	120	160	μA
Delay Circuit Resistor	R_d	Measured from pin 11 or pin 12 to pin 15, $T_A = 25° C$	3.2	4.0	4.8	3.2	4.0	4.8	kΩ

NOTES:

1. $V_{pin\ 2} = 2.5V$, adjust $V_{pin\ 3}$ until $V_{pin\ 4} = V_{pin\ 5}$.
2. A dynamic test, pin 2 = 2.5V, pin 3 pulsed at 100Hz rate, pin 14 pulsed at 200Hz rate.

ELECTRICAL CHARACTERISTICS at $V_{CC1} = 4.4V$, $V_{CC2} = 6.8V$, $-40°C \leq T_A \leq +85°C$, unless otherwise noted. $V_{pin\ 6} = V_{pin\ 7} = V_{pin\ 13} =$ GND. (Continued)

			RPT-81			RPT-82			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
MISCELLANEOUS									
ALBO Threshold	V_{TA}	Differential voltage, measured between pins 4 and 5, required to trip Peak Detector. $T_A = 25°C$	1.35	1.5	1.65	1.35	1.5	1.65	V
Clock Threshold	V_{TC}	Differential voltage, measured between pins 4 and 5, required to drive Fullwave Rectifier. $T_A = 25°C$	0.85	1.0	1.2	0.9	1.08	1.25	V
Logic Threshold	V_{TL}	Differential voltage, measured between pins 4 and 5, required to trip Logic Threshold. $T_A = 25°C$	0.65	0.75	0.85	0.65	0.75	0.85	V
Clock Threshold as % of ALBO Voltage	V_{TC}	$T_A = 25°C$	62	66	70	68	72	76	%
Logic Threshold as % of ALBO Voltage	V_{TL}	$T_A = 25°C$	47	50	53	46	49	52	%
ALBO ON Voltage	V_{O16}	Measured at pin 16, $\|V_{p4}-V_{p5}\|$ = ALBO Threshold	1.0	1.7	2.5	1.0	1.7	2.5	V
ALBO OFF Voltage	V_{F16}	Measured at pin 16 and pin 1 Note 1, $T_A = 25°C$	—	—	75	—	—	75	mV
Minimum ALBO Diode Resistance	R_D Min		—	8	—	—	8	—	Ω
Maximum ALBO Diode Resistance	R_D Max		—	30	—	—	30	—	kΩ

NOTE:

1. $V_{pin\ 2} = 2.5V$, adjust $V_{pin\ 3}$ until $V_{pin\ 4} = V_{pin\ 5}$.

REPEATER DEFINITIONS

ALBO THRESHOLD

The differential voltage measured between pins 4 and 5, required to activate the internal peak detector.

AUTOMATIC LINE BUILD OUT

An automatic gain control circuit which operates by simulating a line "build-out" or extension.

BIPOLAR VIOLATION

The transmission of two consecutive pulses of the same polarity.

CLOCK THRESHOLD

The differential voltage measured between pins 4 and 5, required to drive the internal fullwave rectifier.

DATA THRESHOLD

The differential voltage measured between pins 4 and 5, required to trip logic threshold detector.

DIFFERENTIAL OUTPUT VOLTAGE

The difference in voltage of the two outputs with a binary one output of either polarity.

ALBO DIODE RESISTANCE

Small signal resistance of ALBO diode measured between pins 1 and 6. The ALBO diode is a diode connected transistor whose current-resistance relationship is $R_D = 26/I_O$ where R_D = ALBO diode resistance and I_O = ALBO diode current in mA.

DELAY CIRCUIT RESISTANCE

Resistance seen at pins 11 and 12.

LINE BUILD OUT

The attenuation added to the output of a short line.

MAXIMUM DENSITY

An input signal pattern consisting of all ones.

MINIMUM DENSITY

An input signal pattern consisting of two ones followed by 14 zeros.

OUTPUT PULSE RISE (FALL) TIME

Rise (Fall) time of regenerated pulse. Measured from the 10-90% points.

OUTPUT PULSE WIDTH DIFFERENTIAL

In a T1 carrier system a typical pulse width is 324nsec. The pulse width differential is the difference in pulse width of the two outputs.

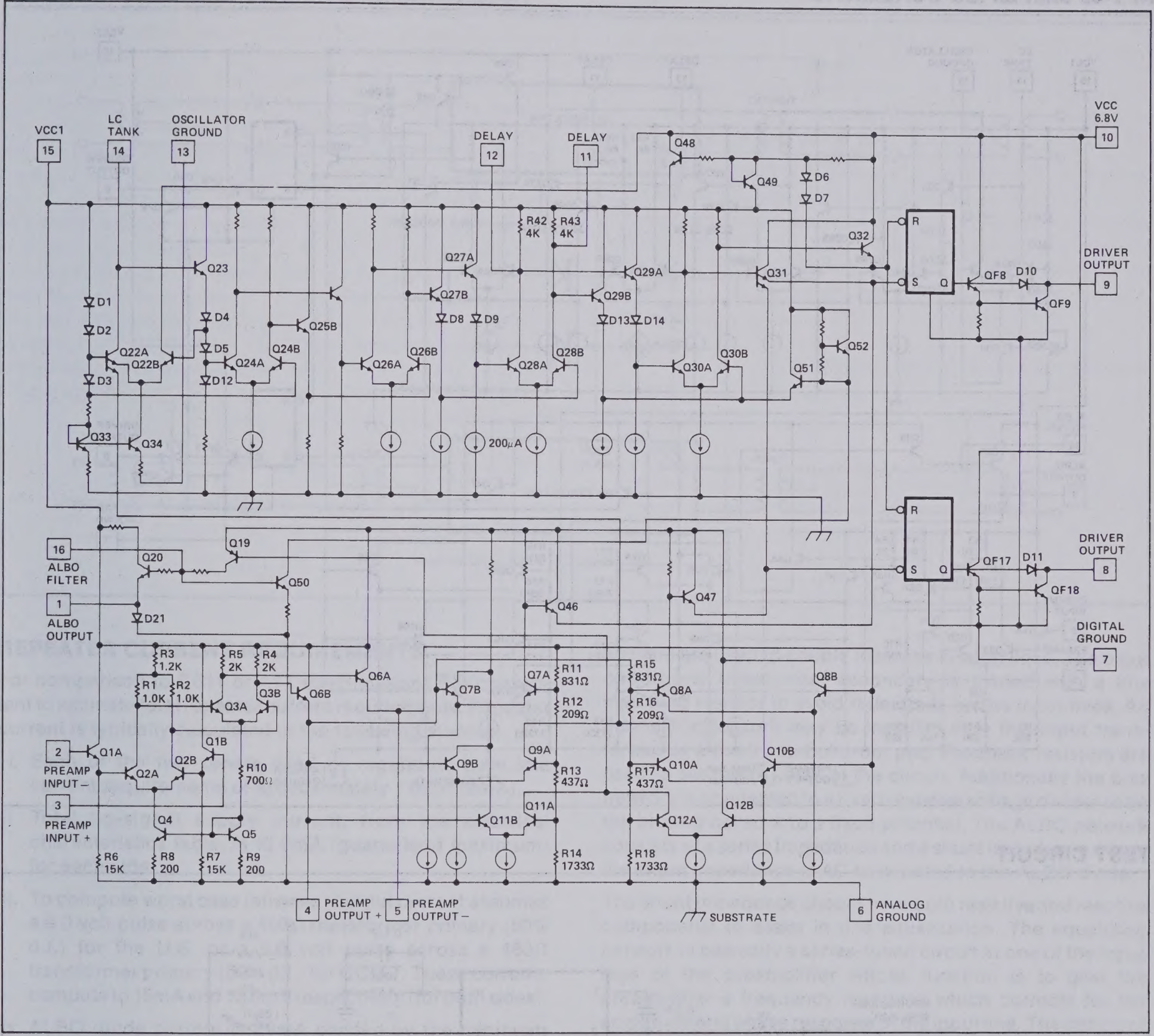
PREAMPLIFIER BANDWIDTH

3dB bandwidth of preamplifier circuit.

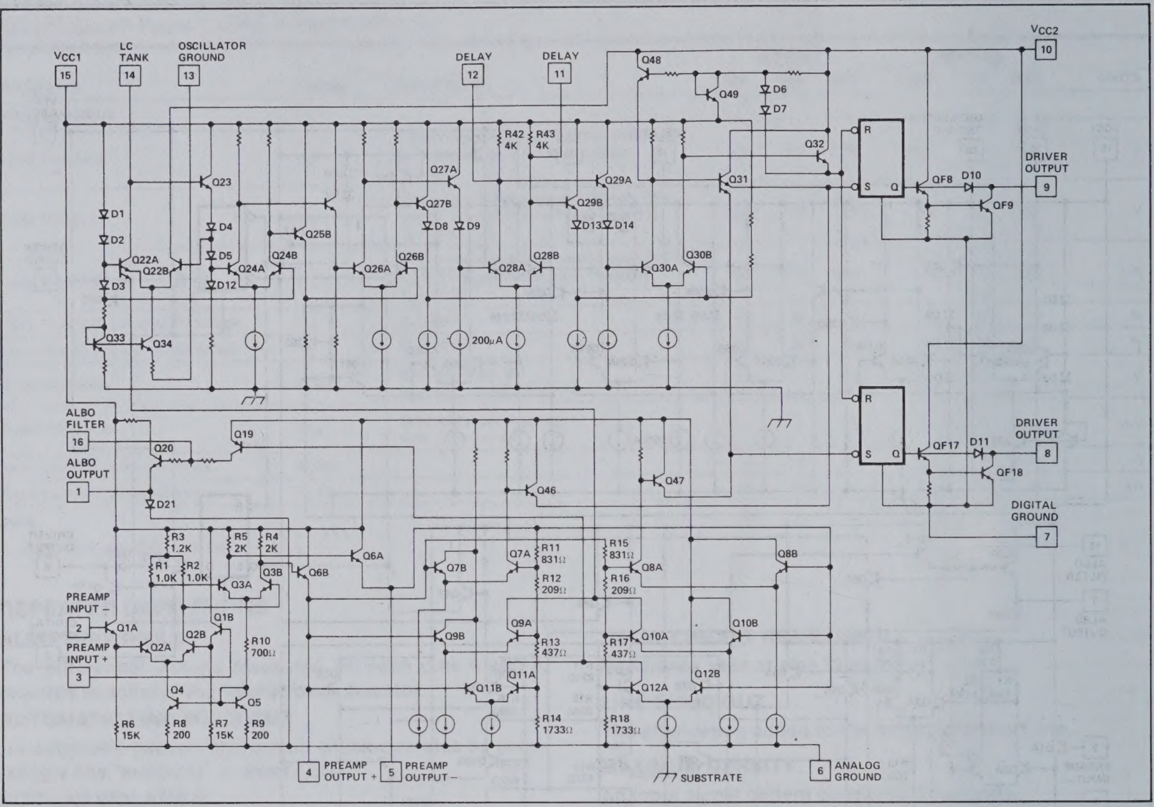
EQUALIZING NETWORK

A network which compensates for the amplitude and phase response of the cable over the operating bandwidth.

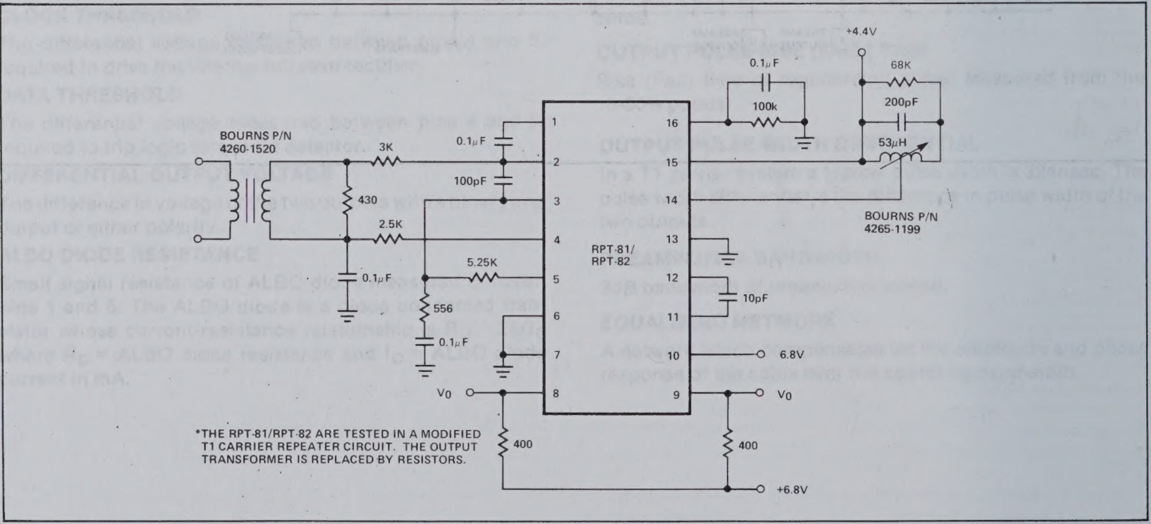
RPT-81 SIMPLIFIED SCHEMATIC


VCC1
15
LC
TANK
14
OSCILLATOR
GROUND
13
DELAY
12
DELAY
11
VCC
6.8V
10
DRIVER
OUTPUT
9
DRIVER
OUTPUT
8
DIGITAL
GROUND
7
ANALOG
GROUND
6
PREAMP
OUTPUT −
5
PREAMP
OUTPUT +
4
PREAMP
INPUT +
3
PREAMP
INPUT −
2
ALBO
OUTPUT
1
ALBO
FILTER
16
SUBSTRATE
Q1A
Q1B
Q2A
Q2B
Q3A
Q3B
Q4
Q5
Q6A
Q6B
Q7A
Q7B
Q8A
Q8B
Q9A
Q9B
Q10A
Q10B
Q11A
Q11B
Q12A
Q12B
Q19
Q20
Q22A
Q22B
Q23
Q24A
Q24B
Q25B
Q26A
Q26B
Q27A
Q27B
Q28A
Q28B
Q29A
Q29B
Q30A
Q30B
Q31
Q32
Q33
Q34
Q46
Q47
Q48
Q49
Q50
Q51
Q52
QF8
QF9
QF17
QF18
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D21
R1 1.0K
R2 1.0K
R3 1.2K
R4 2K
R5 2K
R6 15K
R7 15K
R8 200
R9 200
R10 700Ω
R11 831Ω
R12 209Ω
R13 437Ω
R14 1733Ω
R15 831Ω
R16 209Ω
R17 437Ω
R18 1733Ω
R42 4K
R43 4K
200μA
R
S
Q

RPT-82 SIMPLIFIED SCHEMATIC

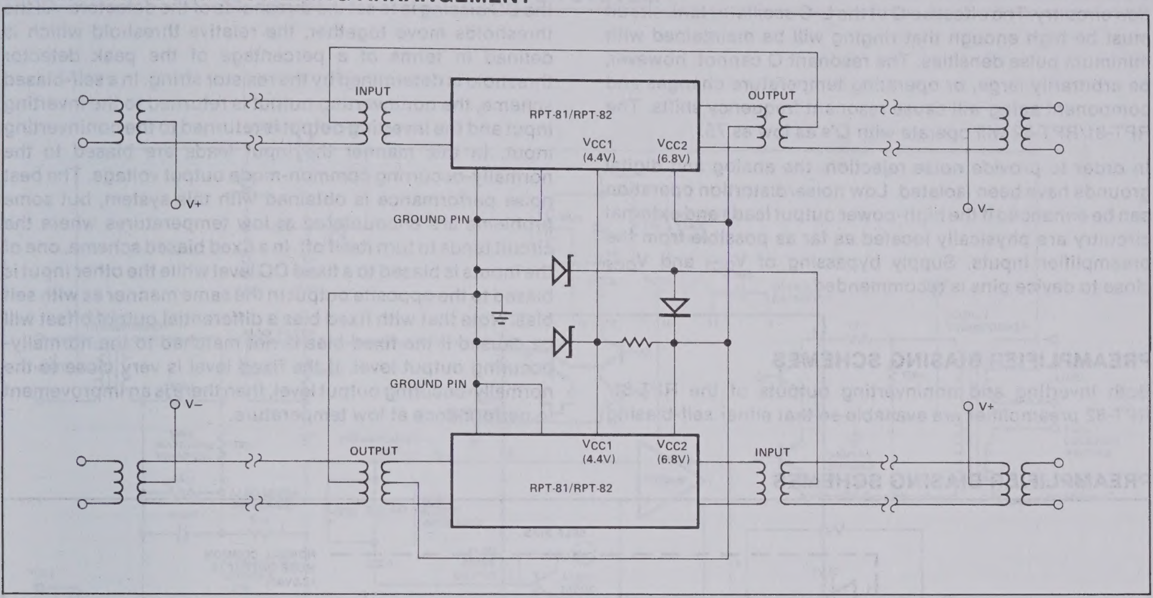

VCC1
15
LC TANK
14
OSCILLATOR GROUND
13
DELAY
12
DELAY
11
VCC2
10
Q48
Q49
D6
D7
R42 4K
R43 4K
Q23
Q27A
Q27B
Q29A
Q29B
Q31
Q32
R
S
Q
QF8
D10
QF9
DRIVER OUTPUT
9
D1
D2
D3
D4
D5
D12
D8
D9
D13
D14
Q22A
Q22B
Q24A
Q24B
Q25B
Q26A
Q26B
Q28A
Q28B
Q30A
Q30B
Q33
Q34
200μA
ALBO FILTER
16
ALBO OUTPUT
1
Q19
Q20
D21
Q46
Q47
QF17
D11
QF18
DRIVER OUTPUT
8
DIGITAL GROUND
7
R3 1.2K
R5 2K
R4 2K
R1 1.0K
R2 1.0K
Q3A
Q3B
Q6A
Q6B
Q7A
Q7B
R11 831Ω
R12 209Ω
R15 831Ω
R16 209Ω
Q8A
Q8B
PREAMP INPUT −
2
PREAMP INPUT +
3
Q1A
Q1B
Q2A
Q2B
R10 700Ω
Q9A
Q9B
R13 437Ω
R17 437Ω
Q10A
Q10B
Q11A
Q11B
Q12A
Q12B
Q4
Q5
R6 15K
R8 200
R7 15K
R9 200
R14 1733Ω
R18 1733Ω
PREAMP OUTPUT +
4
PREAMP OUTPUT −
5
SUBSTRATE
ANALOG GROUND
6

TEST CIRCUIT


BOURNS P/N 4260-1520
3K
430
2.5K
0.1μF
100pF
0.1μF
5.25K
556
0.1μF
V0
400
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
RPT-81/ RPT-82
+4.4V
0.1μF
100k
68K
200pF
53μH
BOURNS P/N 4265-1199
10pF
6.8V
V0
400
+6.8V

*THE RPT-81/RPT-82 ARE TESTED IN A MODIFIED T1 CARRIER REPEATER CIRCUIT. THE OUTPUT TRANSFORMER IS REPLACED BY RESISTORS.

TYPICAL REPEATER POWERING ARRANGEMENT



REPEATER CURRENT REQUIREMENTS

For comparison to CCIT or ATT specifications it is convenient to estimate total repeater current requirements. Repeater current is typically calculated in the following manner:

i. Each of the two zeners used as regulators have idle current requirements of approximately 1.0mA (2mA).

ii. Total no-signal supply current, from the electrical characteristics table, is 13.0mA (guaranteed maximum) for each side.

iii. To compute worst case (all ones) output current assumes a 6.0 volt pulse across a 400Ω transformer primary (50% d.f.) for the U.S. or a 6.0 volt pulse across a 480Ω transformer primary (50% d.f.) for CCITT. These currents compute to 15mA and 12.5mA respectively (for both sides).

iv. ALBO diode current is 26mA divided by the minimum required ALBO resistance (approximately 8Ω), which is 6.5mA for both sides.

Adding the currents in ii, iii, and iv gives the following typical repeater current requirements:

i. U.S. .... 49.5mA (worst case all ones output)
ii. Europe .... 47.0mA (worst case all ones output)

APPLICATIONS INFORMATION

In a typical repeater system extensive external circuitry is required. The regulator network assembled from zener diodes and resistors is used to power the integrated circuit. Normally one common circuit is provided for the two ICs operating in opposite directions. Input and output transformers are used to couple the transmission lines. The input one-to-one transformer secondary is loaded with a line matching resistor to avoid reflections on the input lines. An attenuator network may be installed after this input transformer as a fixed line-build-out pad. Feedback resistors are used to set the DC bias of the circuit. Additionally the bias network is connected to a fixed resistive voltage divider to tie the biasing network to a fixed potential. The ALBO network consists of a series impedance and a shunt impedance where the shunt impedance is AC terminated to the ALBO diode.

The shunt impedance should have both resistive and reactive components to assist in line equalization. The equalizing network is basically a series-tuned circuit in one of the input legs of the preamplifier whose function is to give the preamplifier a frequency response which corrects for the amplitude and phase response of the input line. The design of the equalizing network is very important to the system performance. A lag capacitor across the preamplifier input stabilizes the preamplifier. The output transformer normally incorporates a fault locating winding which is used, in conjunction with appropriate filters, to detect defective repeaters. The input transformer has a center-tapped primary to allow for a simplex powering system.

The RPT-81/RPT-82 oscillator allows two modes of operation controllable by pin 13 (Oscillator Control). When grounded, the oscillator is in a free-running mode. With pin 13 open, the oscillator works in a pulsed, ringing mode. In both cases the external L-C tank circuit determines the oscillation frequency.

The external delay capacitor (across pins 11 and 12) provides 90° of phase shift through the clock amplifier.

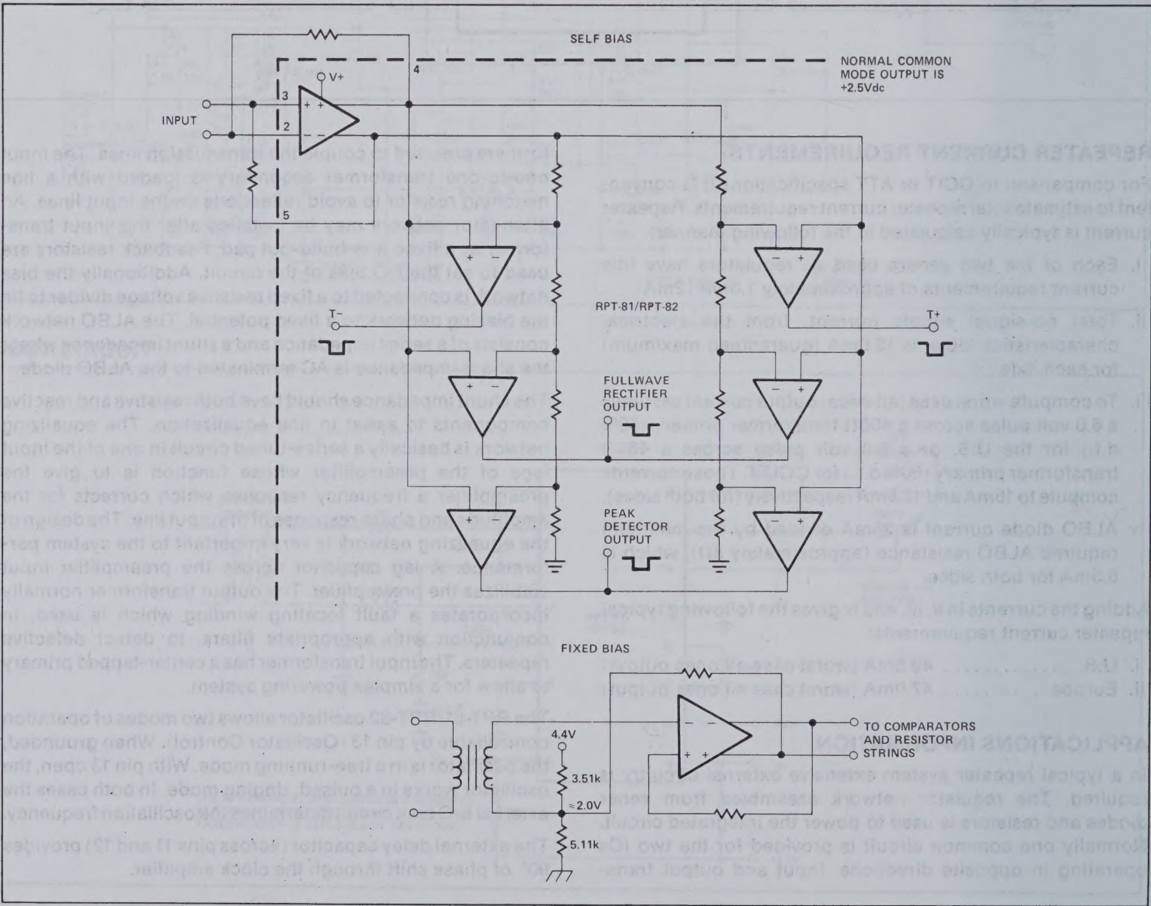
Oscillator-tank-circuit Q directly affects the clock regeneration circuitry. The effective Q of the L-C oscillator tank circuit must be high enough that ringing will be maintained with minimum pulse densities. The resonant Q cannot, however, be arbitrarily large, or operating temperature changes and component aging will cause resonant frequency shifts. The RPT-81/RPT-82 will operate with Q's as low as 75.

In order to provide noise rejection, the analog and digital grounds have been isolated. Low noise/distortion operation can be enhanced if the high-power output leads and external circuitry are physically located as far as possible from the preamplifier inputs. Supply bypassing of V_{CC1} and V_{CC2} close to device pins is recommended.

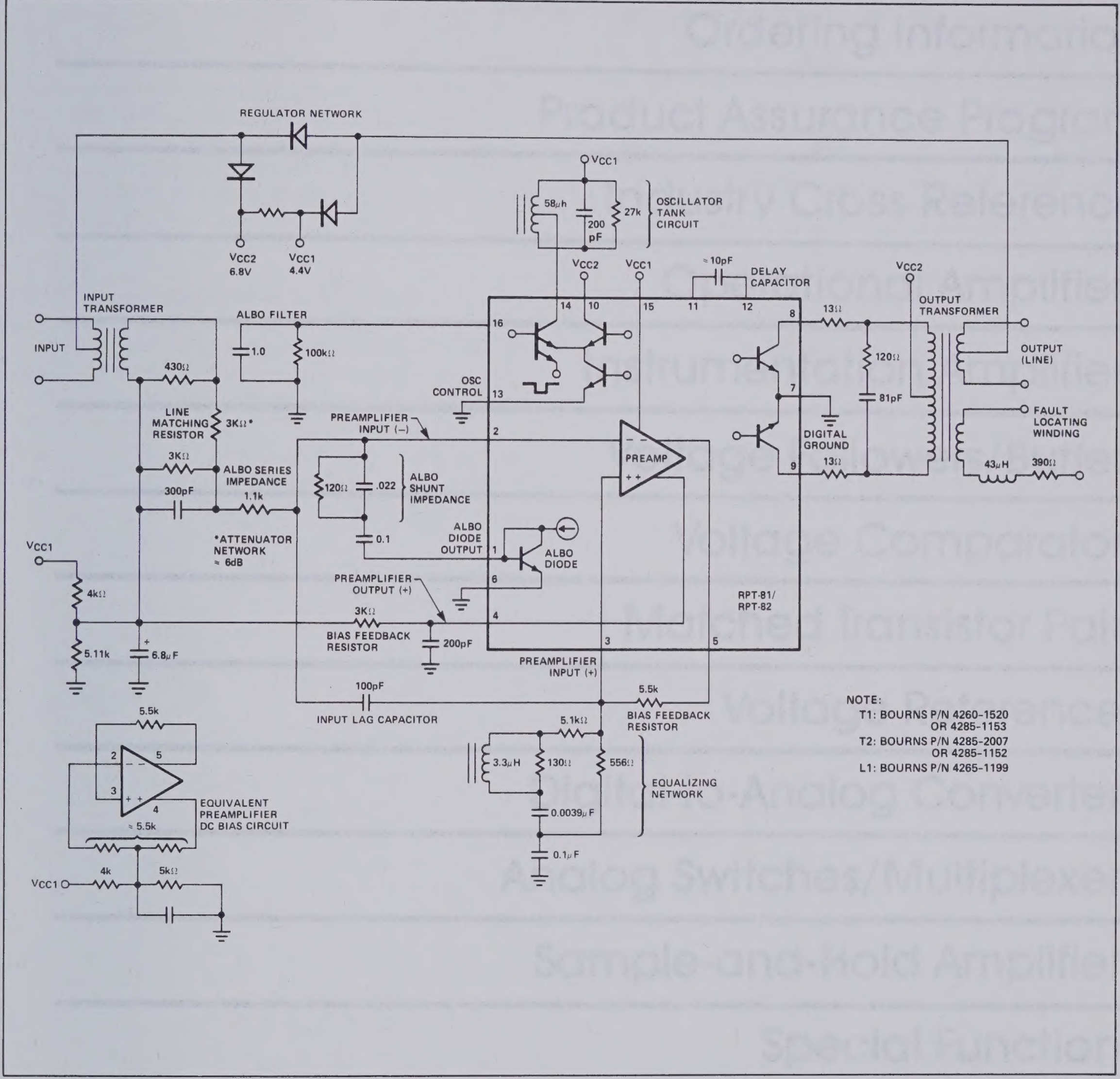
PREAMPLIFIER BIASING SCHEMES

Both inverting and noninverting outputs of the RPT-81/RPT-82 preamplifier are available so that either self-biasing or fixed-biasing techniques may be employed. The effect of the DC biasing is to set the thresholds of the detectors. All the thresholds move together, the relative threshold which is defined in terms of a percentage of the peak detector threshold is determined by the resistor string. In a self-biased scheme, the noninverting output is returned to the inverting input and the inverting output is returned to the noninverting input. In this manner the input leads are biased to the normally-occurring common-mode output voltage. The best noise performance is obtained with this system, but some problems are encountered at low temperatures where the circuit tends to turn itself off. In a fixed biased scheme, one of the inputs is biased to a fixed DC level while the other input is biased to the opposite output in the same manner as with self bias. Note that with fixed bias a differential output offset will be caused if the fixed bias is not matched to the normally-occuring output level. If the fixed level is very close to the normally-occuring output level, then there is an improvement in performance at low temperature.

PREAMPLIFIER BIASING SCHEMES


SELF BIAS
NORMAL COMMON MODE OUTPUT IS +2.5Vdc
V+
4
3
2
5
INPUT
RPT-81/RPT-82
T−
T+
FULLWAVE RECTIFIER OUTPUT
PEAK DETECTOR OUTPUT
FIXED BIAS
4.4V
3.51k
≈2.0V
5.11k
TO COMPARATORS AND RESISTOR STRINGS

RPT-81/RPT-82 IN TYPICAL 1.544MHz T1 REPEATER SYSTEM


REGULATOR NETWORK
VCC2 6.8V
VCC1 4.4V
VCC1
58μh
200 pF
27k
OSCILLATOR TANK CIRCUIT
VCC2
VCC1
≈ 10pF
DELAY CAPACITOR
VCC2
INPUT TRANSFORMER
INPUT
ALBO FILTER
1.0
100kΩ
430Ω
LINE MATCHING RESISTOR
3KΩ *
3KΩ
ALBO SERIES IMPEDANCE
300pF
1.1k
*ATTENUATOR NETWORK ≈ 6dB
OSC CONTROL
PREAMPLIFIER INPUT (−)
120Ω
.022
0.1
ALBO SHUNT IMPEDANCE
ALBO DIODE OUTPUT
ALBO DIODE
PREAMP
PREAMPLIFIER OUTPUT (+)
3KΩ
BIAS FEEDBACK RESISTOR
200pF
VCC1
4kΩ
5.11k
6.8μF
RPT-81/ RPT-82
14
10
15
11
12
16
13
2
1
6
4
3
5
8
7
9
13Ω
120Ω
81pF
13Ω
DIGITAL GROUND
OUTPUT TRANSFORMER
OUTPUT (LINE)
FAULT LOCATING WINDING
43μH
390Ω
PREAMPLIFIER INPUT (+)
100pF
INPUT LAG CAPACITOR
5.5k
BIAS FEEDBACK RESISTOR
5.1kΩ
3.3μH
130Ω
556Ω
EQUALIZING NETWORK
0.0039μF
0.1μF
5.5k
2
5
3
4
EQUIVALENT PREAMPLIFIER DC BIAS CIRCUIT
≈ 5.5k
4k
5kΩ
VCC1

NOTE:
T1: BOURNS P/N 4260-1520
OR 4285-1153
T2: BOURNS P/N 4285-2007
OR 4285-1152
L1: BOURNS P/N 4265-1199

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ADVANCE PRODUCTS INFORMATION

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OP-32 16-4
High-Speed Programmable Micropower Operational Amplifier

MAT-02 16-8
Low-Noise, Matched Dual Monolithic Transistor

ADVANCE PRODUCTS INFORMATION

These products are all in the final phase of product characterization. This preliminary information is given only as a guide to design. Please contact your local PMI sales office or representative for finalized data sheet specifications and availability.

OP-32 Programmable Micropower Operational Amplifier

This is a decompensated OP-22 that offers considerable speed enhancement . Packaging is 8-pin hermetic DIP or 8-pin epoxy. Quiescent supply current is set by one external resistor which also controls the frequency response.

MAT-02 Matched Monolithic Dual Transistors

The MAT-02 is a new monolithic dual transistor designed for very low offset voltage (ΔV_{BE}), low voltage noise, and excellent log conformity. Another design feature is high current-gain over a wide range of collector current. The result is a transistor that approaches the theoretical limits of performance. This new dual transistor is ideal for high-gain input stages or for use in log amplifier and multiplier circuits.

OP-32

HIGH-SPEED PROGRAMMABLE MICROPOWER OPERATIONAL AMPLIFIER (SINGLE OR DUAL SUPPLY)

PRELIMINARY

FEATURES

- **Programmable Supply Current .... 1μA to 2mA**
- **Single Supply Operation .... +3V to +30V**
- **Dual Supply Operation .... ±1.5V to ±15V**
- **Low Input Offset Voltage 100μV**
- **Low Input Offset Voltage Drift .... 0.75μV/°C**
- **High Common-Mode Input Range ... V– to V+ (–1.5V)**
- **High CMRR and PSRR 115dB**
- **High Open-Loop Gain 2000V/mV**
- **±30V Input Overvoltage Protection**
- **Fast .... 1V/μs @ I_{SET} = 20μA**
- **LM4250 Pinout**
- **Compensated for Minimum Gain of 10**

GENERAL DESCRIPTION

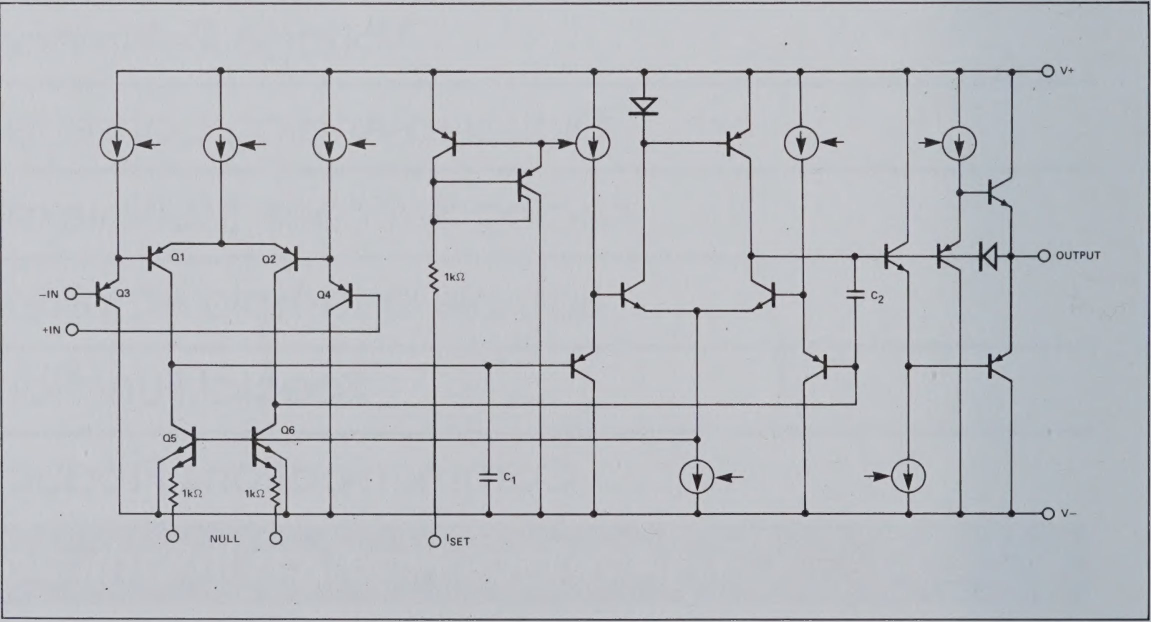
The OP-32 is a high-speed, high-gain programmable operational amplifier. Both offset voltage and offset current are low, and both are stable with changes in temperature, supply voltage, and set current. High CMRR and PSRR ensure precision performance when the OP-32 is used with an unregulated battery or vehicular electrical systems.

The wide input voltage range, including the negative supply or ground, allows use in single-battery applications. The OP-32 is characterized over a wide supply range of ±1.5V to ±15V. This guarantees predictable performance with any commonly available supply.

The ability to operate at relatively high speed with low power consumption makes this amplifier ideal for remote applications where power is limited. The programmability allows each amplifier in a system to be set for the minimum power consumption necessary for each specific application. Programmability also makes it possible to adjust the bandwidth and phase shift.

The OP-32 pinout is identical to the LM4250 and many other micropower operational amplifiers. This allows easy upgrading of system performance.

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage	±18V
Power Dissipation	500mW
Differential Input Voltage	±30
Input Voltage	Supply Voltage
Storage Temperature Range	
Z Package	−65° C to +150° C
P Package	−55° C to +125° C
Operating Temperature Range	
OP-32A, B (Z package)	−55° C to +125° C
OP-32E, F & G (Z or P package)	−25° C to +85° C
Lead Temperature Range (Soldering, 60 sec)	300° C
DICE Junction Temperature	−65° C to +150° C

NOTE:

1. Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm1.5V$ to $\pm15V$, $1\mu A \le I_{SET} \le 30\mu A$, $T_A = +25° C$, unless otherwise noted.

			OP-32A/E			OP-32B/F			OP-32G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		—	100	300	—	200	500	—	400	1000	μV
Input Offset current	I_{OS}	$V_{CM} = 0$	—	0.2	1	—	0.3	2	—	0.5	3	nA
Input Bias Current (Note 1)	I_B	$I_{SET} = 1\mu A$	—	2.6	5	—	3.0	7.5	—	4.0	10	nA
		$I_{SET} = 10\mu A$	—	19	30	—	24	35	—	30	50	
		$I_{SET} = 30\mu A$	—	45	75	—	50	100	—	60	125	
Input Voltage Range	IVR	$V_S = \pm15V$	−15.0/13.5	—	—	−15.0/13.5	—	—	−15.0/13.5	—	—	V
Common-Mode Rejection Ratio	CMRR	$V_S = \pm15V$ $-15V \le V_{CM} \le +13.5V$	100	115	—	95	110	—	85	100	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm1.5V$ to $\pm15V$; and $V- = 0V$, $V+ = 3V$ to $30V$.	—	1	6	—	3	12	—	10	25	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm15V$, $R_L = 100k\Omega$ $R_L = 10k\Omega$, $10\mu A \le I_{SET} \le 30\mu A$	1000	2000	—	750	1500	—	500	1000	—	V/mV
Output Voltage Swing	V_O	$V_S = \pm1.5V$ $R_L = 100k\Omega$, $I_{SET} = 1\mu A$ $R_L = 10k\Omega$, $10\mu A \le I_{SET} \le 30\mu A$	±0.8	±0.88	—	±0.8	±0.88	—	±0.75	±0.85	—	V
		$V_S \pm 15V$ $R_L = 100k\Omega$, $I_{SET} = 1\mu A$ $R_L = 10k\Omega$, $10\mu A \le I_{SET} \le 30\mu A$	±14	±14.2	—	±14	±14.2	—	±13.8	±14.2	—	V
Gain-Bandwidth Product		$I_{SET} = 1\mu A$, $R_L = 100k\Omega$	—	100	—	—	100	—	—	100	—	kHz
		$I_{SET} = 30\mu A$, $R_L = 10k\Omega$	—	4500	—	—	4500	—	—	4500	—	
Slew Rate	SR	$V_S = \pm15V$, $I_{SET} = 10\mu A$, $R_L = 10k\Omega$	—	0.6	—	—	0.6	—	—	0.6	—	$V/\mu s$
Supply Current No Load	I_{SY}	$V_S = \pm15V$, $I_{SET} = 1\mu A$	—	15	17	—	15	19	—	15	21	μA
		$I_{SET} = 10\mu A$	—	150	170	—	150	190	—	150	200	
		$I_{SET} = 30\mu A$	—	450	525	—	450	600	—	450	650	
		$V_S = \pm1.5V$, $I_{SET} = 1\mu A$	—	10.5	12.5	—	11	15	—	11	18	
		$I_{SET} = 10\mu A$	—	105	125	—	110	150	—	110	180	
		$I_{SET} = 30\mu A$	—	350	400	—	350	450	—	350	500	

NOTE:

1. I_B and I_{OS} are measured at $V_{CM} = 0$.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 1.5V$ to $\pm 15V$, $1\mu A \leq I_{SET} \leq 30\mu A$, $-55°C \leq T_A \leq +125°C$ for OP-32AZ and OP-32BZ, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-32A MIN	OP-32A TYP	OP-32A MAX	OP-32B MIN	OP-32B TYP	OP-32B MAX	UNITS
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	Unnulled	—	0.75	2.0	—	1.0	2.0	µV/°C
Input Offset Voltage	V_{OS}		—	175	400	—	350	600	µV
Input Offset Current	I_{OS}	$V_{CM} = 0$	—	0.2	1	—	0.3	2	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 1)	—	1	10	—	3	15	pA/°C
Input Bias Current (Note 2)	I_B	$I_{SET} = 1\mu A$	—	2.8	5	—	3.3	7.5	nA
		$I_{SET} = 10\mu A$	—	21	30	—	27	35	
		$I_{SET} = 30\mu A$	—	40	75	—	50	100	
Input Voltage Range	IVR	$V_S = \pm 15V$	-15.0/13.5	—	—	-15.0/13.5	—	—	V
Common-Mode Rejection Ratio	CMRR	$V_S = \pm 15V$ $-15V \leq V_{CM} \leq +13.5V$	90	110	—	86	105	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 1.5V$ to $\pm 15V$ & $V- = 0V$, $V+ = 3V$ to $30V$	—	2	10	—	2.5	20	µV/V
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$							V/mV
		$R_L = 100k\Omega$	200	400	—	200	500	—	
		$R_L = 10k\Omega$, $10\mu A \leq I_{SET} \leq 30\mu A$	500	1000	—	300	750	—	
Output Voltage Swing	V_O	$V_S = \pm 1.5V$ $R_L = 100k\Omega$, $I_{SET} = 1\mu A$ $R_L = 10k\Omega$, $10\mu A \leq I_{SET} \leq 30\mu A$	±0.65	±0.75	—	±0.65	±0.75	—	V
		$V_S = \pm 15V$ $R_L = 100k\Omega$, $I_{SET} = 1\mu A$ $R_L = 10k\Omega$, $10\mu A \leq I_{SET} \leq 30\mu A$	±13.6	±14.0	—	±13.0	±13.5	—	V
Supply Current No Load	I_{SY}	$V_S = \pm 15V$, $I_{SET} = 1\mu A$	—	16	18	—	16	20	µA
		$I_{SET} = 10\mu A$	—	160	180	—	160	200	
		$I_{SET} = 30\mu A$	—	450	550	—	450	600	
		$V_S = \pm 1.5V$, $I_{SET} = 1\mu A$	—	12	14	—	12	17	
		$I_{SET} = 10\mu A$	—	120	140	—	120	170	
		$I_{SET} = 30\mu A$	—	360	450	—	360	500	

NOTE:

1. Sample tested.
2. I_B and I_{OS} are measured at $V_{CM} = 0$.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 1.5V$ to $\pm 15V$, $1\mu A \leq I_{SET} \leq 30\mu A$, $-25°C \leq T_A \leq +85°C$ for OP-32EP/EZ, OP-32FP/FZ, OP-32GP and OP-32GZ, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-32E MIN	OP-32E TYP	OP-32E MAX	OP-32F MIN	OP-32F TYP	OP-32F MAX	OP-32G MIN	OP-32G TYP	OP-32G MAX	UNITS
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	Unnulled	—	0.75	1.5	—	1.0	2.0	—	1.5	3.0	μV/°C
Input Offset Voltage	V_{OS}		—	100	300	—	200	600	—	500	1200	μV
Input Offset Current	I_{OS}	$V_{CM} = 0$	—	0.2	1	—	0.3	2	—	0.5	3	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 1)	—	2	10	—	3	15	—	5	25	pA/°C
Input Bias Current (Note 2)	I_B	$I_{SET} = 1\mu A$	—	2.6	5	—	3.0	7.5	—	4.0	10	nA
		$I_{SET} = 10\mu A$	—	19	30	—	24	35	—	30	50	
		$I_{SET} = 30\mu A$	—	45	75	—	50	100	—	60	125	
Input Voltage Range	IVR	$V_S = \pm 15V$	−15.0/13.5	—	—	−15.0/13.5	—	—	−15.0/13.5	—	—	V
Common-Mode Rejection Ratio	CMRR	$V_S = \pm 15V$ & $-15V \leq V_{CM} \leq +13.5V$	95	110	—	90	105	—	80	100	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 1.5V$ to $\pm 15V$ & $V- = 0V$, $V+ = 3V$ to $30V$	—	3.2	10	—	10	32	—	32	56	μV/V
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$ $R_L = 100k\Omega$	750	1000	—	500	1200	—	400	1000	—	V/mV
		$R_L = 10k\Omega$, $10\mu A \leq I_{SET} \leq 30\mu A$	750	1000	—	500	1200	—	400	1000	—	
Output Voltage Swing	V_O	$V_S = \pm 1.5V$ $R_L = 100k\Omega$, $I_{SET} = 1\mu A$ $R_L = 10k\Omega$, $10\mu A \leq I_{SET} \leq 30\mu A$	±0.70	±0.75	—	±0.65	±0.75	—	±0.6	±0.7	—	V
		$V_S = \pm 15V$ $R_L = 100k\Omega$, $I_{SET} = 1\mu A$ $R_L = 10k\Omega$, $10\mu A \leq I_{SET} \leq 30\mu A$	±13.8	±14.1	—	±13.6	±14.1	—	±13.0	±14.0	—	V
Supply Current No Load	I_{SY}	$V_S = \pm 15V$, $I_{SET} = 1\mu A$	—	16	18	—	16	20	—	16	25	μA
		$I_{SET} = 10\mu A$	—	160	180	—	160	200	—	160	250	
		$I_{SET} = 30\mu A$	—	450	550	—	450	600	—	450	650	
		$V_S = \pm 1.5V$, $I_{SET} = 1\mu A$	—	12	14	—	12	17	—	12	25	
		$I_{SET} = 10\mu A$	—	120	140	—	120	170	—	120	200	
		$I_{SET} = 30\mu A$	—	360	450	—	360	500	—	360	550	

NOTE:
1. Sample tested.
2. I_B and I_{OS} are measured at $V_{CM} = 0$.

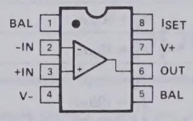
ORDERING INFORMATION†

$T_A = 25°C$ V_{OS} MAX (μV)	PACKAGE EPOXY DIP 8-PIN	PACKAGE HERMETIC DIP 8-PIN	OPERATING TEMPERATURE RANGE
300	OP32AP	OP32AZ*	MIL
300	OP32EP	OP32EZ	IND
500	OP32BP	OP32BZ*	MIL
500	OP32FP	OP32FZ	IND
1000	OP32GP	OP32GZ	IND

*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

PIN CONNECTIONS



8-PIN EPOXY DIP (P-Suffix)

8-PIN HERMETIC DIP (Z-Suffix)

MAT-02

LOW-NOISE, MATCHED DUAL MONOLITHIC TRANSISTOR

PRELIMINARY

FEATURES

- **Low Offset Voltage .... 50μV Max**
- **Low Noise Voltage at 100Hz .... 1.8nV/$\sqrt{\text{Hz}}$ Typ**
- **High Gain (h_{FE}) .... 500 Min at $I_C = 1$mA**
  .... 300 Min at $I_C = 1\mu$A
- **Excellent Log Conformance .... $r_{BE} \simeq 0.3\Omega$**

ORDERING INFORMATION

$T_A = 25°$C V_{OS} Max (μV)	PACKAGE	OPERATING TEMPERATURE RANGE
50	MAT02AH*	MIL
50	MAT02EH	IND
150	MAT02BH*	MIL
150	MAT02FH	IND

*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

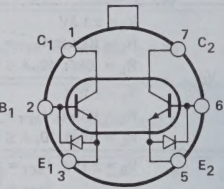
GENERAL DESCRIPTION

The design of the MAT-02 series of NPN dual monolithic transistors is optimized for very low noise, low drift, and low r_{BE}. Precision Monolithics' exclusive Silicon Nitride "Triple-Passivation" process stabilizes the critical device parameters over wide ranges of temperature and elapsed time. Also, the high current gain (h_{FE}) of the MAT-02 is maintained over a wide range of collector current. Exceptional characteristics of the MAT-02 include offset voltage of 50μV max (A/E grades) and 150μV max (B/F grades). Device performance is specified over the full military temperature range as well as at 25° C.

Input protection diodes are provided across the emitter-base junctions to prevent degradation of the device characteristics due to reverse-biased emitter current. The substrate is clamped to the most negative emitter by the parasitic isolation junction created by the protection diodes. This results in isolation between the transistors.

The MAT-02 should be used in any application where low noise is a priority. The MAT-02 can be used as an input stage to make an amplifier with noise voltage of less than 2.0nV/$\sqrt{\text{Hz}}$ at 100Hz. Other applications, such as log/antilog circuits may use the excellent logging conformity of the MAT-02. Typical excess emitter resistance is only 0.3Ω to 0.4Ω. The MAT-02 electrical characteristics approach those of an ideal transistor when operated over a collector current range of 1μA to 10mA.

PIN CONNECTIONS



TO-78
(H-Suffix)

NOTE: Substrate is connected to case. Substrate potential is held at one V_{BE} above the most negative emitter potential.

ELECTRICAL CHARACTERISTICS at $V_{CB} = 15$V, $I_C = 10\mu$A, $T_A = 25°$C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-02A/E MIN	MAT-02A/E TYP	MAT-02A/E MAX	MAT-02B/F MIN	MAT-02B/F TYP	MAT-02B/F MAX	UNITS
Offset Voltage	V_{OS}	$I_C = 10\mu$A	—	—	50	—	—	150	μV
Bias Current	I_B	$I_C = 10\mu$A	—	—	33	—	—	50	nA
Offset Current	I_{OS}	$I_C = 10\mu$A	—	—	0.6	—	—	2	nA
Current Gain	h_{FE}	$I_C = 1$mA	500	—	—	400	—	—	
		$I_C = 100\mu$A	500	—	—	400	—	—	
		$I_C = 10\mu$A	400	—	—	300	—	—	
		$I_C = 1\mu$A	300	—	—	200	—	—	
Current Gain Match	h_{FE} Match	$10\mu A \le I_C \le 1mA$	—	—	2	—	—	4	%
Excess Emitter Resistance	r_{BE}		—	0.3	0.5	—	0.3	0.5	Ω
Noise Voltage	e_n	$I_C = 100\mu$A, f = 100Hz	—	1.8	—	—	1.8	—	nV/$\sqrt{\text{Hz}}$
Collector Base Voltage	V_{CB}		—	—	40	—	—	40	V

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PACKAGE INFORMATION

PMI Letter Designator	Package Description	38510 Applicable Configuration	Page
Package Dimensions — Metal Cans			
H	6-Lead TO-78 Metal Can	—	**17-3**
J	8-Lead TO-99 Metal Can	A1	**17-3**
K	10-Lead TO-100 Metal Can	A2	**17-3**
Package Dimensions — Ceramic DIPs			
Z	8-Lead Ceramic DIP	D4-1	**17-4**
Y	14-Lead Ceramic DIP	D1-1	**17-4**
Q	16-Lead Ceramic DIP	D2-1	**17-5**
X	18-Lead Ceramic DIP	D6-1	**17-5**
R	20-Lead Ceramic DIP	D8-1	**17-6**
V	24-Lead Ceramic DIP	D3-1	**17-7**
T	28-Lead Ceramic DIP	—	**17-8**
Package Dimensions — Side-Brazed DIPs			
YB*	14-Lead Side-Brazed DIP	D1-3	**17-9**
QB*	16-Lead Side-Brazed DIP	D2-3	**17-9**
XB*	18-Lead Side-Brazed DIP	D6-3	**17-10**
RB*	20-Lead Side-Brazed DIP	D8-3	**17-10**
VB*	24-Lead Side-Brazed DIP	D3-3	**17-11**
TB*	28-Lead Side-Brazed DIP	—	**17-12**
Package Dimensions — Epoxy DIPS			
P	8-Lead Epoxy DIP	—	**17-13**
P	14-Lead Epoxy DIP	—	**17-13**
P	16-Lead Epoxy DIP	—	**17-14**
P	18-Lead Epoxy DIP	—	**17-14**
P	20-Lead Epoxy DIP	—	**17-15**
P	24-Lead Epoxy DIP	—	**17-16**

PMI Letter Designator	Package Description	38510 Applicable Configuration	Page
Package Dimensions — Flatpacks			
L	10-Lead Flatpack	F4-1	**17-17**
LB*	10-Lead Flatpack, Bottom-Brazed	F4-2	**17-17**
M*	14-Lead Flatpack	F1-1	**17-17**
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F*	16-Lead Flatpack	F5-1	**17-18**
FB*	16-Lead Flatpack, Bottom-Brazed	F5-2	**17-18**
N*	24-Lead Flatpack	F8-1	**17-18**
NB*	24-Lead Flatpack, Bottom-Brazed	F8-2	**17-18**
Package Dimensions — Leadless Chip Carriers			
RC*	20-Position Chip Carrier	C-2	**17-19**
TC*	28-Position Chip Carrier	C4	**17-20**

*Special Order Only.

Dimensioning Symbols

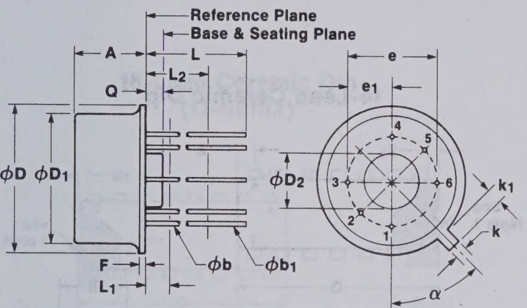
The symbols to be used for dimensioning case outlines will be as listed below. To designate the dimension as a diameter, the lower-case Greek letter ϕ (phi) will be added in front of the dimension symbol.

A — Body dimensions.
ϕb — Terminal lead diameters.
b — Terminal lead widths.
c — Terminal lead thicknesses.
ϕD — Body diameters.
D — Body lengths.
E — Body widths.
e — Terminal lead spacings.
F — Flange dimensions.
k — Index dimensions, length.
L — Terminal lead lengths.
Q — Standoff height. The height from the seating plane or a reference plane parallel to the seating plane.
R — Radius dimensions.
S — Distance between terminal leads and the body end.
α — Angular dimensions.

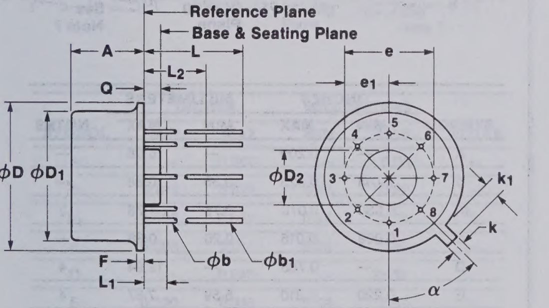
Standard lead finish is matte tin/lead per MIL-STD-883B. Other lead finishes per MIL-STD-883B are available at special request.

PACKAGE DIMENSIONS — METAL CANS

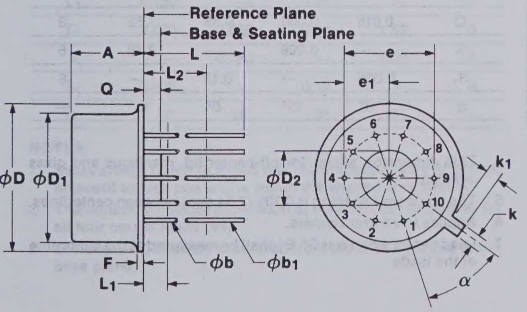
6-Lead TO-78 Metal Can (H-Suffix)


Reference Plane
Base & Seating Plane
A
L
L2
Q
e
e1
ϕD ϕD1
ϕD2
k1
k
F
L1
ϕb
ϕb1
α
1
2
3
4
5
6

8-Lead TO-99 Metal Can (J-Suffix)


Reference Plane
Base & Seating Plane
A
L
L2
Q
e
e1
ϕD ϕD1
ϕD2
k1
k
F
L1
ϕb
ϕb1
α
1
2
3
4
5
6
7
8

10-Lead TO-100 Metal Can (K-Suffix)


Reference Plane
Base & Seating Plane
A
L
L2
Q
e
e1
ϕD ϕD1
ϕD2
k1
k
F
L1
ϕb
ϕb1
α
1
2
3
4
5
6
7
8
9
10

6 & 8-Lead Can Dimensions

	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A	0.165	0.185	4.19	4.70	—
ϕb	0.016	0.019	0.41	0.48	1
ϕb_1	0.016	0.021	0.41	0.53	1
ϕD	0.335	0.370	8.51	9.40	—
ϕD_1	0.305	0.335	7.75	8.51	—
ϕD_2	0.110	0.160	2.79	4.06	—
e	0.200 BSC		5.08 BSC		3
e_1	0.100 BSC		2.54 BSC		3
F	—	0.040	—	1.02	—
k	0.027	0.034	0.69	0.86	—
k_1	0.027	0.045	0.69	1.14	2
L	0.500	0.750	12.70	19.05	1
L_1	—	0.050	—	1.27	1
L_2	0.250	—	6.35	—	1
Q	0.010	0.045	0.25	1.14	—
α	45° BSC		45° BSC		3

10-Lead Can Dimensions

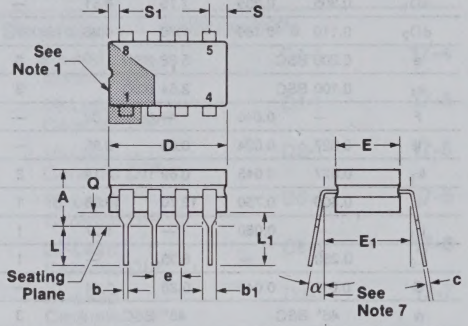
	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A	0.165	0.185	4.19	4.70	—
ϕb	0.016	0.019	0.41	0.48	1
ϕb_1	0.016	0.021	0.41	0.53	1
ϕD	0.335	0.370	8.51	9.40	—
ϕD_1	0.305	0.335	7.75	8.51	—
ϕD_2	0.110	0.160	2.79	4.06	—
e	0.230 BSC		5.84 BSC		3
e_1	0.115 BSC		2.92 BSC		3
F	—	0.040	—	1.02	—
k	0.027	0.034	0.69	0.86	—
k_1	0.027	0.045	0.69	1.14	2
L	0.500	0.750	12.70	19.05	1
L_1	—	0.050	—	1.27	1
L_2	0.250	—	6.35	—	1
Q	0.010	0.045	0.25	1.14	—
α	36° BSC		36° BSC		3

NOTES:

1. (All leads) ϕb applies between L_1 and L_2. ϕb_1 applies between L_2 and 0.500 (12.70 mm) from the reference plane. Diameter is uncontrolled in L_1 and beyond 0.500 (12.70 mm) from the reference plane.
2. Measured from the maximum diameter of the product.
3. Leads having a maximum diameter 0.019 (0.48 mm) measured in gaging plane 0.054 (1.37 mm) + 0.001 (0.03 mm) − 0.000 (0.00 mm) below the base plane of the product is within 0.007 (0.18 mm) of their true position relative to a maximum width tab.

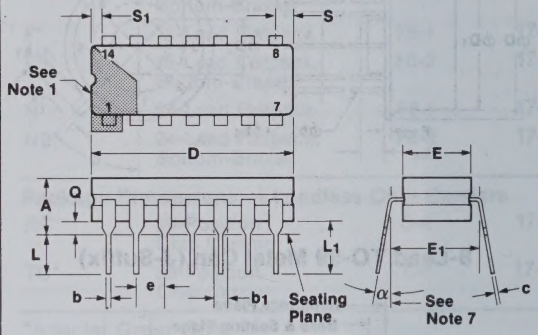
PACKAGE DIMENSIONS — CERAMIC DIPS

8-Lead Ceramic Dip



SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	—	0.200	—	5.08	—
b	0.014	0.023	0.36	0.58	—
b_1	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	—
D	—	0.405	—	10.29	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	—
L_1	0.150	—	3.81	—	—
Q	0.015	0.060	0.38	1.52	3
S	—	0.055	—	1.35	6
S_1	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

14-Lead Ceramic Dip



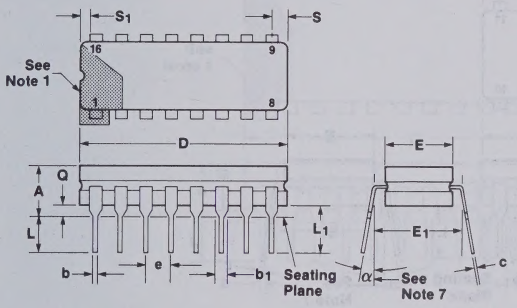
SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	—	0.200	—	5.08	—
b	0.014	0.023	0.36	0.58	—
b_1	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	—
D	—	0.785	—	19.94	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	—
L_1	0.150	—	3.81	—	—
Q	0.015	0.060	0.38	1.52	3
S	—	0.098	—	2.49	6
S_1	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

NOTES:

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum limit for dimension b_1 may be 0.023 (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 (2.54 mm) between centerlines.
6. Applies to all four corners.
7. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.

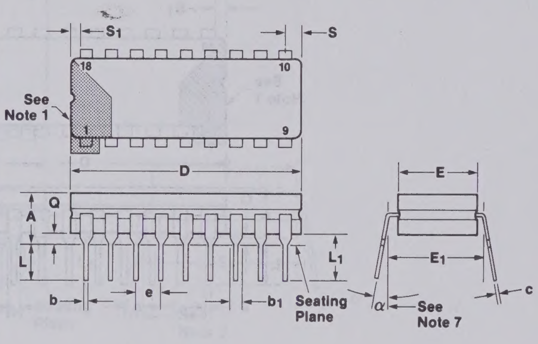
PACKAGE DIMENSIONS — CERAMIC DIPS

16-Lead Ceramic Dip (Q-Suffix)



	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A	—	0.200	—	5.08	—
b	0.014	0.023	0.36	0.58	—
b_1	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	—
D	—	0.840	—	21.34	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	—
L_1	0.150	—	3.81	—	—
Q	0.015	0.060	0.38	1.52	3
S	—	0.080	—	2.03	6
S_1	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

18-Lead Ceramic Dip (X-Suffix)



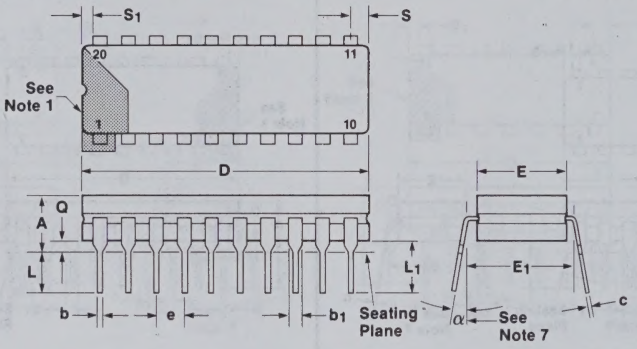
	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A	—	0.200	—	5.08	—
b	0.014	0.023	0.36	0.58	—
b_1	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	—
D	—	0.960	—	24.38	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	—
L_1	0.150	—	3.81	—	—
Q	0.015	0.060	0.38	1.52	3
S	—	0.098	—	2.49	6
S_1	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

NOTES:

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum limit for dimension b_1 may be 0.023 (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 (2.54 mm) between centerlines.
6. Applies to all four corners.
7. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.

PACKAGE DIMENSIONS — CERAMIC DIPS

20-Lead Ceramic Dip (R-Suffix)



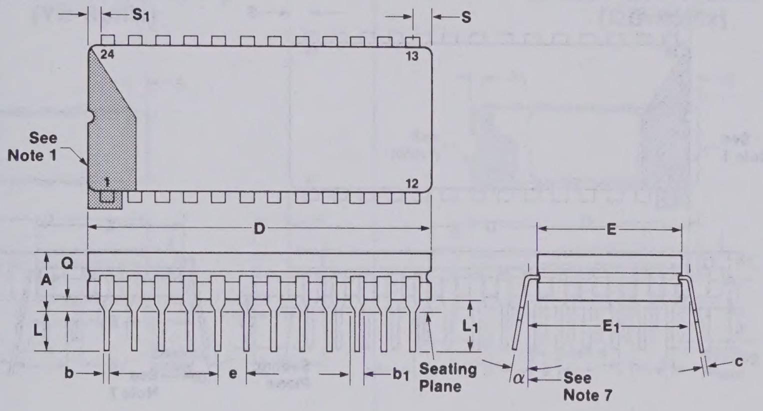
SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	—	0.200	—	5.08	—
b	0.014	0.023	0.36	0.58	—
b_1	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	—
D	—	1.060	—	26.92	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	—
L_1	0.150	—	3.81	—	—
Q	0.015	0.060	0.38	1.52	3
S	—	0.080	—	2.03	6
S_1	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

NOTES:

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum limit for dimension b_1 may be 0.023 (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 (2.54 mm) between centerlines.
6. Applies to all four corners.
7. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.

PACKAGE DIMENSIONS — CERAMIC DIPS

24-Lead Ceramic Dip (V-Suffix)



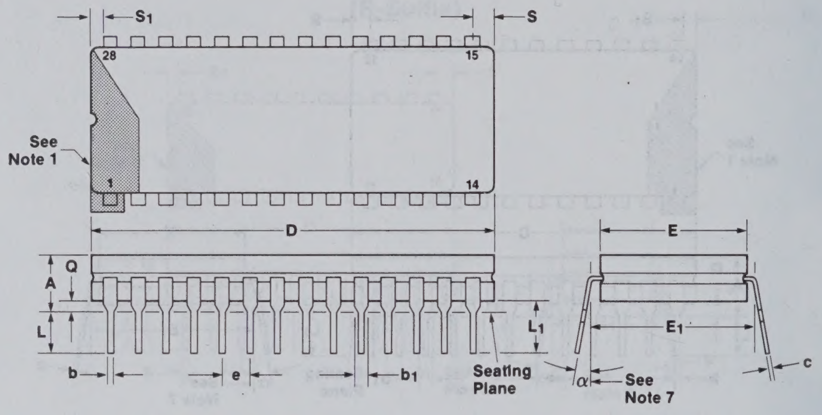
SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	—	0.225	—	5.72	—
b	0.014	0.023	0.36	0.58	—
b_1	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	—
D	—	1.290	—	32.77	4
E	0.500	0.610	12.70	15.49	4
E_1	0.590	0.620	14.99	15.75	7
e	0.100 BSC		2.54 BSC		5
L	0.120	0.200	3.05	5.08	—
L_1	0.150	—	3.81	—	—
Q	0.015	0.075	0.38	1.91	3
S	—	0.098	—	2.49	6
S_1	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

NOTES:

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum limit for dimension b_1 may be 0.023 (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 (2.54 mm) between centerlines.
6. Applies to all four corners.
7. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.

PACKAGE DIMENSIONS — CERAMIC DIPS

28-Lead Ceramic Dip (T-Suffix)



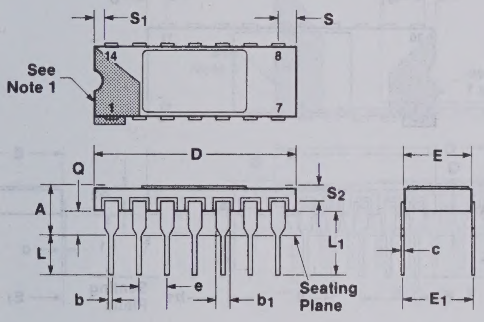
	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A	—	0.225	—	5.72	—
b	0.014	0.023	0.36	0.58	—
b_1	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	—
D	—	1.490	—	37.85	4
E	0.500	0.610	12.70	15.49	4
E_1	0.590	0.620	14.99	15.75	7
e	0.100 BSC		2.54 BSC		5
L	0.120	0.200	3.05	5.08	—
L_1	0.150	—	3.81	—	—
Q	0.015	0.075	0.38	1.91	3
S	—	0.098	—	2.49	6
S_1	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

NOTES:

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum limit for dimension b_1 may be 0.023 (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 (2.54 mm) between centerlines.
6. Applies to all four corners.
7. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.

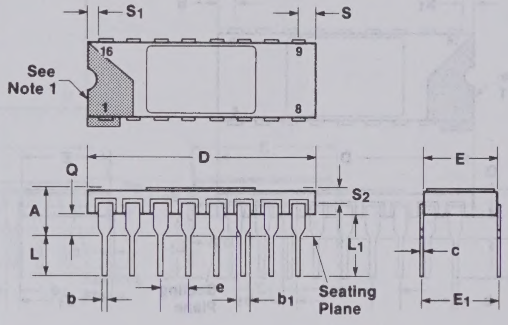
PACKAGE DIMENSIONS — SIDE-BRAZED DIPS

14-Lead Side-Brazed Dip
(YB-Suffix)



	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A	—	0.200	—	5.08	—
b	0.014	0.023	0.36	0.58	—
b_1	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	—
D	—	0.785	—	19.94	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	—
L_1	0.150	—	3.81	—	—
Q	0.015	0.060	0.38	1.52	3
S	—	0.098	—	2.49	6
S_1	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

16-Lead Side-Brazed Dip
(QB-Suffix)



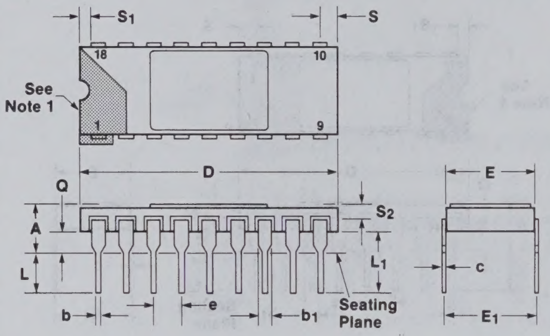
	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A	—	0.200	—	5.08	—
b	0.014	0.023	0.36	0.58	—
b_1	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	—
D	—	0.840	—	21.34	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	—
L_1	0.150	—	3.81	—	—
Q	0.015	0.060	0.38	1.52	3
S	—	0.080	—	2.03	6
S_1	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

NOTES:

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum limit for dimension b_1 may be 0.023 (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 (2.54 mm) between centerlines.
6. Applies to all four corners.
7. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.

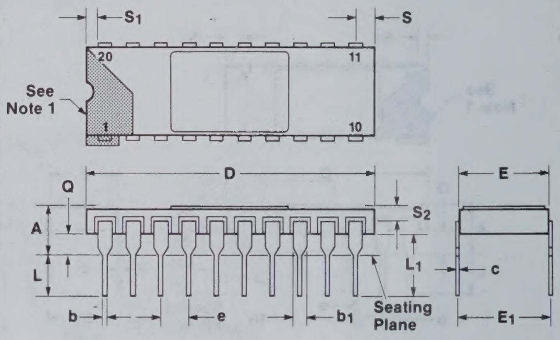
PACKAGE DIMENSIONS — SIDE-BRAZED DIPS

18-Lead Side-Brazed Dip (XB-Suffix)



SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	—	0.200	—	5.08	—
b	0.014	0.023	0.36	0.58	—
b_1	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	—
D	—	0.960	—	24.38	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	—
L_1	0.150	—	3.81	—	—
Q	0.015	0.060	0.38	1.52	3
S	—	0.098	—	2.49	6
S_1	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

20-Lead Side-Brazed Dip (RB-Suffix)



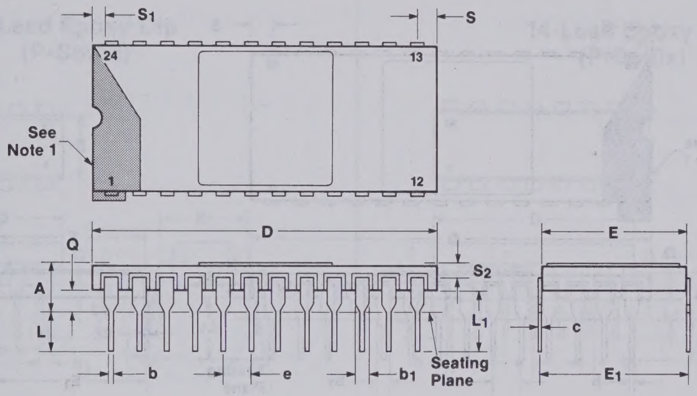
SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	—	0.200	—	5.08	—
b	0.014	0.023	0.36	0.58	—
b_1	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	—
D	—	1.060	—	26.92	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	—
L_1	0.150	—	3.81	—	—
Q	0.015	0.060	0.38	1.52	3
S	—	0.080	—	2.03	6
S_1	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

NOTES:

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum limit for dimension b_1 may be 0.023 (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 (2.54 mm) between centerlines.
6. Applies to all four corners.
7. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.

PACKAGE DIMENSIONS — SIDE-BRAZED DIPS

24-Lead Side-Brazed Dip
(VB-Suffix)



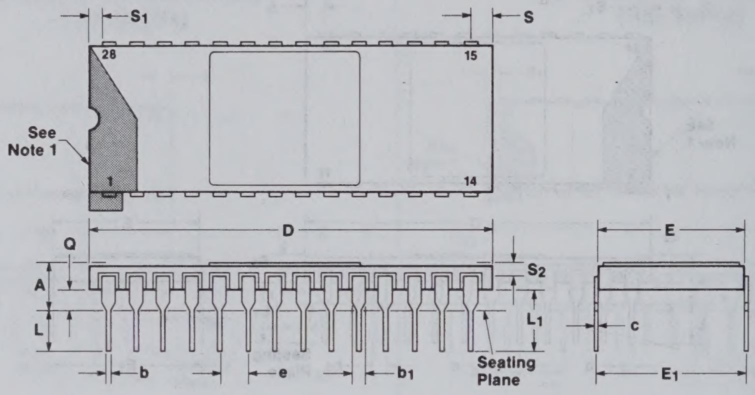
SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	—	0.225	—	5.72	—
b	0.014	0.023	0.36	0.58	—
b_1	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	—
D	—	1.290	—	32.77	4
E	0.500	0.610	12.70	15.49	4
E_1	0.590	0.620	14.99	15.75	7
e	0.100 BSC		2.54 BSC		5
L	0.120	0.200	3.05	5.08	—
L_1	0.150	—	3.81	—	—
Q	0.015	0.075	0.38	1.91	3
S	—	0.098	—	2.49	6
S_1	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

NOTES:

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum limit for dimension b_1 may be 0.023 (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 (2.54 mm) between centerlines.
6. Applies to all four corners.
7. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.

PACKAGE DIMENSIONS — SIDE-BRAZED DIPS

28-Lead Side-Brazed Dip
(TB-Suffix)



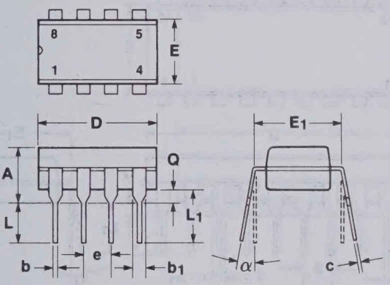
SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	—	0.225	—	5.72	—
b	0.014	0.023	0.36	0.58	—
b_1	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	—
D	—	1.490	—	37.85	4
E	0.500	0.610	12.70	15.49	4
E_1	0.590	0.620	14.99	15.75	7
e	0.100 BSC		2.54 BSC		5
L	0.120	0.200	3.05	5.08	—
L_1	0.150	—	3.81	—	—
Q	0.015	0.075	0.38	1.91	3
S	—	0.098	—	2.49	6
S_1	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

NOTES:

1. Index area; a notch is or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum limit for dimension b_1 may be 0.023 (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 (2.54 mm) between centerlines.
6. Applies to all four corners.
7. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.

PACKAGE DIMENSIONS — EPOXY DIPS

8-Lead Epoxy Dip (P-Suffix)

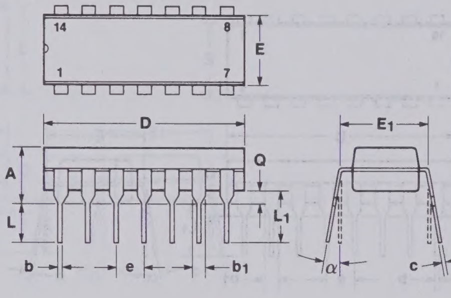


SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.148	0.152	3.76	3.86	—
b	0.016	0.020	0.406	0.508	—
b_1	0.058	0.062	1.47	1.58	—
c	0.008	0.012	0.203	0.304	—
D	0.373	0.382	9.47	9.70	—
E	0.246	0.254	6.25	6.45	—
E_1	0.298	0.302	7.57	7.67	2
e	0.100 BSC		2.54 BSC		—
L	0.128	0.132	3.25	3.35	—
L_1	0.148	0.152	3.76	3.86	—
Q	0.020 TYP		0.508 TYP		—
α	0°	15°	0°	15°	—

NOTES:

1. Minor changes in dimensions may occur without advance notice.
2. Dimension "E_1" to center of leads when formed parallel.

14-Lead Epoxy Dip (P-Suffix)



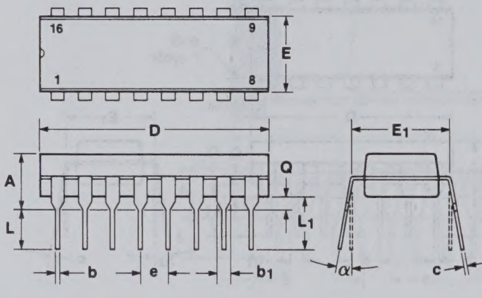
SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	—	0.200	—	5.08	—
b	0.014	0.023	0.36	0.58	—
b_1	0.030	0.070	0.76	1.78	—
c	0.008	0.015	0.20	0.38	—
D	0.748	0.752	18.99	19.1	—
E	0.220	0.310	5.59	7.87	—
E_1	0.290	0.320	7.37	8.13	2
e	0.100 BSC		2.54 BSC		—
L	0.125	0.200	3.18	5.08	—
L_1	0.150	—	3.81	—	—
Q	0.015	0.060	0.38	1.52	—
α	0°	15°	0°	15°	—

NOTES:

1. Minor changes in dimensions may occur without advance notice.
2. Dimension "E_1" to center of leads when formed parallel.

PACKAGE DIMENSIONS — EPOXY DIPS

16-Lead Epoxy Dip (P-Suffix)

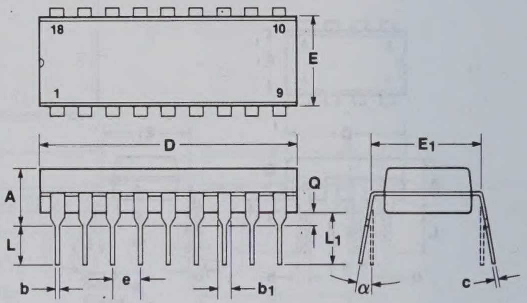


SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	—	0.200	—	5.08	—
b	0.014	0.023	0.36	0.58	—
b_1	0.030	0.070	0.76	1.78	—
c	0.008	0.015	0.20	0.38	—
D	0.748	0.752	18.99	19.1	—
E	0.220	0.310	5.59	7.87	—
E_1	0.290	0.320	7.37	8.13	2
e	0.100 BSC		2.54 BSC		—
L	0.125	0.200	3.18	5.05	—
L_1	0.150	—	3.81	—	—
Q	0.015	0.060	0.38	1.52	—
α	0°	15°	0°	15°	—

NOTES:

1. Minor changes in dimensions may occur without advance notice.
2. Dimension "E_1" to center of leads when formed parallel.

18-Lead Epoxy Dip (P-Suffix)



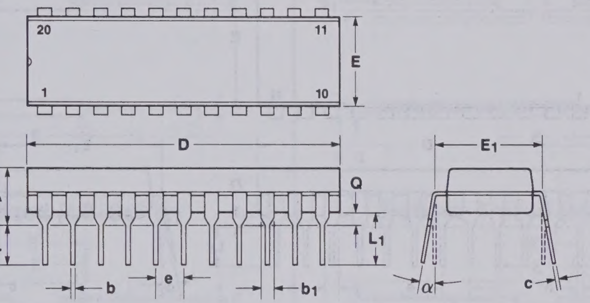
SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	—	0.200	—	5.08	—
b	0.014	0.023	0.36	0.58	—
b_1	0.030	0.070	0.76	1.78	—
c	0.008	0.015	0.20	0.38	—
D	0.898	0.902	22.81	22.91	—
E	0.220	0.310	5.59	7.87	—
E_1	0.290	0.320	7.37	8.13	2
e	0.100 BSC		2.54 BSC		—
L	0.125	0.200	3.18	5.08	—
L_1	0.150	—	3.81	—	—
Q	0.015	0.060	0.38	1.52	—
α	0°	15°	0°	15°	—

NOTES:

1. Minor changes in dimensions may occur without advance notice.
2. Dimension "E_1" to center of leads when formed parallel.

PACKAGE DIMENSIONS — EPOXY DIPS

20-Lead Epoxy Dip (P-Suffix)



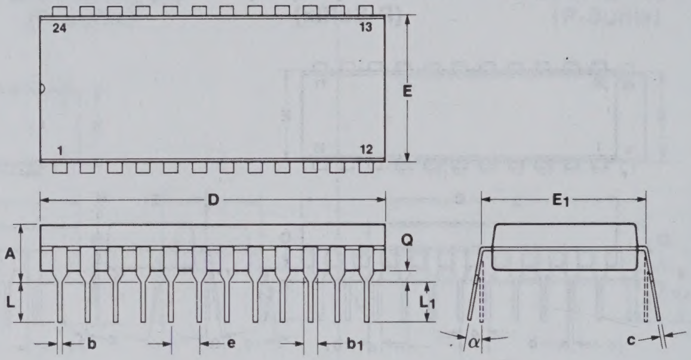
SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	—	0.255	—	5.08	—
b	0.014	0.023	0.36	0.58	—
b_1	0.030	0.070	0.76	1.78	—
c	0.008	0.015	0.20	0.38	—
D	1.029	1.033	26.14	26.24	—
E	0.220	0.310	5.59	7.87	—
E_1	0.290	0.320	7.37	8.13	2
e	0.100 BSC		2.54 BSC		—
L	0.125	0.200	3.18	5.08	—
L_1	0.150	—	3.81	—	—
Q	0.015	0.060	0.38	1.52	—
α	0°	15°	0°	15°	—

NOTES:

1. Minor changes in dimensions may occur without advance notice.
2. Dimension "E_1" to center of leads when formed parallel.

PACKAGE DIMENSIONS — EPOXY DIPS

24-Lead Epoxy Dip (P-Suffix)



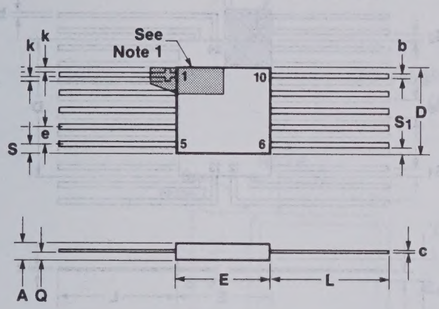
SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	—	0.225	—	5.08	—
b	0.014	0.023	0.36	0.58	—
b_1	0.030	0.070	0.76	1.78	—
c	0.008	0.015	0.20	0.38	—
D	1.248	1.252	31.7	31.8	—
E	0.538	0.542	13.67	13.77	—
E_1	0.598	0.602	15.19	15.29	2
e	0.100 BSC		2.54 BSC		—
L	0.125	0.200	3.18	5.08	—
L_1	0.150	—	3.81	—	—
Q	0.015	0.060	0.38	1.52	—
α	0°	15°	0°	15°	—

NOTES:

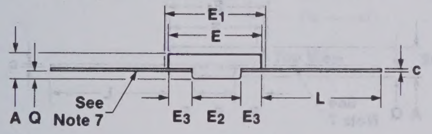
1. Minor changes in dimensions may occur without advance notice.
2. Dimension "E_1" to center of leads when formed parallel.

PACKAGE DIMENSIONS — FLATPACKS

10-Lead Flatpack (L-Suffix)

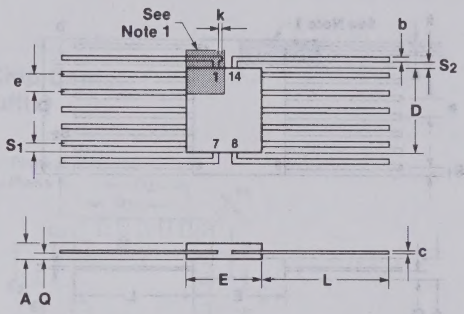


Bottom-Brazed (LB-Suffix)

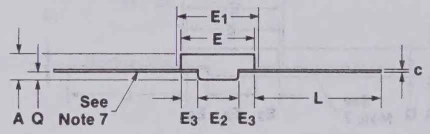


SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.030	0.085	0.76	2.16	—
b	0.010	0.019	0.25	0.48	—
c	0.003	0.006	0.08	0.15	—
D	—	0.290	—	7.37	3
E	0.240	0.260	6.10	6.60	—
E_1	—	0.280	—	7.11	3
E_2	0.125	—	3.18	—	—
E_3	0.030	—	0.76	—	—
e	0.050 BSC		1.27 BSC		4
k	0.008	0.015	0.20	0.38	8
L	0.250	0.370	6.35	9.40	—
Q	0.010	0.040	0.25	1.02	2
S	—	0.045	—	1.14	5
S_1	0.005	—	0.13	—	5, 6

14-Lead Flatpack (M-Suffix)



Bottom-Brazed (MB-Suffix)



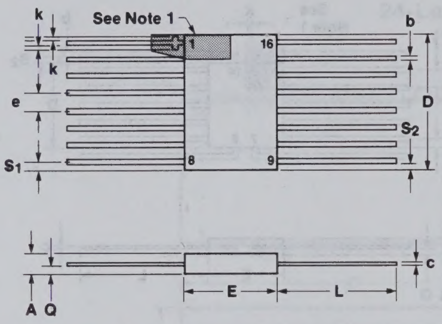
SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.030	0.085	0.76	2.16	—
b	0.010	0.019	0.25	0.48	—
c	0.003	0.006	0.08	0.15	—
D	—	0.280	—	7.11	3
E	0.240	0.260	6.10	6.60	—
E_1	—	0.280	—	7.11	3
E_2	0.125	—	3.18	—	—
E_3	0.030	—	0.76	—	—
e	0.050 BSC		1.27 BSC		4
k	0.008	0.015	0.20	0.38	8
L	0.250	0.370	6.35	9.40	—
Q	0.010	0.040	0.25	1.02	2
S_1	0.005	—	0.13	—	5, 6
S_2	0.004	—	0.10	—	—

NOTES:

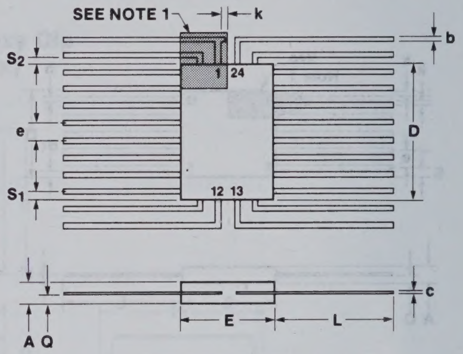
1. Index area; a notch or a lead one identification mark is located adjacent to lead one and shall be located within the shaded area shown. Alternatively, a tab (dim. k) may be used to identify lead one. This tab may be located on either side as shown.
2. Dimension Q shall be measured at the point of exit of the lead from the body.
3. This dimension allows for off-center lid, meniscus and glass overrun.
4. The basic lead spacing is 0.050 (1.27 mm) between centerlines.
5. Applies to all four corners.
6. Dimension S_1 (See 40.3) may be 0.000 (0.00 mm) if corner leads bend toward the cavity of the package within one lead's width from the point of entry of the lead into body.
7. Optional configuration. If this configuration is used, no organic or polymeric materials are molded to the bottom of the package to cover the leads.
8. Optional, see note 1. If a lead one identification mark is used in addition to this tab, the minimum limit of dimension k does not apply.

PACKAGE DIMENSIONS — FLATPACKS

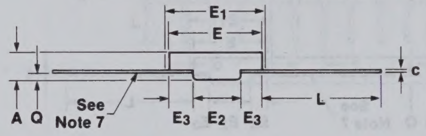
16-Lead Flatpack (F-Suffix)



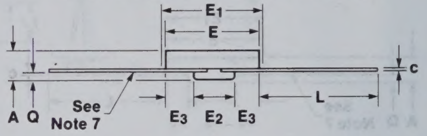
24-Lead Flatpack (N-Suffix)



Bottom-Brazed (FB-Suffix)



Bottom-Brazed (NB-Suffix)



	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A	0.045	0.085	1.14	2.16	—
b	0.015	0.019	0.38	0.48	—
c	0.003	0.006	0.08	0.15	—
D	—	0.440	—	11.18	3
E	0.245	0.285	6.22	7.24	—
E_1	—	0.305	—	7.75	3
E_2	0.130	—	3.30	—	—
E_3	0.030	—	0.76	—	—
e	0.050 BSC		1.27 BSC		4
k	0.008	0.015	0.20	0.38	8
L	0.250	0.370	6.35	9.40	—
Q	0.010	0.040	0.23	1.02	2
S	—	0.045	—	1.14	5
S_1	0.005	—	0.13	—	5, 6

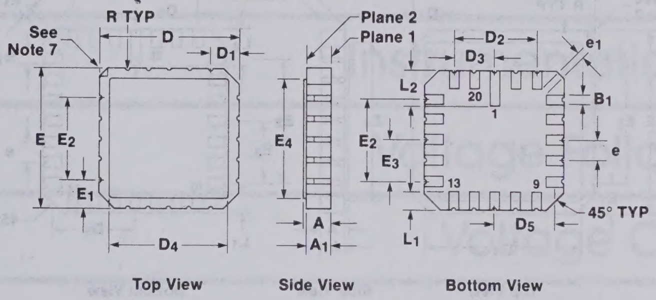
	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A	0.045	0.090	1.14	2.29	—
b	0.015	0.019	0.38	0.48	—
c	0.003	0.006	0.08	0.15	—
D	—	0.0430	—	10.92	3
E	0.245	0.285	6.22	7.24	—
E_1	—	0.305	—	7.75	3
E_2	0.125	—	3.18	—	—
E_3	0.030	—	0.76	—	—
e	0.050 BSC		1.27 BSC		4
k	0.008	0.015	0.20	0.38	8
L	0.250	0.370	6.35	9.40	—
Q	0.010	0.040	0.25	1.02	2
S_1	0.005	—	0.13	—	5, 6
S_2	0.004	—	0.10	—	—

NOTES:

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is located within the shaded area shown. Alternatively, a tab (dim. k) may be used to identify lead one. This tab may be located on either side as shown.
2. Dimension Q shall be measured at the point of exit of the lead from the body.
3. This dimension allows for off-center lid, meniscus and glass overrun.
4. The basic lead spacing is 0.050 (1.27 mm) between centerlines.
5. Applies to all four corners.
6. Dimension S_1 (See 40.3) may be 0.000 (0.00 mm) if corner leads bend toward the cavity of the package within one lead's width from the point of entry of the lead into body.
7. Optional configuration. If this configuration is used, no organic or polymeric materials are molded to the bottom of the package to cover the leads.
8. Optional, see note 1. If a lead one identification mark is used in addition to this tab, the minimum limit of dimension k does not apply.

PACKAGE DIMENSIONS — LEADLESS CHIP CARRIERS

20-Position Chip Carrier (RC-Suffix)



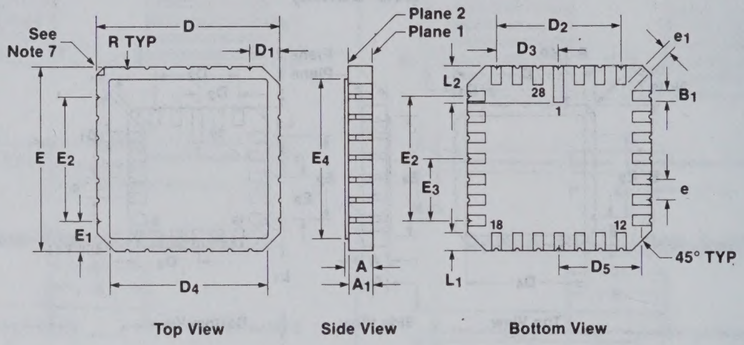
SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.064	0.100	1.63	2.54	5
A_1	0.054	0.088	1.37	2.24	
B_1	0.022	0.028	0.56	0.71	2
D	0.342	0.358	8.69	9.09	—
D_1	0.075 REF		1.91 REF		—
D_2	0.200 REF		5.08 REF		—
D_3	0.100 REF		2.54 REF		—
D_4	—	0.358	—	9.09	3
D_5	0.150 BSC		3.81 BSC		—
E	0.342	0.358	8.69	9.09	—
E_1	0.075 REF		1.91 REF		—
E_2	0.200 REF		5.08 REF		—
E_3	0.100 REF		1.91 REF		—
E_4	—	0.358	—	9.09	3
e	0.050 BSC		1.27 BSC		—
e_1	0.015	—	0.38	—	1
L_1	0.077	0.093	1.96	2.36	4
R	0.007	0.011	0.18	0.28	—

NOTES:

1. A minimum clearance of 0.015" (0.381 mm) is maintained between corner terminals.
2. Electrical connection is required on plane 1. Metallization is optional on plane 2. However, if plane 2 is metallized it must be electrically connected.
3. A minimum clearance of 0.020" (0.508 mm) is maintained between overall dimensions $D_4 \times E_4$ and all other features, including metallization, chamfers and edges.
4. Non-electrical features for No. 1 terminal identification, optical orientation or handling purposes shall be within the shaded area shown on plane 2.
5. Dimension A controls the overall package thickness.
6. Length of pad metallization may increase only toward package periphery.
7. When space is available, the index corner may be metallized on either or both planes 1 and 2. The package edge at the index corner shall not be metallized.

PACKAGE DIMENSIONS — LEADLESS CHIP CARRIERS

28-Position Chip Carrier (TC-Suffix)



SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.064	0.100	1.63	2.54	5
A_1	0.054	0.088	1.37	2.24	—
B_1	0.022	0.028	0.56	0.71	2
D	0.442	0.458	11.23	11.63	—
D_1	0.075 REF		1.91 REF		—
D_2	0.300 REF		7.62 REF		—
D_3	0.150 REF		3.81 REF		—
D_4	—	0.458	—	11.63	3
D_5	0.200 BSC		5.08 BSC		—
E	0.442	0.458	11.23	11.63	—
E_1	0.075 REF		1.91 REF		—
E_2	0.300 REF		7.62 REF		—
E_3	0.150 REF		3.81 REF		—
E_4	—	0.458	—	11.63	3
e	0.050	—	1.27	—	—
e_1	0.015	—	0.38	—	1
L_1	0.077	0.093	1.96	2.36	4
R	0.007	0.011	0.18	0.28	—

NOTES:

1. A minimum clearance of 0.015" (0.381 mm) is maintained between corner terminals.
2. Electrical connection is required on plane 1. Metallization is optional on plane 2. However, if plane 2 is metallized it must be electrically connected.
3. A minimum clearance of 0.020" (0.508 mm) is maintained between overall dimensions $D_4 \times E_4$ and all other features, including metallization, chamfers and edges.
4. Non-electrical features for No. 1 terminal identification, optical orientation or handling purposes shall be within the shaded area shown on plane 2.
5. Dimension A controls the overall package thickness.
6. Length of pad metallization may increase only toward package periphery.
7. When space is available, the index corner may be metallized on either or both planes 1 and 2. The package edge at the index corner shall not be metallized.

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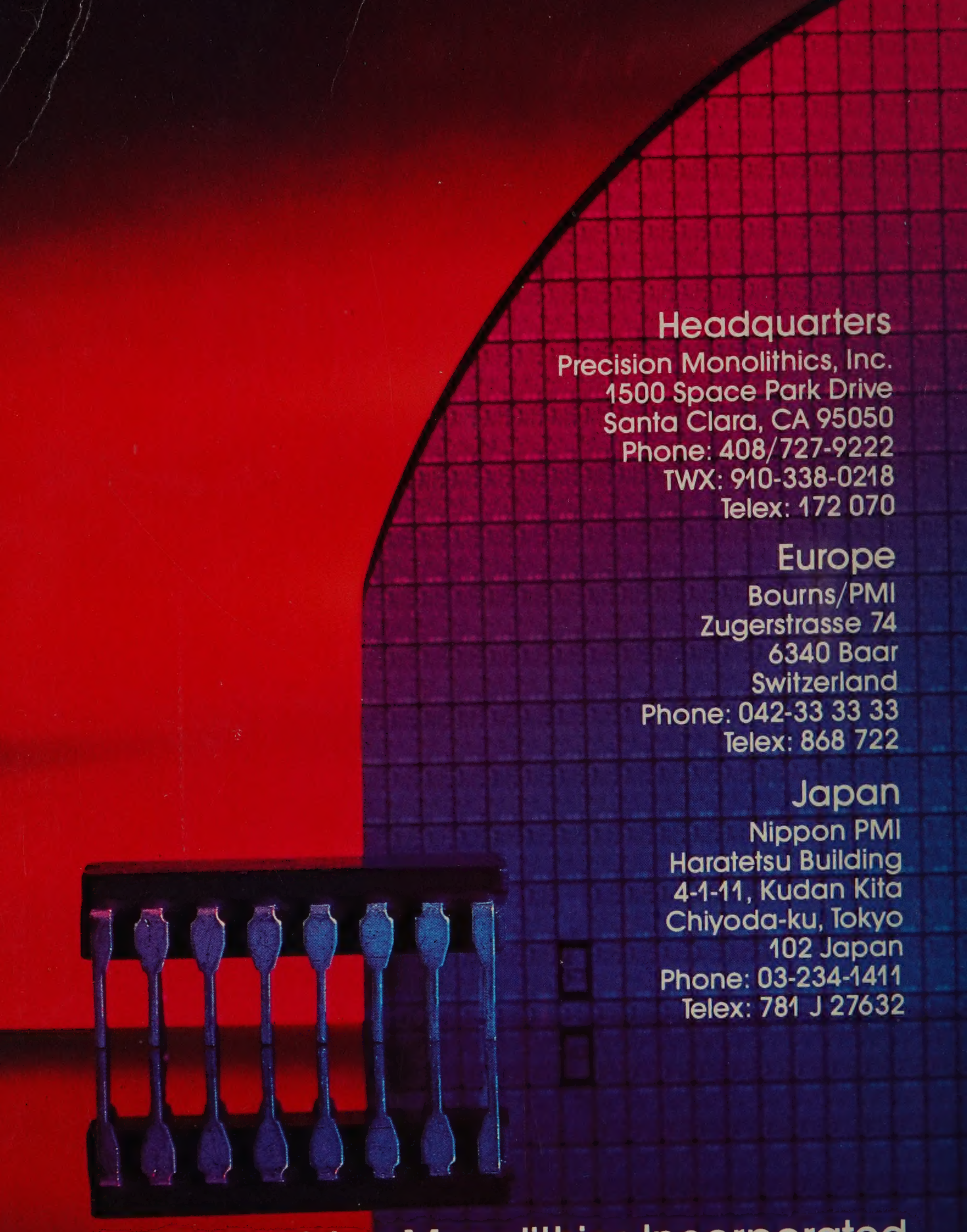

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